Design and Implementation of a Flyback-Assisted Wide-Range Fully Soft-Switched T-Type Inverter

Naim Suleyman Ting, *Member, IEEE*, Yakup Sahin, and Mehmet Cihat Ozgenel

***Abstract*—A novel soft-switched three-level T-type inverter is proposed in this article. The proposed inverter provides turning-ON by zero-voltage transition and turning-OFF by zero-voltage switching (ZVS) for main switches without any voltage or current stresses. The switching energies are transferred to the snubber capacitors, so the turning-OFF process of the main switches is improved by these snubber capacitors. Besides, the auxiliary switches are turned ON by zero-current switching and turned OFF by ZVS. Furthermore, all snubber diodes are operated by soft-switching (SS), and the proposed SS snubber cell decreases the electromagnetic interference noises. The novel snubber cell has a simple structure, ease of application, common-ground switches, and low-cost features. The theoretical analysis of the inverter is clarified, and the operating modes for steady-state analysis are presented in detail. The experimental results rated 1-kW output power and 100-kHz switching frequency are provided to justify the theoretical analysis. The proposed unique snubber cell can be easily implemented in other three-level inverters, and the practice is demonstrated in the article.**

***Index Terms*—Active snubber cell, soft switching (SS), three-level inverter (3LI), T-type inverter, zero-voltage transition (ZVT).**

I. Introduction

DC–AC power converters are used in many critical fields in which power density and efficiency are significant issues, including photovoltaic power systems, electric vehicle drivers, and uninterruptible power supply systems. DC–AC converters are configured as two-level (2LIs), three-level (3LIs), and multilevel inverters (MLIs). Conventional 3LIs have several advantages over 2LIs, including improved harmonic distortion, reduced switching losses, and higher power density. Besides, MLIs provide many advantages over 3LIs, such as more sinusoidal output voltage, reduced semiconductor voltage stress, and improved efficiency. Although increasing the voltage level at output voltage provides many advantages, it induces more complexity, control difficulty, and increased cost. Accordingly, the price–performance ratio is essential for choosing an inverter, and 3LIs present a great opportunity for such.

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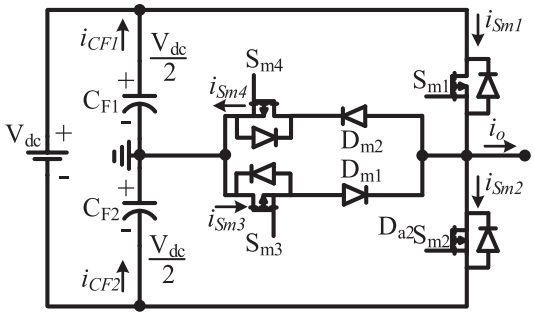


Fig. 1. Circuit of a conventional single-phase 3LT^{2}I.

Three-level T-type inverter (3LT^{2}I) illustrated in Fig. 1 is a popular converter and presents unique advantages in the family of 3LIs. This inverter has fewer components: a simple structure, ease of control, and low-cost features. Besides, it can handle higher power levels due to its multilevel capability [1].

The three-level I-type inverter, named three-level neutral-point clamped inverter (3LNPCI), was first introduced in [2]. Notwithstanding the structure of 3LT^{2}I and 3LNPCI converters is similar, a 3LNPCI includes two extra power diodes than 3LT^{2}I. These additional semiconductor diodes lead to conduction loss and decrease the total efficiency of the converter [3]. Hence, 3LT^{2}I has better efficiency, in particular, at low switching frequencies. However, the efficiency of 3LT^{2}I is reduced compared to 3LNPCI at high switching frequencies and high input voltages, since the leg power MOSFETs of 3LT^{2}I are exposed to more dc voltage, and the high voltage leads to an increased switching power loss. Consequently, a 3LT^{2}I has a lower cost and simple structure than a 3LNPCI owing to fewer component numbers [4].

3LT^{2}I has received great attention from researchers, particularly in medium to high power [5]. Subsequently, several other topologies have been introduced to the literature to improve 3LT^{2}I. A new topology called a square T-type module is created by connecting two T-type inverters as back-to-back connections [6]. This converter increases both the voltage level and output power. Additionally, reducing the number of components used in the converter is essential when the voltage level is increased. Therefore, a generalized switch-ladder topology with the lowest switch count among all the currently available cascaded MLIs is created, further optimizing the T-type-based module structure [7].

3LT^{2}Is have two dc bulk filter capacitors to supply divided input voltage, and these capacitors have large equivalent series resistors (ESRs) that increase power losses. Moreover, the inverters require an *LC* output filter because the output voltage is square. The internal resistor inductor and ESR of the capacitor increase power consumption. Additionally, the input bulk capacitors and output filters increase the power loss and cost while decreasing the power density because they have large sizes. Increasing the switching frequency decreases the size of the inductor and the capacitor used in the converter. Consequently, using smaller value inductors and capacitors increases power density and reduces power loss and cost. However, the switching power loss and electromagnetic interference (EMI) are increased at high switching frequencies. To overcome these issues at high switching frequencies, soft-switching (SS) techniques should be implemented [8]. These techniques performed by snubber cells keep the total efficiency higher because of the reduced switching loss, and decrease the cost as well as increase the power density due to smaller value *LC* components and size of heatsinks. Moreover, the dynamic performance of the converter is improved and the EMI is reduced owing to slowing *dv*/*dt* and *di*/*dt* [9], [10], [11], [12]. SS techniques are provided by the passive and active snubber cells.

Passive snubber cells include passive components, such as inductors, capacitors, and diodes. They provide zero-current switching (ZCS) or zero-voltage switching (ZVS) for the power semiconductors to reduce switching power loss. The passive snubber cells are easy to implement owing to their simple structure. Therefore, the application of passive snubber cells is commonly used as seen in [13], [14], [15], and [16]. The total cost of the converter may increase since the snubber cell creates voltage or current stress on the power semiconductors, despite the passive snubber cells having a low price. Yet again, this leads to an increased cost for the converter since the voltage or current rating of semiconductor devices used in the converter is increased [17], [18], [19], [20]. Furthermore, the working principle of a passive snubber cell depends on the resonance between inductors and capacitors used in the snubber cell. Thus, the *LC* resonance duration is crucial for the operating performance of the snubber. The best performance of the snubber cell is set to the maximum output power to achieve high efficiency. As a result, the performance of the passive snubber cell is reduced at the light loads because of the long resonance duration [21], [22].

Active snubber cells include an active switch in addition to passive components to eliminate power losses [23], [24], [25]. Even though the reliability of the converters diminishes due to the active semiconductor switch, the active snubber cells present excellent benefits. The switching power losses can be eliminated by zero-voltage transition (ZVT) and zero-current transition at the turning-ON and turning-OFF switching, respectively. Besides, the cost of the main circuit does not increase because, generally, there is no extra voltage or current stress on the main semiconductors [26]. It is commonly known that the active snubber cells at the light loads usually perform well since they have an active control method. The inherited feature of active snubber cells enables the operation within a comprehensive output power range to compensate for the sophistical control of the converter.

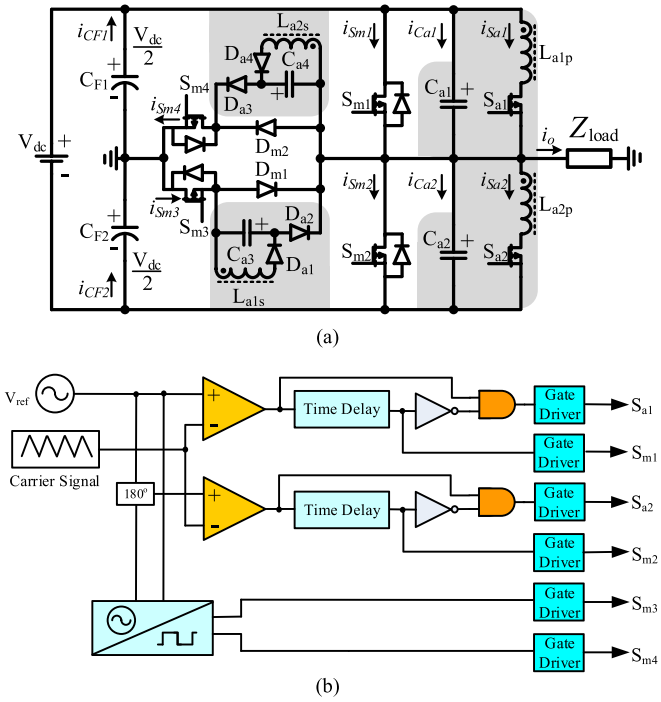


Fig. 2. Circuit schema (a) and the control block diagram (b) of the proposed single-phase 3LT^{2}I.

This article introduces a novel soft-switched with active snubber cell 3LT^{2}I. This article is the extension of the previously published conference paper in [5]. The proposed snubber cell consists of an auxiliary switch, a coupled inductor, two diodes, and two snubber capacitors for one main power switch. The proposed inverter enables the main switches to turn ON by ZVT and turn OFF by ZVS without any voltage or current stresses. Additionally, the auxiliary switches are turned ON by ZCS and turned OFF by ZVS. Besides, all snubber diodes are operated by SS.

II. Operation Modes of the Proposed 3LT^{2}I

A. Conventional Three-Level T-Type Inverter

The circuit of a conventional single-phase 3LT^{2}I, where the output of each inverter leg is connected to the neutral point of the inverter through a bidirectional switch is illustrated in Fig. 1. The bidirectional switches allow a controllable path between the neutral point inverter and the load terminal. This inverter creates three states at the output voltage level. The output voltage is 0.5 $V_{\rm dc}$ when the upper switch S_{m1} is in ON-state; the output voltage inverter is -0.5 $V_{\rm dc}$ when the lower switch S_{m2} is in ON-state; and the output voltage is zero when S_{m3} or S_{m4} is in ON-state.

B. Proposed Three-Level T-Type Inverter

The novel soft-switched 3LT^{2}I and its control block diagram are presented in Fig. 2.

In the inverter's main circuit, S_{m1} and S_{m2} are the main leg switches; S_{m3} and S_{m4} are the neutral main switches; and also

D_{m1} and D_{m2} are the neutral diodes. The proposed snubber cell includes S_{a1} and S_{a2} as the auxiliary switches, and the auxiliary capacitors and diodes are symbolized between C_{a1} to C_{a4} and D_{a1} to D_{a4}, respectively. L_{a1p} and L_{a2p} exhibit the primary windings, while L_{a1s} and L_{a2s} indicate the secondary windings of each coupled inductor. Finally, $Z_{\rm Load}$ is the load constructed by a power resistor and inductor.

In the control block diagram of the proposed inverter, sinusoidal PWM (SPWM) signals are obtained by comparing a reference ac signal to a carrier signal. The SPWM signals are delayed from the time delay blocks to produce the control signals of the main switches S_{m1} and S_{m2}. Then, the reverse of produced signals from the time delay block and the SPWM signals are passed through the AND logic gate, and the control signals of the auxiliary switches S_{a1} and S_{a2} are produced. Finally, the control signals of the S_{m3} and S_{m4} switches are created by converting the reference ac voltage to square waves. Some assumptions are utilized to help simplify the steady-state theoretical analysis of the proposed 3LT^{2}I during one switching cycle as follows:

1) The input voltage $V_{\rm dc}$ and load current i_o are constant.
2) The auxiliary capacitors C_{a1} and C_{a2} include parasitic capacitors of power switches.
3) All parasitic effects and voltage drops are neglected.

In the steady-state analysis of the inverter, the eight operational modes occur during one switching cycle. The neutral switch S_{m3} is in ON-state, and there is no transition during these eight modes. Fig. 3 illustrates the equivalent circuits for each operational mode. Furthermore, the fundamental waveforms of all operating modes are portrayed in Fig. 4.

Mode 1 [$t_0 < t < t_1$: Fig. 3(a)]: Before this mode, all semiconductor switches are in OFF-state except S_{m3}. This mode starts when the control signal is applied to the gate of the auxiliary switch S_{a1} at t_0. This switch is turned ON by ZCS with the aid of the series inductor $L_{a1\rm p}$, and so the turning-ON switching power loss is reduced. The current of S_{a1} increases linearly under the constant input voltage $V_{\rm dc}/2$, while the current of S_{m3} decreases during this mode.

When the current of S_{a1} reaches the output current, then the current of S_{m3} falls to zero at t_1, and this mode is terminated. The following equations are valid for this mode:

$$i_{Sa1} = i_{La1p} = \frac{V_{\rm dc}}{2L_{a1p}}(t - t_0) \tag{1}$$

$$i_{Sm3} = I_o - i_{Sa1} = I_o - \frac{V_{\rm dc}}{2L_{a1p}}(t - t_0) \tag{2}$$

$$t_{01} = \frac{I_o 2L_{a1p}}{V_{\rm dc}}. \tag{3}$$

Mode 2 [$t_1 < t < t_2$: Fig. 3(b)]: This mode starts when the neutral main switch S_{m3} is turned OFF at t_1. An *LC* resonance occurs between the inductor L_{a1p} and the equivalent capacitors represented by C_{S1}. The voltage of C_{a1} decreases to zero while the voltage of C_{a2} increases to the $V_{\rm dc}$ level during this mode. The current of L_{a1p} reaches a peak rating when the voltage of C_{a1} falls to zero, and this mode is terminated at t_2. Fundamental equations for this mode are as follows:

$$i_{Sa1} = i_{La1p} = I_o + \frac{V_{\rm dc}}{2Z_1}\sin(\omega_1(t - t_1)) \tag{4}$$

$$v_{Ca1} = v_{Sm1} = \frac{V_{\rm dc}}{2}\cos(\omega_1(t - t_1)) \tag{5}$$

$$v_{Ca2} = v_{Sm2} = \frac{V_{\rm dc}}{2}(1 + \cos(\omega_1(t - t_1))) \tag{6}$$

where

$$C_{S1} = C_{a1} + C_{a2} \tag{7}$$

$$\omega_1 = \frac{1}{\sqrt{L_{a1p}C_{S1}}} \tag{8}$$

$$Z_1 = \sqrt{\frac{L_{a1p}}{C_{S1}}}. \tag{9}$$

Mode 3 [$t_2 < t < t_3$: Fig. 3(c)]: The internal diode of the main switch S_{m1} is turned ON, and this mode is initiated at t_2. This mode is called ZVT mode since the voltage across the main switch S_{m1} is zero during this mode. The control signal is applied to the gate of S_{m1} in the middle of this mode, and the switch is turned ON by ZVT. The turning-ON switching loss of S_{m1} is eliminated thoroughly and the switch is turned ON completely lossless. The duration of the ZVT mode should be as short as possible for fewer conduction losses. The mode terminates when the control signal of S_{a1} is removed at t_3. The basic equations at the end of the mode are as follows:

$$i_{La1p} = I_{La1p(\rm peak)} \tag{10}$$

$$i_{Sa1} = I_o - I_{La1p(\rm peak)}. \tag{11}$$

Mode 4 [$t_3 < t < t_4$: Fig. 3(d)]: This mode starts when the auxiliary switch S_{a1} is turned OFF. The energy stored in the primary inductor L_{a1p} is transferred to the secondary inductor of coupled inductor L_{a1s}, and resonance occurs between L_{a1s} and C_{a3}. The S_{a1} is turned OFF by ZVS due to the resonance, and the turning-OFF switching power loss of the switch is reduced. The output current starts to flow through the main switch S_{m1} from the beginning of this mode. This mode terminates at t_4 when the voltage of C_{a3} reaches $V_{\rm dc}/2$. For this mode, the following equations apply:

$$i_{La1s} = I_{La1s(\rm peak)}\cos(\omega_2(t - t_3)) \tag{12}$$

$$v_{Ca3} = I_{La1s(\rm peak)}Z_2\sin(\omega_2(t - t_3)) \tag{13}$$

where

$$\omega_2 = \frac{1}{\sqrt{L_{a1s}C_{a3}}} \tag{14}$$

$$Z_2 = \sqrt{\frac{L_{a1s}}{C_{a3}}}. \tag{15}$$

Mode 5 [$t_4 < t < t_5$: Fig. 3(e)]: The neutral main switch S_{m3} is turned ON by ZVS, and this mode starts at t_4. Mode 5 occurs when stored energy in the L_{a1s} is more than the energy C_{a3} can store. Otherwise, this mode is obsoleted. The current of L_{a1s} decreases linearly under constant $V_{\rm dc}/2$ voltage, and a ripple occurs on the current of S_{m1} during this mode. The neutral

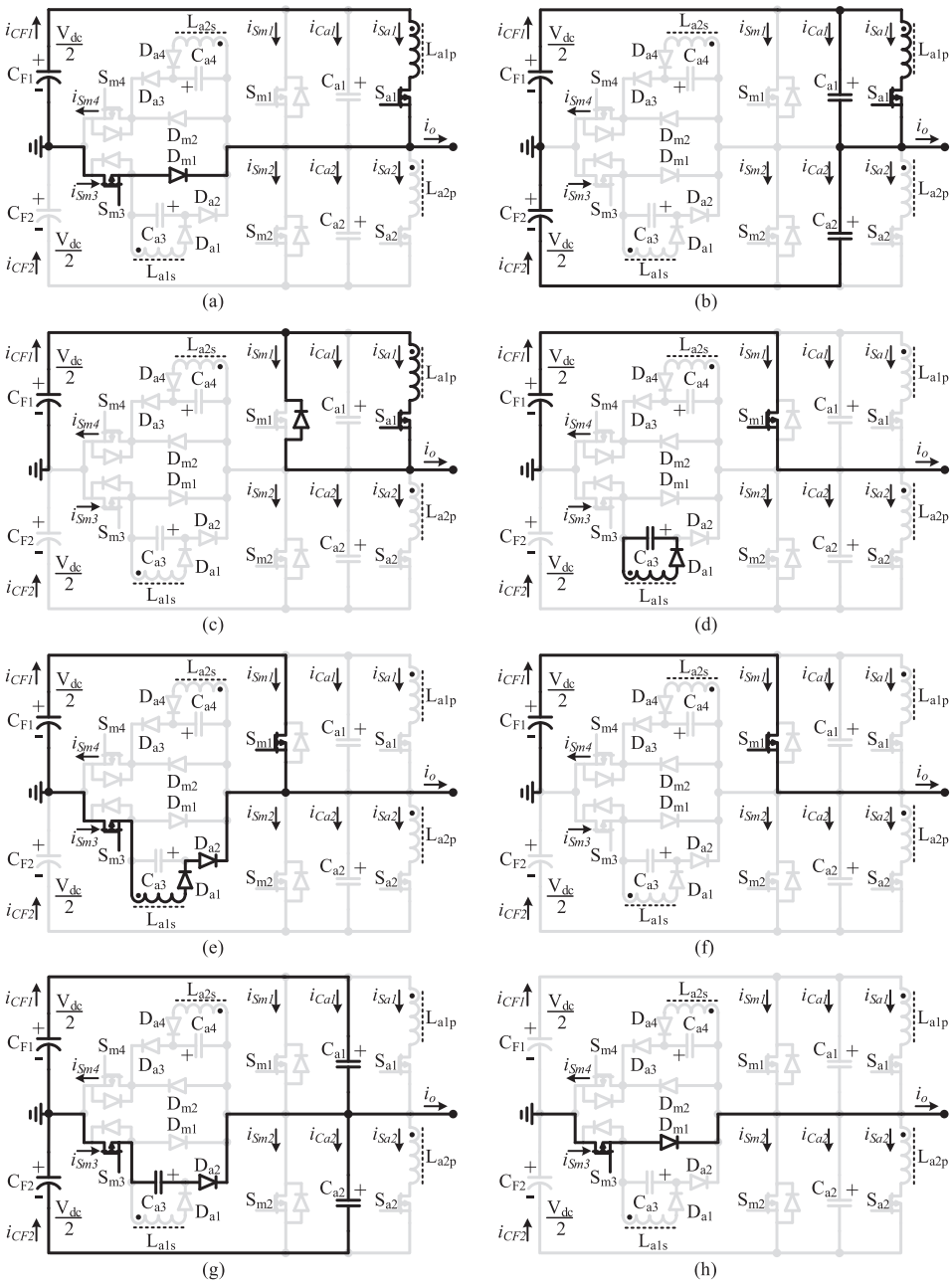


Fig. 3. Equivalent circuits of the operating modes in the proposed 3LT^{2}I: (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5, (f) mode 6, (g) mode 7, and (h) mode 8.

main switch S_{m3} is turned OFF by both ZVS and ZCS when the current of L_{a1s} falls to zero at t_5. The equations for this mode are as follows:

$$i_{Sm3} = i_{La1s} = \frac{V_{\rm dc}}{2I_{La1s4}}\,(t - t_4) \tag{16}$$

$$i_{Sm1} = I_o - \frac{V_{\rm dc}}{2I_{La1s4}}\,(t - t_4)\,. \tag{17}$$

Mode 6 [$t_5 < t < t_6$: Fig. 3(f)]: The output current flows through the main switch S_{a1} during this mode. This mode is called inverter ON-state mode, and the snubber cell is passive in this mode. The equation for S_{m1} is

$$i_{Sm1} = I_o. \tag{18}$$

Mode 7 [$t_6 < t < t_7$: Fig. 3(g)]: The control signal of S_{m1} is removed, and this mode starts at t_6. The main switch S_{m3} is turned ON at the beginning of this mode. C_{a2} and C_{a3} discharge, while C_{a1} is charging during this mode. The main switch S_{m1} is turned OFF by ZVS since the voltage across the switch is equal to zero. Thus, the turning-OFF switching power loss of S_{m1} is reduced. C_{a1}, C_{a2}, and C_{a3} concurrently reduce the turning-OFF switching loss, so the snubber cell provides excellent ZVS

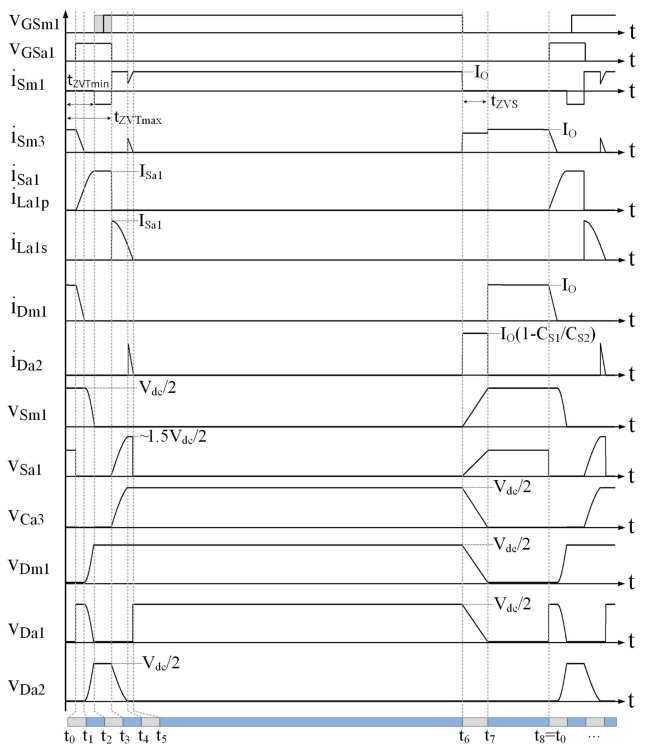


Fig. 4. Fundamental SS waveforms of the proposed 3LT^{2}I.

performance. The voltage equations for the auxiliary capacitors are as follows:

$$v_{Ca1} = v_{Sm1} = \frac{C_{a1} I_o}{C_{S2}} (t - t_6) \tag{19}$$

$$v_{Ca2} = v_{Sm2} = V_{\text{dc}} - \frac{C_{a2} I_o}{C_{S2}} (t - t_6) \tag{20}$$

$$v_{Ca3} = \frac{V_{\text{dc}}}{2} - \frac{C_{a3} I_o}{C_{S2}} (t - t_6) \tag{21}$$

where

$$C_{S2} = C_{a1} + C_{a2} + C_{a3}. \tag{22}$$

Mode 8 [$t_7 < t < t_8$: Fig. 3(h)]: This mode starts at t_7 and is called inverter OFF-state mode. The duration of this mode depends on PWM duration, and the output current flows through the neutral main switch S_{m3}. When the control signal is applied to the gate of S_{a1}, one switching cycle is completed. At t_8, it returns to Mode 1 and repeats these eight intervals for the next cycle. The equation for S_{m3} is provided as follows:

$$i_{Sm3} = I_o. \tag{23}$$

III. Performance Evaluation of the Proposed 3LT^{2}I

A. Design Guideline of the Proposed 3LT^{2}I

1) Determination of L_{a1p} and L_{a1s}: The primary inductor windings of the coupled inductors affect the turning-ON switching power loss of S_{a1}. To obtain a sufficient ZCS, the current rise time of L_{a1p} must be lower than the rise time of S_{a1}. Finally, the value of L_{a1p} is equal to the value of L_{a1s} because the turns ratio is equal to 1

$$L_{a1p} = L_{a1s} > \frac{1}{C_{S1}} \left(\frac{2t_r}{\pi} \right)^2 \tag{24}$$

where t_r is the rise time of the S_{a1}.

2) Determination of C_{a3} and C_{a4}: The energy storage capacity of C_{a3} should be equal to the stored energy in the L_{a1p} at the maximum output current rating. The large capacity leads to a long transient resonance duration, while the small value causes a ripple in the current of main leg switches

$$C_{a3} = C_{a4} = L_{a1p} \left(\frac{2I_{o(\text{peak})}}{V_{\text{dc}}} \right)^2. \tag{25}$$

3) Determination of C_{a1} and C_{a2}: The ZVS turning-OFF for the S_{m1} strictly depends on the equivalent capacitor C_{S1}. The duration of voltage rising across the S_{m1} should be longer than the fall time of the switch

$$C_{S1} = C_{a1} + C_{a2} > \frac{2I_{o(\text{peak})}}{V_{\text{dc}}} t_f \tag{26}$$

where t_f is the fall time of the S_{m1}.

4) Determination of Turns Ratio (n)*:* The turns ratio is $n = N_1/N_2$, where N_1 represents the number of primary windings, while N_2 is the number of secondary windings. The voltage reflected across the S_{a1} decreases when the turns ratio is under one. However, the coupled inductor may not be reset because the resonance duration increases. On the contrary, despite the reduced resonance duration, high-voltage stress occurs across the S_{a1} when the turns ratio is under one. Accordingly, the turns ratio is selected equal to one for optimum design ($L_{a1p} = L_{a1s}$ and $L_{a2p} = L_{a2s}$).

B. Soft-Switching Condition and Device Stresses

There are two resonances in the proposed snubber cell: the first is before the main switch turning-ON process and the other is at the turning-OFF process. The energy stored in the C_{S1} capacitor has to ensure adequate current for the ZVT operation. The maximum ZVT current is obtained near the sinusoidal zero crossing of the output current

$$I_{\text{ZVTmax}} = \sqrt{\frac{C_{S1}}{L_{a1p}}} \frac{V_{\text{dc}}}{2}. \tag{27}$$

Furthermore, the minimum ZVT current is obtained at the sinusoidal maximum of the output current

$$I_{\text{ZVTmin}} = \sqrt{I_{o(\text{peak})}^2 + C_{S1} V_{\text{dc}}^2 / (4L_{a1p})} - I_{o(\text{peak})}. \tag{28}$$

The maximum value of the output current is considered to ensure the minimum ZVT duration even in the worst-case conditions

$$t_{\text{ZVTmin}} = \frac{2L_{a1p}}{V_{dc}} I_{o(\text{peak})} + \frac{\pi}{2} \sqrt{L_{a1p} C_{S1}}. \tag{29}$$

TABLE I
TRANSITIONS AND VOLTAGE/CURRENT STRESS OF SEMICONDUCTOR DEVICES USED IN THE PROPOSED INVERTER

Device	Turning		Voltage stress	Current stress
	on	off		
S_{m1}, S_{m2}	ZVT	ZVS	V_{dc}	$I_{o(peak)}$
S_{m3}, S_{m4}	No transition		$V_{dc}/2$	$I_{o(peak)}$
D_{m1}, D_{m2}	ZVS	ZVZCS	$V_{dc}/2$	$I_{o(peak)}$
S_{a1}, S_{a2}	ZCS	ZVS	V_{dc}	$\left(I_{o(peak)}^2 + C_{S1}V_{dc}^2/\left(4L_{a1p}\right)\right)^{0.5}$
D_{a1}, D_{a4}	ZVS	ZCS	$V_{dc}/2$	$\left(I_{o(peak)}^2 + C_{S1}V_{dc}^2/\left(4L_{a1p}\right)\right)^{0.5}$
D_{a2}, D_{a3}	ZVS	ZCS	$V_{dc}/2$	$I_{o(peak)}\left(1-\frac{C_{S1}}{C_{S2}}\right)$

The snubber capacitor is charged by the energy stored in the coupled inductor as follows:

$$v_{Ca3} = \sqrt{\frac{L_{a1p}}{C_{a3}}(I_{o\max}\sin(\omega_3 t))^2 + \frac{C_{S1}}{C_{a3}}\left(\frac{V_{\rm dc}}{2}\right)^2} \quad (30)$$

where

$$\omega_3 = 2\pi f_o \quad (31)$$

and f_o is the output frequency.

ZVS reduces power dissipation on the turning-OFF process for main switches. The equivalent snubber capacitor C_{S2} ensures full ZVS for the main switch at $I_{o(\rm peak)}$ because the design of the converter is configured for the maximum output current. When the output current is lower than the maximum level, V_{Ca3} cannot reach $V_{\rm dc}/2$. So first, the ZVS is provided by the equivalent snubber capacitor C_{S1} until its voltage reaches $V_{\rm dc}/2-V_{Ca3}$; last, C_{S2} provides ZVS. Accordingly, the ZVS duration can be calculated as follows:

$$t_{\rm ZVS} = \frac{C_{S1}}{I_{o(\rm peak)}\sin(\omega_3 t)}\left(\frac{V_{\rm dc}}{2} - v_{Ca3}\right) + \frac{C_{S2}}{I_{o(\rm peak)}\sin(\omega_3 t)}v_{Ca3}. \quad (32)$$

The maximum current in the primary of the coupled inductor is considered when choosing the core and calculated as follows:

$$I_{La1p(\rm peak)} = \sqrt{I_{o(\rm peak)}^2 + 2C_{a1}V_{\rm dc}^2/(4L_{a1p})}. \quad (33)$$

The turning-ON and turning-OFF transitions, as well as voltage and current stress for each semiconductor device, are presented in Table I. All semiconductor devices are switched by SS techniques, and switching power losses are eliminated or reduced. Additionally, any voltage and current stress do not occur on the main semiconductor switches, and the auxiliary devices have no voltage stress. The neutral switch S_{m3} is in ON-state during half of the output period. Therefore, switching power losses do not occur, but conduction loss on the switch because the switch does not require a transition.

C. Power Loss Evaluation

1) Calculation for HS 3LT^{2}I: Two significant losses occur in an HS 3LT^{2}I: conduction and switching losses. The switching power loss occurs because of the overlapping voltage across the switch and the current flows through the switch during the turning-ON or OFF process. The switching power loss occurs only on S_{m1} and S_{m4}. Since the neutral switches are continually in ON-state for each half period, the switching power loss does not occur on these switches. The switching power loss for each main switch is equal, and hence the loss calculation for any switch represents the loss that occurs and is formulated as follows:

$$P_{sw(Sm)} = \frac{V_{sm}I_{o(\rm rms)}}{2}(t_r + t_f)f_{\rm sw} \quad (34)$$

where $P_{{\rm sw}(sm)}$ is the total switching power loss, $f_{\rm sw}$ is the switching frequency, and V_{sm}, t_r, and t_f are the voltage, the rise time, and the fall time of the main switch, respectively.

Conduction loss is another loss and depends on the ON-resistor for MOSFETs or voltage drop for diodes. Any of the power switches is in ON-state during a switching period. So all switches can be assumed as one switch for conduction loss calculation as follows:

$$P_{Con(Sm)} = R_{\rm DS(on\_Sm)}I_{o(\rm rms)}^2 \quad (35)$$

where $R_{{\rm DS(on}\cdot Sm)}$ is the ON-resistor of the main switch.

The total conduction loss of the main diodes is as follows:

$$P_{Con(Dm)} = V_{F(Dm)}I_o/\pi \quad (36)$$

where $V_{F(Dm)}$ is the forward voltage of the main diode.

2) Calculation for SS 3LT^{2}I: The main switches do not have switching loss but conduction loss in SS 3LT^{2}I. Main switches and diodes conduction losses are similar to HS 3LT^{2}I. The switching power loss does not occur on the auxiliary switches, and the total conduction loss is as follows:

$$P_{Con(Sa)} = R_{\rm DS(on\_Sa)}I_{Sa(\rm peak)}^2 D_{Sa} \quad (37)$$

where $R_{{\rm DS(ON}\cdot{\rm Sa})}$ is the ON-resistor of the auxiliary switch. D_{Sa} represents the duty cycle of the auxiliary switch and can be calculated as follows:

$$D_{Sa} = \left(\frac{2I_oL_{a1p}}{V_{\rm dc}} + \frac{\pi}{2}\sqrt{L_{a1p}C_{S1}} + t_{\rm opt}\right)f_{\rm sw} \quad (38)$$

where $t_{\rm opt}$ is an optional duration used to set ZVT time.

The total conduction loss of the auxiliary diodes is as follows:

$$P_{{\rm Con}(Da)} = V_{F(Da)}\left(I_{Sa}\pi\sqrt{L_{a1p}C_{a3}} + C_{a3}V_{\rm dc}\right)f_{\rm sw}/2 \quad (39)$$

where $V_{F(Da)}$ is the forward voltage of the auxiliary diodes.

The leakage inductor loss, the core loss, and the wire loss are formulated as follows, respectively:

$$P_{\rm Llk} = \frac{L_{lk}I_{Sa}^2}{2}f_{\rm sw} \quad (40)$$

$$P_{\rm Core} = K_cB_{\rm pk}^{\beta}f_{\rm sw}^{\lambda} \quad (41)$$

$$P_{\rm Wire} = \frac{R_wI_{Sa}^2}{2}\left(D_{Sa} + \frac{\pi\sqrt{L_{a1p}C_{a3}}}{2}f_{\rm sw}\right) \quad (42)$$

where L_{lk} is the leakage inductor, K_c, β, and λ are constants depending on the core, $B_{\rm pk}$ is the flux swing of the core, and R_w is the wire resistor.

TABLE II
POWER LOSSES OF EACH SEMICONDUCTOR DEVICE

Operation	Power losses (W)							
	Main switches	Neutral switches	Main diodes	Aux. switches	Aux. diodes	Additional	Total	η (%)
SS	2.2	2.2	3.2	6	2.4	3.2	19.2	98.1
HS	50.4	2.2	3.2	—	—	11.2	67	93.7

The calculations are realized for each semiconductor device used in HS and SS inverter operation at 1-kW output power to determine the switching and conduction losses, as Table II outlines.

D. Parasitic Effects on the Inverter

The parasitic capacitors of power MOSFETs have small values than the snubber capacitors. Therefore, parasitic capacitors are assumed in the snubber capacitors and are neglected in the theoretical analysis. However, the leakage inductor of coupled inductor leads to significant issues. The current stored in the leakage inductor leads to a high-voltage spike when the auxiliary switch is turned OFF. Besides, a power loss occurs because of the leakage inductor. A basic snubber is added to the parallel of the primary windings to overcome the voltage spikes. Hence, the peak voltage of the auxiliary switch is reduced to about 1.5 $V_{\rm dc}/2$, as illustrated in Fig. 5(b). A tight winding and a suitable core selection are required to reduce the leakage inductor issues. A powder core toroid is used in the coupled inductor since this core leads to low loss, and the air gap is evenly distributed in the core shape. Then, the value of the leakage inductor is reduced.

An oscillation occurs on the current flow through the main switch, which can be observed in Fig. 5(a), and this underdamped oscillation is expressed as follows [27]:

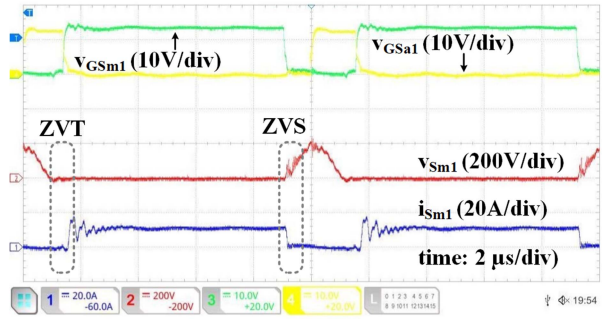
$$I(t) = K_1 e^{-\alpha t} \sin(\omega_r t) \tag{43}$$

where K_1 is the peak value of the oscillation current, α is the damping factor, and ω_r is the oscillation frequency. Ultimately, this oscillation does not affect the proposed inverter's SS or normal PWM operation.

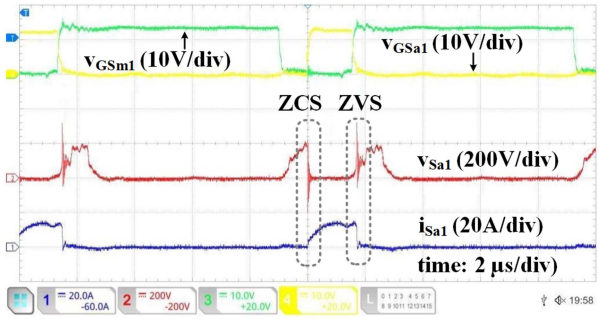
IV. HARDWARE IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

An experimental prototype of the proposed 3LT^{2}I is set up under 100 kHz switching frequency and 1 kW output power to verify the theoretical analysis. The semiconductor devices used in the proposed 3LT^{2}I are introduced in Table III. The corresponding fundamental parameters of the proposed inverter are summarized in Table IV.

Fig. 5 presents the voltage and current waveforms of both S_{m1} and S_{a1} with the control signals at full load. The voltage of S_{m1} has fallen to zero, and then the internal diode of the switch is turned ON with the aid of the snubber cell. The voltage



(a)



(b)

Fig. 5. Experimental results at full load. (a) Control signals of S_{m1}, S_{a1}, the voltage and current of S_{m1}. (b) Control signals of S_{m1}, S_{a1}, the voltage and current of S_{a1}.

TABLE III
SEMICONDUCTOR DEVICES USED IN THE PROPOSED INVERTER

Device	Part number	Mfr.	V (V)	I (A)	t_r (ns)	t_f (ns)	t_{rr} (ns)
Main sw.	FCA47N60	ONSEMI	600	47	450	160	590
Main D.	FFP30S60S	ONSEMI	600	30	N/A	N/A	40
Aux. sw.	FCP20N60	ONSEMI	600	20	290	140	530
Aux. D.	SF68G	TSMC	600	6	N/A	N/A	35

TABLE IV
PARAMETERS OF THE EXPERIMENTAL VERIFICATION

Symbol	Value	Unit
V_{dc}	400	V
L_{a1p}, L_{a2p}	10	μH
L_{a1s}, L_{a2s}	10	μH
C_{a1}, C_{a2}	6.6	nF
C_{a3}, C_{a4}	33	nF
Turns ration, n	1	N/A
Core (Kool Mμ)	77586	N/A
C_{F1}, C_{F2}	470	μF
Load resistor	16	Ω
Load inductor	500	μH

and the current of S_{m1} are zero when the switch is turned ON, as shown in the ZVT region in Fig. 5(a). Thus, the turning-ON switching power losses are eliminated by ZVT switching. Furthermore, when the switch is turned OFF, the voltage across the switch is zero, and then the voltage rises slowly with the aid of the equivalent snubber capacitor C_{S2}. Hence, the turning-OFF

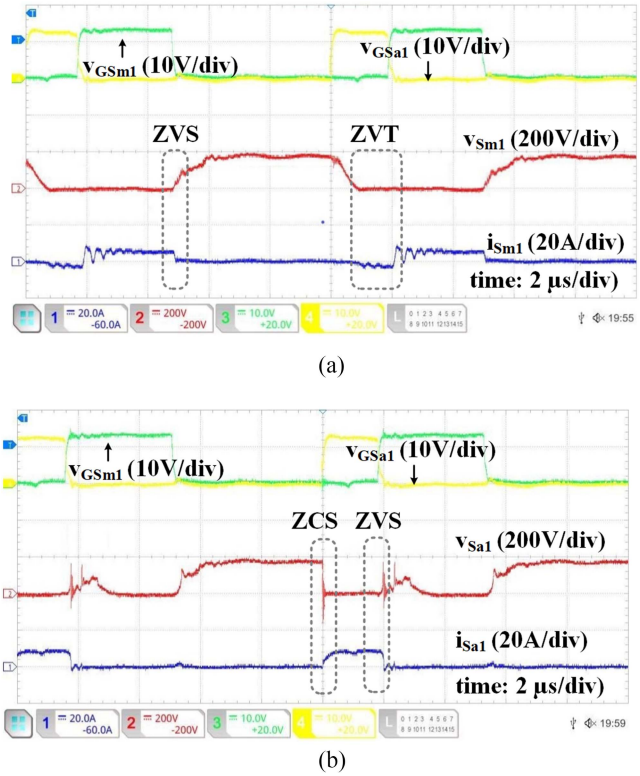


Fig. 6. Experimental results at light load. (a) Control signals of S_{m1}, S_{a1}, the voltage and current of S_{m1}. (b) Control signals of S_{m1}, S_{a1}, the voltage and current of S_{a1}.

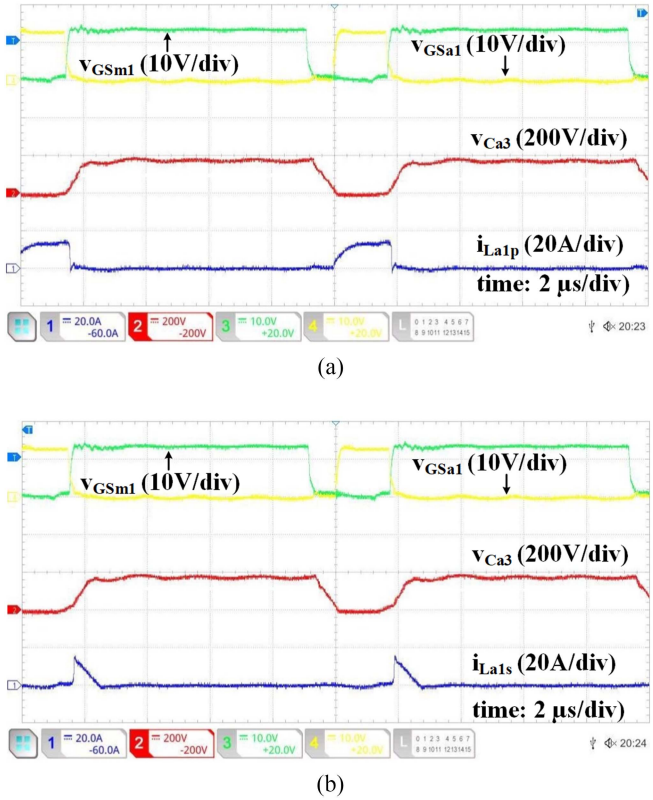


Fig. 7. Experimental waveforms at full load. (a) Control signal of S_{m1}, S_{a1}, the voltage of C_{a3} and the current of L_{a1p}. (b) Control signal of S_{m1}, S_{a1}, the voltage of C_{a3} and the current of L_{a1s}.

switching losses are significantly reduced by ZVS switching, as shown in the ZVS region in Fig. 5(a). The extra voltage or current stress does not occur on the S_{m1}.

Fig. 5(b) shows that the current of the auxiliary switch rises slowly because of the series L_{a1p} inductor when the switch is turned ON. The turning-ON switching power losses of S_{a1} are reduced by ZCS switching. Additionally, when the switch is turned OFF, the energy stored in the coupled inductor is transferred to the snubber capacitor C_{a3} by secondary inductor L_{a1s}. The voltage produced by L_{a1s} increases from zero to $V_{\rm dc}/2$ because the voltage across C_{a3} is zero when the switch is turned OFF. Finally, the turning-OFF switching power losses of S_{a1} are reduced by ZVS. The extra voltage stress does not occur on the S_{a1} and the current stress of the S_{a1} is significantly low.

Fig. 6 shows the voltage and the current waveforms of S_{m1} and S_{a1} with the control signals at light load. The main switch S_{m1} is turned ON by ZVT and turned OFF by ZVS, and also the auxiliary switch S_{a1} is turned ON by ZCS and turned OFF by ZVS under light load. Consequently, the proposed snubber cell properly works under light loads, and switching power losses are eliminated for the main switch.

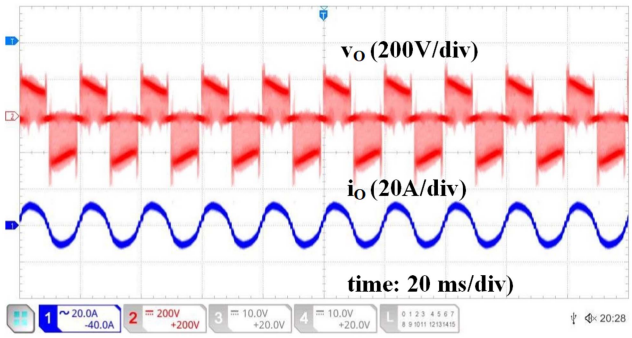
The control signals of the main and auxiliary switches, the voltage of snubber capacitor C_{a3}, and the current of the L_{a1p} and L_{a1s} are presented for the full output load in Fig. 7. Since the turns ratio of coupled inductor is one, the current levels of the primary and secondary windings are similar when the S_{a1} is turned OFF. The coupled inductor transfers its energy to the snubber capacitor C_{a3} and charges the C_{a3} to $V_{\rm dc}/2$. The maximum voltage level of C_{a3} cannot exceed $V_{\rm dc}/2$ and does not produce voltage stress on the semiconductor devices. The fully charged capacitor C_{a3} discharges when the main switch is turned OFF, which helps reduce the main switch's switching power losses during the turning-OFF process.

The voltage and the current waveforms for the input and output are presented in Fig. 8. The input voltage level $V_{\rm dc}$ is equal to 400 V when the maximum of the square output voltage level is equal to 200 V. Moreover, the output current is sinusoidal because the $Z_{\rm Load}$ is constructed by RL and the input current is a direct current.

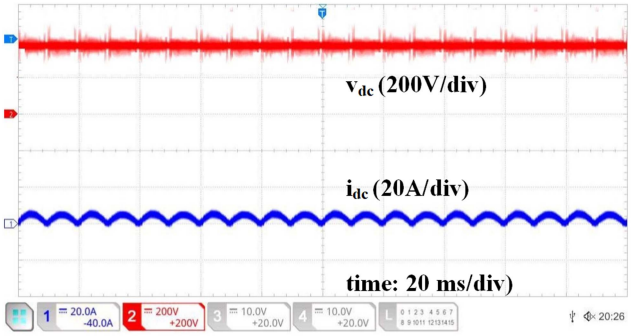
The overall efficiency of the proposed novel 3LT^{2}I is illustrated in Fig. 9. The maximum efficiency of the proposed SS inverter is 96.6% at the full output power, while the efficiency of the HS inverter is 92.4%. The calculated efficiency is presented in Table II. There is a difference of %1.5 between calculated and measured efficiency in SS operation. A difference of 1.3% occurs between calculated and measured efficiency in HS operation. These differences are from the unmeasurable losses and the nonlinearity of the components.

The proposed unique snubber cell can be easily implemented in other 3LI. The implementation of the novel snubber cell to a single-phase of an NPCI, and a voltage-source inverter is illustrated in Fig. 10.

The proposed inverter is compared with other SS 3LIs in the literature, and the comparison is presented in Table V. The study in [22] introduces a passive snubber cell, and the snubber



(a)



(b)

Fig. 8. Experimental waveforms at full load. (a) Output voltage and current. (b) Input voltage and current.

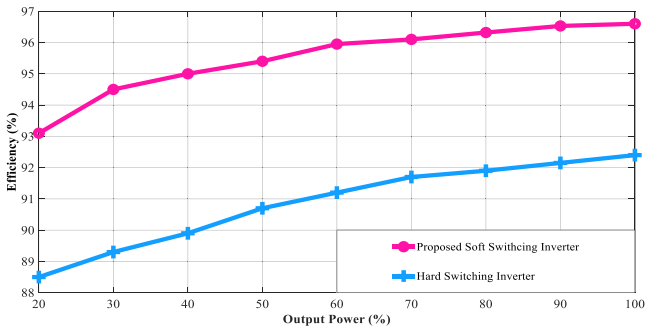
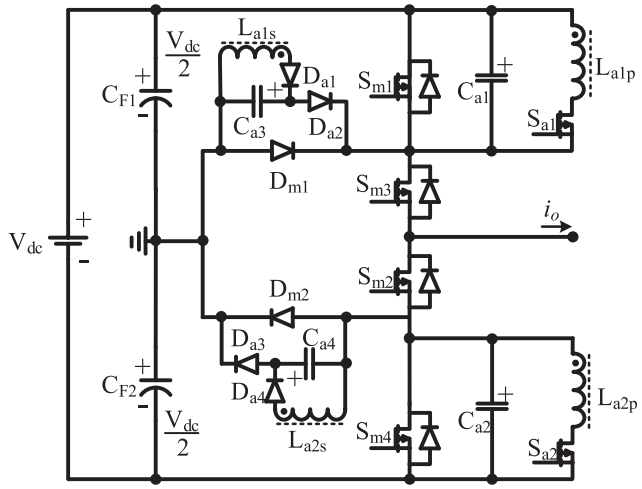


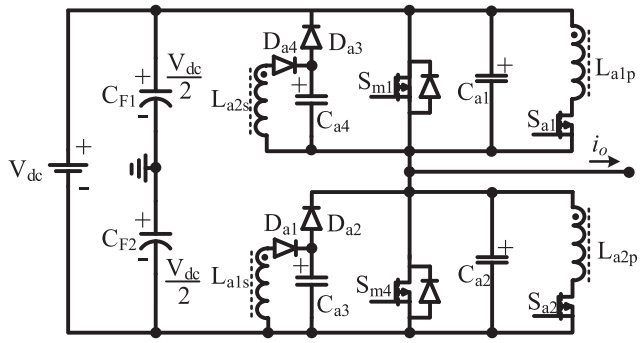
Fig. 9. Overall SS and HS efficiency curves of the proposed 3LT^{2}I.

has a simple structure. However, its switching frequency and efficiency are lower than the proposed inverter. The inverter introduced in [25] has an active snubber cell for T-Type inverters. This article is more expensive and has sophisticated control from the proposed inverter as it has more components and an extra flyback circuit. Furthermore, the proposed inverter has better efficiency owing to fewer conduction losses. The findings in [28] reveal that the converter has high efficiency since the switching frequency is only 3 kHz. However, SS does not require such low switching frequencies. Moreover, this inverter consists of many auxiliary semiconductors.

Consequently, the proposed inverter is cheaper, simpler in structure, and easier to control than the one proposed in [28].



(a)



(b)

Fig. 10. Implementation of the proposed snubber cell to a single phase of (a) NPCI and (b) VSI.

TABLE V
OVERVIEW COMPARISON OF THE PROPOSED INVERTER WITH OTHER SS 3LIS

Specification	Novel	Ref. [22]	Ref. [25]	Ref. [28]	Ref. [29]
Type of inverter	T-Type	T-Type	T-Type	NPC	NPC
Type of snubber	Active	Passive	Active	Active	Active
No. aux. switch	2	0	3	4	4
No. aux. diode	4	0	5	8	0
No. snubber L	0	2	1	4	2
No. snubber C	4	1	4	4	8
No. snubber coupled inductor	2	0	3	0	0
Input voltage	400 V	300 V	800 V	300V	600 V
Output voltage	120 V	110 V	220 V	N/A	380 V
Output power	1 kW	2.4 kW	1 kW	3kW	1.8 kW
Switching frequency	100 kHz	66.8 kHz	100 kHz	3 kHz	18 kHz
Output power	1 kW	2.4 kW	1 kW	3 kW	1.8 kW
Efficiency	% 96.6	% 96	% 94.8	% 99	N/A

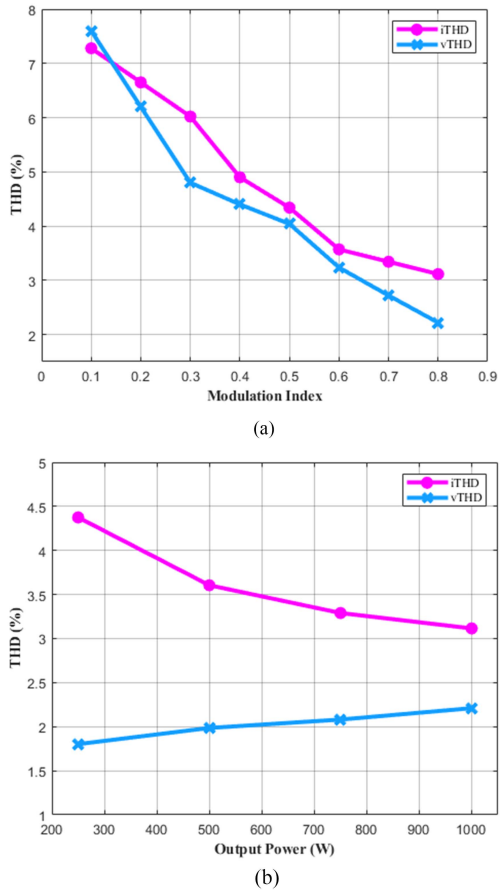


Fig. 11. iTHD and vTHD variations versus (a) modulation index and (b) output power.

The study in [29] includes many auxiliary passive components in addition to switches, and the switching frequency of the inverter is pretty low. Using more devices increases the cost of the inverter and complicates the control. Additionally, the conduction power loss increases and the total efficiency decreases since auxiliary inductors are connected to the main current path.

The total harmonic distortion (THD) performance of the proposed inverter has been analyzed and the output current THD (iTHD) and the output voltage THD (vTHD) curves are portrayed in Fig. 11. The percentage change of iTHD and vTHD according to the modulation index is presented in Fig. 11(a). The converter's THD performance is improving at a higher modulation index. Further, iTHD and vTHD are examined in terms of output load variations. The modulation index is chosen as 0.8 at the different loads since this modulation index provides minimum THD, and the THD curves are presented in Fig. 11(b). The iTHD is 3.27% and the vTHD is 2.2% at the full output power condition, which are well below the IEEE 1547 standards.

V. Conclusion

This article introduces a novel ZVT active snubber cell for a 3LT^{2}I. The main switches are switched by ZVT and ZVS at the turning-ON and the turning-OFF processes, respectively. Hence, the switching power losses of the main semiconductors are eliminated, and the total efficiency of the inverter is saved. The semiconductors in the snubber cell are switched with SS techniques. There are no extra voltage and current stress on the main semiconductor switches. The proposed snubber cell has a lower cost and a simpler structure than other SS 3LIs with active snubber cells due to the involvement of fewer devices. Moreover, the snubber cell has an easy control feature because of the common ground between the main and the auxiliary switches. A detailed theoretical analysis of the novel inverter is conducted, and an experimental prototype is set to demonstrate the theoretical analysis. The voltage and current waveforms for semiconductor devices are presented for full and light load conditions. The novel inverter is operated at 100 kHz switching frequency, and 96.6% peak efficiency is evaluated at 1-kW full output power.

References

[1] S. T. Meraj, K. Hasan, and A. Masaoud, "A novel configuration of cross-switched T-type (CT-type) multilevel inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3688–3696, Apr. 2020, doi: 10.1109/TPEL.2019.2935612.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981, doi: 10.1109/TIA.1981.4503992.

[3] M. F. Mohammed and M. A. Qasim, "Single phase T-type multilevel inverters for renewable energy systems, topology, modulation, and control techniques: A review," *Energies*, vol. 15, no. 22, Nov. 2022, Art. no. 8720, doi: 10.3390/en15228720.

[4] K. Kumari, S. Mapa, and R. Maheshwari, "Loss analysis of NPC and T-type three-level converter for Si, SiC, and GaN based devices," in *Proc. IEEE 9th Power India Int. Conf.*, 2020, pp. 1–6, doi: 10.1109/PICON49524.2020.9112873.

[5] Y. Sahin, N. S. Ting, E. Akboy, and I. Aksoy, "A new soft switching three level T-type inverter," in *Proc. 10th Int. Conf. Compat., Power Electron. Power Eng.*, 2016, pp. 314–318, doi: 10.1109/CPE.2016.7544206.

[6] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018, doi: 10.1109/TPEL.2017.2675381.

[7] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2072–2080, Mar. 2017, doi: 10.1109/TIE.2016.2627019.

[8] S. Bagawade, M. Pahlevani, and P. Jain, "Novel soft-switched three-phase inverter with output current ripple cancellation," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 1232–1248, Jan. 2023, doi: 10.1109/TPEL.2022.3203055.

[9] S. A. Chowdhury, S.-W. Kim, S.-M. Kim, J. Moon, I.-K. Cho, and D. Ahn, "Automatic tuning receiver for improved efficiency and EMI suppression in spread-spectrum wireless power transfer," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 352–363, Jan. 2023, doi: 10.1109/TIE.2022.3153820.

[10] Y. Sahin, N. S. Ting, and I. Aksoy, "A highly efficient ZVT-ZCT PWM boost converter with direct power transfer," *Elect. Eng.*, vol. 100, no. 2, pp. 1113–1123, Jun. 2018, doi: 10.1007/s00202-017-0546-y.

[11] M. S. Rana, D. Yogi, A. Gambhir, and S. K. Mishra, "Analysis and design of a zero-current switching non-isolated high gain inverter," *IEEE Open J. Power Electron.*, vol. 2, no. 2, pp. 614–626, Dec. 2021, doi: 10.1109/OJPEL.2021.3133274.

[12] N. S. Ting, F. Aslay, and Y. Sahin, "A novel zero voltage transition boost converter and artificial neural network-based estimation of converter efficiency," *Int. J. Circuit Theory Appl.*, vol. 50, no. 9, pp. 3251–3265, Sep. 2022, doi: 10.1002/cta.3337.

[13] A. Mondzik, R. Stala, S. Piróg, A. Penczek, P. Gucwa, and M. Szarek, "High efficiency DC–DC boost converter with passive snubber and reduced switching losses," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2500–2510, Mar. 2022, doi: 10.1109/TIE.2021.3063874.

[14] Y. Sahin and N. S. Ting, "Soft switching passive snubber cell for family of PWM DC–DC converters," *Elect. Eng.*, vol. 100, no. 3, pp. 1785–1796, Sep. 2018, doi: 10.1007/s00202-017-0655-7.

[15] B. Zhu, S. Chen, Y. Zhang, and Y. Huang, "An interleaved zero-voltage zero-current switching high step-up DC-DC converter," *IEEE Access*, vol. 9, pp. 5563–5572, 2021, doi: 10.1109/ACCESS.2020.3048387.
[16] X. Yu, J. Su, S. Guo, S. Zhong, Y. Shi, and J. Lai, "Properties and synthesis of lossless snubbers and passive soft-switching PWM converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3807–3827, Apr. 2020, doi: 10.1109/TPEL.2019.2939928.
[17] Z. Zhang, X. Yang, T. Q. Zheng, and J. Zhang, "A passive soft-switching snubber with energy active recovery circuit for PWM inverters," *IEEE Access*, vol. 8, pp. 100031–100043, 2020, doi: 10.1109/ACCESS.2020.2998147.
[18] J. Wei, B. Kou, L. Zhang, H. Zhang, and W. Chen, "Auxiliary snubber cell for dual buckfull bridge inverter," in *Proc. 22nd Int. Conf. Elect. Mach. Syst.*, 2019, pp. 1–6, doi: 10.1109/ICEMS.2019.8922528.
[19] E. Chu, Z. Wang, and Y. Kang, "Analysis and implementation of passive soft switching snubber for PWM inverters," *J. Power Electron.*, vol. 23, pp. 48–57, 2023, doi: 10.1007/s43236-022-00520-z.
[20] R. Heidari, E. Adib, K.-I. Jeong, and J.-W. Ahn, "Soft-switched boost-Cuk-type high step-up converter for grid-tied with half-bridge inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 786–795, Feb. 2023, doi: 10.1109/JESTPE.2022.3203614.
[21] E. Karimi, B. M. Tehrani, and E. Adib, "A soft-switching double-input micro-inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6721–6728, Aug. 2021, doi: 10.1109/TIE.2020.3000124.
[22] T. Chen and M. Narimani, "Soft-switching T-type multilevel inverter," *J. Power Electron.*, vol. 19, no. 5, pp. 1182–1192, Sep. 2019, doi: 10.6113/JPE.2019.19.5.1182.
[23] A. Pal and K. Basu, "A PWM ZVS high-frequency-link three-phase inverter with T-type NPC unfolder," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7146–7156, Sep. 2020, doi: 10.1109/TIE.2019.2942540.
[24] J. Deng, C. Hu, K. Shi, M. Chen, and D. Xu, "A ZVS-PWM scheme for three-phase active-clamping T-type inverters," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3951–3964, Mar. 2023, doi: 10.1109/TPEL.2022.3215204.
[25] H. Bodur, E. Akboy, and H. Yeşilyurt, "A new and modular active snubber cell for inverters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 288–296, Jan. 2020, doi: 10.1109/TIE.2019.2896126.
[26] A. Penczek, A. Mondzik, S. Piróg, M. Twaróg, and R. Stala, "New three-level soft turn-off T-type NPC inverter," in *Proc. 21st Int. Symp. Power Electron.*, 2021, pp. 1–5, doi: 10.1109/Ee53374.2021.9628388.
[27] H. Hizarci, U. Pekperlak, and U. Arifoglu, "Conducted emission suppression using an EMI filter for grid-tied three-phase/level T-type solar inverter," *IEEE Access*, vol. 9, pp. 67417–67431, 2021, doi: 10.1109/ACCESS.2021.3077380.
[28] Z. Szular, B. Rozegnal, and W. Mazgaj, "A new soft-switching solution in three-level neutral-point-clamped voltage source inverters," *Energies*, vol. 14, no. 8, Apr. 2021, Art. no. 2247, doi: 10.3390/en14082247.
[29] N. He, Y. Chen, D. Xu, K. Ma, and F. Blaabjerg, "A new zero voltage switching three-level NPC inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2309–2316, doi: 10.1109/APEC.2015.7104671.

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