Control Development and Fault Current Commutation Test for the EDISON Hybrid Circuit Breaker

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***Abstract*—The dc circuit breaker is an indispensable building block for dc network systems. Hybrid circuit breakers that combine mechanical and solid-state switches have more potential to be utilized in dc distribution networks because of their lower conduction losses and fast interrupt speed. The efficient energy dc interrupter with surge protection (EDISON) removes any solid-state circuit in the main current path, thereby substantially reducing the conduction losses during normal operations. However, it requires a dedicated control with fast dynamics because any false triggering of the mechanical switch or solid-state switches of the breaker would lead to a commutation failure and a potential unquenchable arc. This article proposes an FSM-based control scheme that guarantees the accurate and fast control response during a fault event. Due to this fast response requirement, a dual-core-CPU-based control architecture is applied featuring parallel taskings and negligible communication delays between the two cores. Furthermore, a control-law accelerator is employed to further reduce the latency of the program execution by 33%. The controller hardware-in-the-loop (CHIL) model of the EDISON breaker is implemented in OPAL-RT to verify the control scheme and derisk the prototype test. A fifth-order *RLC* network is developed to characterize the mechanical switch behavior such that the hybrid circuit model can be simulated in the CHIL solely by circuit components. Finally, the proposed control scheme is implemented and validated in a prototype test with a 3 kA interrupting current and a 60 A/μs current commutation rate.**

***Index Terms*—Controller hardware-in-the-loop (CHIL), dc circuit breaker, finite-state-machine (FSM), medium-voltage direct-current (MVdc) system.**

I. Introduction

MEDIUM-VOLTAGE direct-current (MVdc) distribution networks have become increasingly popular in various applications, such as dc microgrids [1], dc electric shipboards [2], offshore wind farms [3], electrified aircraft [4], and data centers [5]. Lower distribution losses and higher power densities cause dc systems to be more advantageous over ac distribution networks. However, risks associated with electrical faults continue to stifle the expansion of dc networks. In contrast to ac systems in which natural current zero-crossing points inherently exist, dc systems deliver power without zero crossings, making the traditional circuit breakers ineffectual in fault scenarios [6]. Therefore, developing a fast and reliable dc circuit breaker is critical to benefit from dc systems fully [7], [8].

One commonly used dc circuit breaker in lower voltage applications is the mechanical circuit breaker [9], [10], [11], [12], [13], [14], [15], [16], [17]. However, the inherent lack of current zero-crossing points limits this type of breaker's voltage scalability, making arc quenching extremely difficult. Furthermore, the mechanical switching speed falls between 1 and 100 ms, making it unsuitable for ubiquitous use in MVdc systems as faster fault clearing is required. Solid-state circuit breakers, however, overcome the disadvantages of the mechanical switches with possibly less than a 300 μs interrupting time [3], [18], [19], [20]. By leveraging the benefits of wide-bandgap devices with fast switching speeds and high-voltage blocking capabilities, the solid-state circuit breakers have become propitious in the MVdc systems [21], [22]. Despite being fast and scalable in voltage ratings, the solid-state breakers suffer from conduction losses causing complex thermal designs. Hence, a hybrid dc circuit breaker that combines the merits of the mechanical switch and the solid-state switch could be a more promising solution to the MVdc systems [23], [24], [25], [26], [27], [28], [29], [30], [31], [32].

The state-of-the-art hybrid circuit breaker proposed by ABB requires solid-state switches in the main current path, where

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conduction losses are still present [29]. However, the efficient energy dc interrupter with surge protection (EDISON) proposed in [12], [30] uses a fault current commutation circuit (FC3) in the commutation branch, thus eliminating solid-state switches in the main current path and realizing negligible conduction losses. By turning OFF insulated-gate bipolar transistors (IGBTs) in the commutation branch, the fault current will eventually flow to metal-oxide varistors (MOVs) where the energy is dissipated. Moreover, the piezo-based mechanical switch with a supercritical environment operates with approximately a 250 μs opening time compared with the traditional mechanical switches.

To provide the accurate and fast control for the EDISON breaker with a 3 kA interrupting current and a 60 A/μs current commutation rate, the following requirements need to be met.

1) *Correct control sequence:* Any false triggering of the mechanical switch or IGBTs in a wrong sequence will result in a giant unquenchable arc that could fail the current commutation and destroy the breaker.
2) *Fast fault response and minimized control delay:* Since the current commutation time is aimed below 50 μs, the controller must be fast enough in response to the current slew rate. Any additional delay caused by the controller or the measurement would postpone the current commutation process and increase the peak value of a fault current, which eventually could lead to a fault current interrupting failure.

This article, thus, presents the control implementation in the EDISON breaker to address the above challenges. A finite-state-machine (FSM) based control scheme is developed to guarantee that the triggering of the mechanical switch and the IGBTs is in the correct sequence in response to the fault events. Time delays from both hardware and software operations are carefully broken down and examined to implement an optimized operation. Since the mechanical switch demands a supercritical environment, the temperature and pressure are monitored with 1 kHz sampling rates, which are primarily limited by the bandwidth of the temperature and pressure sensors [25]. Since the current commutation process is time critical, the minimized latency of the control execution is preferred. Hence, a comparative analysis of four distinct methods of implementing the FSM, including a dual-core implementation, a single-core implementation without postprocessing blocks (PPBs) [33], a single-core implementation with PPB from a single ADC module, and a single-core implementation with PPB from three separate ADC modules. It is found that the dual-core-CPU-based control scheme features low latency and higher extensibility for more inputs while maintaining relatively low coding complexity among the four methods. This architecture permits the hybrid circuit breaker to broaden its monitoring and protection capabilities to encompass a wider range of elements, such as the FC3 precharger, IGBT monitoring, historical data storage and retrieval, and so forth. Hence, this article endeavors to archive the development of the controller on a dual-core architecture that accommodates multi-threaded applications. Consequently, the dual-core-CPU-based control scheme is adopted where one CPU (namely, CPU 1) is responsible for monitoring the status of the mechanical switch with 1 kHz, whereas the other CPU (namely, CPU 2) is used for implementing the FSM control with 125 kHz. The communication between the two cores is via DSP internal buses, and thus, the communication delay is negligible. To further reduce the control latency, a comprehensive time delay breakdown is investigated, and a CLA is employed to increase the bandwidth of the CPU so that the execution time is shortened by 33%. The proposed control method and its implementation not only reveals the challenges associated with the time sequence and minimized delay in generic dc circuit breakers but also provides a viable solution for the development of time-critical control for dc circuit breakers.

To verify the proposed control scheme and derisk the hardware prototype, a control hardware-in-the-loop (CHIL) model is implemented in OPAL-RT. A fifth-order *RLC* network is used to characterize the mechanical switch behavior because the travel distance of the mechanical switch is dependent on the voltage applied across the mechanical switch [17]. To that end, the proposed CHIL model comprising mechanical components and solid-state switches is solely represented by circuit components. The control scheme is implemented with the CHIL model to verify its effectiveness. Finally, the control scheme is validated in the experimental prototype with a 3 kA interrupting current, 60 A/μs current commutation rate, and 50 μs current commutation time.

The rest of this article is organized as follows. In Section II, the operation principles of the EDISON breaker accompanied by the mathematical model of the variable inductor are described. In Section III, the FSM-based control method is introduced followed by a detailed delay time breakdown. The CHIL modeling results and the experimental results are discussed in Section IV and Section V, respectively. A comparison of the EDISON breaker with a few selected state-of-the-art hybrid breakers is presented in Section VI. Finally, Section VII concludes this article.

II. OPERATION PRINCIPLE OF THE EDISON BREAKER

Fig. 1 shows the circuit diagram of the EDISON hybrid circuit breaker. The main current path consists of a variable inductor and a mechanical switch. The commutation branch includes an FC3 and series-connected IGBTs with MOVs. The variable inductor, designed for saturation at nominal current flow, desaturates and exhibits high impedance as i_{main} approaches zero, allowing the mechanical switch to be turned OFF near the zero current. The capacitor of the FC3 is precharged before a fault occurs. R_s, R_M, and R_{loop} represent the source parasitic resistance, the mechanical switch resistance, and the loop parasitic resistance, respectively. It should be noted that the 2 mΩ resistance of the mechanical switch, which encompasses all contact, conductor, and interfacial resistances, is considered the worst-case scenario. L_s and L_{loop} represent the source inductance and the loop stray inductance, respectively. The capacitor is charged by the charger prior to the connection of the circuit breaker to the main circuit.

To illustrate the operation principle of the EDISON breaker, a simulation model is built in PSIM. Table I summarizes the

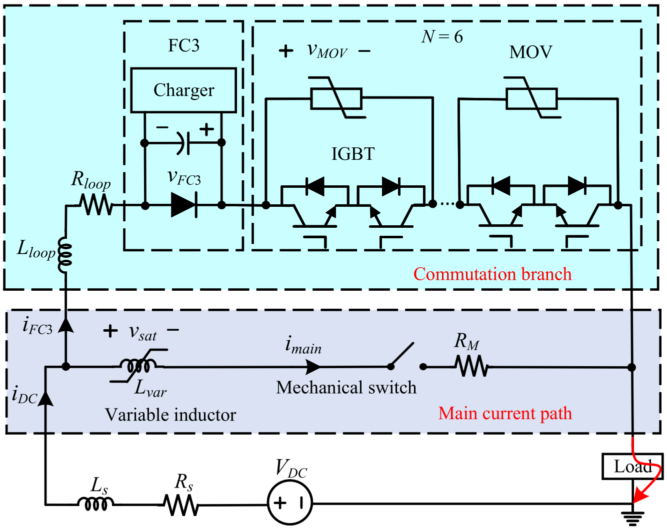


Fig. 1. Circuit diagram of the EDISON breaker.

TABLE I
CIRCUIT PARAMETERS OF THE EDISON BREAKER FOR CIRCUIT SIMULATIONS

Description	Symbol	Value
Rated dc voltage	V_{DC}	12 kV
Rated dc current	i_{DC}	2 kA
FC3 voltage	v_{FC3}	280 V
FC3 capacitance	C_{FC3}	250 µF
Loop inductance	L_{loop}	300 nH
Source inductance	L_s	300 µH
Source resistance	R_s	10 mΩ
Mechanical switch resistance	R_M	2 mΩ
Loop parasitic resistance	R_{loop}	1 mΩ
Submodule count	N	6
MOV clamping voltage	v_{MOV}	4 kV
ON-state voltage drop of single IGBT	$v_{\mathrm{on,drop}}$	3 V

system ratings and circuit parameters. In the simulation, the IGBTs are adopted from Infineon FZ750R65KE3 [34] with a detailed Spice model. The typical ON-state voltage drop for each IGBT is 3 V. The maximum blocking voltage for a single IGBT can reach up to 6.5 kV so that the total voltage blocking capabilities for six submodules can be up to 39 kV, which is three times higher than the dc source voltage [28]. Fig. 2 shows the key simulation results.

A. Normal Operation (0–t_0)

During the normal operation, the IGBTs are all turned OFF, and the mechanical switch is turned ON. The nominal dc current flows through the main current path via the mechanical switch, as shown in Fig. 3(a). Since the variable inductor is saturated by the dc current, its inductance is negligible (i.e., $L_{\mathrm{var}} \approx 0$). Meanwhile, the conduction losses during normal operation are negligible because no solid-state switches are in the main current path.

B. Fault Detected (t_0–t_1)

Fig. 3(b) shows that when a short circuit occurs, the current flowing through the main path will rapidly increase. The fault

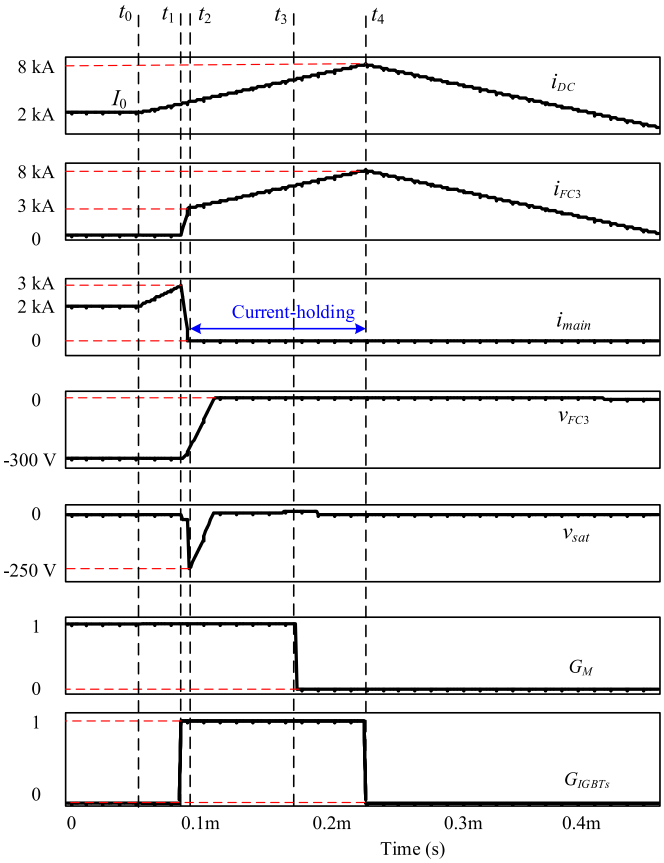
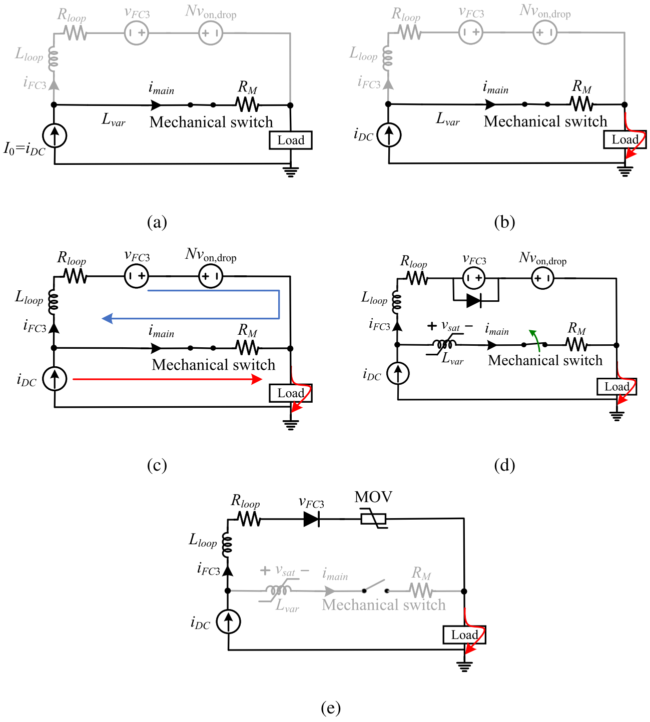


Fig. 2. Simulation waveforms of the EDISON breaker.



(a) (b) (c) (d) (e)

Fig. 3. Equivalent circuit of the EDISON breaker. (a) Normal operation. (b) Fault detected. (c) Commutation process. (d) Current-holding period. (e) Energy absorption.

current is given as follows:

$$i_{\mathrm{DC}} = i_{\text{main}} = \frac{V_{\mathrm{DC}}}{L_s} t + I_0 \tag{1}$$

where I_0 is the initial current before a fault occurs. The increasing rate is determined by L_s and V_{DC}. When the current reaches the threshold (3 kA), the fault interrupt procedure will be initiated.

C. Commutation Process (t_1–t_2)

During the commutation process, the controller triggers all the IGBTs to be turned ON. The FC3 capacitor discharges a loop current that superimposes on the fault current in the opposite direction. The rate of the current generated by the FC3 can be calculated as follows:

$$\frac{di_{\mathrm{FC3}}}{dt} = \frac{1}{L_{\text{loop}}} \left(v_{\mathrm{FC3}} - N v_{\text{on,drop}}\right) \tag{2}$$

where v_{FC3} is the capacitor voltage of the FC3; $v_{\text{on,drop}}$ is the ON-state voltage drop of the IGBTs. Hence, the rate of i_{main} is

$$\frac{di_{\text{main}}}{dt} = \frac{di_{\mathrm{DC}}}{dt} - \frac{di_{\mathrm{FC3}}}{dt}. \tag{3}$$

It should be noted that L_{loop} is primarily determined by the busbar inductance, which is in the range of several hundred nH to 3 μH, depending on the physical layouts and voltage levels [35], [36], [37]. L_{loop} should be minimized to ensure fast current commutation. Compared with L_s in the MVdc systems [38], L_{loop} can be thousands of times smaller. As a result of the rate of i_{FC3} being much larger than that of i_{DC}, i_{main} decreases rapidly from the threshold current. Based on the energy required for commutation, the minimum required voltage for the FC3 can be estimated as follows:

$$\frac{1}{2} C_{\mathrm{FC3}} \cdot v_{\mathrm{FC3}}^2 \geqslant \frac{1}{2} L_{\text{loop}} \cdot i_{pk}^2 \tag{4}$$

where i_{pk} is the threshold current at which the commutation process begins. Moreover, the voltage level of the FC3 is subject to various constraints, including the power rating of the charger, physical size, insulation requirements, and so on. With regard to (4) and the system parameters, only a few hundred volts are needed for the precharged capacitor to commutate the fault current at the medium-voltage level (12 kV). Once the FC3 voltage is selected, the capacitance of FC3 can be estimated as follows:

$$C_{\mathrm{FC3}} = \frac{L_{\text{loop}}^2 i_{pk}^2}{v_{\mathrm{FC3}}^2}. \tag{5}$$

Accurate sizing of the FC3 can be accomplished through a time-domain circuit analysis. The equivalent circuit during the commutation process is depicted in Fig. 3(c), where the fault current, i_{DC}, is modeled as a current source with a specified rate of rise (represented by the red line). The FC3 discharges a countercurrent (represented by the blue line) to neutralize the fault current in the main current path. We have

$$C_{\mathrm{FC3}} \frac{dv_{\mathrm{FC3}}}{dt} = -i_{\mathrm{FC3}} \tag{6}$$

$$v_{\mathrm{FC3}} - N \cdot v_{\text{on,drop}} = i_{\mathrm{FC3}} \cdot (R_M + R_{\text{loop}}) + L_{\text{loop}} \frac{di_{\mathrm{FC3}}}{dt} \tag{7}$$

$$i_{\text{main}} = i_{\mathrm{D\,C}} - i_{\mathrm{FC3}}. \tag{8}$$

Equations (6)–(8) dictate that the following conditions must be satisfied for a successful commutation.

1) The main path current must reach zero at the conclusion of the commutation process, i.e., $i_{\text{main}}(t_2) = 0$. t_2 marks the completion of the commutation process.
2) The FC3 voltage must be greater than the IGBTs' ON-state voltage drop, i.e., $v_{\mathrm{FC3}}(t_2) \geq N v_{\text{on,drop}}$.

These constraints provide solutions for the FC3 voltage and capacitance.

It is shown that during the commutation process, the voltage across the variable inductor v_{sat} ramps up in the negative direction as the main current decreases. G_{IGBTs} represents the controller output signal of all the IGBTs. Thus, G_{IGBTs} has high outputs at t_1, initiating the commutation process.

D. Current-Holding Period (t_2 — t_4)

Fig. 3(d) illustrates the equivalent circuit of the circuit breaker during the current-holding period. During this current-holding period, the main current is regulated within a range (±10 A), thanks to the large inductance of the desaturated variable inductor. The rate of i_{main} is

$$\frac{di_{\text{main}}}{dt} = \frac{V_{\mathrm{D\,C}}}{L_s} - \frac{v_{\mathrm{FC3}} - N v_{\text{on, drop}}}{L_{\text{loop}} + L_{\text{var}}}. \tag{9}$$

In this scenario, the variable inductor becomes the dominant component relative to L_{loop}. This increase in inductance leads to a decrease in the rate of i_{FC3}, thereby limiting the rate of i_{main}. It should be noted that the ±10 A threshold value of the EDISON breaker is established by its mechanical switch. It demonstrates the amount of current that the mechanical switch can quench. In other words, this 10 A threshold value remains the same as long as the mechanical switch remains unchanged.

During t_2 and t_3, the main path current remains almost zero, and the fault current was commutated to the commutation branch. At t_3, the mechanical switch is completely turned OFF, as is indicated by G_M.

The inductance of the variable inductor L_{var} can be calculated as follows:

$$L_{\text{var}} = \frac{\partial \lambda}{\partial i_{\text{main}}} = \frac{n A_{\text{core}} \frac{\partial B}{\partial t}}{\frac{\partial i_{\text{main}}}{\partial t}} \tag{10}$$

where λ is the magnetic flux linkage; B is the magnetic flux density; A_{core} is the surface area through which the main current passes; and n represents the winding turns.

According to Ampere's law

$$\frac{\partial i_{\text{main}}}{\partial t} = \frac{l_m}{n} \frac{\partial H}{\partial t} \tag{11}$$

where l_m is the magnetic length path; H is the magnetic field. Meanwhile, $\frac{\partial B}{\partial t}$ can be written as follows:

$$\frac{\partial B}{\partial t} = \frac{\partial B}{\partial H} \cdot \frac{\partial H}{\partial t}. \tag{12}$$

Combining (10)–(12), L_{var} can be reorganized as follows:

$$L_{\text{var}} = \frac{n^2 A_{\text{core}}}{l_m} \cdot \frac{\partial B}{\partial H}. \tag{13}$$

When the core gets saturated, the magnetic field is given as follows:

$$H_{\text{sat}} = \frac{B_{\text{sat}}}{\mu_0 \mu_r} \tag{14}$$

where B_{sat} is the magnetic flux density when the core gets saturated and is provided by the manufacturers; μ_0 and μ_r are the vacuum permeability and relative permeability, respectively.

The relationship between the magnetic flux density B and the magnetic field H can be derived from the *B–H* curve as follows:

$$\frac{\partial B}{\partial H} = \begin{cases} \mu_0, & i_{\text{main}} \geqslant I_{\text{sat}}(\text{saturated}) \\ \mu_0 \cdot \mu_r, & i_{\text{main}} < I_{\text{sat}}(\text{desaturated}) \end{cases}. \tag{15}$$

Therefore, according to (13) and (15), the inductance can be expressed as follows:

$$L_{\text{var}} = \begin{cases} \mu_0 \cdot \frac{n^2 A_{\text{core}}}{l_m}, & i_{\text{main}} \geqslant I_{\text{sat}}(\text{saturated}) \\ \mu_0 \cdot \mu_r \cdot \frac{n^2 A_{\text{core}}}{l_m}, & i_{\text{main}} < I_{\text{sat}}(\text{desaturated}) \end{cases}. \tag{16}$$

Based on Ampere's law, the corresponding saturation current is

$$I_{\text{sat}} = \frac{l_m}{n} \cdot H_{\text{sat}} = \frac{l_m}{n} \cdot \frac{B_{\text{sat}}}{\mu_0 \mu_r}. \tag{17}$$

Based on (16), it can be found that the inductance of the desaturated inductor is μ_r times than that of the saturated inductor. For nanocrystalline magnetic cores, μ_r is approximately 15 000 [39]. Under normal operation, the nominal main path current saturates the variable inductor, and the inductance is approximately 1 nH, which is negligible. In contrast, once the main current approaches zero, the variable inductor desaturates and becomes a large inductor (approximately 10 μH), which restricts the rate of i_{FC3} and, in turn, limits the rate of i_{main}, as shown in Fig. 3(d).

During the current-holding period, the inductance of the desaturated variable inductor L_{var} (i.e., 10 μH) is hundreds of times larger than that of the loop stray inductance L_{loop} (i.e., 300 nH), and therefore holds the current within $\pm$10 A. In addition, even if the zero crossing of the main current occurs during a nonfault condition (e.g., for the sake of maintenance), the inductance of the desaturated inductor is one order of magnitude smaller than that of the source inductance L_s (i.e., 300 μH). As a result, even during the nonfault condition with a zero current, the variable inductor has negligible effects on the normal operation.

E. Energy Absorption

At t_4, the IGBTs are all turned OFf, and the fault current flows into the MOVs where the energy is absorbed, as shown in Fig. 3(e).

III. FSM-BASED CONTROL FOR THE EDISON BREAKER

Any false triggering of the mechanical switch or the IGBTs would cause significant issues. For instance, if there is any electromagnetic interference (EMI) noise induced from the cables or the high current slew rate during the commutation process, the signal conditioning circuit and the controller would be contaminated and could be falsely triggered to turn OFFthe mechanical switch under thousands of current amperes. This false turning OFFof the mechanical switch would lead to a catastrophic failure, and the entire system would be damaged. Such a catastrophe would also occur if the IGBTs were falsely triggered. As a result, it is of great importance to develop a robust control scheme capable of dealing with contingencies and providing the correct control sequence.

Moreover, the mechanical switch with supercritical fluids requires a certain temperature and pressure [25]. Any abnormal temperature and pressure will also impact the current interrupting capabilities. To that end, it is critical to monitor the real-time condition of the mechanical switch in terms of the temperature and pressure.

A. FSM-Based Control Scheme

Table II presents the logic rules of 16 states based on four inputs received by the controller. The four inputs are as follows.

1) Temperature, pressure, and ready signal of the auxiliary power supply (PS): Temperature and pressure sensors are used to monitor the status of the mechanical switch. If the temperature or the pressure is not within the desired range, it will send a signal to the controller to indicate its malfunction. The auxiliary PS for the charging circuit is also critical, as the FC3 voltage determines whether the fault current can be fully commutated to the commutation branch. Therefore, the status of the auxiliary PS, in conjunction with the temperature and pressure status, is the precondition for the circuit breaker's normal operation.
2) Current sensor in the main path: The trigger signal for the current sensor is generated by comparing the detected current with the established threshold currents. To increase the noise immunity, a hysteresis comparator is utilized [40]. Upon attainment of the upper threshold, the output will register as low, generating a falling edge that signifies an electrical fault occurrence. Conversely, upon reaching the lower threshold, the output will become high, generating a rising edge. The falling edge of the current sensor output will be classified as "0" in FSM, while the ascending edge is classified as "1," as depicted in Table II. Typically, commercial hall-effect current sensors for the MVdc system have a 0.3% accuracy and 150 kHz bandwidth (denoted as f_c). Since the sensor delay is related to the bandwidth given by $\tau = \frac{1}{2\pi f_c}$, the minimum resolution that the sensors can distinguish is approximately 15 A with 1 μs delay when considering the threshold of 5 kA. This value is higher than the arc quenching limit of the mechanical switch, posing significant challenges for the system to detect the accurate zero-crossing point. Therefore, detecting the

TABLE II
TRUTH TABLE OF THE FSM

States	Temperature/Pressure/ Auxiliary PS 0: Normal operation 1: Malfunction	Main path current sensor 0: Rising edge 1: Falling edge	Safe-to-open signal 0: Rising edge 1: Falling edge	Mechanical gauge sensor 0: Mechanical switch closed 1: Mechanical switch opened
Malfunction	1	X*	X	X
	0	X	0	1
Normal	0	0	0	0
Commutation	0	1	0	0
Open the mechanical switch	0	X	1	0
Energy absorption	0	X	1	1

*X indicates that it does not matter if it is 1 or 0.

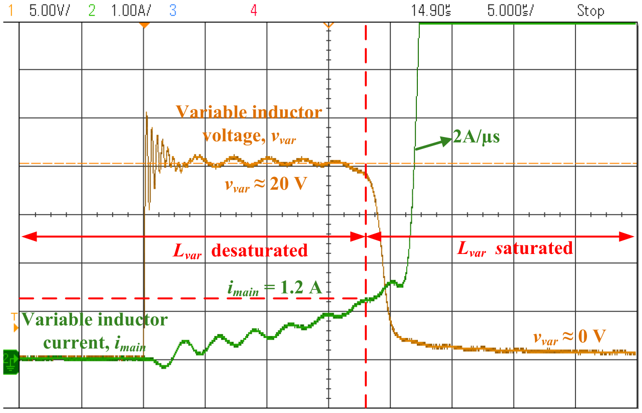


Fig. 4. Safe-to-open voltage signal generated under the desaturated inductor.

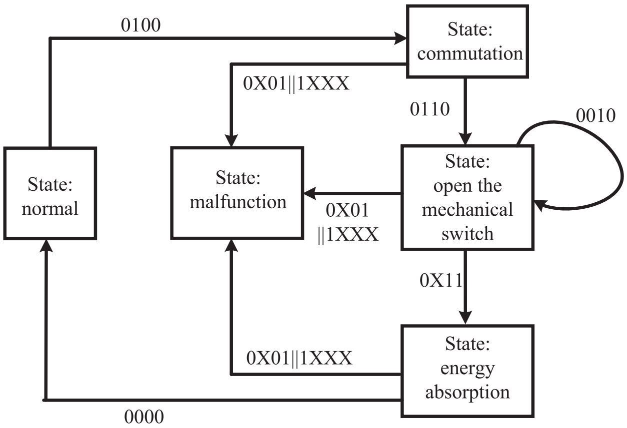


Fig. 5. FSM flowchart.

accurate zero-crossing point relies on the safe-to-open signal.

3) Safe-to-open signal: The safe-to-open signal is used to indicate that the current is small enough such that it is safe to open the mechanical switch without an arc. Fig. 4 shows the voltage and current relationship of the variable inductor L_{var} under saturated and desaturated regions. The variable inductor is desaturated when the inductor current is less than 1.2 A. Under this condition, the variable inductor voltage v_{var} is 20 V. In contrast, when the current increases, the variable inductor suddenly gets saturated, and the voltage across it becomes approximately zero. Based on the voltage differences of the variable inductor within its saturated and unsaturated regions, a safe-to-open signal can be generated. During the fault event, the current increases with a positive *di/dt* and the inductor is saturated. The voltage across it is approximate to zero but remains greater than 0. This voltage is then compared with a negative threshold voltage to generate the safe-to-open signal. In this case, as the negative threshold voltage is less than the voltage across the inductor, the safe-to-open is low. On the other hand, when the commutation process begins, the current drops rapidly with a negative *di/dt*, leading to an increase in the voltage across the inductor but with a negative sign. Thus, the safe-to-open becomes high. After the commutation process is completed, the inductor desaturates with a positive voltage. Hence, the safe-to-open signal returns to low again. Since the state machine is edge-trigger based, the state machine will interpret the rising edge of the safe-to-open signal output (i.e., transition from low to high) as 0 and the falling edge (i.e., transition from high to low) as 1, as shown in Table II. During the transition from commutation to current-holding time, the safe-to-open signal transits from high to low accordingly, indicating that the current is now below the threshold value of the mechanical switch and it is safe-to-open.

4) Mechanical gauge sensor: The mechanical gauge sensor measures the travel distance between the mechanical switch contacts. Once the distance between the contacts is wide enough to build up enough voltage withstanding capabilities, it is defined as an open state. Otherwise, it is closed during normal operation with negligible resistance.

Fig. 5 shows the FSM flowchart where the digits correspond to the truth table bits in precisely the same order. State 0100, for example, represents that the current has reached the threshold value. With this FSM, only five states are needed. The state machine guarantees the unidirectional flow that can prevent the false triggering of the mechanical switch and IGBTs.

Fig. 6 shows the hardware connection diagram between the controller and system components. Since all the system components are isolated from the high-voltage side, the low-voltage box needs no additional insulation. Proper grounding and isolation between the low-voltage signal conditioning circuits and the high-current power loop is the key to being immune to high

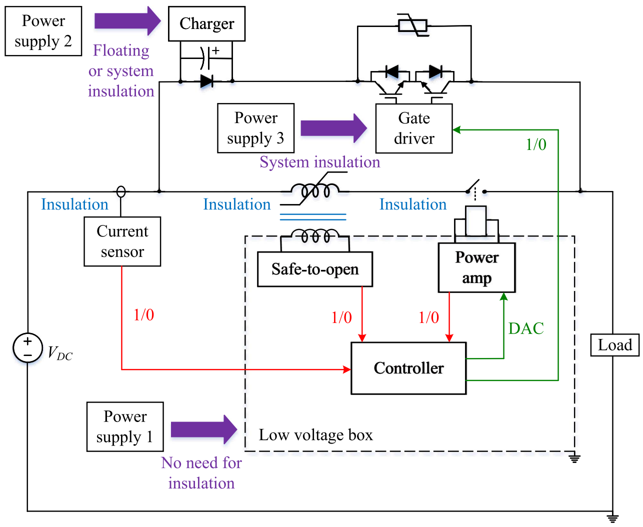


Fig. 6. Controller diagram with the auxiliary PS and system insulation.

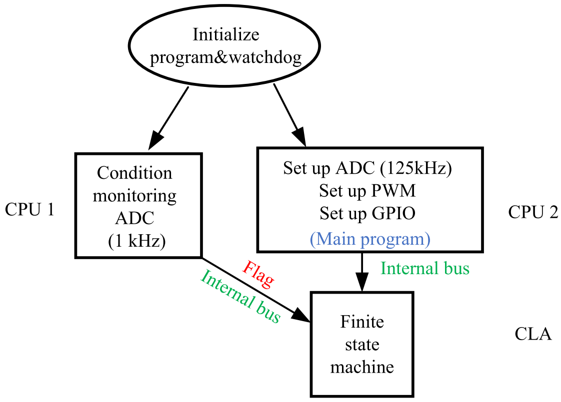


Fig. 7. Dual-core CPU control implementation with the CLA.

noise generated by high current; thus, false triggering by EMI noise can be prevented [41], [42].

B. Time Delay Breakdown and Optimization

The accurate and fast response from the controller is indispensable since the slew rate of the fault current is extremely high. The delay results in a slight increase in the main path current beyond the expected threshold. To accommodate this higher current, the mechanical switch and FC3 must be designed with appropriate safety margins. As a result, it is critical to investigate the time delay and propose an optimal control to shorten the latency as much as possible.

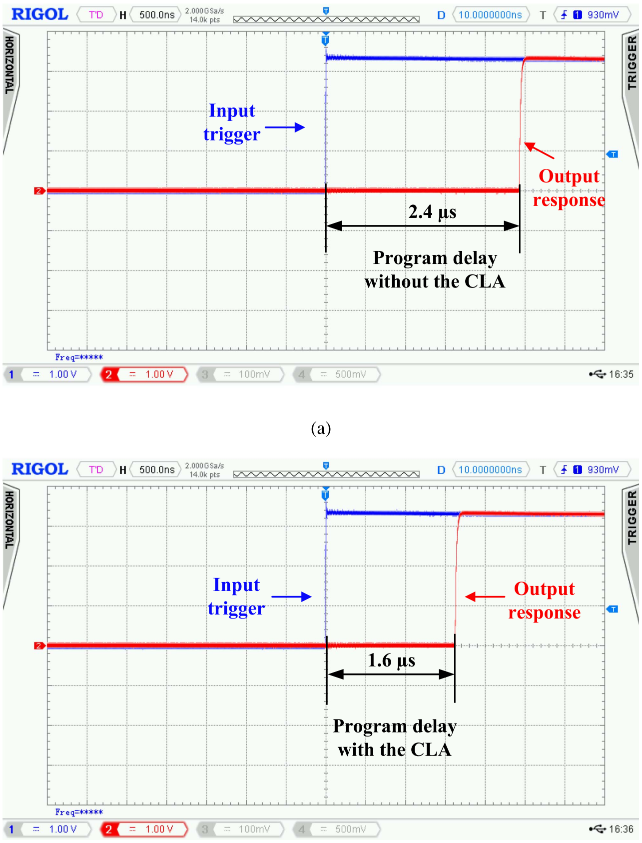
To increase the program's execution speed, the CLA is used [33]. The CLA is independent of the CPU in response to the peripheral interrupts so that it can free up the CPU for other tasks and increase the CPU bandwidth. The implementation of this control on the TI 28379D launchpad is illustrated in Fig. 7.

To test the delay time of the control program, a signal generator is used to generate a triggering signal for the state machine so that it can enter each state to run the whole control program. Two approaches are used to measure the delay. One is to set a breakpoint in the TI code composer studio (CCS) by calculating how many cycles are used; the other approach is to toggle the general purpose input/output (GPIO) output high and observe the delay via an oscilloscope.

1) Delay between GPIO input and output: This delay is defined as the time interval between the input pin receiving the signal and the output being toggled high as is set in the control. The rising edge delay is 196 ns, while the falling edge delay is 288 ns from the measurement. Another method to measure it is through the CCS software by counting cycles. With a CPU speed 200 MHz, it is shown that the rising edge takes 36 cycles (i.e., $\frac{1}{200\,\text{MHz}} \cdot 36 = 180\,\text{ns}$), while the falling edge takes 54 cycles (i.e., $\frac{1}{200\,\text{MHz}} \cdot 54 = 270\,\text{ns}$), which shows great agreement with the hardware measurement.
2) Delay between GPIO input and DAC output: This delay is the time interval between the input pin receiving the signal and the generated DAC output. Since the DAC is used to drive the power amplifier of the mechanical switch, it is essential to measure this type of delay to prevent any failure to turn OFFthe mechanical switch. It is found that the delay is approximately 800 ns from the measurement. The delay measured by counting the cycles is 157 cycles.
3) Comparison of the program execution time: The program execution time is defined as the state machine that runs to completion, which includes not only the delay between the GPIO input and output as well as the delay GPIO input and DAC output, but also the interrupt service routine and the FSM execution time. Fig. 8 shows the program execution time with and without the CLA. It can be seen that with the CLA, the whole program execution time reduces by 33% (from 2.4 to 1.6 μs). The delays measured by counting the cycles without the CLA and with the CLA are 478 and 317 cycles, respectively. Therefore, the CLA is a huge differentiator in terms of achieving fast and accurate control.

It should be noted that the sampling rate for monitoring the status of the mechanical switch (i.e., temperature and pressure) and auxiliary PS (i.e., charging for FC3) is approximately 1 kHz, which is limited by the sensor bandwidth, whereas the sampling rate for the other three inputs (i.e., main path current, safe-to-open, and the travel distance of the gauge) is up to 125 kHz, which is constrained by the switching speed and control delay. Therefore, to increase the speed of the control execution time, a dual-core microcontroller, TI 28379D is used where one CPU core is only used to monitor the status of the mechanical and auxiliary PS, whereas the other core is used to implement the FSM. The communication of two CPUs is achieved by a one-bit flag via an internal bus, which has little time delay. Compared with the single-core CPU approach, this dual-core CPU control features parallel tasking. The code for monitoring the condition of the mechanical switch and the FSM control is executed independently on two cores, thus reducing the delay significantly.

An alternative approach is to utilize the PPB of the ADC modules. The comparison function is integrated within the PPB and



(a)

(b)

Fig. 8. Control program execution delay. (a) Without the CLA. (b) With the CLA.

can be promptly employed following the ADC conversion. As a result, the monitoring aspect can be delegated to a single CPU. A comparative analysis of four distinct methods of executing the FSM is conducted, including (a) dual-core implementation, (b) single-core implementation without PPB, (c) single-core implementation with PPB from a single ADC module, and (d) single-core implementation with PPB from three separate ADC modules. To evaluate the relative merits and limitations of these four methods, two cases were analyzed. Case 1: Normal operation of the monitoring; Case 2: An abrupt malfunction in the monitoring. For method (b), the monitoring and the fast control loop (i.e, 125 kHz) are executed in a single core with two separate interrupt routines. Given that the monitoring of the system is a prerequisite for the effective operation of the fast control, the monitoring is prioritized in the interrupt nesting hierarchy. There are two viable options for the PPB implementation: one option is to use the ADC channels from a single module (e.g., ADCINA0, ADCINA1, and ADCINA2), while another option is to employ three separate modules (e.g., ADCINA0, ADCINB0, and ADCINC0). Consequently, the single core with PPB implementation is divided into two distinct variations, represented by methods (c) and (d), respectively.

It is found that, in case 1, the monitoring interrupt will not activate and the dual-core operates like a single-core executed at 125 kHz with 1.6 μs execution time, resulting in no distinguishable differences among the four methods. However, the independent operation of the dual core facilitates an instantaneous interruption of the fast control loop in response to the malfunction in monitoring. Nonetheless, for method (b), the monitoring interrupt is prioritized and executed prior while the fast control loop awaits, leading to a 480 ns delay. This delay encompasses code execution for the monitoring aspects, nesting of interrupts, and restoration of relevant registers. Due to this delay, the total time of the fast control loop amounts to 2.1 μs, restricting the maximum fast control loop frequency to about 500 kHz beyond which the code execution becomes incomplete.

TABLE III
COMPARISONS OF DIFFERENT METHODS TO IMPLEMENT THE FSM

Methods	Metrics		
	Latency	Extensibility for more inputs	Code complexity
(a) Dual-core	Low	High	Relative low
(b) Single-core without PPB	High	Relative high	High
(c) Single-core with PPB from 1 ADC module	Relative low	Relative high	High
(d) Single-core with PPB from three ADC modules	Low	Low	Low

To conclude, Table III summarizes the comparative analysis of the various methods for implementing the FSM from various perspectives. From a latency perspective, the dual-core approach [method (a)] is similar to the PPB approach [method (c) and method (d)] and exhibits a 25% reduction compared with method (b). While no discernible difference between methods (c) and (d) is observed in our scenario, it can be anticipated that method (c) will incur a slightly extended delay compared with method (d) in situations where multiple interrupts are required for multiple ADC inputs. The extended delay is due to the necessity of accessing the ADCEVTSTAT register to identify the source of the interrupt [33]. In terms of the extensibility of inputs, the dual-core method offers the greatest capability with access to all peripherals independently. On the other hand, method (d) may not be as favorable as method (c) in this regard, as there are only four available modules. In terms of coding complexity, methods (a) and (d) are more favorable as they do not require interrupt nesting or access to the data register, which are necessary in method (b) and method (c), respectively.

The proposed dual-core approach presents low latency, a slight increase in structure and coding complexity, but great extensibility for handling multiple inputs and data processing, in comparison to the single-core PPB method. This architecture permits the hybrid circuit breaker to broaden its monitoring and protection capabilities to encompass a wider range of elements, such as the FC3 precharger, IGBT monitoring, historical data storage and retrieval, and so forth. Hence, this article endeavors to archive the development of the controller on a dual-core architecture that accommodates multithreaded applications.

Fig. 9 shows a comprehensive time delay breakdown of the control scheme. When the current reaches the threshold value at T_1, the first contributor to the delay is the pick-up delay,

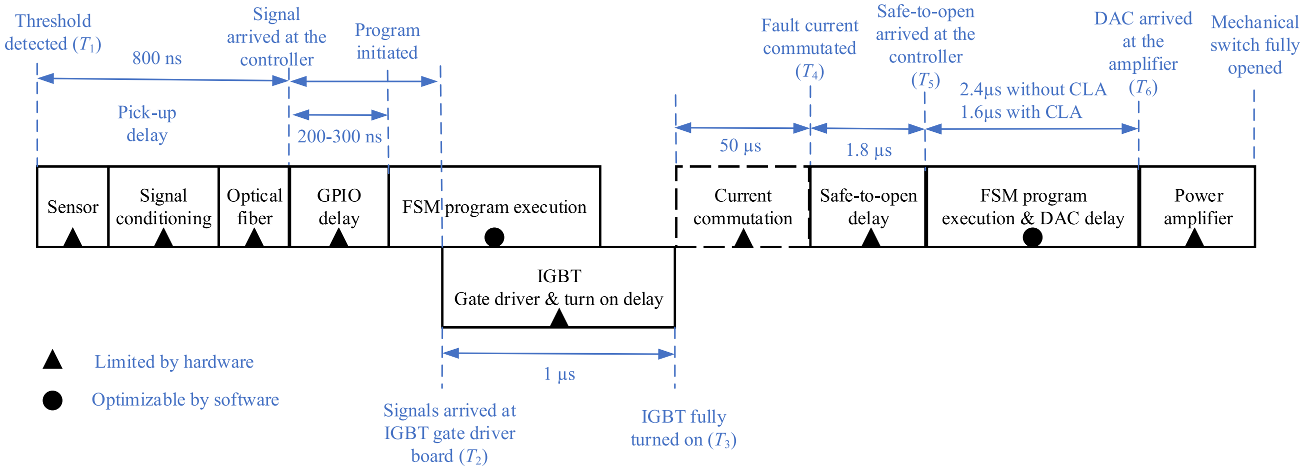
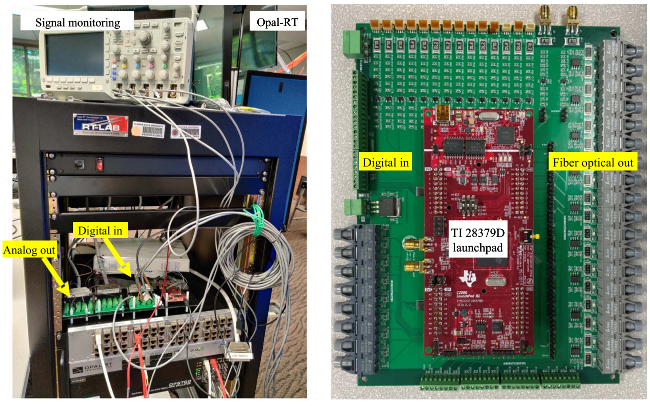


Fig. 9. Breakdown of the control delay.

including the current sensor, the signal conditioning circuit, and the optical fiber transmission delays. The total pick-up delay is approximately 800 ns, and it is mainly dependent on the selected hardware. The second part of the delay is the GPIO delay that takes up to 200–300 ns. The major part of the delay comes from the program execution. Once the state machine enters the commutation state, the IGBT triggering signal will be sent to the gate driver boards at T_2. The delay of the gate driver boards and fully turning ON IGBTs at T_3 is approximately 1 μs. After the commutation is completed at T_4, the safe-to-open signal is generated from the desaturated variable inductor at T_5. The safe-to-open delay between T_4 and T_5 is 1.8 μs. The state machine continues running to turn OFFthe mechanical switch by sending out a DAC signal. The program execution delay combined with the DAC delay in total is 1.6 μs with the CLA used.



(a) (b)

Fig. 10. CHIL system configuration. (a) OPAL-RT configuration for the EDISON breaker's circuit model. (b) Control board configuration for the EDISON breaker's control.

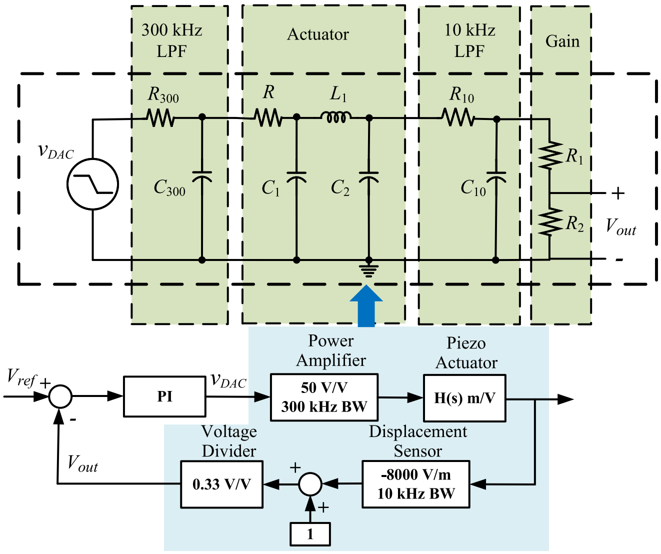


Fig. 11. Fifth-order circuit model of the mechanical switch.

IV. CHIL VERIFICATION OF THE CONTROL SCHEME

A. CHIL System Configuration

Fig. 10(a) shows the configuration of the CHIL system. The CHIL model is built in Simulink and will be implemented in OPAL-RT. Fig. 10(b) shows the interface board with the TI Launchpad. The purpose of the control board is for signal conditioning and noise filtering.

B. Mechanical Switch Circuit Model

Fig. 11 shows the *RLC* circuit model of the mechanical switch. In Fig. 11, the power amplifier moves the mechanical switch using a piezoactuator. The displacement sensor measures the contact distance, which is converted into a voltage signal V_{out} and compared with the desired travel curve V_{ref}. The error of V_{out} and V_{ref} will be tuned by the proportional integral (PI) controller and the output is the desired output voltage v_{DAC} to drive the mechanical switch; therefore, the contact distance is controlled by the voltage signal v_{DAC}. The primary of the PI objective control is to minimize overshoot and undershoot, which are the primary causes of insulation failures. A relatively

TABLE IV
RLC NETWORK REPRESENTATION OF MECHANICAL SWITCH

Symbol	Value
R_{300}	$1\,\Omega$
R_{10}	$1\,\Omega$
R_1	$1\,\mathrm{M}\Omega$
R_2	$118\,\mathrm{k}\Omega$
R	$100\,\Omega$
L_1	$2.64\,\mathrm{mH}$
C_1	$496\,\mathrm{nF}$
C_2	$549\,\mathrm{nF}$
C_{300}	$0.5\,\mu\mathrm{F}$
C_{10}	$15\,\mu\mathrm{F}$

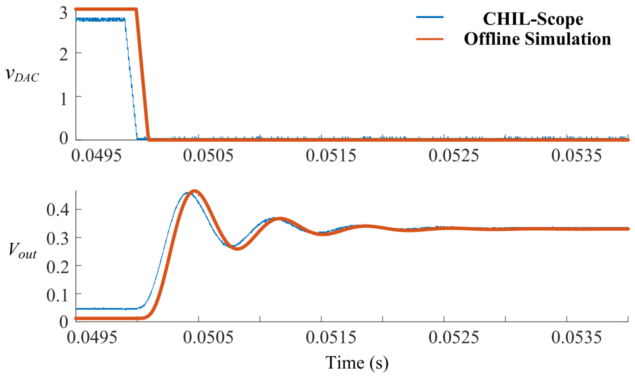


Fig. 12. CHIL and offline simulation results of v_{DAC} and V_{out}.

low proportional gain is used to prioritize minimized oscillations over settling time [17]. As a result, the mechanical system can be represented with a higher order *RLC* network where the output voltage controls the travel distance of the mechanical switch actuators.

The mechanical switch model encompasses a power amplifier, a piezo-based actuator, a displacement sensor, and a voltage divider. The power amplifier can be modeled with a 300 kHz bandwidth low-pass filter with a voltage ratio of 50:1, while the actuator model can be modeled as a third-order *LC* network [25]. The displacement sensor is also a low-pass filter with a 10 kHz bandwidth. With this model, the mechanical switch can be built in OPAL-RT with solely passive elements. The circuit parameters of the *RLC* network are presented in Table IV.

The solver time step of OPAL-RT is 200 ns, and the DAC signal v_{DAC} is from the control board while the output of the voltage V_{out} is measured via an oscilloscope. The offline simulation is built on the PSIM and compared with the CHIL model to verify the control scheme. Fig. 12 shows the DAC output and the driving voltage of the mechanical switch during the opening process of the mechanical switch. The DAC voltage v_{DAC} decreases from 3.3 V to 0, while the voltage across the piezocontact starts to increase to open the contacts of the mechanical switch. Once the mechanical switch is completely turned OFF, the control output voltage for the piezoactuator will maintain a constant at 0.33 V. The initial v_{DAC} in the CHIL results is slightly lower than 3.3 V. This discrepancy with the offline simulation is caused by the signal conditioning circuit board connected to OPAL-RT. It is found that the CHIL simulation matches the offline simulation well.

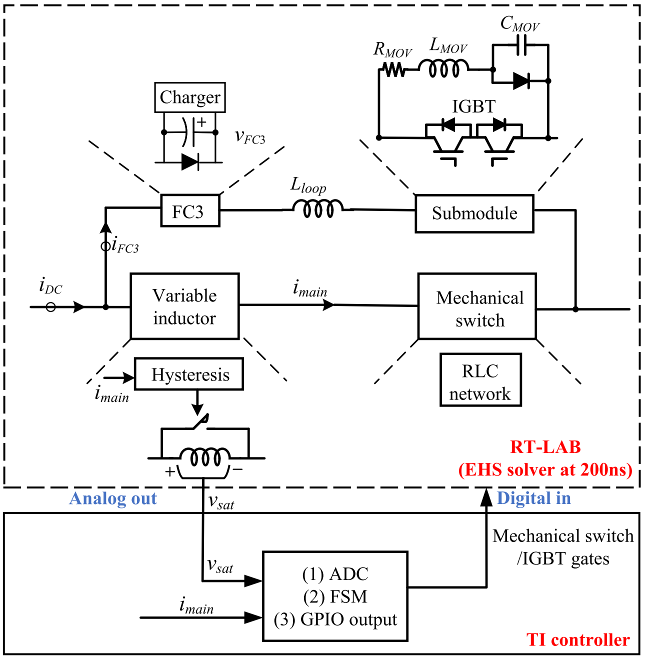


Fig. 13. Implementation of the EDISON breaker in the CHIL system.

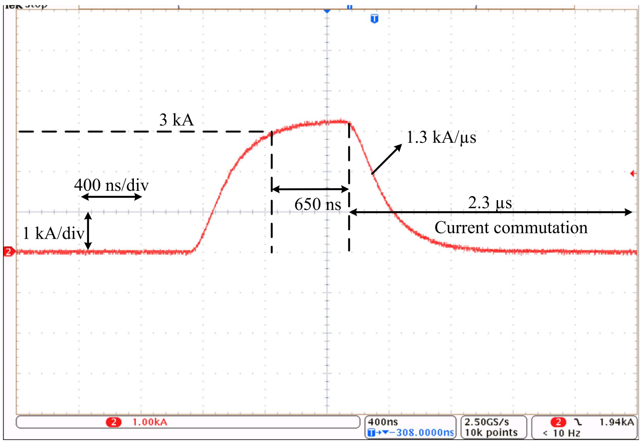


Fig. 14. CHIL test results of EDISON breaker.

C. CHIL System Results

Fig. 13 shows the implementation of the EDISON breaker in the CHIL system. Since the MOV and the variable inductor are not readily available in OPAL-RTs library, the MOV is represented by a diode and a snubber circuit, while the variable inductor is represented by an inductor that is in parallel with an ideal switch to mimic the saturation and desaturation effect. The mechanical switch is represented by the fifth-order *RLC* circuit, as shown in Fig. 11. The inductance and resistance are identical to those of Table I.

Fig. 14 shows the CHIL test results where the fault current takes about 2.3 μs to complete the current commutation with a $1.3\,\mathrm{kA}/\mu\mathrm{s}$ slew rate under 600 V FC3 capacitor's voltage. The time delay between the threshold detected and the beginning of the commutation is about 650 ns. Because the CHIL results are based on the analog outputs from OPAL-RT as opposed to the

TABLE V
HARDWARE LIST

Components	Manufacturer	Part number
IGBT	Infineon	FZ750R65KE3
MOV	Littlefuse	V142CA60
FC3 capacitor	Kyocera	AVX FFVE410107
Current sensor	LEM	LF-2010
DC PS	Magna	XR series
FC3 charging circuit	Texas Instruments	LMG3410-HB-EVM
Controller PS	Delta Electronics	PMT-24V50W1AA
Variable inductor's core	VAC T60006	L2050-V146

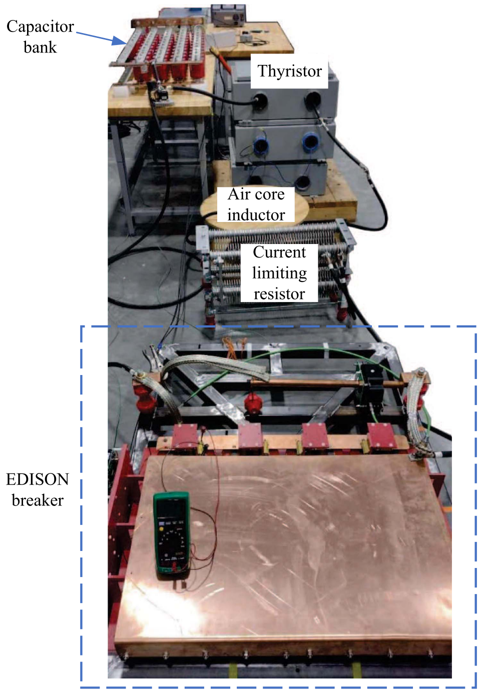
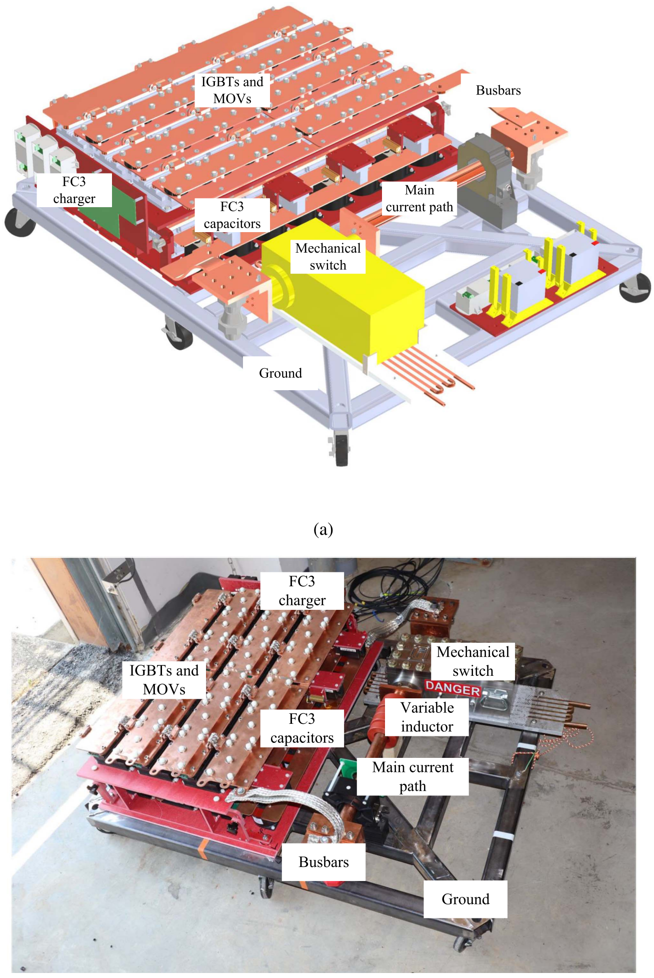


Fig. 15. Experimental setup for the current commutation test.



(a)

(b)

Fig. 16. CAD model and hardware prototype of the EDISON breaker. (a) CAD model. (b) Hardware prototype.

experimental tests where the current sensors cause delay, the time delay is slightly shorter.

V. EXPERIMENTAL VERIFICATION

Table V lists the experimental specification, and Fig. 15 shows the experimental setup for the current commutation test. A capacitor bank with an air-core source inductor is used to mimic 3 kA current with a higher slew rate of the fault current. A capacitor bank is precharged by a dc PS from the Magna XR series with a 1.2 kV dc voltage rating. A thyristor is added to enforce a fault condition.

Fig. 16 shows the computer-aided design (CAD) model of the EDISON breaker and its hardware prototype. IGBTs in the commutation branch can withstand 6.5 kV maximum rated voltages. The MOVs are capable of clamping 1750 V dc voltage, and the maximum allowed pulse current is up to 70 kA. For each submodule, three MOVs are connected in series to increase the voltage clamping capabilities. The film capacitors of the FC3 are charged by a boost converter to boost the voltage up to 300 V. The control circuit is powered by a 24 V dc PS. The variable inductor cores have a high relative permeability (i.e., $\mu_r = 15\,000$).

Fig. 17 shows the experimental waveforms of the current commutation test. At T_1, the fault current reaches the threshold value (3 kA), and the current commutation process is initiated with the current sensor output being low. Because of the falling edge of the current sensor output, the controller responds to the fault event by turning ON the IGBTs in the commutation branch at T_2. The delay time between T_1 and T_2 is 1.2 μs due to the execution time of the control program, including GPIO delay and the state machine program. The fault current continues to rise until T_3 because of the IGBT gate driver and IGBT turn-ON delays, taking 1 μs to fully turn ON the IGBT. The main path current will drop with 60 A/μs slew rate during the commutation process, which takes 50 μs to reach zero crossing at T_4. During this commutation process, the safe-to-open signal becomes high because of the negative rate of the main path current. Once the current is small enough, the voltage across the variable inductor will increase due to the desaturation of the inductor; hence, the

TABLE VI
COMPARISON OF THE EDISON BREAKER AND A FEW SELECTED HYBRID CIRCUIT BREAKERS

Reference	Year	Voltage rating	Nominal current	Interrupting current	Current Commutation rate	Current commutation time	Commutation switches
[15]	2017	200 V	18 A	18 A	2.3 A/µs	6 µs	Antiseries MOSFETs
[43]	2018	175 V	500 A	500 A	0.11 A/µs	4.4 ms	N/A
[10]	2019	300 V	7 A	20 A	1.3 A/µs	15 µs	H-bridge
[23]	2019	1 kV	100 A	100 A	5 A/µs	20 µs	IGBT module
[44]	2022	100 V	25 A	25 A	0.05 A/µs	0.5 ms	Antiseries MOSFETs
[45]	2022	100 V	40 A	50 A	0.1 A/µs	0.5 ms	Antiseries MOSFETs
[13]	2022	600 V	30 A	30 A	3 A/µs	10 µs	JFET+IGBT
EDISON	2022	12 kV	2000 A	3000 A	60 A/µs	50 µs	Diode+capacitor

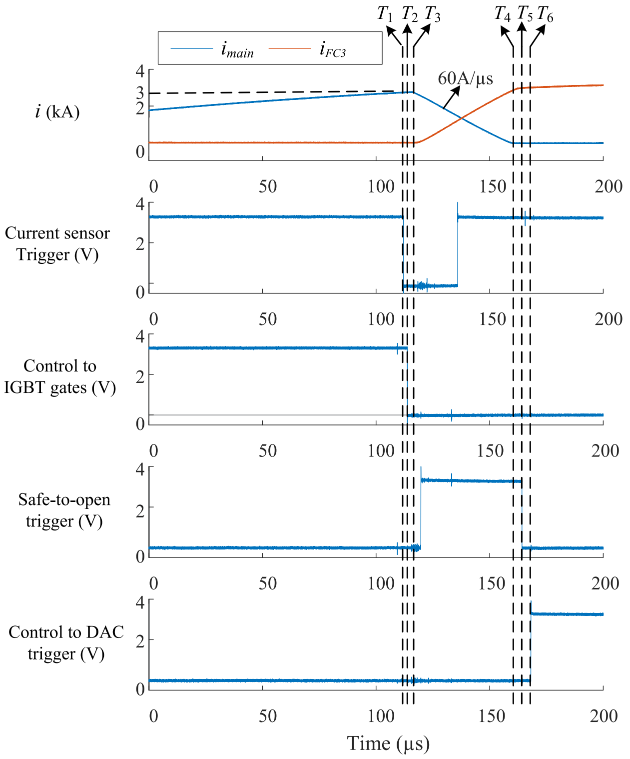


Fig. 17. Experimental waveforms of the current commutation test.

safe-to-open signal becomes low at T_5. The delay time between T_4 and T_5 is 1.8 μs because of the hysteresis characteristics of the *B–H* curve. Once the control safe-to-open signal is created, the mechanical switch starts to open at T_6. The time delay between T_5 and T_6 is about 1.6 μs, which is due to the program execution and the DAC output delay.

VI. DISCUSSION AND COMPARISON OF THE STATE-OF-THE-ART DC CIRCUIT BREAKERS

Table VI compares the key features between the existing hybrid circuit breakers and the EDISON breaker. In this table, the voltage rating, nominal current, interrupting current, current commutation rate, current commutation time, and commutation switches are listed.

A recent hybrid circuit breaker developed in [15] utilizes a newly invented emitter turn-OFF(ETO) as its solid-state switching device. ETOs have a faster interrupting speed than the traditional silicon-controlled rectifier (SCR) thyristors that have a longer reverse recovery time. Unlike the EDISON breaker with the FC3 assisting the commutation, the interrupting speed of the breaker proposed in [15] is still dictated by the switching device. However, the ETO is still not commercially available, and more research efforts are needed to investigate its properties.

Ray et al. [10] and Shen et al. [13] use coupled inductors to achieve current commutation. However, the coupling coefficients must be carefully designed, and the magnetic properties of the inductors would limit its current commutation slew rate.

Pei et al. [43] require a cryogenic environment that is still difficult to achieve in real applications. Bartosik et al. [23] still need a fuse to interrupt the fault current, which slows down the current commutation process.

The essential difference between the various hybrid circuit breakers lies in the technique used to achieve commutation. It should also be noted that the commutation switches of the EDISON breaker (i.e, FC3) rely solely on a capacitor and a diode for commutation, rendering it a cost-effective option as a passive circuit compared with the active switch-based counterparts.

The current commutation time for the EDISON breaker is 50 μs with a 60 A/μs slew rate. In spite of the fact that the requirement for controlling such a fast circuit breaker, involving a coordinated control of both the mechanical and solid-state switches with high current, is much more stringent, the proposed control scheme herein is able to tackle this challenge and offer insights for other generic MVdc hybrid circuit breakers' modeling and control development.

VII. CONCLUSION

This article has proposed the accurate and fast control scheme for a novel MVdc hybrid circuit breaker that has 3 kA current interrupting capabilities and 50 μs current commutation time. Because of the current commutation time, the EDISON breaker poses enormous challenges to the control scheme in terms of the guarantee of the correct control sequence.

The operation principle of the circuit is demonstrated and verified in offline simulation. An FSM is proposed to guarantee the control sequence. Since the latency is critical in high-current commutation processes, a thorough time delay breakdown of the entire control sequence is investigated. It reveals that the CLA accelerates the control execution speed by 33%. To derisk the entire system before performing high-power tests, a CHIL model is built with a fifth-order *RLC* network representing the mechanical switch so that a hybrid of the mechanical switch and solid-state switches can be simulated in CHIL solely with circuit models. During the experimental verification, a total time of 50 μs with a 60 A/μs slew rate of the current commutation is measured. Finally, the comparisons of the EDISON breaker with other state-of-the-art hybrid circuit breakers highlight the superiority of the proposed control strategy.

It is possible to further increase the fault interrupting speed, which is mainly dictated by the speed of the mechanical switch. Therefore, the feasibility of optimizing the operating condition of the mechanical switch to achieve faster interrupting speeds will be discussed in future work.

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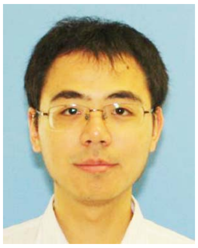

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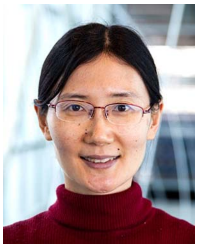

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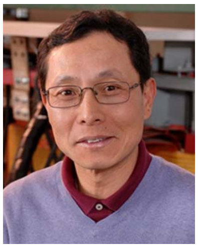

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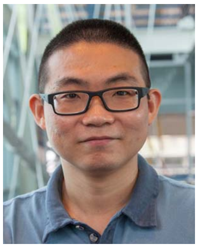

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