Characterization of Electrical Switching Safe Operation Area on Schottky-Type P-GaN Gate HEMTs

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***Abstract*—Gallium nitride (GaN) high electron mobility transistors (HEMTs) have demonstrated their superior performance in consumer electronics. However, their longer-lifetime-demanding application has not been well-explored yet, due to the limited electrical reliability, especially the existence of ON-resistance degradation in hard-switching conditions. In this article, four testing modes, including double-pulse testing (DP), continuous hard switching testing (HSW), high-voltage dc stress testing (DC) and recovery testing (RE), are adopted to characterize time-resolved dynamic R_{ON} of GaN HEMT devices, based on the multimode evaluation platform. Much higher dynamic R_{ON} is obtained by time-resolved characterization, compared with traditional double-pulse testing. The contribution of the dc-stress- or transient-stress-induced dynamic R_{ON} is distinguished by our proposed stressing sequence (DC-HSW-DC-RE). Based on the stressing pattern, a novel physical-based characterization method is delivered to identify the irreversible degradation of dynamic R_{ON} on GaN power devices, featuring excellent sensitivity for irreversible degradation detection. In addition, lifetime acceleration experiments are conducted, and the R_{ON} degradation shows strong dependence on voltage and current, and weak dependence on temperature. Finally, switching safe operation area and switching lifetime are plotted.**

***Index Terms*—Dynamic R_{ON}, GaN HEMTs, irreversible degradation, lifetime acceleration factor, multimode, switching safe operation area (SSOA).**

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I. Introduction

GaN-ON-SI lateral power device technology is emerging as one of the mainstream technologies for next-generation high-density power systems, due to its low specific ON-resistance (R_{ON}), high current density, high breakdown voltage and high switching speed [1], [2], [3]. Its outstanding performance values have been demonstrated in the mass production of consumer electronics [4]. However, the deployment in the longer-lifetime-demanding field, such as power supply systems for data centers, base stations, etc., is bottlenecked by its limited electrical reliability [5], [6], [7].

The reliability issues on gallium nitride (GaN) power switches are categorized into two major aspects: time-dependent breakdown or increased leakage on the gate and drain terminals, i.e., gate/drain-TDDB [8], [9], [10] and degradation of the ON-state conduction [11], [12], [13]. Specific gate driving circuits are implemented to deal with the TDDB issue, and the drain bus voltage is limited [14], [15]. In this article, we will focus on the degradation of conduction, particularly under hard-switching stress conditions [16], [17]. Hard-switching operation mode, such as CCM-mode in a PFC system, is preferred in the cost-effective power system design which features easy control and low cost. Compared with its silicon counterpart, GaN power device is more suitable for hard-switching operation due to the extremely low output capacitance C_{oss} attributed to the nature of the lateral device structure. Therefore, it is worthwhile to accurately define the safe operation area (SOA) and the lifetime acceleration factors under hard-switching stress conditions. Based on the obtained acceleration factors, for a certain power system mission profile, the lifetime of the power switch can be estimated.

The existence of a large number of traps in the gate-drain access region, GaN buffer, and passivation dielectric of the GaN power device [18], lead to difficulty in identifying the ON-resistance degradation, which is disturbed by the "noise" raised by its intrinsic properties, i.e., dynamic R_{ON}. Despite lots of efforts have been made to suppress the dynamic R_{ON}, such as multiple field plates [19], [20], low-damage surface passivation technology [21], etc., an obvious R_{ON} increase can still be observed in the fast-switching evaluation system. In other words, the stability issue is wrapped up in the reliability testing which introduces difficulties in the failure criteria definition.

From the physics point of view [22], reliability stands for the generation of defects that are not recoverable in the operating temperature range. As for stability issues, performance drops or shifts are not permanent and will return to their initial state within a certain time interval.

Several evaluation platforms have previously been demonstrated to characterize the time-resolved dynamic $R_{\rm ON}$ under various hard-switching stress conditions [23], [24], [25], [26], [27], [28], [29]. However, these systems provide no solutions for identifying the root cause of device degradation, nor can they determine whether the degradation is recoverable or not. In this article, the authors proposed a novel physical-based characterization scheme to identify the switching SOA (SSOA) for the lateral GaN power device, based on a multimode hard-switching stress evaluation system.

The rest of this article is organized as follows. Section II presents the details of the evaluation circuit and the equipment setup for device dynamics characterization. With this platform, multiple stress, monitor modes and their combination modes are defined to study the time-resolved dynamic $R_{\rm ON}$ of the device under test (DUT), by which the building-up, saturation and recovery processes are observed. Based on the physical definition of the SOA, Section III proposes a novel characterization scheme that enables the detection of the irreversible $R_{\rm ON}$ degradation quantitatively both in stress conditions and degradation magnitude. In addition, the degradation mechanism of *p*-GaN gate high electron mobility transistors (HEMTs) is discussed. In Section IV, lifetime acceleration factors and/or activation energy in terms of drain voltage, loading current and temperature are extracted and lifetime-oriented switching SOA is plotted. Finally, the conclusion is drawn in Section V.

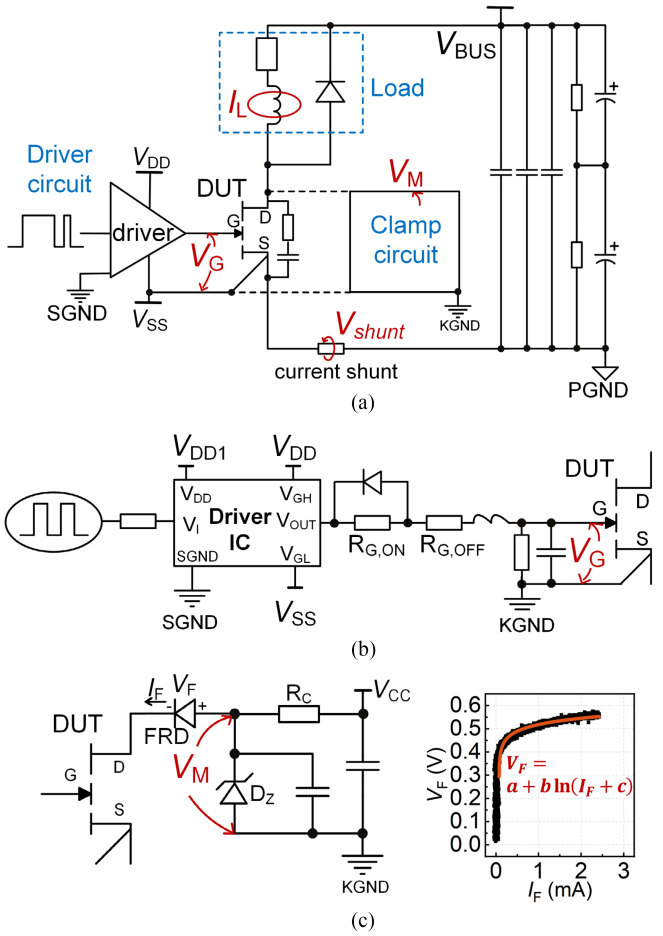

Fig. 1. (a) Circuit schematic plot of evaluation board for GaN power device. (b) and (c) Detailed circuit diagram of driver circuit and clamp circuit. The forward I_F-V_F curve and fitting curve for the clamp diode is inserted in (c).

II. Multimode Switching Evaluation System

A. Design of the Multiple-Pulse Tester

Multiple/double-pulse measurement is a widely used method to evaluate the switching transient of the power device, such as $E_{\rm ON}$ and $E_{\rm OFF}$ [30], [31]. For the GaN power device, this method is adopted to measure the hard-switching-driven dynamic $R_{\rm ON}$ [32], [33], [34], [35], [36].

A typical multiple-pulse tester mainly consists of three components: a driving circuit, a voltage-clamping circuit, and a power supply/load circuit, as shown in the circuit schematic plot in Fig. 1(a). Due to the low intrinsic parasitic capacitance, high $dV_{\rm DS}/dt$ and $dI_{\rm DS}/dt$ events are usually obtained on GaN power HEMTs, which may cause the oscillation of the vulnerable gate. For this reason, the gate driver design is challenging. Fig. 1(b) illustrates the details of the driver circuit, in which an isolated gate driver IC (ADUM4121) [37] is selected, enabling the independent tuning of the gate turn-ON and turn-OFF voltage. A ferrite bead is used to suppress the high-frequency oscillation in the gate driver loop. To ensure fast turn-OFF and smooth turn-ON of the device simultaneously, turn-ON and turn-OFF resistance is adjusted by $R_{G,\rm ON}$ and $R_{G,\rm OFF}$ independently. In the article, $R_{G,\rm ON}$ and $R_{G,\rm OFF}$ are fixed at 300 and 50 Ω. A large $R_{G,\rm ON}$ is adopted for slowing down the turn ON process to achieve smooth gate waveform. A small $R_{G,\rm OFF}$ is required to ensure fast turn OFF of the device.

In the power loop design, to implement the continuous switching operation of the DUT, a power resistor (1 Ω, 100 W) is used to dissipate the energy stored in the inductance (1 mH) during the freewheeling period. A SiC Schottky barrier diode is used for freewheeling diodes. A series-*RC* snubber circuit is chosen to be connected in parallel with the device to dampen the ringing energy and improve the voltage and current waveforms. For $I_{\rm DS}$ measurement, a 0.1-Ω current shunt resistor (SSDN-414-10) is used.

To deal with the problem raised by the dynamic range limit of the $V_{\rm DS}$ measurement (several-hundred voltage high in OFF-state while lower than 1 V in ON-state), a diode clamping circuit with excellent transient response characteristics is utilized to measure the ON-state $V_{\rm DS}$, as depicted in Fig. 1(c) (left). During the OFF-state, the reverse-biased high-voltage fast recovery diode (FRD) isolates the drain and the drain voltage measurement point V_M, and V_M is close to $V_{\rm CC}$. When the device is turned on, once the drain voltage is lower than $V_{\rm CC}$, the isolation diode is forward-biased, and the V_M follows the $V_{\rm DS}$ with a voltage gap V_F, which is the voltage drop on the FRD. Fig. 1(c) (right) shows the actual

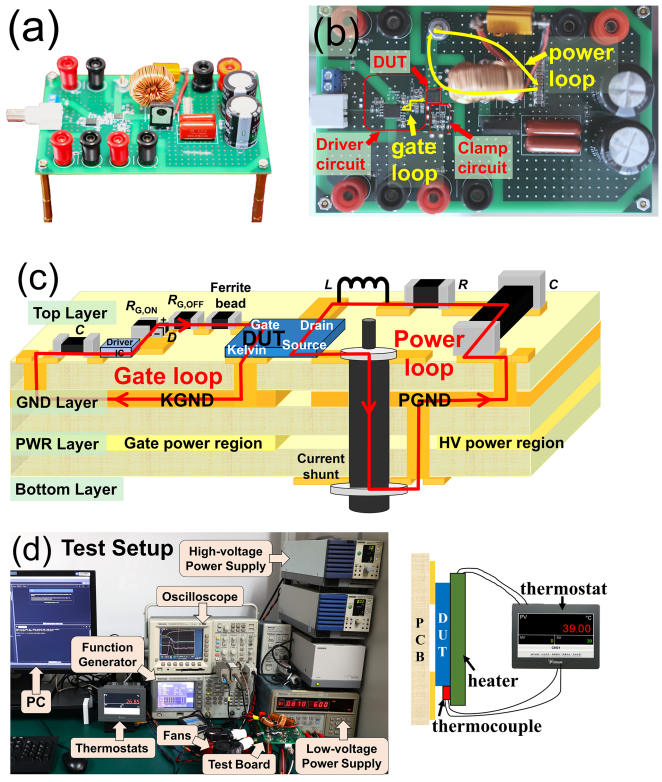

Fig. 2. (a) Photograph of the test board with four-layer PCB for R_{ON} evaluation. (b) Top view of test board, and (c) Detailed gate driver loop and power loop with tight layout. (d) Automatic test system including voltage, current, temperature control for R_{ON} evaluation.

and fitting curve for the clamp diode I_F-V_F characteristics. The value of I_F is calculated by formula: $I_F = (V_{CC}\text{-}V_M)/R_C$. Thus, R_{ON} can be calculated through the following formula:

$$R_{ON} = (V_M - V_F)/(V_{shunt}/0.1) \quad (1)$$

In this design, multiple grounds are used to avoid crosstalk noise. Three grounds are organized in the circuit: signal ground; power ground; and Kelvin source ground. Kelvin connection can separate the driving loop and power loop so that the common-source inductance is bypassed in the gate loop.

B. Setup of the Evaluation System

In this article, a four-layer PCB has been chosen to implement the evaluation board, in which the second layer is divided into three separate ground planes to minimize the loop inductance, as shown in Fig. 2(a)–(c). The independent tunning of the bus voltage, gate drive voltage, load current, and switching frequency is achieved by remote control of a high-voltage power supply (Kikusui PAS500-1.2) for the bus voltage, a signal generator (Tektronix AFG3021B) to generate pulse signals, a 500-MHz bandwidth oscilloscope (Tektronix TDS3054B) to capture the terminal voltage signals, and a low-voltage power supply for driver chip and voltage-clamping circuits, via the GPIB port of a PC, as depicted in Fig. 2(d). The junction temperature is controlled by an external micro ceramic heater, which is mounted on the front side of the device. In addition, a thermocouple is also attached on the case of the device to monitor the real-time device case temperature. It is noticed that, all of the following measurements are performed on the same configuration of the testing board.

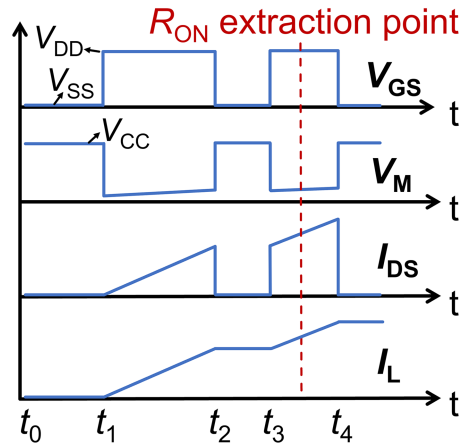

Fig. 3. Schematic voltage/current waveforms under double-pulse testing. Dynamic R_{ON} is extracted at 1 μs after second turn ON of the DUT.

TABLE I
SETUP OF THE INPUT PULSES FOR DOUBLE PULSE TEST

V_{BUS} (V)	50	100	150	200	250	300	350	400	450	500
t_2-t_1 (μs)	24	12	8	6	4.8	4	3.43	3	2.6	2.4

Note: OFF-state time (t_3-t_2) is fixed at 1 μs, turn-ON time (t_4-t_3) is fixed at 1.5 μs. The pulse width of the first pulse (t_2-t_1) varies with bus stress to ensure the same turn ON current of 1 A in the second pulse.

C. Double-Pulse Testing and Dynamic RON Extraction

Fig. 3 plots the schematic waveform of a typical double-pulse measurement. In the first pulse, the DUT is turned ON to charge the load inductance, and a CCM hard-switching turned-ON occurs at the rising edge of the second gate pulse. To evaluate the effect of hard-switching stress, dynamic R_{ON} is extracted with a pre-defined stabilization delay (1 μs) after the second turn-ON of the gate. In this article, a commercially available 650 V, 4 A rated Schottky-type p-gate GaN HEMTs are used as the DUT (GS-065-004-1-L from GaN Systems). In the test circuit for the DUT, a ON-state V_{GS} is 6 V [38], [39], and a -2 V gate-source voltage is chosen for preventing false turn ON during the turn OFF transient [40], [41]. Table I plots the configuration of the input pulses under different bus voltage for double pulse test.

Fig. 4 exhibits the measured waveforms under double-pulse testing with a V_{BUS} of 500 V. Smooth gate turn-ON/OFF transient is obtained, indicating that the gate driving loop and power loop are appropriately designed and the parasitic inductance is effectively minimized. Hence, it is straightforward that by adjusting the high-voltage power supply, the dynamic R_{ON} can be measured under various stress voltages, as shown in Fig. 5(a). Dynamic R_{ON} extraction time is set at 1 μs after the rising edge of the gate signal, which is sufficient for waveform stabilization. Fig. 5(b) plots the ratio of the dynamic R_{ON} to static R_{ON} (or

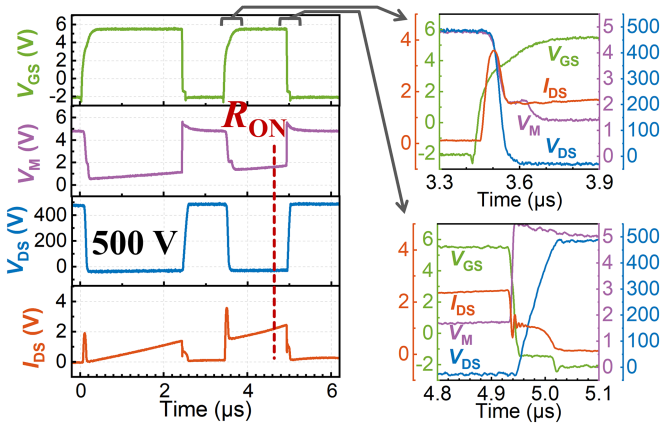

Fig. 4. (a) Double-pulse waveforms under stress condition at $V_{BUS} = 500$ V, $I_{DS} = 1.5$ A, and $T_j = 25$ °C. The turn-ON transient and turn-OFF transient show smooth gate and drain transient behaviors.

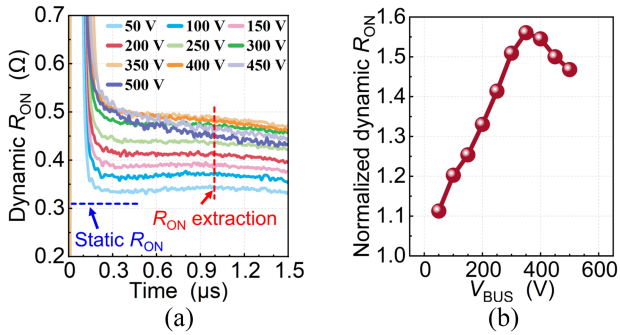

Fig. 5. (a) Dynamic R_{ON} with various bus voltages during the second turn-ON pulse under double-pulse testing, and (b) normalized dynamic R_{ON} versus V_{BUS} is extracted (a) at 1 μs after gate turned-ON.

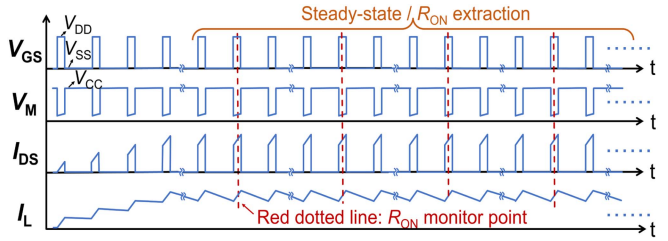

Fig. 6. Control signals and related voltage/current waveforms under multiple-pulse testing. Dynamic R_{ON} is extracted after stabilization of the loading current I_L.

normalized dynamic R_{ON}) versus bus voltages, and it reaches its peak of 1.55 at 350 V.

D. Multiple-Pulse Testing and Switching-Stressed and DC-Stressed Saturated Dynamic RON

Fig. 6 shows the schematic plot of the waveforms under the multiple-pulse condition. In the first few pulses, the loading current on the inductor is increased and finally stabilized, due to the power dissipation from the load power resistor. According to energy conservation law, in each period, the turn-ON current is a

TABLE II
SETUP OF THE INPUT PULSES FOR MULTIPLE PULSE TESTING

V_{BUS} (V)	50	100	200	300	400	450	500	550	600
Frequency (kHz)	40	20	10	6.67	5	4.44	4	3.63	3.33
Duty cycle	6%	3%	1.5%	1%	0.75%	0.67%	0.6%	0.55%	0.5%

Note: The pulse width is fixed at 1.5 μs. The frequency and duty cycle vary with bus stress to ensure the same average current 1.5 A during turn-ON.

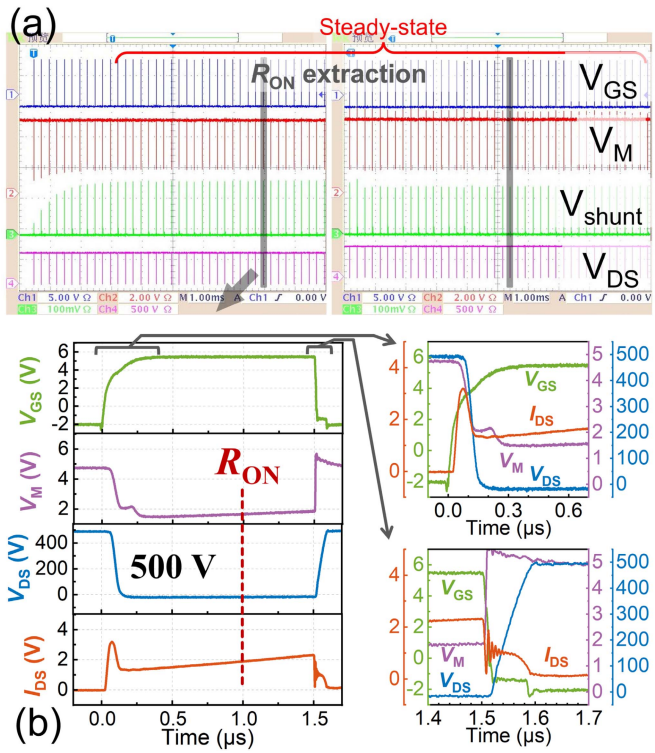

Fig. 7. (a) Multiple-pulse waveforms under stress condition at $V_{BUS} = 500$ V, average $I_{DS} = 1.5$ A, and $T_j = 25$ °C, and ON-state waveform is shown in (b). Smooth turn-ON transient and turn-OFF transient indicate the well-optimized gate and power loop of the PCB.

constant, and the dynamic R_{ON} could theoretically be monitored in each ON-state period.

Table II gives the setup of the input PWM signals for multiple pulse testing. A low switching frequency and duty-cycle is adopted to prevent the self-heating effect. Fig. 7 shows the 500 V measurement results under the multiple-pulse testing at a frequency of 4 kHz and a duty cycle of 0.6%. The building up of the inductive loading current is accomplished in the first 2 ms, and then it is self-balanced. Fig. 7(b) plots the enlarged waveform after stabilization of the inductive loading current. In this measurement, the minimal time interval of dynamic R_{ON} recording is ~1 s, which is limited by the sampling rate and storage capacity of the oscilloscope. The time-resolved dynamic R_{ON} with V_{BUS} ranging from 50 to 500 V is plotted in Fig. 8, in which an obvious building-up process is observed, which then gradually becomes saturated. In this article, we define the stable time-resolved dynamic R_{ON} as "saturated dynamic R_{ON}" ($R_{ON,SW}$), corresponding to a dynamic equilibrium status of trapping/de-trapping in the GaN power device.

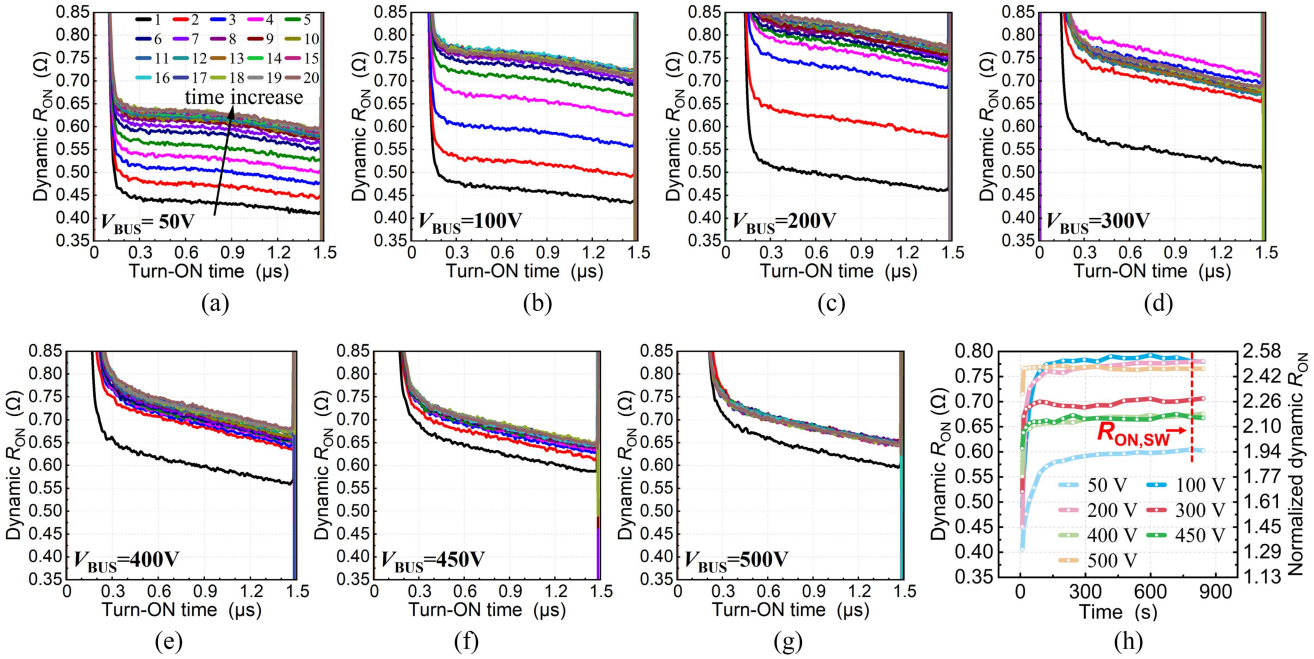

Fig. 8. (a)–(g) Dynamic R_{ON} with various bus voltages ranging from 50 to 500 V during the turn-ON pulse under continuous hard switching stress. (h) Summarized time-resolved R_{ON} extracted at 1 μs after gate turn ON. The saturated dynamic R_{ON} is defined as $R_{ON,SW}$.

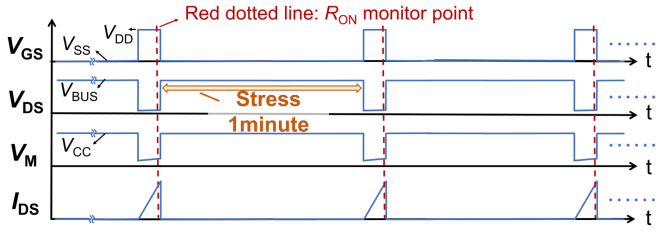

Fig. 9. Schematic voltage/current waveforms under high-voltage DC stress testing. A single pulse is intermittently generated (every few seconds) to monitor the R_{ON}.

A high-voltage dc stress mode is proposed and designed to differentiate the effects of reverse-biased high-voltage stress and the I-V overlap transient. Fig. 9 plots the waveform setup of this stressing mode. Most of the time, the DUT is biased at the dc blocking region, and a single gate turn-ON pulse of 1.5 -μs pulse width is intermittently generated to measure the R_{ON} per minute. The waveform of the gate turn-ON single pulse is shown in Fig. 10. Fig. 11 plots the time-resolved dc-stressed dynamic R_{ON}, in which we could also find a building-up process followed by a final saturation, defined as $R_{ON,DC}$.

Fig. 12 summarizes the two different saturated dynamic R_{ON} and double-pulse R_{ON} versus V_{BUS} voltages. It is found that, compared with the switching-stressed dynamic R_{ON} ($R_{ON,SW}$), the traditional double-pulse testing ($R_{ON,DP}$) underestimates the dynamic R_{ON} a lot. In addition, since the same reverse-biased high-voltage stress is applied on the DUT, bell-shape curves are founded in both $R_{ON,SW}$ and $R_{ON,DC}$, which have been well understood by the leaky dielectric model relating to the time-dependent charge storage in the GaN buffer [42]. Compared with

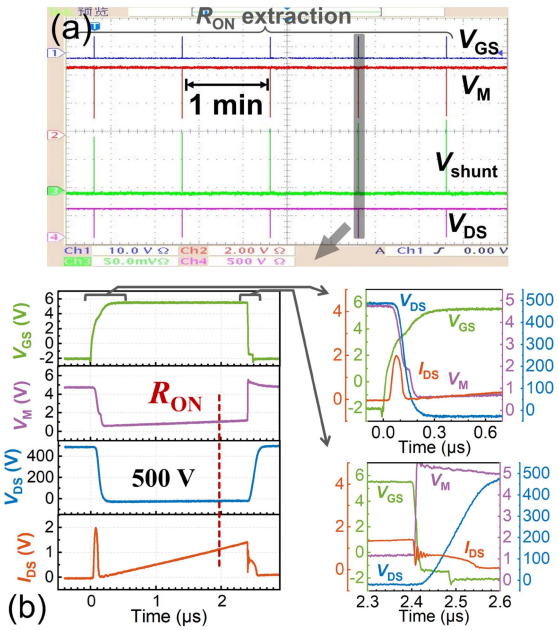

Fig. 10. (a) Schematic diagram of test waveforms under DC stress condition at V_{BUS} = 500 V, average I_{DS} = 1.5 A, and T_j = 25 °C, ON-state is shown in (b).

$R_{ON,DC}$, the extra increase of the dynamic R_{ON} value in $R_{ON,SW}$ is speculated due to the *I–V* overlap stress during the ON-OFF transients It shows the same peak R_{ON} values in dc-stressed and switching-stressed conditions (~100 V), which differ from the double-pulse testing (~350 V). Dynamic R_{ON} has a max shift at 100 V, which is the most sensitive to degradation.

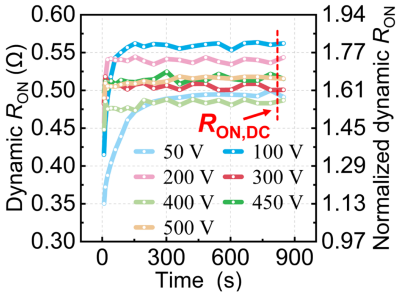

Fig. 11. Time-resolved R_{ON} with different V_{BUS} from 50 to 500 V under DC stress. The saturated dynamic R_{ON} is defined as $R_{ON,DC}$.

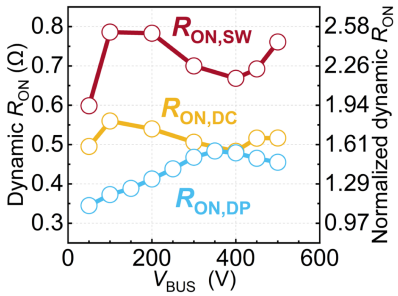

Fig. 12. Summarized dynamic R_{ON} shift under double-pulse testing ($R_{ON,DP}$), high-voltage DC stress testing ($R_{ON,DC}$), and multiple-pulse testing ($R_{ON,SW}$).

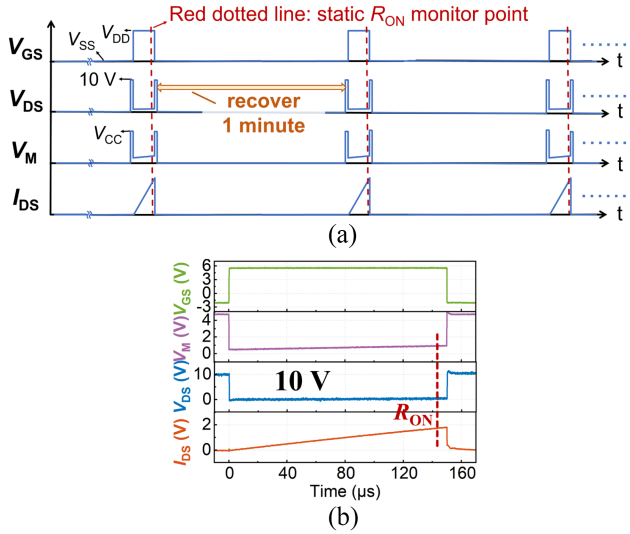

Fig. 13. (a) Schematic voltage/current waveforms under recovery testing. A low-voltage (10 V) single pulse is intermittently applied before the gate pulse (every few seconds) to monitor the static R_{ON}. (b) Measurement waveform of the R_{ON} during the recovery process.

E. Recovery Process of the Dynamic RON

In order to investigate the fully dynamic behavior of the dynamic R_{ON}, we also develop the function of measuring the recovery process of the dynamic R_{ON}. Fig. 13 describes the setup of the waveform, in which a low V_{BUS} is used to guarantee that no trapping events are experienced in this mode. Compared to the high-voltage dc stress testing, the low-voltage dc mode measures the R_{ON} of the DUT by an intermitted single-gate pulse.

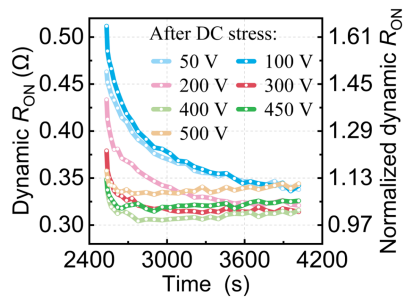

Fig. 14. Time-resolved RON under recovery process after DC stress ranging from 50 to 500 V.

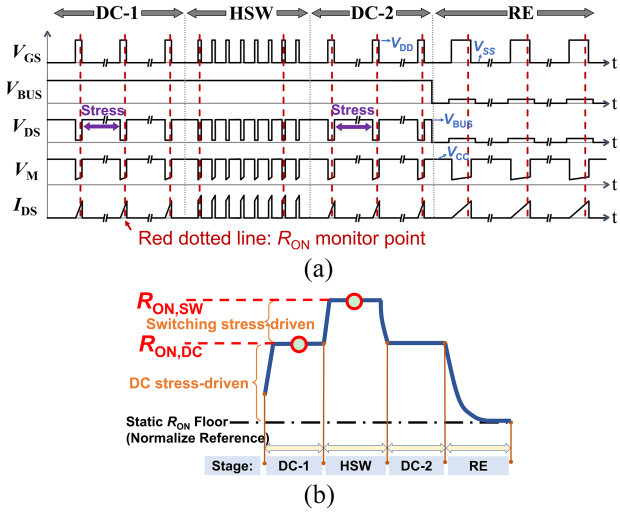

Fig. 15. (a) Proposed stress pattern combing three stress modes (DC, HSW, and RE), and (b) $R_{ON,DC}$ corresponds to the saturation value under dc stress, and $R_{ON,SW}$ corresponds to the saturation value under switching stress.

Fig. 14 shows the recovery process of a DUT after 50 to 500 V high-voltage dc stress. At modest stress (50–200 V), a long recovery time constant is obtained. In higher bias condition, the recovery process is accelerated, may corresponding to sufficient hole injection through the band to band tunneling in the GaN buffer [42].

F. Stressing Pattern "DC-HSW-DC-RE"

In the previous sections, we have implemented four kinds of stressing modes based on our evaluation system: double-pulse testing (short as DP); and multiple-pulse testing (short as HSW);high-voltage dc stress testing (short as DC) and recovery monitoring (short as RE). The above four test modes are all performed on the same setup, and can be automatically switched within a short transition time (< 1 s). Based on this, a stressing sequence is proposed to investigate both the DC stress-driven dynamic R_{ON} and the switching stress-driven dynamic R_{ON}, as shown in Fig. 15, which combines three stress (DC1, HSW, and DC2) and a recovery process (RE), in sequence.

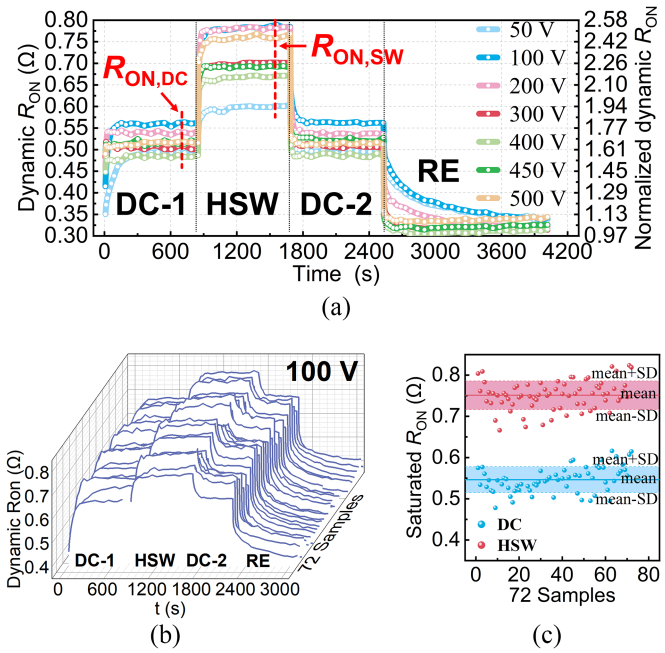

Fig. 16. (a) Time-resolved R_{ON} under varying stress conditions from 50 to 500 V for proposed stress pattern in Fig. 15. Two building-up process and two dynamic R_{ON} plateau are observed. (b) Summarized stressing pattern (DC-HSW-DC-RE) result of 72 samples under 100-V, and (c) the averages and standard deviations (SD) of saturated R_{ON} under DC stress and HSW stress.

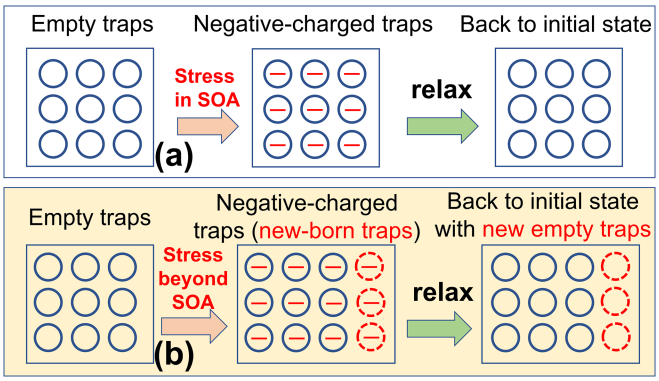

Fig. 17. Physics-based definition for SOA, corresponding to generation of new traps. (a) Recoverable degradation. (b) irreversible degradation.

Fig. 16(a) plots the measured results with the proposed stressing sequence at different V_{BUS} voltages. Two dynamic R_{ON} plateaus ($R_{ON,SW}$ and $R_{ON,DC}$), two building-up (DC-1 and HSW stages) and two recovery processes (DC-2 and RE stages) are observed. First, a high-voltage DC stress is applied to the DUT (DC-1 stage). After building up of the dynamic equilibrium between the trapping and de-trapping processes, dynamic R_{ON} becomes saturated ($R_{ON,DC}$). In the second stage, the device is switched to the hard switching stress mode (HSW stage), and a new dynamic equilibrium is re-established, featuring a higher dynamic R_{ON} ($R_{ON,SW}$). Thirdly, when high voltage is kept and the continuous switching is closed, R_{ON} will return to $R_{ON,DC}$ (DC-2 stage). In RE mode, R_{ON} gradually recovers to its initial static value.

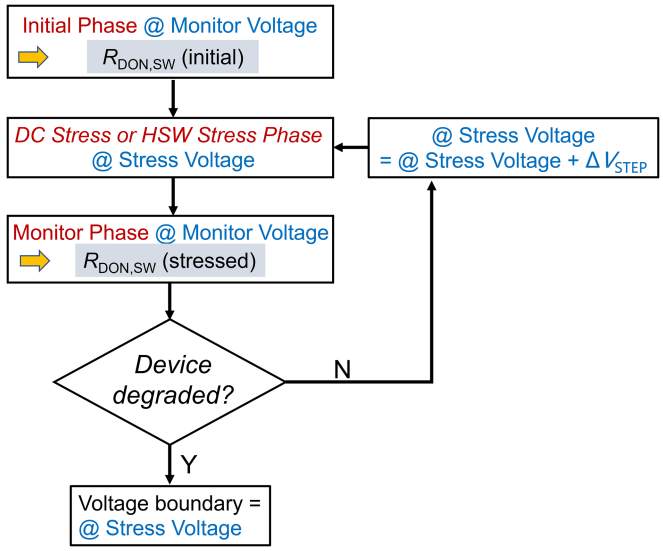

Fig. 18. Proposed characterization scheme following "stress-monitor" sequence to detect irreversible degradation.

It is noticed that, the time constant of the building up or recovery processes between $R_{ON,DC}$ and $R_{ON,SW}$ (HSW and DC-2 stages) is much faster than the time constant of the building up or recovery processes between $R_{ON,DC}$ and static R_{ON} (DC-1 and RE stages), indicating that the *I*–*V*-overlap-induced trapping has a shallow energy level or a small de-trapping energy barrier. Based on our understanding, it is suggested that the hot electron-induced dynamic R_{ON} is mainly attributed to the electrons trapping in the passivation/AlGaN interface [43]. On the other hand, the high-voltage DC-induced dynamic R_{ON} is related to the negative charge generation in the GaN buffer [44].

To check the reproducibility of our measurement setup, more than 100 devices were tested. Fig. 16(b) and (c) show the time-resolved dynamic R_{ON} for 72 GaN HEMTs under 100-V stressing pattern (DC-HSW-DC-RE), as well as the statistical results.

III. Proposed Characterization Method for Identifying the Irreversible RON Degradation in GaN Power Device

To investigate the reliability of GaN power devices, the most challenging task is ruling out influence of the stability issues caused by the dynamics of the trap states. In previous studies or companies' reliability reports, the boundary of the SOA is defined by a certain magnitude of R_{ON} increase, e.g., a 30% increase of the static R_{ON} after stress, or a 30% increase of the dynamic R_{ON} during stress (noted as methods A and B, respectively) [45], [46], [47], [48]. However, this definition is controversial, because it cannot identify whether the degradation is recoverable or not. In this article, we would like to introduce a method to identify the irreversible degradation of R_{ON} in GaN power devices.

First, a physics-based definition of recoverable and irreversible degradation is explained in Fig. 17 [22]. For recoverable

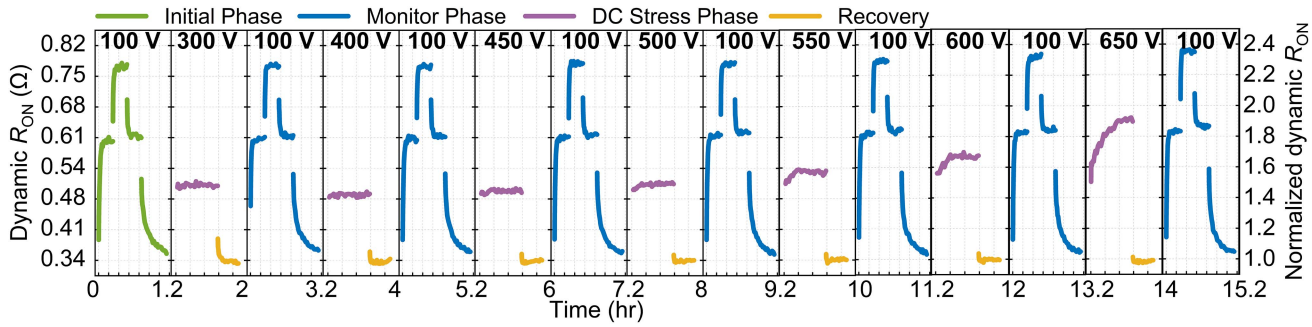

Fig. 19. Time-resolved characterization results for voltage dependence on device degradation under DC stress condition following the "stress-monitor" sequence shown in Fig. 18.

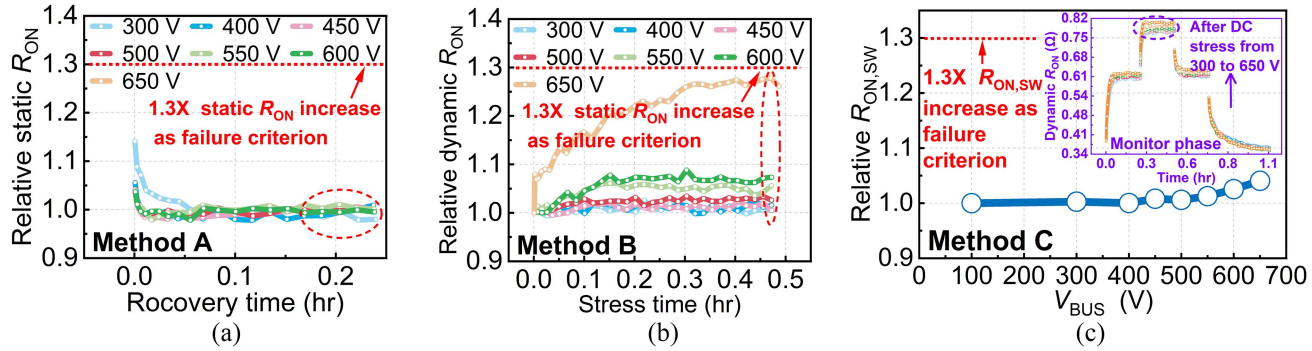

Fig. 20. Failure evaluation method, (a) a 30% increase in static R_{ON} after stress, (b) a 30% increase in dynamic R_{ON} under stressing phase, (c) a 30% increase in $R_{ON,SW}$ under monitor phase proposed in this article, and insert: results on each after-stress monitor phase. It is shown that device irreversible degradation does not occur under DC-stressed condition.

degradation [see Fig. 17(a)], traps are occupied by negative charges during the stressing period, leading to an increase in the ON-resistance, which will be returned to its initial state after the release of the stress. Since no extra trap states are generated in the stressing period, the stressed device performs the same as the virgin one. On the contrary, if new traps are created under the stress, it means irreversible damage to the device, as depicted in Fig. 17(b). It is noticed that, even new traps are generated, through a sufficient recovery time, the negative charges are pumped out, the static R_{ON} can still return back to the initial value. However, when the high voltage stress is re-applied, the new-born traps will be charged quickly, leading to a higher dynamic R_{ON}.

Thus, it is highly desirable to find an unambiguous feature of the DUT that would not only detect permanent damage but also measure quantitatively the degree of degradation. Here, the switching-induced saturated R_{ON} ($R_{ON,SW}$), which has been defined in Section II, is chosen as the index for tracing the irreversible device degradation. If irreversible degradation happens, the newly generated traps would break the previous trapping/de-trapping equilibrium, resulting in a higher dynamic $R_{ON,SW}$ value.

Fig. 18 plots a characterization scheme to detect irreversible degradation. In order to assess the degradation accurately, the effect of trap generation is evaluated under the most defect-sensitive condition in the monitor phase. As shown in Fig. 12, $R_{ON,SW}$ in 100 V is chosen as the degradation index for the DUT device used in this article, which features the maximum dynamic R_{ON} shift versus V_{BUS} voltage.

The measurement scheme is set to follow the "stress phase (@stress voltage) → monitor phase (@monitor voltage)" sequence. For each monitor phase, time-resolved R_{ON} is measured as the stress pattern under 100-V stressing sequence. The monitor phase itself is safe, and would not bring any damage to the device.

A. ON-Resistance Degradation Evaluation Under High-Voltage DC Stress

Fig. 19(a) shows the time-resolved measurement results with step-increased dc stress, and the monitor phases after multiple stress voltages are summarized in Fig. 20(c). After 650 V dc stress, nearly no dynamic R_{ON} increase is observed. One intriguing phenomenon is that under the 650-V dc-stressed condition, significant dynamic R_{ON} degradation is observed. However, by checking the dynamic R_{ON} in the following monitor phase, it indicates that the degradation previously observed is recoverable. Thus, if we use the increase of the dynamic R_{ON} under 650 V as the device failure criterion, an incorrect conclusion will be delivered. Fig. 20 shows the various failure criteria, methods A, B, and C, under DC stress. Fig. 23(a) summarizes the sensitivity of the three methods for detecting device degradation.

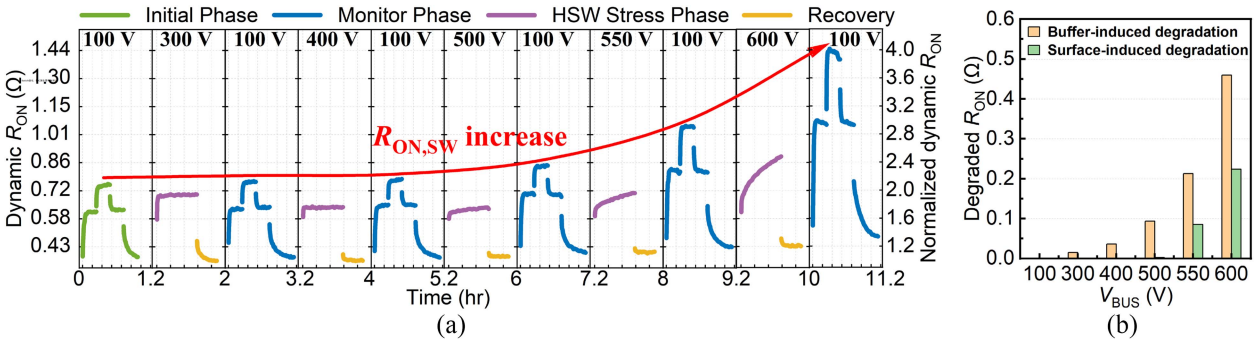

Fig. 21. (a) Time-resolved characterization results for voltage dependence on device degradation under HSW stress condition following the "stress-monitor" sequence shown in Fig. 18. (b) Contributions of buffer-induced R_{ON} degradation and surface-related R_{ON} degradation.

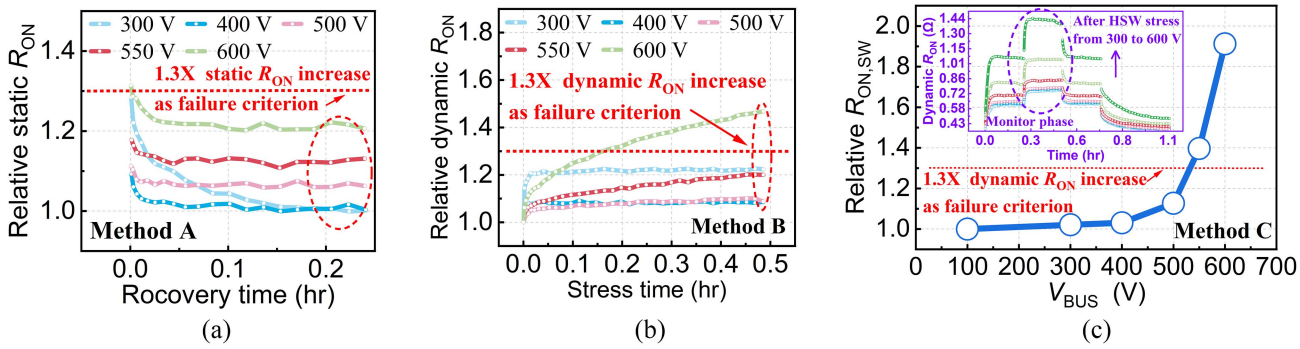

Fig. 22. Failure evaluation method, (a) a 30% increase in static R_{ON} after stress, (b) a 30% increase in dynamic R_{ON} under stressing phase, (c) a 30% increase in $R_{ON,SW}$ under monitor phase proposed in this article, and insert: results on each after-stress monitor phase. Obvious dynamic R_{ON} irreversible degradation is obtained when V_{BUS} is larger than 500 V.

B. ON-Resistance Degradation Evaluation Under High-Voltage Hard-Switching Stress Through Multiple-Pulse Testing

Fig. 21(a) demonstrates the time-resolved measurement results under variable high-voltage hard-switching stress. When the bus voltage exceeds 500 V, the dynamic R_{ON} increases dramatically. Both the dc-stressed dynamic R_{ON} ($R_{ON,DC}$) and the switching-stressed dynamic R_{ON} ($R_{ON,SW}$) increase during the 100-V monitor phase, indicating that degradation occurs in both the buffer and the surface. The contributions of buffer-induced R_{ON} degradation and surface-related R_{ON} degradation are depicted in Fig. 21(b). It is believed that, under high-voltage switching stress, the depletion region expands to the drain side of the device, and hot electrons are injected into the buffer and surface passivation dielectric, generating dangling bonds in the dielectric and point defects in the GaN buffer. The various failure criteria for methods A, B, and C under switching stress are shown in Fig. 22. Fig. 23(b) summarizes the sensitivity of the three methods, in which method C obviously outperforms the others, featuring the highest sensitivity.

IV. Evaluation of Switching SOA and Lifetime

Accurate lifetime prediction under application-driven stress conditions is highly desirable for expanding the application

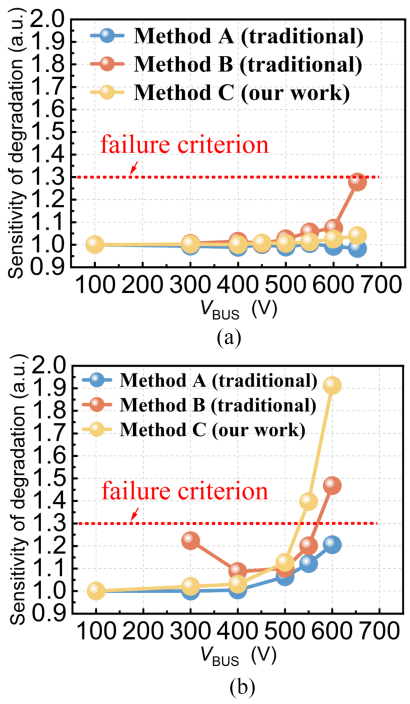

Fig. 23. Sensitivity of device degradation for three indices, (a) under DC stress and (b) under HSW stress.

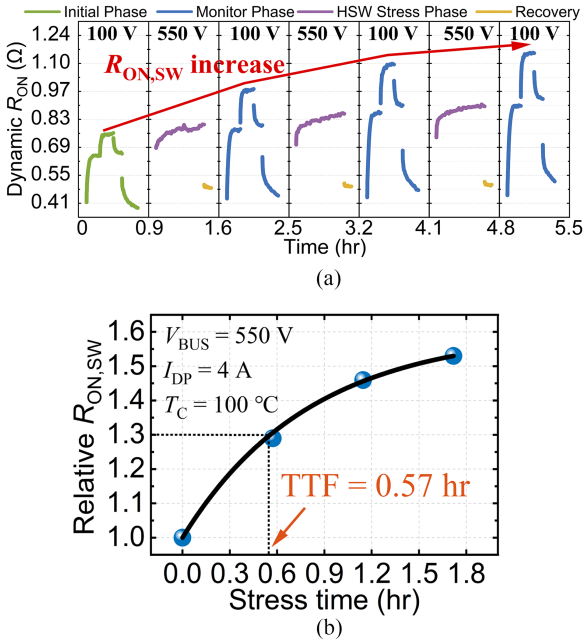

Fig. 24. (a) Method of reliability testing for determining the time to failure. $R_{ON,SW}$ is regarded as the failure index, and relative $R_{ON,SW}$ is shown in (b). Note: Initial Phase and Monitor Phase operation conditions are T_j = 25 °C, V_{BUS} = 100 V, I_{DP} = 4 A; HSW stress phase operation condition is T_j = 100 °C, V_{BUS} = 550 V, I_{DP} = 4 A; and recovery phase operation condition is T_j = 25 °C, V_{BUS} = 0 V.

field of GaN HEMTs. In this article, based on our proposed characterization scheme, the lifetime acceleration factors [49] or activation energy, in terms of bus voltage, loading current, and temperature are extracted. The time-to-failure (TTF) of the DUT is defined when the switching-stressed dynamic R_{ON} in the monitor phase ($R_{ON,SW}$ corresponds to 100-V V_{BUS} in this article) increases to 1.3 times the initial value.

Fig. 24(a) shows the characterization method to determine the TTF of the device. In each stressing phase, a ∼30-mins hard-switching stress is applied to the DUT, alternated with the monitoring phase to sample the degree of degradation. Fig. 24(b) shows the dependence of the stressing time on the $R_{ON,SW}$ increase, and exponential interpolation is used to determine the failure time.

A. Drain Voltage Acceleration

As demonstrated in Fig. 21, a significant increase in $R_{ON,SW}$ occurs when V_{BUS} is above 550 V. Therefore, in this article, the drain voltage acceleration is determined to be conducted at V_{BUS} of 550/575/600 V, I_{DP} of 4 A and T_j of 25 °C. During the turn-ON transient, the device encounters high voltage and high current. Fig. 25(c) plots the I_{DS} – V_{DS} locus of the turn-ON transient with various bus voltages. Ten sample devices are tested at each stress level in acceleration experiment.

Fig. 25(a) depicts the obtained Weibull plot of the cumulative failure rate with a lognormal distribution lifetime. The data points are distributed evenly along one or both sides of the fitted line. The three fitted lines have identical slopes, indicating that the tested device's failure mechanism is the same within the three voltage stresses chosen. In this article, the mean-time-to-failure (MTTF) is defined as the time at 63.2% probability of failure.

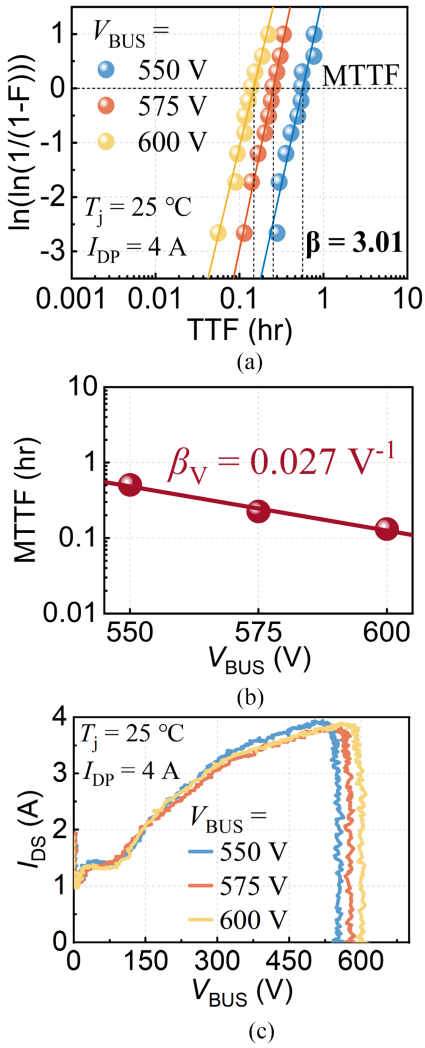

Fig. 25. (a) Weibull plot of the drain voltage acceleration measurement under V_{BUS} = 550 V, 575 V and 600 V (10 measurement samples for each stress condition). (b) Extracted voltage acceleration factor β_V and (c) I_{DS} - V_{DS} locus under HSW testing.

Here, the Arrhenius model is applied to extract the voltage acceleration factor with the formula shown as

$$\ln(\text{MTTF}) = \alpha_V + \beta_V V_{BUS}. \quad (2)$$

As shown in Fig. 25(b), the extracted voltage acceleration factor of β_V is 0.027 /V with a α_V of 14.092.

B. Drain Current Acceleration

In this article, three peak currents (I_{DP}) of 3.5, 4, and 4.5 A are performed to determine the current acceleration factor of the device, with V_{BUS} of 550 V and T_j of 25 °C, and the I_{DS} –V_{DS} locus is plotted in Fig. 26(c). The Weibull plot shown in Fig. 26(a) exhibits a similar slope in different current conditions, indicating the same manner of failure. By applying Arrhenius law, current acceleration factor of β_C is obtained to be 2.05 /A with a α_C is 7.123, as shown in Fig. 26(b). The formula is as follows:

$$\ln(\text{MTTF}) = \alpha_C + \beta_C I_{DP}. \quad (3)$$

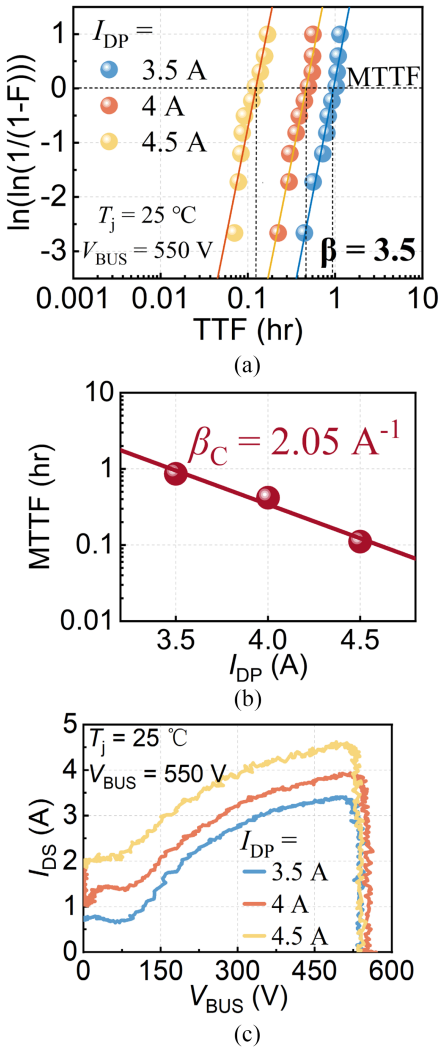

Fig. 26. (a) Weibull plot of the drain current acceleration measurement with I_{DP} of 3.5, 4 and 4.5 A (10 measurement samples for each stress condition), (b) extracted current acceleration factor β_C, and (c) I_{DS} - V_{DS} locus under HSW testing.

C. Temperature Acceleration

Activation energy is the key parameter to describe the magnitude of the temperature acceleration. In order to determine the activation energy E_a, the hard-switching stressing sequence is applied at three different temperatures. In this article, the junction temperature of the device is controlled by the mounted heater. The summary of the temperature-dependent device degradation is shown in Fig. 27(a), and it is found that the temperature acceleration is very weak. To extract the activation energy, the following formula is used:

$$\ln(\text{MTTF}) = \alpha_T + E_a/(\text{kT}) \tag{4}$$

where k is the Boltzmann constant, 8.617E-5 eV/K. The Arrhenius plot of MTTF is depicted in Fig. 27(b), and the extracted E_a is 0.082 eV.

D. Evaluation of Switching Safe Operating Area

In this section, the switching lifetime is determined based on the obtained acceleration factors. MTTF is described as

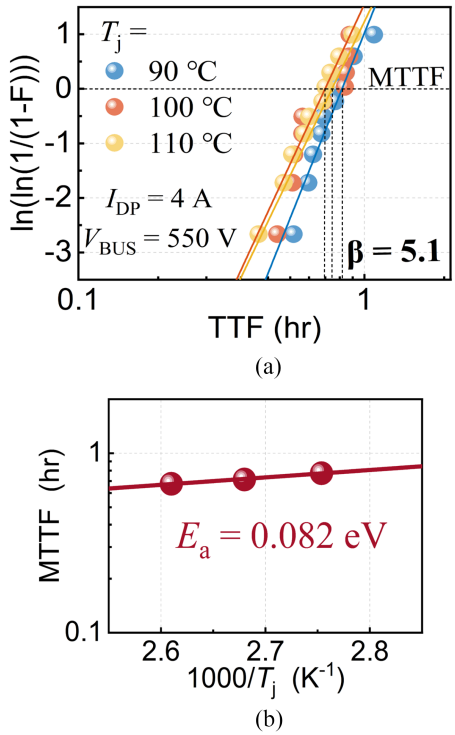

Fig. 27. (a) Weibull plot of the temperature acceleration measurement with temperature of 90 °C, 100 °C, and 110 °C. (b) Arrhenius plot to extract activation energy which shows a weakly dependence on temperature. .

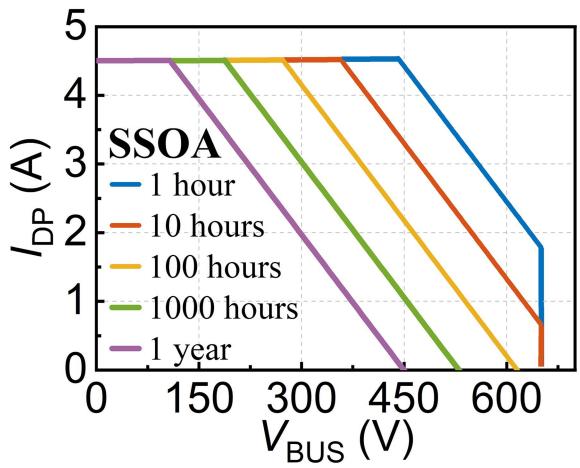

Fig. 28. SSOA for GaN device in this article under 1-, 10-, 100-, 1000-hours and 1-year operations.

$$\text{MTTF} = A\exp\{-(\beta_C I_{DP} + \beta_V V_{BUS})\} \tag{5}$$

on the condition that the acceleration of current and voltage are independent [20], and the temperature acceleration can be ignored due to its weak dependence on lifetime. The coefficient of A is equal to $\{\exp(\alpha_V+\alpha_C)\}$.The current can be set as a function of voltage

$$I_{DP} = -(\beta_V/\beta_C)V_{BUS} + [ln(\text{MTTF}/A)]/\beta_C. \tag{6}$$

Based on this equation, the contour of the SSOA for 1-, 10-, 100-, 1000-h and 1-year switching operations is obtained in Fig. 28.

V. Conclusion

The purpose of the article is to investigate the dynamic behaviors of GaN power devices and to assess the SSOA of these devices. In this article, the time-resolved dynamic R_{ON} behaviors of state-of-the-art commercial Schottky type *p*-GaN gate devices were measured under dc stress and switching stress, utilizing an automatic laboratory setup along with a novel characterization procedure. Additionally, based on the observed dynamic behaviors, we proposed a novel characterization scheme to detect the irreversible ON-resistance degradation quantitatively, considering both the stress conditions and the magnitude of the degradation. The switching lifetime and SSOAwere then evaluated using the proposed characterization scheme. To our knowledge, the suggested characterization scheme performs remarkably well in terms of identifying irreversible degradation and evaluating lifetime. The following key conclusions can be drawn from this article.

1) When the voltage is less than 500 V, time-resolved dynamic RON will initially rise and then reach saturation due to the equilibrium of the trapping and de-trapping effects. HSW-driven dynamic R_{ON} is higher than its dc stress-driven counterpart, due to the extra switching stress applied during the ON/OFF transients. Based on our understanding, it is speculated that the accumulated negative charges are the main contributor to the dc-driven dynamic R_{ON}, and the dependence on the bus voltage follows the "leaky dielectric model."
2) When bus voltage is higher than ∼500 V, the trapping/detrapping balance is broken in the DUT, especially under the HSW stressing condition, where the time-resolved R_{ON} will not saturate. By using the proposed characterization scheme, it is able to probe the irreversible degradation is mainly caused by the hot electron induced damage.
3) Based on our proposed failure evaluation method, i.e., a 30% increase in saturate dynamic R_{ON} during multiple-pulse testing under the monitor voltage, switching lifetime and SSOA are determined. Our proposed failure criterion is more sensitive to detecting irreversible degradation than the traditional failure criterion.
4) These findings have significant implications for the understanding of the stability and reliability issues in lateral GaN devices. Although only one type of commercial device is tested in this article, the proposed characterization scheme "stress/monitor/stress" for SSOA identification and switching lifetime evaluation is applicable to other types of GaN power devices.

References

[1] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[2] H. Amano et al., "The 2018 GaN power electronics roadmap," *J. Phys. D, Appl. Phys.*, vol. 51, no. 16, Mar. 2018, Art. no. 163001.

[3] U. K. Mishra, P. Parikh, and Y. - F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002, doi: 10.1109/JPROC.2002.1021567.

[4] G. Deboy, *Gallium Nitride Technology in Adapter and Charger Applications*. Neubiberg, Germany: Infineon, 2018.

[5] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-Based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[6] T. McDonald, *Reliability and Qualification of CoolGaN*. Neubiberg, Germany: Infineon, 2018, pp. 10–2018.

[7] J. P. Kozak et al., "Degradation and recovery of GaN HEMTs in overvoltage hard switching near breakdown voltage," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 435–446, Jan. 2023, doi: 10.1109/TPEL.2022.3198838.

[8] P. Moens et al., "(Invited) intrinsic reliability assessment of 650V rated AlGaN/GaN based power devices: An industry perspective," *ECS Trans.*, vol. 72, no. 4, May 2016, Art. no. 65.

[9] G. Meneghesso et al., "Reliability and parasitic issues in GaN-based power HEMTs: A review," *Semicond. Sci. Technol.*, vol. 31, no. 9, Sep. 2016, Art. no. 093004.

[10] J. He, J. Wei, S. Yang, Y. Wang, K. Zhong, and K. J. Chen, "Frequency- and temperature-dependent gate reliability of schottky-type p-GaN gate HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3453–3458, Aug. 2019, doi: 10.1109/TED.2019.2924675.

[11] C. Hu, S. C. Tam, F.-C. Hsu, P. -. K. Ko, T.-Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation - Model, monitor, and improvement," *IEEE J. Solid-State Circuits*, vol. 20, no. 1, pp. 295–305, Feb. 1985, doi: 10.1109/JSSC.1985.1052306.

[12] G. Meneghesso et al., "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008, doi: 10.1109/TDMR.2008.923743.

[13] Y. S. Puzyrev et al., "Dehydrogenation of defects and hot-electron degradation in GaN high-electron-mobility transistors," *J. Appl. Phys.*, vol. 109, 2011, Art. no. 034501.

[14] T. Bonifield, "Enabling high voltage signal isolation quality and reliability," *Texas Instrum.*, vol. 9, 2017, Art. no. 036521.

[15] T. Bonifield, H. Guo, J. West, H. Shichijo, and T. Tahir, "High frequency TDDB of reinforced isolation dielectric systems," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–4. doi: 10.1109/IRPS45951.2020.9128352.

[16] G. Zulauf, M. Guacci, and J. W. Kolar, "Dynamic on-Resistance in GaN-on-Si HEMTs: Origins, dependencies, and future characterization frameworks," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5581–5588, Jun. 2020, doi: 10.1109/TPEL.2019.2955656.

[17] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-State resistance test and evaluation of GaN power devices under Hard- and Soft-Switching conditions by double and multiple pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019, doi: 10.1109/TPEL.2018.2844302.

[18] S. Yang, S. Han, K. Sheng, and K. J. Chen, "Dynamic on-resistance in GaN power devices: Mechanisms, characterizations, and modeling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1425–1439, Sep. 2019, doi: 10.1109/JESTPE.2019.2925117.

[19] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN–GaN HEMTs achieved by multiple field plates," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 161–163, Apr. 2004, doi: 10.1109/LED.2004.824845.

[20] W. Saito, "Reliability of GaN-hemts for high-voltage switching applications," in *Proc. Int. Rel. Phys. Symp.*, 2011, pp. 4E.1.1–4E.1.5, doi: 10.1109/IRPS.2011.5784510.

[21] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001, doi: 10.1109/16.906451.

[22] J. A. del Alamo and E. S. Lee, "Stability and reliability of lateral GaN power field-effect transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4578–4590, Nov. 2019, doi: 10.1109/TED.2019.2931718.

[23] A. Pozo, R. Strittmatter, S. Zhang, and A. Lidow, "(Invited) understanding dynamic $R_{\mathrm{DS(on)}}$ in GaN devices," *ECS Trans.*, vol. 104, no. 7, pp. 125–138, 2021, doi: 10.1149/10407.0125ecst.

[24] A. Ikoshi et al., "Lifetime evaluation for hybrid-drain-embedded gate injection transistor (HD-GIT) under practical switching operations," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, pp. 4E.2–4E.1–4E.2–7, doi: 10.1109/IRPS.2018.8353594.

[25] M. - C. Lin et al., "New circuit topology for system-level reliability of GaN," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs*, 2019, pp. 299–302.

[26] S. Yin et al., "Evaluation of reliability and lifetime of 650-V GaN-on-Si power devices fabricated on 200-mm CMOS-Compatible process platform for high-density power converter application," in *Proc. IEEE 34th Int. Symp. Power Semicond. Devices ICs*, 2022, pp. 93–96. doi: 10.1109/ISPSD49238.2022.9813684.

[27] Y. - F. Wu, J. Guerrero, J. McKay, and K. Smith, "Advances in reliability and operation space of high-voltage GaN power devices on Si substrates," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2014, pp. 30–32, doi: 10.1109/WiPDA.2014.6964618.
[28] S. R. Bahl, F. Baltazar, and Y. Xie, "A generalized approach to determine the switching lifetime of a GaN FET," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–6. doi: 10.1109/IRPS45951.2020.9129631.
[29] P. J. Martinez, P. F. Miaja, E. Maset, and J. Rodriguez, "A test circuit for GaN HEMTs dynamic R_{ON} characterization in power electronics applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1456–1464, Sep. 2019, doi: 10.1109/JESTPE.2019.2912130.
[30] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9307–9318, Dec. 2017, doi: 10.1109/TPEL.2017.2655491.
[31] J. Gareau, R. Hou, and A. Emadi, "Review of loss distribution, analysis, and measurement techniques for GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7405–7418, Jul. 2020, doi: 10.1109/TPEL.2019.2954819.
[32] JEDEC Solid State Technology Association, "Dynamic ON-resistance test method guidelines for GaN HEMT based power conversion devices," *in JEP-173*, Jan. 2021.
[33] JEDEC Solid State Technology Association, "Test method for continuous switching evaluation of gallium nitride power conversion devices," *in JEP-182*, Jan. 2021.
[34] G. Zu et al., "Review of pulse test setup for the switching characterization of GaN power devices," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3003–3013, Jun. 2022, doi: 10.1109/TED.2022.3168238.
[35] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-level reliability of GaN devices," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2016, pp. 4A–43–1–4A–3–6, doi: 10.1109/IRPS.2016.7574528.
[36] S. R. Bahl, J. Joh, L. Fu, A. Sasikumar, T. Chatterjee, and S. Pendharkar, "Application reliability validation of GaN power devices," in *Proc. IEEE Int. Electron Devices Meeting*, 2016, pp. 20.5.1–20.5.4, doi: 10.1109/IEDM.2016.7838461.
[37] P. Wiener, "GN012 application note," GaN Systems Inc, Ann Arbor, MI. USA, Tech. Rep. IR2130/IR2132(J)(S), 2022.
[38] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017, doi: 10.1109/TPEL.2016.2610460.
[39] K. Zhong et al., "I_G- and V_{GS}-Dependent dynamic R_{ON} Characterization of commercial high-voltage P-GaN gate power HEMTs," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8387–8395, Aug. 2022, doi: 10.1109/TIE.2021.3104592.
[40] Y. Wang, J. Wei, S. Yang, J. Lei, M. Hua, and K. J. Chen, "Investigation of dynamic I_{OFF} Under switching operation in schottky-type p-GaN gate HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3789–3794, Sep. 2019, doi: 10.1109/TED.2019.2930315.
[41] Z. Jiang et al., "Negative gate bias induced dynamic ON-Resistance degradation in Schottky-type p-GaN gate HEMTs," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6018–6025, May 2022, doi: 10.1109/TPEL.2021.3130767.
[42] M. J. Uren et al., "'Leaky dielectric' model for the suppression of dynamic R_{ON} in carbon-doped AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2826–2834, Jul. 2017, doi: 10.1109/TED.2017.2706090.
[43] G. Meneghesso, A. Paccagnella, Y. Haddab, C. Canali, and E. Zanoni, "Evidence of interface trap creation by hot-electrons in AlGaAs/GaAs high electron mobility transistors," *Appl. Phys. Lett.*, vol. 69, no. 10, pp. 1411–1413, Sep. 1996, doi: 10.1063/1.117598.
[44] S. C. Binari et al., "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 465–471, Mar. 2001, doi: 10.1109/16.906437.
[45] K. Tanaka et al., "Reliability of hybrid-drain-embedded gate injection transistor," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2017, pp. 4B–2.1–4B–2.10, doi: 10.1109/IRPS.2017.7936308.
[46] S. Singhal et al., "Qualification and reliability of a GaN process platform," in *Proc. Int. Conf. Compound Semicond. MANTECH Tech. Dig.*, 2007, Art. no. 15315169.
[47] P. Moens et al., "Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs," in *Proc. IEEE Int. Electron Devices Meeting*, 2015, pp. 35.2.1–35.2.4. doi: 10.1109/IEDM.2015.7409831.
[48] B. Lambert et al., "Reliability data's of 0.5μm AlGaN/GaN on SiC technology qualification," *Microelectronics Rel.*, vol. 52, no. 9, pp. 2200–2204, Sep. 2012, doi: 10.1016/j.microrel.2012.06.098.
[49] JEDEC Solid State Technology Association, "Guideline for switching reliability evaluation procedures for gallium nitride power conversion devices," *in JEP-180.01*, Jan. 2021.

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