Asymmetric Trapezoidal Wave Modulation of Modular Multilevel Resonant DC/DC Converter for Current Stress Optimization

Haozhe Jin, Wu Chen, *Senior Member, IEEE*, Yeyuan Xie, Liangcai Shu, and Yutao Xu

***Abstract*—A modular multilevel resonant dc/dc converter (MMRDC) possesses high power and high voltage rating, which is adopted for high step-ratio interconnection in dc grid applications. However, the current stress and reactive power of MMRDC are high with the conventional quasi-square-wave modulation scheme when in a wide voltage range and light load conditions. Hence, this article proposes an optimized asymmetric trapezoidal wave (ATW) modulation scheme that reduces current stress over wide load and voltage ranges by separately modulating the duty cycles of string output voltage rising and falling processes. The time-domain mathematical model of MMRDC with the ATW modulation scheme is established. Then, based on the soft switching characteristic and reactive current analysis, the optimized operating point of MMRDC can be derived while considering low current stress and zero voltage switching constraint of low voltage side full-bridge switches. On this basis, the numerical solutions of optimized control variables are obtained, and a control block diagram is presented for the practical implementation of the optimized ATW modulation scheme. Finally, a 4 kW MMRDC prototype is constructed, and the experimental results verify the correctness and effectiveness of the analysis and the optimized ATW modulation scheme.**

***Index Terms*—DC/DC converter, modular multilevel converter (MMC), resonant converter, soft switching.**

I. Introduction

With the rapid development of large-scale renewable energy sources, such as the offshore wind farm and the solar power station, dc collection and transmission technologies are viewed as profitable solutions for future renewable energy systems due to their high efficiency, reliability, and flexibility [1], [2], [3]. The high voltage high power dc/dc converter is essential for dc collection and transmission grids as the critical equipment for voltage conversion, power flow control, and fault protection [4], [5]. The existing high-power dc/dc converter schemes can be divided into nonisolated and isolated types. The isolated dc/dc converter is more suitable in medium voltage (MV) dc grids on account of galvanic isolation, high step-ratio, and better device utilization.

Conventional isolated dc/dc converter is challenged to directly implement in MV applications due to the incremental voltage stress of power devices and passive components [6], [7]. One solution for MV dc conversion is forming a front-to-front dc/dc converter by employing the modular multilevel converter (MMC) on the MV side with a centralized transformer [8], [9]. The series-connected submodules (SMs) of the modular multilevel dc/dc converter (MMDC) can reduce device voltage stress, improve reliability, and achieve high modularity and redundancy [10]. Besides, a centralized high-power medium-frequency transformer (MFT) features simpler insulation isolation, less manufacturing difficulty, and higher power density than multiple distributed high-frequency transformers [11]. However, the abundance of SMs in the conventional MMC results in high capital costs and substantial footprints [12]. In [13], a half-bridge-type MMDC based on the dual-active-bridge (DAB) structure is proposed to reduce the number of SMs. Nevertheless, there are concentrated capacitors on the MV side for the half-bridge-type MMDC. A sharing-branch modular multilevel dc transformer is proposed in [14], which reduces the number of SMs and eliminates concentrated capacitors at the MV terminal. Additionally, the resonant structure can also be used in MMDC to reduce switching loss and the harmonic in MFTs as shown in Fig. 1(a) [15], [16], [17]. A modular multilevel resonant (MMR) dc/dc converter (MMRDC) is proposed in [18] by combining the MMC and LLC resonant converter. Zero voltage switching (ZVS) for half of MV-side SM switches and zero current switching (ZCS) for low voltage (LV) side rectifier diodes can be achieved. A high step-down ratio isolated resonant MMC (RMMC) is presented in [19]. And ZVS is achieved for all SM switches. Because of the substantial conduction loss at MV side, RMMC is preferable for low-power tapping applications [20]. In [21], an MMRDC is proposed for high step-ratio applications. Soft switching and fixed frequency operation can be achieved.

Inherits from modular multilevel structures, various modulation schemes, and power control strategies for MMCs that have

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Haozhe Jin and Wu Chen are with the Center for Advanced Power Conversion Technology and Equipment, School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: jinhaozhe974@hotmail.com; chenwu@seu.edu.cn).

Yeyuan Xie is with the NR Electric Company, Ltd., Nanjing 211102, China (e-mail: xieyy@nrec.com).

Liangcai Shu is with the Department of Electrical Engineering, Eindhoven University of Technology, 5612 AP Eindhoven, The Netherlands (e-mail: 18362961507@163.com).

Yutao Xu is with the Electric Power Research Institute of Guizhou Power Grid Company, Ltd., Guiyang 550002, China (e-mail: 95616048@qq.com).

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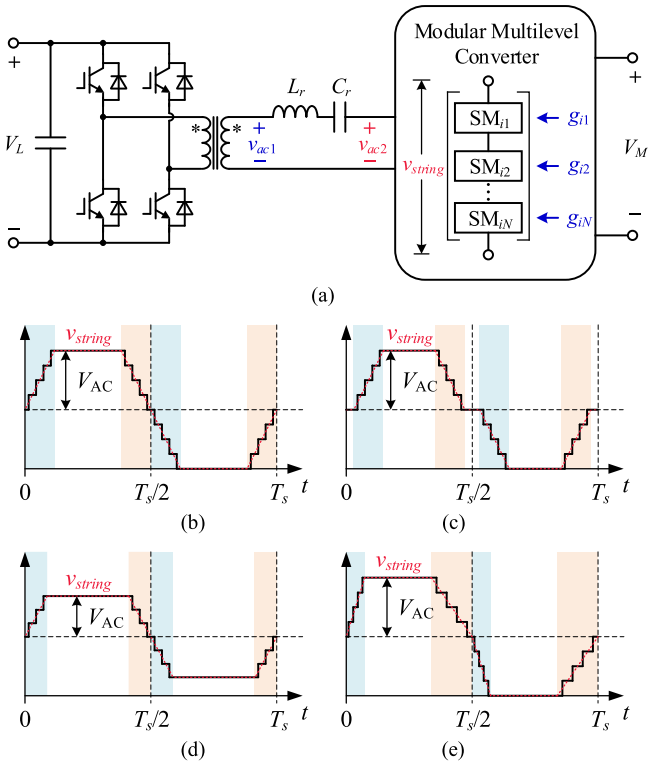

Fig. 1. Resonant type MMDC topology and different modulation schemes. (a) Topology. (b) Conventional QSW modulation. (c) QSW modulation with zero voltage stage added. (d) QSW modulation with constantly inserted and bypassed SMs. (e) Proposed ATW modulation.

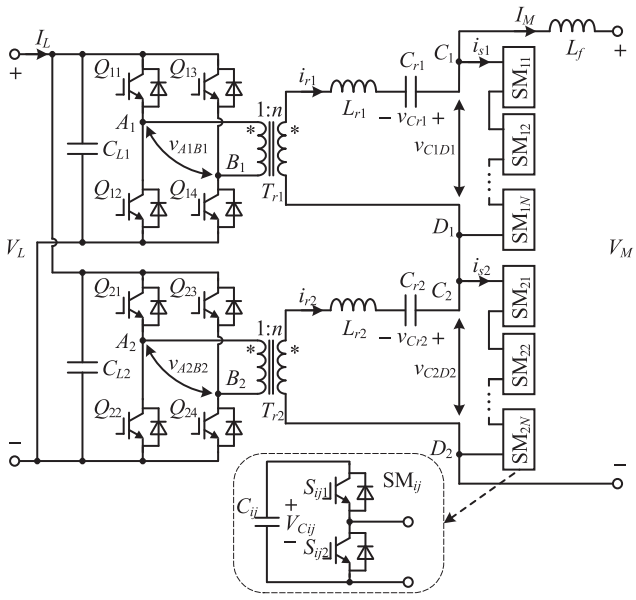

Fig. 2. Topology of MMRDC.

been validated and implemented can be extended to MMDCs [9], [11]. However, the ac link frequency for the conventional pulsewidth modulation (PWM) schemes is usually in tens to hundreds of hertz, resulting in large passive components [22]. In order to achieve higher ac link frequency, quasi-square-wave (QSW) modulation is proposed, as shown in Fig. 1(b) [23], [24]. With the QSW modulation, MMDCs operate as the convention two-level dc/dc converter with mitigated *dv*/*dt* stress on the MFT. The power density can be improved, and soft switching can be achieved under certain conditions. In [25], [26], and [27], DAB-type MMDCs with different topologies adopting QSW modulation and single-phase-shifted control are reported, which can achieve ZVS for all switches. Furthermore, the dual-phase-shift control [24] and trapezoidal current control [28], [29], [30] have been applied for DAB-type MMDCs to reduce the current stress and power loss, achieving higher efficiency.

The above modulation schemes regulate the ac-link voltage by adding a zero voltage stage shown in Fig. 1(c) and are similar to the conventional two-level converter. Besides, based on the QSW modulation, some advanced modulation schemes and control strategies have been employed in MMDCs. As shown in Fig. 1(d), the ac-link voltage can be adjusted by changing the constantly inserted and bypassed SM number, achieving wide voltage range regulation [14], [18], [31]. Moreover, the internal phase-shifted angle is used to regulate the ac-link voltage for MMRDC [21]. The internal phase-shifted control scheme allows MMRDC to operate in resonant current discontinuous conduction mode (DCM) with the fixed switching frequency, achieving ZCS for LV-side full bridges and ZVS for partial switches on MV-side SM strings. However, similar to the conventional DAB series resonant converter, the forward mode MMRDC employing the QSW modulation scheme exhibits high current stress and reactive current when operating in a wide voltage range and light load conditions.

To address the above problem, this article proposed a novel asymmetric trapezoidal wave (ATW) modulation scheme with an optimized control strategy for MMRDC. As shown in Fig. 1(e), the string output voltage is modulated as an asymmetric trapezoidal voltage waveform with different rising and falling process duty cycles by assigning different internal phase-shifted angles of SMs. Based on the time-domain mathematic model, the optimized control method is obtained considering low current stress and ZCS constraint for LV-side full-bridge switches. The rest of this article is organized as follows. In Section II, the ATW modulation for MMRDC is introduced. And Section III provides the optimization process and control strategy. In Section IV, experimental results are carried out. In Section V, some discussions are given. Finally, Section VI concludes the article.

II. ATW Modulation for MMRDC

A. Circuit Configuration

Fig. 2 illustrates the topology of the MMRDC proposed in [21]. The MMRDC is mainly composed of two phases. Each phase includes an LV-side full bridge Q_{i1}–Q_{i4} ($i = 1, 2$), an MFT T_{ri}, a resonant inductor L_{ri}, a resonant capacitor $C_{ri,}$ and an N series-connected half-bridge SM string. Two LV-side full bridges connected in parallel to interface with the LV terminal. The filter inductor L_f and two half-bridge SM strings are connected in series to interface with the MV terminal. V_L and V_M

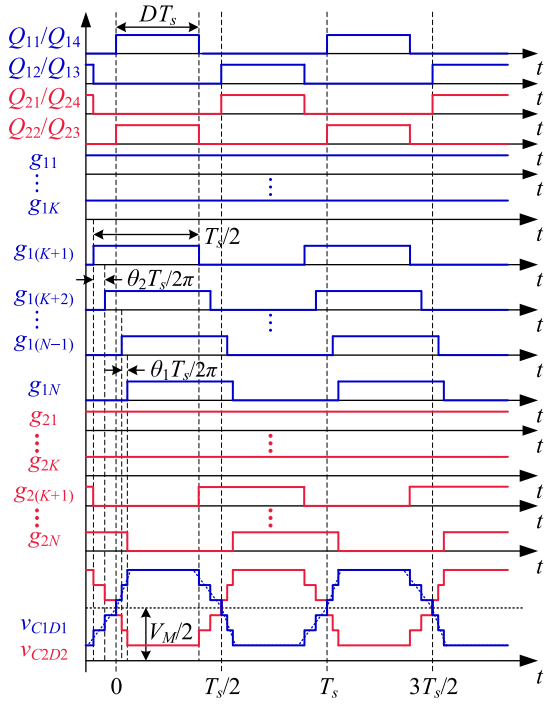

Fig. 3. Proposed ATW modulation scheme.

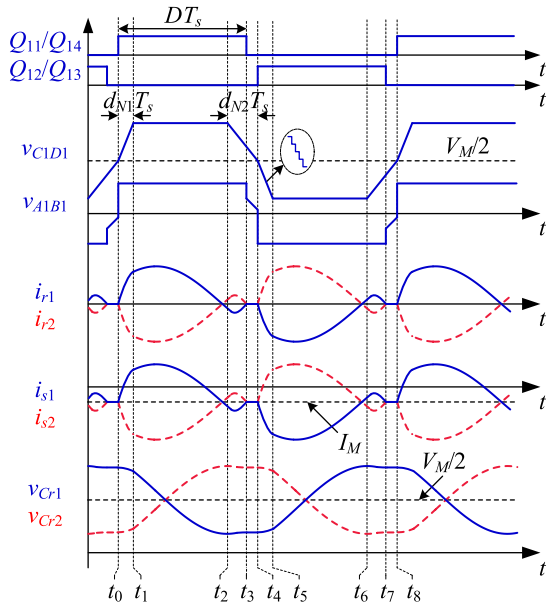

Fig. 4. Operating waveforms of MMRDC with ATW modulation scheme.

are the voltage across LV and MV terminals, respectively. The turns ratio of T_{ri} is 1:n.

B. ATW Modulation

The proposed ATW modulation scheme is shown in Fig. 3. The full bridges on the LV side employ a basic PWM control strategy with duty cycle D. The driving signals of two full bridges are phase-shifted by 180°. For MV-side half-bridge SMs, the driving signals of upper and lower switches in each SMs are complementary with sufficient dead time. The driving signal of the upper switch is denoted as g_{ij} ($i = 1, 2, j = 1, 2, \ldots, N$). As shown in Fig. 3, K SMs are constantly inserted for each SM string, while $N-K$ SMs work with 50% duty cycle. Additionally, an internal phase-shifted angle is introduced between two adjacent driving signals with 50% duty cycle ($g_{i(K+1)} \sim g_{iN}$). And the internal phase-shifted angles before and after $t = 0$ are denoted as θ_2 and θ_1, respectively. Assuming that the SM capacitor voltage V_{Cij} is well balanced, the string output voltages v_{C1D1} and v_{C2D2} are staircase waveforms with $N-K+1$ steps. In addition, the driving signals of two strings are phase-shifted 180° with each other. Hence, a total number of $N+K$ SMs are inserted at any instant to withstand the MV terminal voltage. Accordingly, the MV terminal voltage V_M can be expressed as

$$V_M = v_{C1D1} + v_{C2D2} = (N + K)\, V_C. \tag{1}$$

Based on (1), the SM capacitor voltage V_C can be expressed as

$$V_C = \frac{V_M}{N + K}. \tag{2}$$

According to Fig. 3 and (2), the dc bias component of v_{C1D1} and v_{C2D2}, which are denoted as V_{d1} and V_{d2}, respectively, can be calculated as

$$V_{d1} = V_{d2} = \frac{1}{2}\left(KV_C + NV_C\right) = \frac{V_M}{2}. \tag{3}$$

In addition, the amplitude of ac components of v_{C1D1} and v_{C2D2} can be expressed as

$$V_{C1D1} = V_{C2D2} = \frac{N - K}{2\,(N + K)} V_M. \tag{4}$$

As shown in Fig. 3, the ac components of v_{C1D1} and v_{C2D2} can be regarded as a trapezoidal voltage waveform in reference to $V_M/2$ over half switching period $T_s/2$. When $\theta_1 \neq \theta_2$, the ac components of v_{C1D1} and v_{C2D2} are asymmetric trapezoidal voltage waveforms. Hence, the proposed modulation scheme is called ATW modulation. And when $\theta_1 = \theta_2$, the ac components of v_{C1D1} and v_{C2D2} are isosceles trapezoid voltage waveforms, namely, conventionally QSW modulation scheme [23], [24].

Fig. 4 shows the operating waveforms of MMRDC with the proposed ATW modulation scheme. The string current of each phase is composed of the resonant current i_{ri} and circulating current I_M, which can be expressed as (5) where P_t is the transmission power of MMRDC

$$i_{si} = i_{ri} - I_M = i_{ri} - \frac{P_t}{V_M}. \tag{5}$$

C. Transmission Power

The MMRDC operates in resonant current DCM to achieve low switching loss in forward and backward modes. Similar to the traditional DAB series resonant converter, the MMRDC with the conventional QSW modulation scheme suffers large reactive current when operating over a wide voltage range and under light load conditions in forward mode, resulting in low efficiency [21].

Therefore, this article focuses on the forward mode and proposes the ATW modulation scheme to further improve the performance of MMDC over wide power and voltage ranges.

The staircase voltage during the rising and falling processes of v_{C1D1} and v_{C2D2} are simplified into oblique lines with different slopes in the case of a large number of SMs for practical applications to facilitate the analysis and calculation [13]. As shown in Fig. 4, the duty cycles of the rising and falling processes are denoted as d_{N1} and d_{N2}, respectively. Referring to Fig. 3, $d_{N1} = (N-K)\theta_1/4\pi$, $d_{N2} = (N-K)\theta_2/4\pi$. In addition, the ranges of d_{N1}, d_{N2}, and $d_{N1}+d_{N2}$ are set as [0, 0.5]. The ac components of v_{C1D1} and v_{C2D2} are square voltage waveforms when $d_{N1}+d_{N2} = 0$, namely $d_{N1} = d_{N2} = 0$. And when $d_{N1}+d_{N2} = 0.5$, the ac components of v_{C1D1} and v_{C2D2} are triangular voltage waveforms. It should be noted that the lower limits of d_{N1} and d_{N2} need to be slightly greater than 0 for practical applications to reduce dv/dt.

Since the operation principle of the two phases is identical, the example of $i = 1$ is used in the following description. According to Fig. 4, v_{A1B1} and v_{C1D1} can be expressed as (6) and (7), where v_{Cr1} is the voltage across resonant capacitor C_{r1}

$$v_{A1B1}(t) = \begin{cases} V_L, & t_0 \le t < t_3 \\ \frac{v_{C1D1}(t)-v_{Cr1}(t)}{n}, & t_3 \le t < t_4 \end{cases} \tag{6}$$

$$v_{C1D1}(t) = \begin{cases} \frac{V_M}{2} + \frac{(N-K)V_M}{2(N+K)d_{N1}T_s}(t-t_0), & t_0 \le t < t_1 \\ \frac{NV_M}{N+K}, & t_1 \le t < t_2 \\ \frac{NV_M}{N+K} - \frac{(N-K)V_M}{2(N+K)d_{N2}T_s}(t-t_2), & t_2 \le t < t_4 \end{cases}. \tag{7}$$

The power conversion of MMRDC can be viewed as the power exchange between voltage sources v_{A1B1} and v_{C1D1} through the resonant inductor L_{r1}, the resonant capacitor C_{r1}, and the MFT T_{r1}. Therefore, the state equation of the circuit is obtained as

$$\begin{cases} L_{r1}\frac{di_{r1}(t)}{dt} = v_{Cr1}(t) + nv_{A1B1}(t) - v_{C1D1}(t) \\ C_{r1}\frac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{8}$$

By substituting (6) and (7) into (8), the resonant current i_{r1} and the resonant capacitor voltage v_{Cr1} can be expressed as (A1) and (A2) in the Appendix, where the resonant frequency f_r and the characteristic impedance of the resonant tank Z_r are defined as

$$f_r = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}} = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}} = \frac{1}{2\pi\sqrt{L_rC_r}} \tag{9}$$

$$Z_r = \sqrt{\frac{L_{r1}}{C_{r1}}} = \sqrt{\frac{L_{r2}}{C_{r2}}} = \sqrt{\frac{L_r}{C_r}}. \tag{10}$$

According to Fig. 4, the waveforms of i_{r1} and v_{Cr1} are symmetrical in one switching period so that the following relationships for i_{r1} and v_{Cr1} can be obtained, where the initial resonant current $i_{r1}(t_0)$ is zero

$$\begin{cases} i_{r1}(t_0) = i_{r1}(t_4) = i_{r1}(t_8) = 0 \\ v_{Cr1}(t_0) = V_M - v_{Cr1}(t_4) = v_{Cr1}(t_8) \end{cases}. \tag{11}$$

TABLE I
PARAMETERS OF MMRDC TO BE OPTIMIZED

Parameters	Value
LV terminal voltage V_L/V	80–100
MV terminal voltage V_M/kV	1
Rated power P_N/kW	4
Switching frequency f_s/kHz	10
Number of SMs per string N	4
Number of constantly inserted SMs K	1
SM capacitor C_{ij}/μF	150
Filter inductor L_f/mH	2.5
Resonant inductor L_{ri}/μH	85
Resonant capacitor C_{ri}/μF	4
Transformer turns ratio 1:n	1:2.9
LV-side capacitor C_{Li}/μF	940

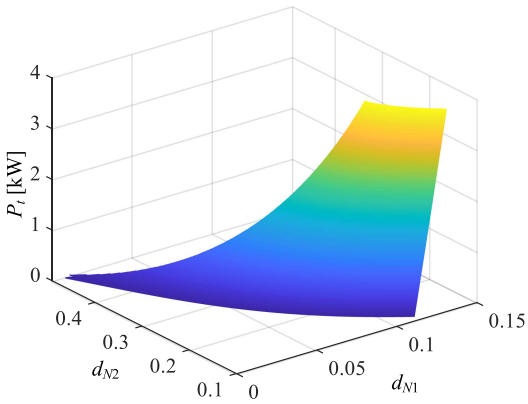

Fig. 5. Power transmission P_t versus the duty cycles of string voltage rising process d_{N1} and falling process d_{N2}.

In addition, the transmission power of MMRDC P_t can be expressed as

$$P_t = \frac{4}{T_s}\int_{t_0}^{t_4} nv_{A1B1}(t)i_{r1}(t)\mathrm{d}t. \tag{12}$$

According to (A1), (A2), and (12), the transmission power of MMRDC can be derived as (A3) in Appendix. And the numerical solution of transmission power can be solved with (11) and (A3) based on the parameters in Table I, which is also taken as the instance for the following optimization and the final verification. The result is shown in Fig. 5, where V_L is set as 90 V. As shown in Fig. 5, P_t increases with the increase of d_{N1} and d_{N2}. Hence, the transmission power P_t can be regulated by d_{N1} and d_{N2} under the fixed switching frequency. Additionally, multiple combinations of d_{N1} and d_{N2} exist for the same P_t.

D. Switching Characteristics

For MMRDC, the switching characteristics behave differently between LV-side full-bridge switches and MV-side half-bridge SM switches. LV-side full-bridge switches can achieve ZCS-OFF with the proposed ATW modulation scheme. While the switches of MV-side half-bridge SMs have different switching characteristics due to the dc circulating current and the values of d_{N1} and d_{N2}.

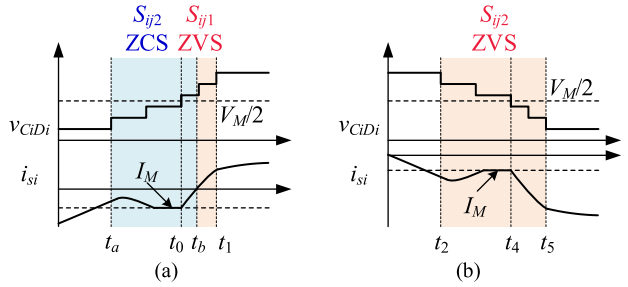

Fig. 6. Switching characteristics of SM switches. (a) String voltage rising stage. (b) String voltage falling stage.

According to Fig. 4, taking $i = 1$ as an example, the resonant current i_{r1} decreases from positive to zero after $t = t_1$ to guarantee the ZCS-OFF of LV-side full-bridge switches. Namely, the minimum value of i_{r1} is negative. In addition, i_{r1} should rise to zero at $t = t_3 = DT_s$ before $t = t_4 = T_s/2$ to ensure the DCM operation of MMRDC. Therefore, the following equation can be obtained to realize the ZCS-OFF and DCM operation for MMRDC, where $I_{r1\mathrm{m}}$ is the minimum value of the resonant current i_{r1}

$$I_{r1\mathrm{m}} \le 0 \tag{13}$$

$$0.5 - d_{N2} \le D \le 0.5. \tag{14}$$

In practice, the LV-side full-bridge switches can be turned OFF with negative i_{r1} before t_3. It should be noted that the ZCS-OFF of LV-side full-bridge switches can be ensured with the ATW modulation scheme and appropriated parameters design.

The switching characteristics of MV-side half-bridge SMs switches are determined by the transition process of string voltage v_{CiDi} and the string current i_{si} as shown in Fig. 6. During the string voltage rising stage, SMs are inserted one by one. For the inserted SM, the lower switch S_{ij2} can be turned OFF with ZCS when string current i_{si}<0, while the upper switch S_{ij1} can achieve ZVS-ON with positive i_{si}. As illustrated in Fig. 6(a), from t_a to t_b, the lower switches of inserted SMs achieve ZCS-OFF, and the upper switches of SMs inserted from t_b to t_1 realize ZVS-ON. During the string voltage falling stage shown in Fig. 6(b), the lower switches of the bypassed SMs can achieve ZVS-ON with negative i_{si}.

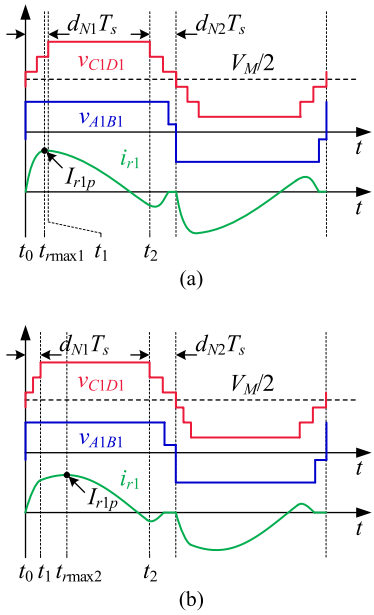

Fig. 7. Two cases of the peak resonant current I_{r1p}. (a) Case 1: I_{r1p} reaches during $[t_0, t_1]$. (b) Case 2: I_{r1p} reaches during $[t_1, t_2]$.

E. Current Stress

According to (8), (A1), and (A2), it can be proved that there must be one peak resonant current I_{r1p} within $[t_0, t_2]$. And based on the different operation modes, I_{r1p} can be discussed and solved in two cases, as illustrated in Fig. 7. According to Fig. 7(a), the peak value of resonant current I_{r1p} reaches at $t_{r\max1}$ in Case 1, which is located within $[t_0, t_1]$, namely the string voltage v_{C1D1} rising stage. Based on (A1), $t_{r\max1}$ and I_{r1p} can be written as (15) and (16), respectively.

Fig. 7(b) shows that the peak value of resonant current I_{r1p} reaches at $t_{r\max2}$ during $[t_1, t_2]$ in Case 2. Therefore, according to (A1), $t_{r\max2}$ and I_{r1p} can be expressed as (17), shown at the bottom of the page and (18), respectively

$$\begin{aligned} I_{r1p} &= i_{r1}\left(t_{r\max 2}\right) \\ &= \sqrt{i_{r1}^2\left(t_1\right) + \left(v_{Cr1}\left(t_1\right) + nV_L - \frac{NV_M}{N+K}\right)^2 \frac{1}{Z_r^2}}. \end{aligned} \tag{18}$$

$$t_{r\max 1} = \frac{1}{\omega_r}\arctan\left(\frac{2\left(N+K\right)\omega_r d_{N1}T_s}{\left(N-K\right)V_M}\left(v_{Cr1}\left(t_0\right) + nV_L - \frac{V_M}{2}\right)\right) \tag{15}$$

$$I_{r1p} = i_{r1}\left(t_{r\max 1}\right) = \sqrt{\left(\frac{1}{\omega_r Z_r}\frac{\left(N-K\right)V_M}{2\left(N+K\right)d_{N1}T_s}\right)^2 + \left(v_{Cr1}\left(t_0\right) + nV_L - \frac{V_M}{2}\right)^2\frac{1}{Z_r^2}} - \frac{1}{\omega_r Z_r}\frac{\left(N-K\right)V_M}{2\left(N+K\right)d_{N1}T_s}. \tag{16}$$

$$t_{r\max 2} = \frac{1}{\omega_r}\arctan\left(\frac{1}{Z_r i_{r1}\left(t_1\right)}\left(v_{Cr1}\left(t_1\right) + nV_L - \frac{NV_M}{N+K}\right)\right) + t_1 \tag{17}$$

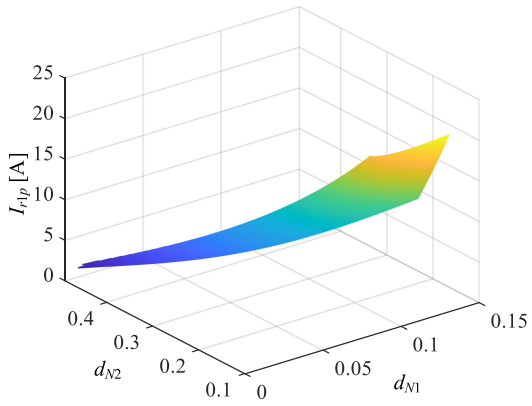

Fig. 8. Current stress I_{r1p} versus the duty cycles of string voltage rising process d_{N1} and falling process d_{N2}.

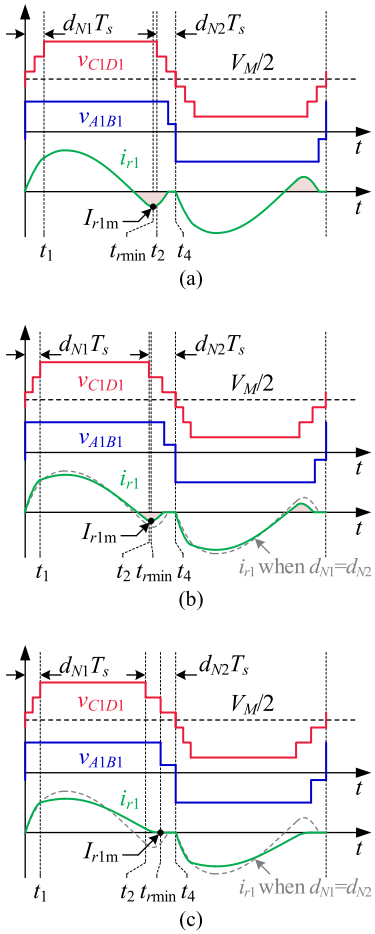

Fig. 9. Operation waveforms of MMRDC with different combinations of d_{N1} and d_{N2}. (a) With the conventional QSW modulation. (b) With the ATW modulation. (c) With the optimized ATM modulation.

In addition, according to (5), the peak value of string current I_{s1p} can be expressed as (19), where P_t and V_M are constant values when MMRDC operates in a steady state

$$I_{s1p} = I_{r1p} + \frac{P_t}{V_M}. \tag{19}$$

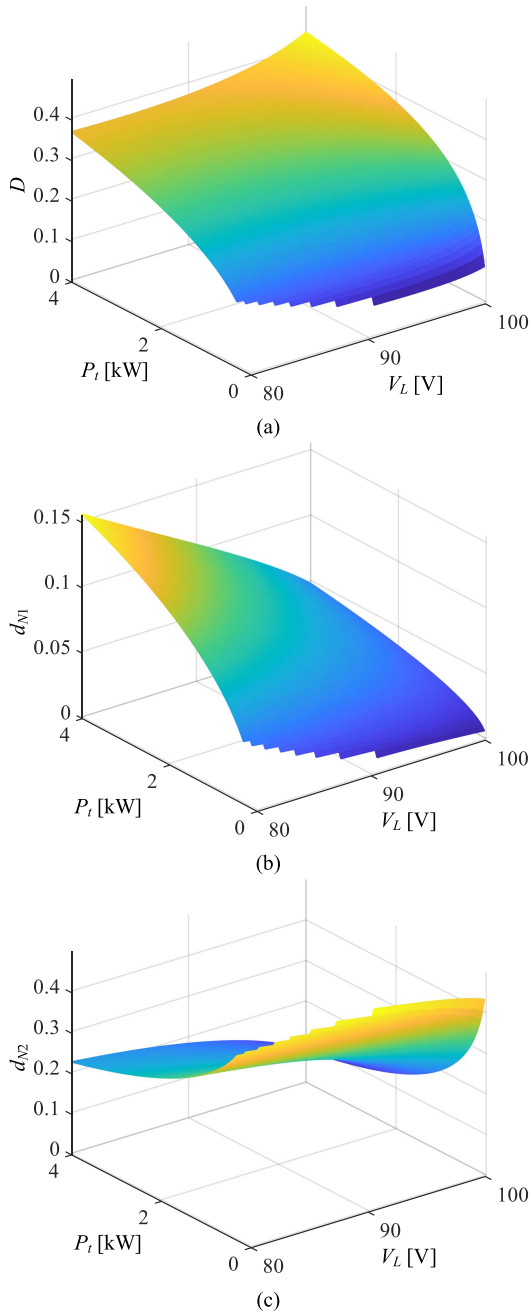

Fig. 10. Optimized solutions with the proposed ATW modulation. (a) Optimized results of D. (b) Optimized results of d_{N1}. (c) Optimized results of d_{N2}.

Therefore, I_{r1p} can be defined as the current stress of MMRDC, which can also indicate the reactive power.

The curves of current stress I_{r1p} versus the string voltage rising stage duty cycle d_{N1} and the falling stage duty cycle d_{N2} is present in Fig. 8, where V_M is set at 90 V. Fig. 8 demonstrates that the current stress of the MMRDC increases with the increase of d_{N1} and d_{N2}. As mentioned before, for a specific transmission power P_t, there are plenty of combinations of d_{N1} and d_{N2} that can be chosen. Therefore, the current stress I_{r1p} can be changed by the different d_{N1} and d_{N2} with the proposed ATW modulation scheme.

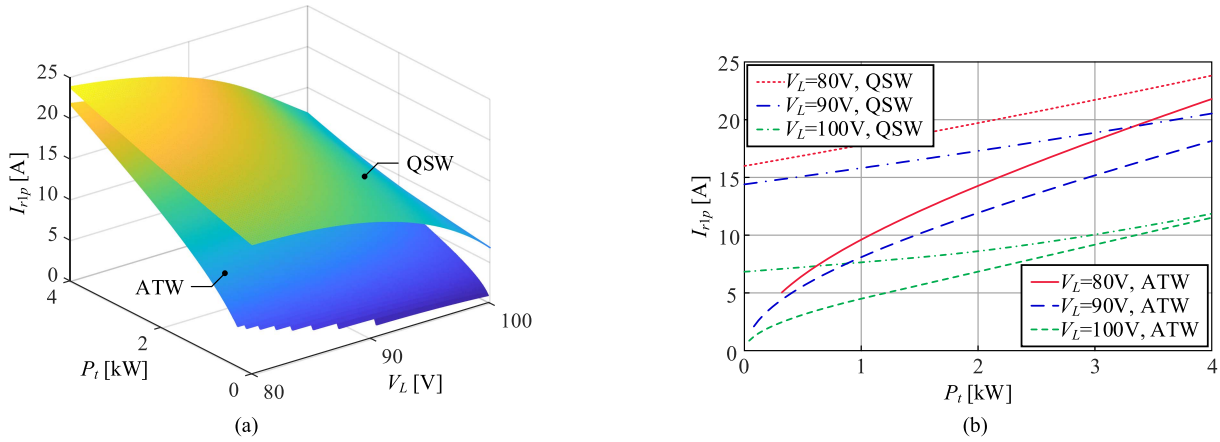

Fig. 11. Characteristics of current stress I_{r1p} with different modulation schemes. (a) I_{r1p} versus V_L and P_t. (b) I_{r1p} versus P_t under different V_L.

III. Optimization and Control Strategy

According to the preceding analysis, the current stress of MMRDC can be optimized by the ATW modulation scheme. Fig. 9 shows the operation waveform with different combinations of d_{N1} and d_{N2} under the same transmission power P_t. Fig. 9(a) shows the operation waveforms with the conventional QSW modulation, namely $d_{N1} = d_{N2}$. The resonant current involves a portion of the reverse current (shadow area), which is defined as the reactive current of MMRDC. And the reactive current will increase the current stress of MMRDC, leading to high conduction loss of power switches and copper loss of transformers [32]. With the proposed ATW modulation scheme, d_{N1} and d_{N2} can be controlled separately, as shown in Fig. 9(b) and (c). According to Fig. 9(b), the reactive current and current stress of MMRDC are reduced compared to the conventional QSW modulation when $d_{N1}<d_{N2}$. When further increasing d_{N2}, there exists a specific combination of d_{N1} and d_{N2} with zero reactive current and low current stress for the same transmission power. The optimized operation condition with zero reactive current is shown in Fig. 9(c). According to Fig. 9(c), i_{r1} is resonant to zero during the string voltage falling stage. And the ZCS-OFF of LV-side full-bridge switches is realized critically under this condition.

Based on Fig. 9(c), i_{r1} resonant to zero at $t_{r\min}$. According to (A1), the value of $t_{r\min}$ can be obtained as

$$t_{r\min} = t_2 + \frac{1}{\omega_r}\arctan\left(\frac{v_{Cr1}(t_2) + nV_L - \frac{NV_M}{N+K}}{Z_r i_{r1}(t_2) - \frac{1}{\omega_r}\frac{(N-K)V_M}{2(N+K)d_{N2}T_s}}\right). \tag{20}$$

Besides, the $t_{r\min}$ can also be expressed as (21) under this condition

$$t_{r\min} = DT_s. \tag{21}$$

Therefore, an additional constraint to realize the optimized operating condition can be obtained by substituting (20) into (21).

According to (11), (20), (21), and (A3), the optimized solutions of d_{N1}, d_{N2}, and D with the proposed ATW modulation are shown in Fig. 10. Since the MV terminal voltage is set as the controlling target, the optimized solutions are only versus LV terminal voltage V_L and transmission power P_t. As shown in Fig. 10(a), D rises with LV terminal voltage V_L and transmission power P_t. Additionally, d_{N1} increases with the increase of P_t and the decrease of V_L in Fig. 10(b), while d_{N2} increases with the decrease of P_t and V_L in Fig. 10(c). It should be noted that zero reactive current characteristics may be lost when in light load and low LV terminal voltage due to the upper and lower limits of d_{N1} and d_{N2}. When the terminal voltage varies over a wider range, a cooperative control can be used to achieve low current stress by changing the number of constantly inserted SMs in combination with the optimized ATW modulation scheme [14].

From (15) to (18), the current stress I_{r1p} of MMRDC with optimized ATW modulation and conventional QSW modulation schemes are presented in Fig. 11. According to Fig. 11, the current stress I_{r1p} of QSW modulation and optimized ATW modulation increase with the increase of transmission power P_t and the decrease of LV terminal voltage V_L. The optimized ATW modulation scheme can achieve lower current stress I_{r1p} than the conventional QSW modulation scheme. And the reduction is more significant for operating conditions with low LV terminal voltage and light load conditions.

Fig. 12 shows the theoretical and simulation values of current stress I_{r1p} and root mean square (RMS) resonant current $I_{r1\mathrm{RMS}}$ with optimized ATW modulation scheme and conventional QSW modulation scheme. According to Fig. 12, the theoretical value is consistent with the corresponding simulation value. Additionally, the optimized ATW modulation scheme can decrease I_{r1p} while dramatically reducing $I_{r1\mathrm{RMS}}$. And the difference in currents of two different modulation schemes is more noticeable under low LV terminal voltage and light load conditions.

Based on the previous analysis, the power loss of semiconductor switches is performed in Fig. 13, including conduction loss and switching loss. IKW40N65ET7 IGBTs are used as both LV-side full-bridge switches and MV-side half-bridge SM

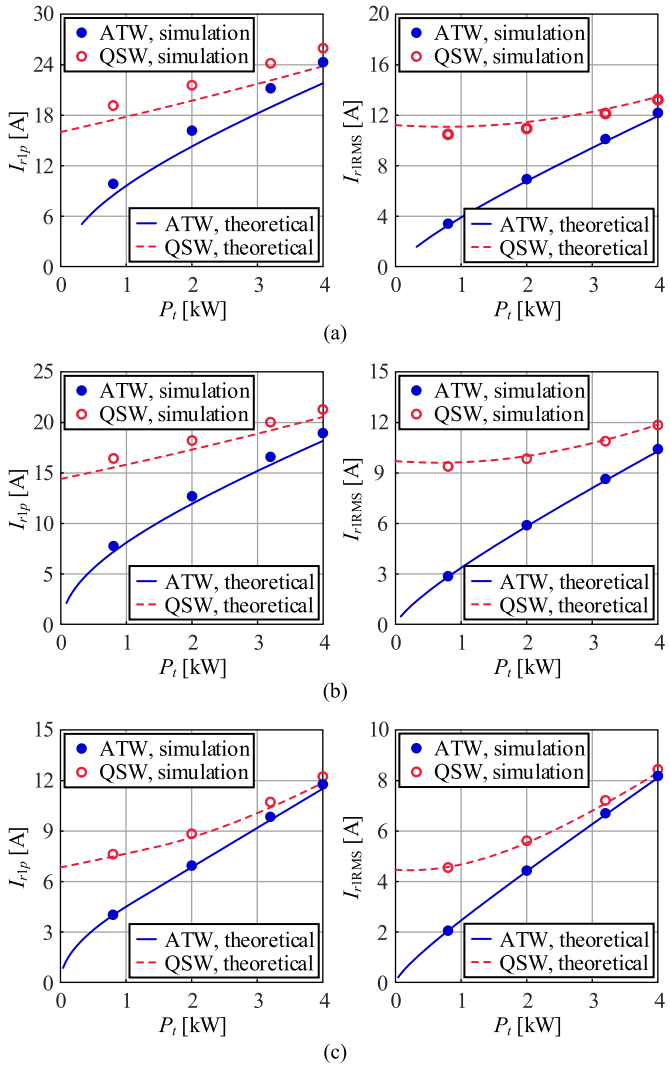

Fig. 12. Current stress I_{r1p} and RMS resonant current $I_{r1\mathrm{RMS}}$ versus transmission power P_t based on theoretical analysis and simulation with different modulation schemes. (a) $V_L = 80$ V. (b) $V_L = 90$ V. (c) $V_L = 100$ V.

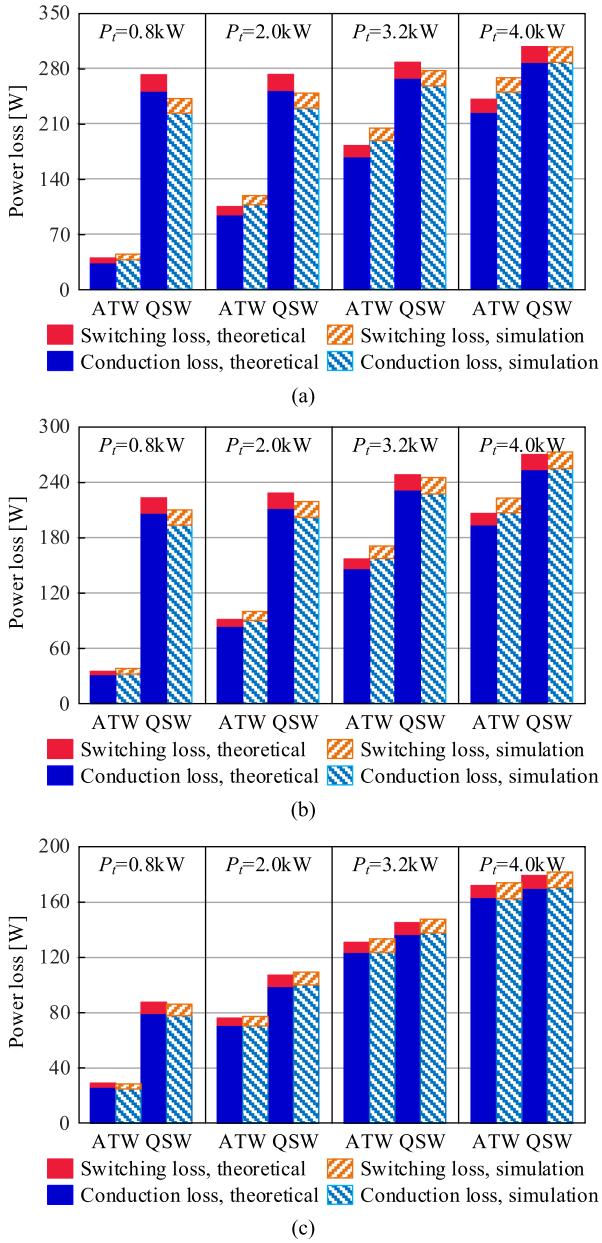

Fig. 13. Power loss of switches with different transmission power P_t under two modulation schemes. (a) $V_L = 80$ V. (b) $V_L = 90$ V. (c) $V_L = 100$ V.

switches. The detailed calculation processes of conduction loss and switching loss can be founded in [21]. And the simulation results of the power loss are obtained by PLECS. As shown in Fig. 13, the conduction loss is relatively greater than the switching loss, and both losses rise as transmission power P_t increase and the LV terminal voltage V_L decrease. MMRDC with the optimized ATW modulation scheme can achieve lower switching and conduction loss than the conventional QSW modulation scheme due to the lower current stress I_{r1p} and RMS resonant current $I_{r1\mathrm{RMS}}$.

The control strategy of MMRDC is implemented by combining closed-loop and look-up table control methods to avoid complicated computation in real-time control, as illustrated in Fig. 14. The MV terminal voltage v_M is sampled and feedback to generate the given transmission power $p_t{}^*$. The average SM capacitor voltages of each string $V_{C1\mathrm{ave}}$ and $V_{C2\mathrm{ave}}$ are compared to obtain the compensation $\Delta p_t{}^*$ for $p_t{}^*$ to achieve voltage balancing between two half-bridge SM strings. With $p_t{}^*$, $\Delta p_t{}^*$, $v_{M,}$ and v_L, the control variables D_i, $d_{N1i,}$ and d_{N2i} for each string can be obtained by searching the optimized results table. Since the optimized results are discrete, the interpolation method is employed to further regulate D_i, $d_{N1i,}$ and d_{N2i} under different terminal voltage and load conditions. The open loop rotation modulation scheme is adopted for the experimental prototype to achieve SM voltage balancing [25], [33]. N-dimensional rotational SM voltage balance sequences $\boldsymbol{R}_{Ni}$ can be obtained with N and K, which indicate the switching patterns of SMs within the rotational SM voltage balance period NT_s for each string. Then, based on $\boldsymbol{R}_{Ni}$, D_i, $d_{N1i,}$ and d_{N2i}, the driving signals for MV-side SMs and LV-side full-bridge are generated utilizing the carrier phase-shifted (CPS) modulation

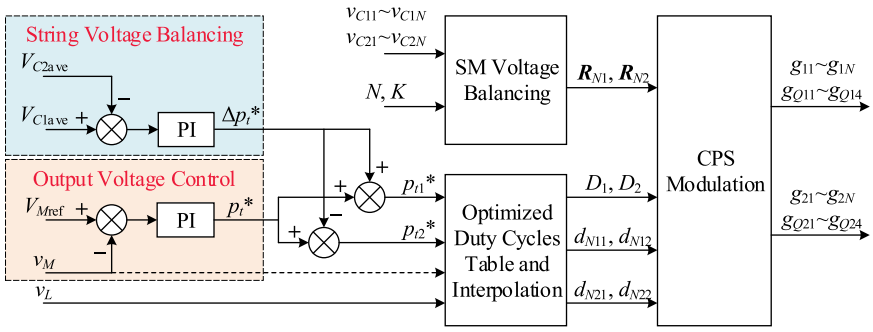

Fig. 14. Control block diagram for MMRDC with the optimized ATW modulation scheme.

strategy. It should be noted that the SM capacitor voltage sorting algorithm can be used in practical applications to achieve SM capacitor voltage balance [34].

In practical applications, the parallel control system architecture can be employed to implement the control strategy of MMRDC, which enables high-speed communication with scalability and broadcasting capability [35]. The output voltage control, string voltage balancing control, SM voltage balancing control, and optimized control can be executed by the central controller, generating internal phase-shifted angles and duty cycles for each SM and LV-side full bridge. Then, the central controller sends the internal phase-shifted angles and duty cycles to the corresponding local controller for gate signal generation. Additionally, an accurate synchronization signal, such as a synchronization data packet, is broadcast to each local controller to inform them about the reference phase in every switching period [36].

IV. Experimental Verification

In this section, a 4 kW prototype is established to verify the present analysis. Experimental parameters are listed in Table I, where the LV terminal voltage V_L ranges from 80 to 100 V while the MV terminal voltage V_M is controlled as 1 kV. A TMS320F28346 DSP and a C6SLX16-2FTG256I FPGA are utilized to implement the control strategy. The dead time is set as 2 μs. The experimental waveforms are shown in Figs. 15 –19 based on the optimized results of the proposed ATW modulation scheme in Fig. 10.

Fig. 15 illustrates the steady-state experimental waveforms of v_{A1B1}, v_{C1D1}, $i_{r1,}$ and i_{r2} with the optimized ATW modulation scheme when $V_L = 100$ V. When one SM is constantly inserted, the string voltage v_{C1D1} is a three-step asymmetric trapezoidal staircase waveform with a minimum value of 200 V and a maximum value of 800 V. And the resonant currents i_{r1} and i_{r2} have a phase-shifted angle of 180° between each other. As shown in Fig. 15(a), d_{N1} is 0.10 and d_{N2} is 0.17 when $P_t = 4$ kW. And the peak value of i_{r1} and i_{r2} is 17.2 A in this condition. In Fig. 15(b), where $P_t = 2$ kW, d_{N1} decrease to 0.07 and d_{N2} increase to 0.23. Both i_{r1} and i_{r2} have a peak value of 11.2 A. Fig. 15(c) presents the waveforms when $P_t = 800$ W. The value of d_{N1} and d_{N2} are changed to 0.04 and 0.36, respectively. The peak value of i_{r1} and i_{r2} is 6.2 A. Because of the low SM number ($N = 4$, $K = 1$) and saturation voltage of power

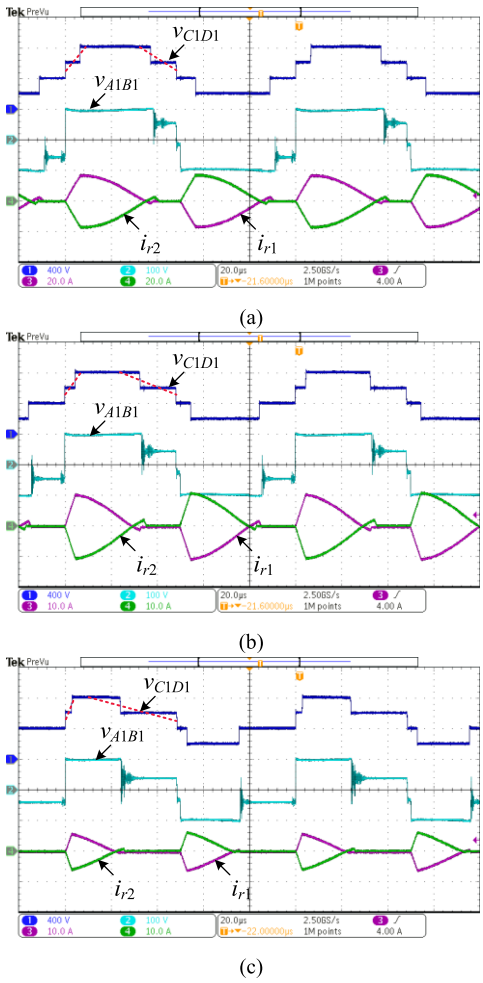

Fig. 15. Steady-state experimental waveforms of v_{A1B1}, v_{C1D1}, $i_{r1,}$ and i_{r2} with the optimized ATW modulation scheme when $V_L = 100$ V. (a)$P_t = 4$ kW. (b)$P_t = 2$ kW. (c) $P_t = 800$ W.

switches, the control variables d_{N1}, $d_{N2,}$ and the peak value of i_{r1} and i_{r2} are greater than the corresponding analysis results. This can be avoided in practical applications where the number of SMs is large to sustain the MV terminal voltage (usually tens of kilovolts). Furthermore, the positive and negative periods of i_{r1} and i_{r2} are not strictly symmetrical due to the dead time of power devices. These experimental results demonstrate that

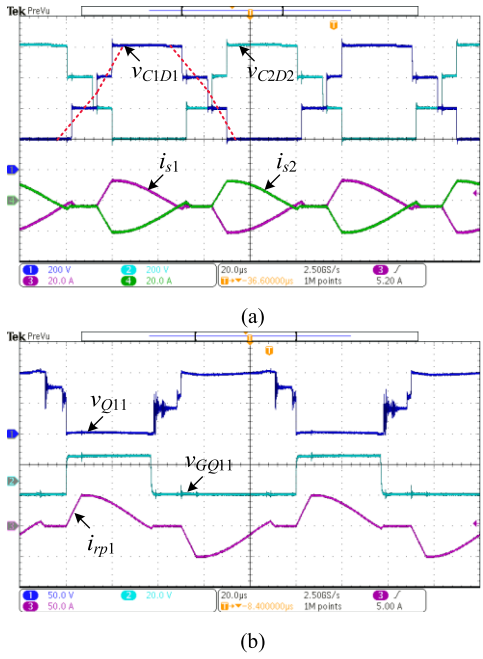

Fig. 16. Steady-state experimental waveforms with the optimized ATW modulation scheme when $V_L = 100$ V and $P_t = 4$ kW. (a) v_{C1D1}, v_{C2D2}, i_{s1}, and i_{s2}. (b) v_{Q11}, v_{GQ11}, and i_{rp1}.

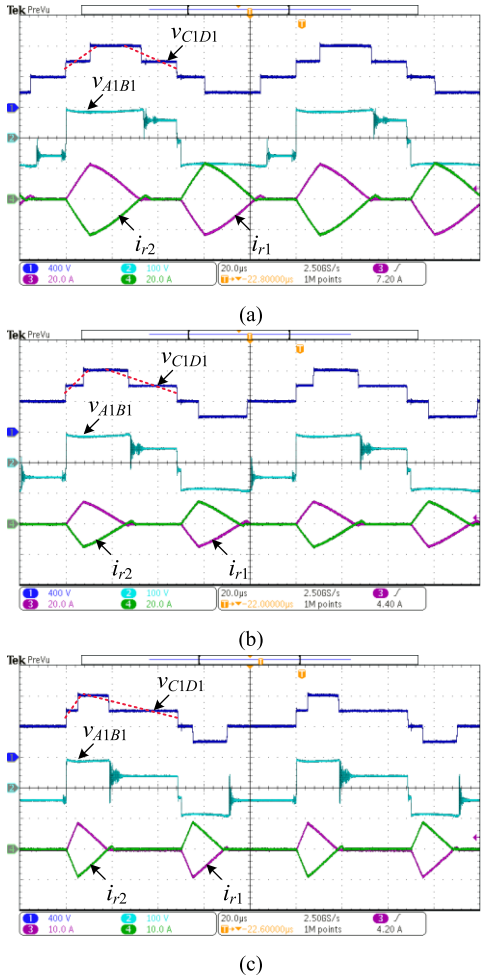

Fig. 17. Steady-state experimental waveforms of v_{A1B1}, v_{C1D1}, i_{r1}, and i_{r2} with the optimized ATW modulation scheme when $V_L = 90$ V. (a) $P_t = 4$ kW. (b) $P_t = 2$ kW. (c) $P_t = 800$ W.

employing the optimized ATW modulation scheme can achieve a low reactive current of MMRDC no matter under light- or heavy-load situations.

As indicated in Fig. 16(a), the string voltage v_{C1D1} and v_{C2D2}, as well as the string current i_{s1} and i_{s2}, are phase-shifted by 180°. And i_{s1} and i_{s2} have an -4 A dc bias when $V_L = 100$ V and $P_t = 4$ kW. During the string voltage rising stage, two lower switches can achieve ZCS-OFF with negative i_{s1} and i_{s2}, whereas one upper switch can achieve ZVS-ON with positive i_{s1} and i_{s2}. Additionally, during the string voltage falling stage, i_{s1} and i_{s2} are negative, indicating that all SM lower switches are turned ON with ZVS. As shown in Fig. 16(b), v_{Q11} and v_{GQ11} are the waveforms of the voltage across Q_{11} and the driving signal of Q_{11}, respectively. And i_{rp1} is the primary current of the transformer. The ZCS-OFF of LV-side full-bridge switch Q_{11} can be achieved with the negative turn-OFF current.

Figs. 17 and 18 show the experimental waveforms of v_{A1B1}, v_{C1D1}, i_{r1}, and i_{r2} with the optimized ATW modulation scheme when V_L is set as 90 and 80 V, respectively. These experimental results verify that the MMRDC can achieve minimum reactive current (hence low current stress) with the optimized results of d_{N1}, d_{N2}, and D given in Fig. 10 under different LV terminal voltage and transmission power conditions.

Fig. 19 shows the experimental waveforms of v_{A1B1}, v_{C1D1}, i_{r1}, and i_{r2} with different modulation schemes when $V_L = 100$ V and $P_t = 1$ kW. According to Fig. 19(a), when MMRDC employed the conventional QSW modulation, $d_{N1} = d_{N2} = 0.09$. And i_{r1} and i_{r2} have a peak value of 10.5 A. In Fig. 19(b), where the optimized ATW modulation scheme is employed, d_{N1} and d_{N2} are 0.05 and 0.33, respectively. The peak value of i_{r1} and i_{r2} is 6.8 A.

The current stress I_{r1p} versus transmission power P_t with the conventional QSW modulation scheme and the optimized ATW modulation scheme is plotted in Fig. 20 when V_L is set as 80, 90, and 100 V, respectively. The current stress increase as P_t increases and V_L decreases. Besides, under different LV terminal voltage and transmission power conditions, the MMRDC modulated with the proposed optimized ATW scheme has lower current stress than the conventional QSW modulation scheme.

Fig. 21 compares the measured efficiency of the conventional QSW modulation scheme and optimized ATW modulation scheme, where V_L ranges from 80 to 100 V and P_t varies from 400 W to 4 kW. Because of the lower current stress, the high-efficiency advantage of the proposed modulation scheme becomes apparent, especially under light-load and low LV terminal voltage conditions.

In addition, a loss breakdown comparison of the above-mentioned experiments with two different modulation schemes is carried out, as shown in Fig. 22, to demonstrate how the current

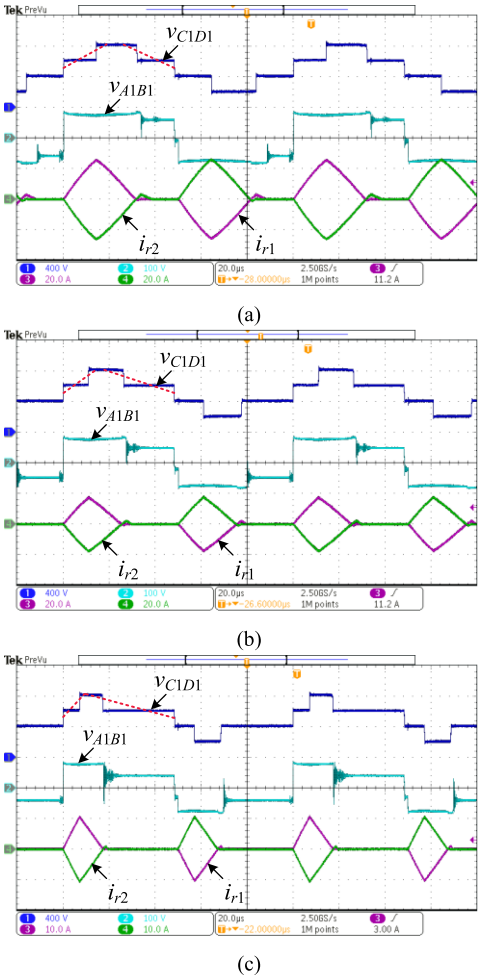

Fig. 18. Steady-state experimental waveforms of v_{A1B1}, v_{C1D1}, i_{r1}, and i_{r2} with the optimized ATW modulation scheme when $V_L = 80$ V. (a) $P_t = 4$ kW. (b) $P_t = 2$ kW. (c) $P_t = 800$ W.

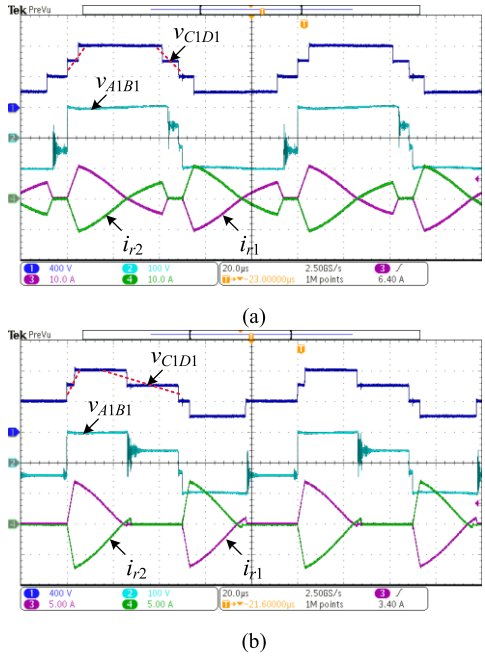

Fig. 19. Steady-state experimental waveforms of v_{A1B1}, v_{C1D1}, i_{r1}, and i_{r2} when $V_L = 100$ V and $P_t = 1$ kW with different modulation schemes. (a) QSW modulation scheme. (b) Optimized ATW modulation scheme.

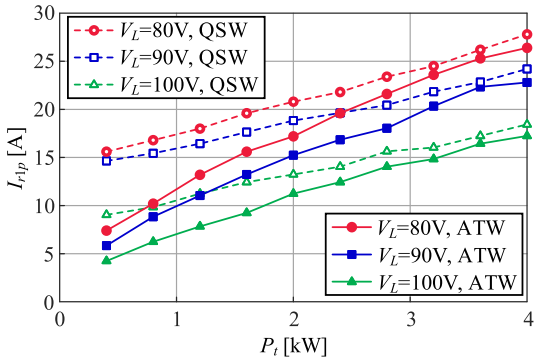

Fig. 20. Current stress I_{r1p} versus transmission power P_t with the conventional QSW modulation scheme and the optimized ATW modulation scheme under different V_L.

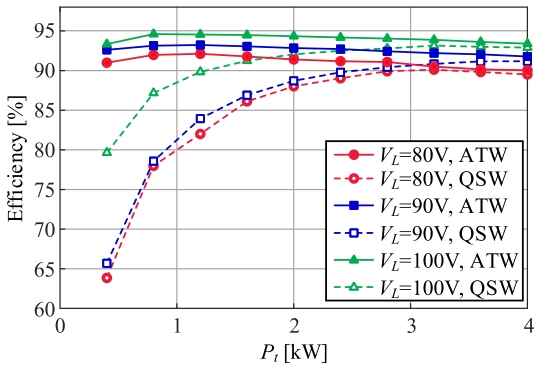

Fig. 21. Measured efficiency versus transmission power P_t with conventional QSW modulation scheme and optimized ATW modulation scheme. (a) $V_L = 80$ V. (b) $V_L = 90$ V. (c) $V_L = 100$ V.

stress decrement benefits loss reduction and efficiency improvement. It indicates that the conduction loss always accounts for the largest proportion of MMRDC under two modulation schemes. In this case, the overall loss can be significantly reduced by employing the optimized ATW modulation scheme with lower current stress, particularly under light-load and low LV terminal voltage conditions.

V. Discussion

In comparison to conventional isolated dc/dc converters, MMDCs can operate with additional control degrees of freedom benefiting from the modular multilevel structure. In this section, a brief comparison with some existing modulation schemes is provided.

For MMRDC with conventional QSW modulation, only one control variable can be used to regulate the transmission power with a fixed switching frequency [21]. With the proposed ATW modulation, two control variables can be used to achieve optimized current stress control for forward mode MMRDC. And

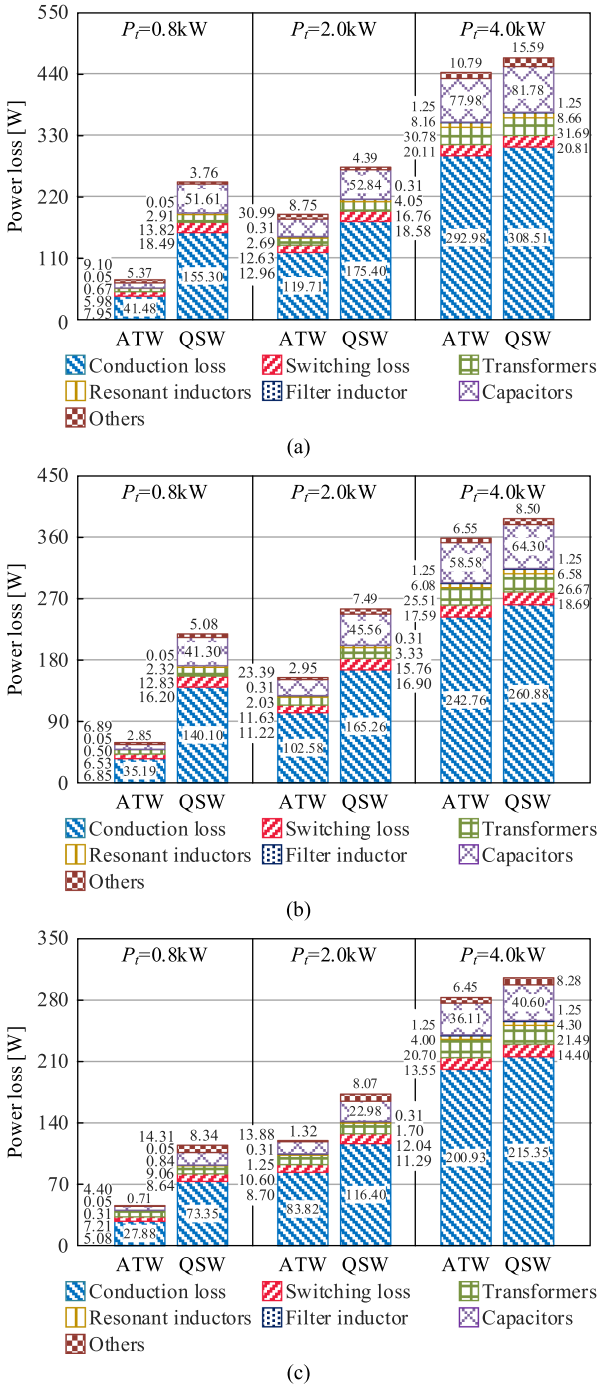

Fig. 22. Power loss breakdown with the conventional QSW modulation scheme and the optimized ATW modulation scheme under different V_L and P_t. (a) $V_L = 80$ V. (b) $V_L = 90$ V. (c) $V_L = 100$ V.

according to the aforementioned analysis, the suppression of reactive current is mainly achieved by controlling the duty cycle of the string voltage falling process d_{N2}. At the same time, the transmission power is primarily influenced by the duty cycle of the string voltage rising process d_{N1}.

The optimized current stress control can also be realized by adding a zero voltage stage into the ac-link voltage with QSW modulation. However, the QSW modulation with zero voltage stage added is only feasible when the number of string

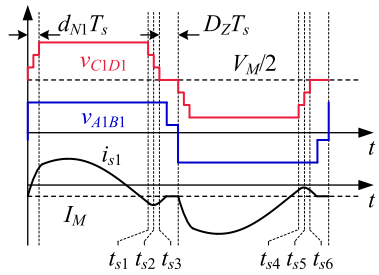

Fig. 23. Operation waveforms of MMRDC using QSW modulation with zero voltage stage added.

voltage step $N-K+1$ is odd for some MMDC structures, such as the MMRDC and half-bridge-type MMDCs. Fig. 23 depicts the operation waveforms of MMRDC with zero-voltage stage-added modulation. The reactive current can be reduced by increasing the duty cycle of zero voltage stage D_z and decreasing the duty cycle of the string voltage rising process d_{N1} ($d_{N1} = d_{N2}$ when using this control strategy). When zero reactive current is achieved, this control strategy obtains the same current suppression effect as the ATW modulation scheme but with a much higher dv/dt stress during the string voltage falling process. Furthermore, owing to the steeper string voltage falling process, the turn-OFF currents of lagging bypassed SM uppers switches increase during $[t_{s1}, t_{s3}]$ while the turn-ON currents of leading inserted SM upper switches decrease during $[t_{s4}, t_{s6}]$. However, because of the upper and lower limits of d_{N1} and d_{N2}, the ATW modulation has a smaller regulation range than the QSW modulation with zero voltage stage added. And this drawback could be overcome by utilizing additional control degrees of freedom, such as increasing the number of constant inserted SMs.

VI. Conclusion

This article proposes an optimized ATW modulation scheme to improve the performance of MMRDC over wide voltage and load ranges. The string output voltage is modulated as an asymmetric trapezoidal voltage waveform with different rising and falling process duty cycles using the ATW modulation scheme. And the detailed model of MMRDC under the ATW modulation scheme is established by employing the time-domain method. On this basis, the optimized operating point of MMRDC with low current stress can be founded while taking into account low current stress and ZCS constraint for LV-side full-bridge switches. And the numerical solutions of optimized control variables are then obtained. Finally, experiments with a 4 kW prototype are carried out, and the results verify the feasibility of the optimized ATW modulation scheme. Additionally, the proposed concept and strategy can also be applied in other MMDCs.

Appendix

By substituting (6) and (7) into (8), the resonant current i_{r1} and the resonant capacitor voltage v_{Cr1} can be expressed as (A1) and (A2), shown at the top of next page.

According to (A1), (A2), and (12), the transmission power of MMRDC can be derived as (A3).

$$i_{r1}(t)=\begin{cases}\left(i_{r1}(t_0)+\frac{1}{\omega_r Z_r}\frac{(N-K)V_M}{2(N+K)d_{N1}T_s}\right)\cos(\omega_r(t-t_0))+\left(v_{Cr1}(t_0)+nV_L-\frac{V_M}{2}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_0))-\frac{1}{\omega_r Z_r}\frac{(N-K)V_M}{2(N+K)d_{N1}T_s}, & t_0\le t<t_1\\ i_{r1}(t_1)\cos(\omega_r(t-t_1))+\left(v_{Cr1}(t_1)+nV_L-\frac{NV_M}{N+K}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_1)), & t_1\le t<t_2\\ \left(i_{r1}(t_2)-\frac{1}{\omega_r Z_r}\frac{(N-K)V_M}{2(N+K)d_{N2}T_s}\right)\cos(\omega_r(t-t_2))+\left(v_{Cr1}(t_2)+nV_L-\frac{NV_M}{N+K}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_2))+\frac{1}{\omega_r Z_r}\frac{(N-K)V_M}{2(N+K)d_{N2}T_s}, & t_2\le t<t_3\\ i_{r1}(t_3), & t_3\le t<t_4\end{cases} \tag{A1}$$

$$v_{Cr1}(t)=\begin{cases}-\left(i_{r1}(t_0)+\frac{1}{\omega_r Z_r}\frac{(N-K)V_M}{2(N+K)d_{N1}T_s}\right)Z_r\sin(\omega_r(t-t_0))+\left(v_{Cr1}(t_0)+nV_L-\frac{V_M}{2}\right)\cos(\omega_r(t-t_0))+\frac{(N-K)V_M}{2(N+K)d_{N1}T_s}(t-t_0) & \\ -nV_L+\frac{V_M}{2}, & t_0\le t<t_1\\ -i_{r1}(t_1)Z_r\sin(\omega_r(t-t_1))+\left(v_{Cr1}(t_1)+nV_L-\frac{NV_M}{N+K}\right)\cos(\omega_r(t-t_1))-nV_L+\frac{NV_M}{N+K}, & t_1\le t<t_2\\ -\left(i_{r1}(t_2)-\frac{1}{\omega_r Z_r}\frac{(N-K)V_M}{2(N+K)d_{N2}T_s}\right)Z_r\sin(\omega_r(t-t_2))+\left(v_{Cr1}(t_2)+nV_L-\frac{NV_M}{N+K}\right)\cos(\omega_r(t-t_2)) & \\ -\frac{(N-K)V_M}{2(N+K)d_{N2}T_s}(t-t_2)-nV_L+\frac{NV_M}{N+K}, & t_2\le t<t_3\\ v_{Cr1}(t_3), & t_3\le t<t_4\end{cases} \tag{A2}$$

$$P_t=\frac{2(N-K)nV_LV_Mf_s}{(N+K)Z_r\omega_r}\left(\frac{f_s\left(\sin\left(\frac{\omega_r}{2f_s}D\right)-\sin\left(\frac{\omega_r}{2f_s}(D-2d_{N1})\right)\right)}{\omega_r d_{N1}\cos\left(\frac{\omega_r}{2f_s}D\right)}-\frac{f_s\left(\sin\left(\frac{\omega_r}{2f_s}D\right)+\sin\left(\frac{\omega_r}{2f_s}(D+2d_{N2}-1)\right)\right)}{\omega_r d_{N2}\cos\left(\frac{\omega_r}{2f_s}D\right)}-\frac{1-2D}{2d_{N2}}\right). \tag{A3}$$

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Haozhe Jin was born in Zhejiang, China, in 1997. He received the B.S. degree in electrical engineering from the Southwest Jiaotong University, Chengdu, China, in 2019. He is currently working toward the Ph.D. degree in electrical engineering from the Southeast University (SEU), Nanjing, China.

His research interests include the dc transformer and soft switching dc/dc converter.

Wu Chen (Senior Member, IEEE) was born in Jiangsu, China, in 1981. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2003, 2006, and 2009, respectively.

From 2009 to 2010, he was a Senior Research Assistant with the Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong. In 2010–2011, he was a Postdoctoral Researcher with Future Electric Energy Delivery and Management Systems Center, North Carolina State University, Raleigh, NC, USA. Since September 2011, he has been an Associate Research Fellow with the School of Electrical Engineering, Southeast University, Nanjing, China, where he has been a Professor since 2016. His main research interests include soft-switching converters, power delivery, and power electronic system integration.

Dr. Chen serves as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, *Journal of Power Electronics*, and *CPSS Transactions on Power Electronics and Applications*.

Yeyuan Xie was born in April 1978. He received the B.S. degree in power systems and automation and the M.S. degree in power electronics and power transmission from Zhejiang University, Hangzhou, China, in 1998 and 2006, respectively. He is a professor-level Senior Engineer, works for NR Electric Company, Ltd., and has been engaged in flexible dc/ac transmission technology for a long time. Since 2020, he has been as a member of Cigre DC transmission B4 China region and is a member of the expert group in the field of electric equipment of the National Industrial Foundation Expert Committee.

Liangcai Shu was born in Jiangsu, China, in 1994. He received the B.S. degree in electrical engineering from the Nanjing University of Science and Technology (NJUST), Nanjing, China, in 2016, the Ph.D. degree in electrical engineering from the Southeast University (SEU), Nanjing, China, in 2022.

Since 2022, he has been a Post-Doctoral Researcher with the Department of Electrical Engineering, Eindhoven University of Technology, Eindhoven, Netherlands. His research interests include the high-power converters and control methods for medium-voltage dc/ac grids with renewable energy resources.

Yutao Xu received the B.S. degree in information engineering from the Northwestern Polytechnical University, Xi'an, China, in 2006, the M.S. degree in electrical engineering from Chongqing University, Chongqing, China, in 2012.

He is a Senior Engineer with Electric Power Research Institute of Guizhou Power Grid Company, Ltd, Guiyang, China. His current research interests include the areas of flexible dc distribution network control and energy internet.