Analysis and Design of a Partial Power Processing Architecture for High Step-Up Applications

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***Abstract*—Combining the advantageous features of the traditional two-stage and input-parallel-output-series structure, this article proposes a partial power connection method for step-up applications with the advantages of wide input voltage range, galvanic isolation and partial power voltage regulation. In the proposed structure, the nonisolated dc–dc converter handles a small portion of the total power to regulate the system output voltage by simple pulsewidth modulation control. The latter stage should be a full bridge structure and the partial power processing is realized with different input voltages of the two bridge arms, which is beneficial to reduce the total number and cost of components, and two connection architectures are achieved in this way. The operation characteristics of the two architectures are analyzed in detail in this article, and an optimal structure is obtained from the perspective of fewer components and better partial power processing capacity. Furthermore, an isolated full bridge dc–dc converter with secondary resonance is selected to operate at the unregulated state as an application case to verify the feasibility and advantages of the proposed structure. An experimental prototype with 32–40 V input voltage range and 400 V/ 0.5 A output is built with 1 MHz switching frequency. The peak measured efficiency at 40 V full load is 95.3%.**

***Index Terms*—High efficiency, high step-up, input-parallel-output-series (IPOS), partial power processing architecture.**

I. Introduction

THE high step-up dc–dc converter has obtained widespread attention in renewable energy systems, such as photovoltaic module-integrated converters, fuel cells, hybrid electric vehicles, and uninterruptible power supplies [1], [2], [3], [4]. A high-efficiency dc–dc converter with low input voltage in a wide range and high conversion ratio is usually required in these systems to achieve the high voltage level required by the dc link terminal. Generally, the high step-up dc–dc converters can be divided into isolated and nonisolated types. The nonisolated converters usually adopt coupled inductors, voltage multiplier cells, switched-inductor and switched-capacitor to realize the boost capability [5], [6], [7], [8]. The isolated structures realize the expected voltage gain by adjusting the turns ratio of transformer, which is also conducive to reducing the voltage stress of power switches. Besides, the transformer in the isolated converters provides galvanic isolation between the system input and output, possessing higher safety, and reliability performance than the nonisolated converters, which is preferable for those applications with high safety requirements [9], [10], [11], [12], [13].

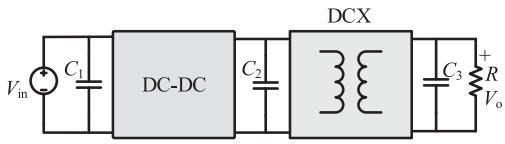

Fig. 1. Conventional two-stage scheme.

The resonant converters have excellent soft switching performance and wide applications, and high efficiency can be achieved with the optimal design at the resonant point. However, the system voltage regulation ability is limited by pulse frequency modulation. The change of switching frequency will make the resonant point deviate from the ideal state, resulting in additional reactive power and complicating the design of magnetic components, so it is challenging to obtain high efficiency in a wide input range [14], [15], [16], [17]. In order to extend the input voltage range, the converter can operate in different working modes by controlling the ON/OFF timing sequence of switches [18], [19], [20], [21], [22]. However, it will increase the complexity of switches control and may introduce mode transition issues additionally. The two-stage architecture is a popular solution for the wide input range application, as shown in Fig. 1, where the system dynamic regulation is achieved by the simple control strategy of the front dc–dc stage and the latter stage can perform as a dc transformer (DCX) at the unregulated state [23], [24], [25], [26], [27], [28]. Nevertheless, a potential disadvantage is that both stages need to transmit the full load power, which is not conducive to efficiency improvement.

To improve the system efficiency in a wide input range furtherly, the concept of partial power processing has gained more attention. Compared with the conventional converters transmitting full power, an amount of the system power can realize direct transmission from the source to the load side with approximately no power loss in partial power converters, resulting in efficiency

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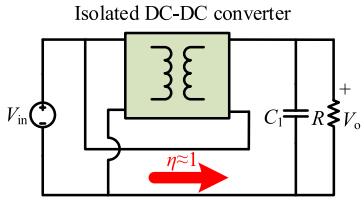

Fig. 2. Concept of the partial power converter.

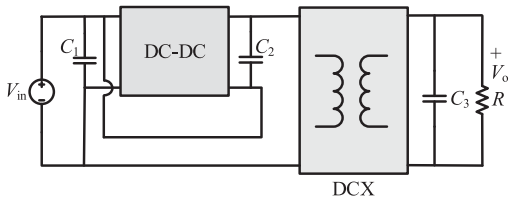

Fig. 3. Two-stage partial power structure in [32].

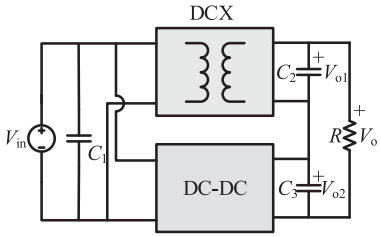

Fig. 4. IPOS structure [35], [36], [37].

improvement [29], [30], [31]. The concept of the partial power converter is shown in Fig. 2, and the converter should be isolated to achieve this connection. Furthermore, it is pointed out in [30] that the direct power transmission path can be alternated by a high-efficiency resonant converter operating at the optimal open-loop state, while the other dc–dc converter performs as a system dynamic voltage regulator, which transmits a small portion of the total power. Thus, the devices stress of the dc–dc voltage regulator is reduced and the power loss still has little impact on the total efficiency, which is more conducive to improving efficiency.

On this basis, a variety of partial power voltage regulation methods have been proposed successively [32], [33], [34], [35], [36], [37], [38], [39]. Among them, Li et al. [32], Xu et al. [33], and Wilson et al. [34] are the two-stage solutions, as shown in Fig. 3, where the front-stage dc–dc voltage regulator is required to be isolated and only processes a fraction part of the power. The galvanic isolation of the system is realized by the latter stage, which still needs to transmit all the power. The converters in [35], [36], and [37] realize input-parallel-output-series (IPOS) connections, as shown in Fig. 4, both the upper and lower parts transmit a portion of the total power, which helps to improve the system efficiency. Similarly, in order to realize the galvanic isolation of the system, the dc–dc voltage regulator in the lower part needs to be isolated, two transformers increase the complexity of the system design.

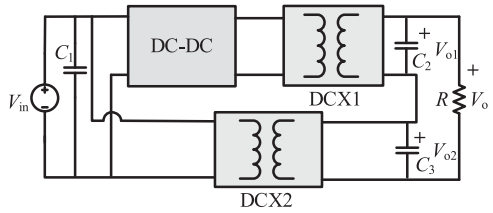

Fig. 5. Partial power structure for high step-up applications [38].

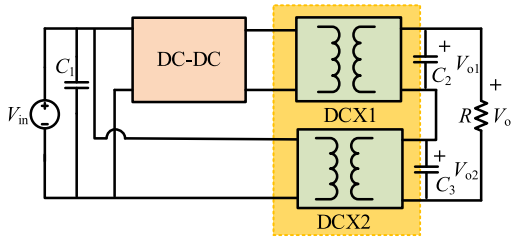

Fig. 6. Proposed partial power processing architecture.

Combining the advantages of the traditional two-stage and the IPOS architecture, Fig. 5 shows a partial power structure suitable for high step-up applications, which can achieve both galvanic isolation and wide input range. In Fig. 5, the dc–dc converter, which handles a small portion of the total power, can be nonisolated and regulates the system output voltage by simple pulsewidth modulation (PWM) control. Compared to the conventional two-stage scheme, the device stresses of the nonisolated dc–dc voltage regulator are lower, which is conducive to reducing power losses and improving efficiency under a wide input range. However, two isolated dc–dc converters are needed to achieve a constant conversion ratio in Fig. 5, which increases the number of system components and design complexity.

In this article, a partial power processing architecture is proposed, as shown in Fig. 6, which integrates the two DCXs in Fig. 5 as one. In order to achieve this connection, the primary side of the DCXs should be a full bridge structure. Two partial power connection structures are achieved with different input voltages of the two bridge arms and an optimal structure is obtained aiming at fewer components and less power handled by the dc–dc voltage regulator. Besides, secondary resonance is adopted for the step-up application to reduce current stress.

The rest of this article is organized as follows. The proposed partial power processing architectures are introduced and analyzed in detail in Section II. In Section III, the working principle of the proposed converter based on the optimal structure is described. The parameter design of the main components, the partial power voltage regulation scheme and the performance comparison of the proposed converter are presented in Section IV, while Sections V and VI give the analysis of the experiment results and conclusion, respectively.

II. Proposed Partial Power Processing Architecture

With different input voltages of the two bridge arms of the full bridge structure, two partial power connection structures

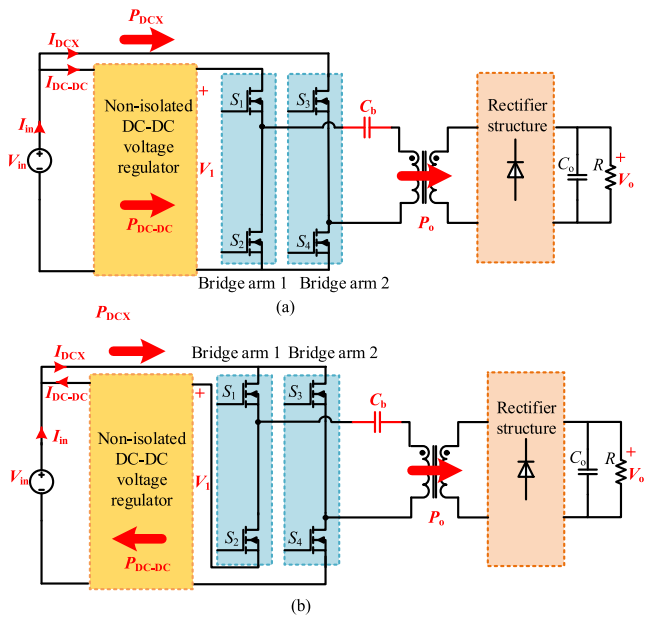

Fig. 7. Proposed two partial power connection structures. (a) Structure I. (b) Structure II.

are obtained, as shown in Fig. 7. The dc blocking capacitor C_b plays the role of balancing the bridge voltage. The capacitance of C_b is large enough, so the voltage can be regarded as constant. As shown in Fig. 7, different connection methods will generate different power flow modes. In order to compare the power processed by the nonisolated dc–dc voltage regulator in different structures, k is defined as the ratio of the power dealt by the nonisolated dc–dc voltage regulator to the system total power. Taking the structure I in Fig. 7(a) as an example, since the nonisolated dc–dc voltage regulator is connected in parallel with the system at the input side, k can be expressed as

$$k = \frac{I_{\mathrm{dc-dc}}}{I_{\mathrm{in}}} = \frac{I_{\mathrm{dc-dc}}}{I_{\mathrm{dc-dc}} + I_{\mathrm{DCX}}}. \tag{1}$$

Besides, the efficiency of the nonisolated dc–dc voltage regulator can be defined as

$$\eta_{\mathrm{dc-dc}} = \frac{V_1 I_{\mathrm{DCX}}}{V_{\mathrm{in}} I_{\mathrm{dc-dc}}}. \tag{2}$$

Based on (2), k can be derived as

$$k = \frac{1}{\eta_{\mathrm{dc-dc}}/G + 1} \tag{3}$$

where $G = V_1/V_{\mathrm{in}}$ represents the voltage gain of the nonisolated dc–dc voltage regulator.

Similarly, the expressions of the power ratio k for the IPOS structure in Fig. 4 and the structure II in Fig. 7(b) can be obtained shown in Table I, where M_{DCX} and η_{DCX} represent the voltage gain and efficiency of DCX in Fig. 4, respectively.

According to Table I, Fig. 8 shows the curves of k for different architectures, where η is considered ideal. It can be seen that the power handled by the voltage regulator in structure I is always smaller than that of structure II under the same voltage gain

TABLE I
POWER RATIO K FOR DIFFERENT ARCHITECTURES

Architecture type	Power ratio k
Structure I [see Fig. 7(a)]	$\frac{1}{\eta_{\mathrm{DC\text{-}DC}}/G+1}$
Structure II [see Fig. 7(b)]	$\frac{1}{2/G-\eta_{\mathrm{DC\text{-}DC}}}$
IPOS (see Fig. 4)	$\frac{1}{M_{DCX}\eta_{\mathrm{DC\text{-}DC}}/G\eta_{\mathrm{DCX}}+1}$

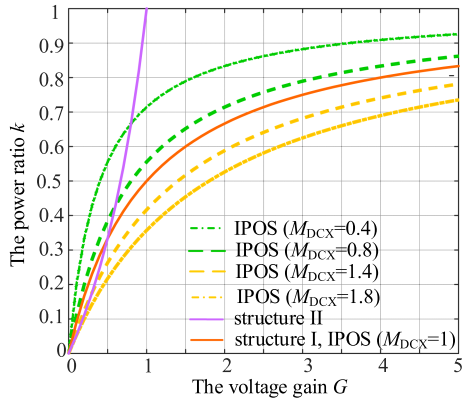

Fig. 8. Curves of the power ratio k for the architectures in Table I.

TABLE II
QUALITATIVE PERFORMANCE COMPARISON OF DIFFERENT STRUCTURES

Architecture type	Number of transformers	Galvanic isolation	Partial power
Structure I [see Fig. 7(a)]	1	Yes	Yes
Structure II [see Fig. 7(b)]	1	Yes	Yes
IPOS (see Fig. 4)	1	No	Yes
Conventional two-stage (see Fig. 1)	1	Yes	No
Partial power two-stage (see Fig. 3)	2	Yes	Yes

approximately. For the IPOS structure, when $M_{\mathrm{DCX}} > 1$, as shown by the curve below the red one referring to $M_{\mathrm{DCX}} = 1$, the power handled by the voltage regulator is smaller than that of the structure I. When $M_{\mathrm{DCX}} < 1$, the conclusion is opposite. Moreover, the lower the voltage gain G is, the smaller the power ratio k is, which is beneficial for partial power voltage regulation. However, taking into account the number and cost of system components as well as the power ratio k of the voltage regulator, the structure I is more advantageous.

Table II summarizes and compares the characteristics of different structures in Figs. 1, 3, 4, and 7 qualitatively, including galvanic isolation, number of transformers and partial power processing capacity. It can be seen from Table II that the structures proposed in Fig. 7 can realize both isolation and partial power processing with fewer transformers, which is conducive to improving the power density and working efficiency.

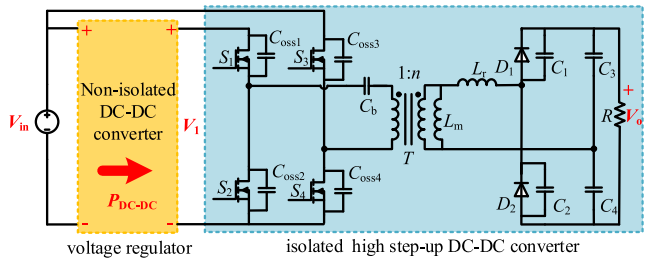

Fig. 9. Proposed isolated high step-up DC–DC converter based on structure I.

III. Operational Principle of the Proposed Converter

In this section, an isolated high step-up dc–dc converter with partial power voltage regulator based on structure I is designed to verify the application feasibility and advantages of the proposed structure, as shown in Fig. 9. It should be pointed out that the latter stage here is not a DCX, but only an isolated dc–dc converter operating at the open-loop state.

The proposed converter is composed of two parts. The primary side of the main isolated dc–dc converter consists of switches S_1–S_4 and capacitor C_b. C_{oss1}–C_{oss4} are the internal parasitic drain-source capacitors of the four switches. The secondary side includes diodes D_1, D_2, resonant inductor L_r, magnetic inductor L_m, and capacitors C_1 and C_2, which are adopted as split resonant capacitors with the same values, forming a resonant circuit loop with L_r. Diodes D_1 and D_2 are connected in parallel with C_1 and C_2 as clamping diodes, which also constitute a voltage-doubling rectification structure with C_3 and C_4. n is the turn ratio between the primary and secondary windings of transformer T. In the main isolated dc–dc converter, the soft-switching properties can be naturally realized by the power devices in the entire working range and the current stress of the resonant components on the secondary side decrease, which is seven times less than that on the primary side. Hence, the power loss caused by capacitor ESR is reduced significantly.

There are six working modes in one switching period of the main converter. For ease of description, modes 1–3 are defined as the positive half-period mode while modes 4–6 are the negative half-period mode. Since modes 4–6 and modes 1–3 are symmetrical, only the positive half-period operation principle is described here, as shown in Fig. 10. The duty cycles for switches S_1–S_4 are all 0.5 theoretically and the drive signals for the switches of the same bridge are complementary, so it is necessary to add a dead zone between the two driving signals of the same bridge to prevent the primary windings of the transformer from short-circuiting. Assuming that the resonant capacitors $C_1 = C_2 = C_r$ and the output filter capacitors $C_3 = C_4$. The current directions in each mode are shown as the red arrows and the reference positive directions are defined in Fig. 10. The key waveforms are illustrated in Fig. 11.

Mode 1(t_0-t_1): During the dead zone of S_1 and S_2, the secondary currents of L_m and L_r provide the charging and discharging currents for the drain-source capacitors of S_1–S_4 jointly, which provide sufficient conditions for the ZVS turn-ON of S_1 and S_4. On the secondary side of the transformer, capacitors C_1 and C_2 resonate with L_r through two current paths, which

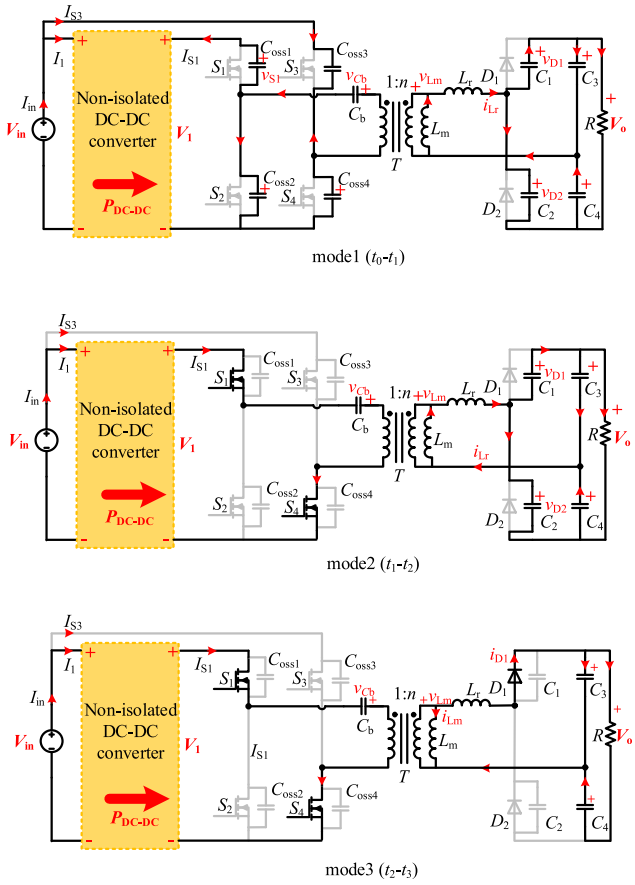

Fig. 10. Equivalent circuits of the proposed converter for the positive-half period.

consist of L_r, C_1, C_3 and L_r, C_2, C_4. Since the capacitance of C_3 and C_4 is large to filter the output voltage, it can be considered that the voltage of both is constant and equal to $V_o/2$. Therefore, only C_1 and C_2 are involved in the resonance.

Mode 2(t_1-t_2): At t_1, the drive signal of S_1 and S_4 arrives, and switches S_1 and S_4 realize ZVS turn-ON. Capacitors C_1, C_2 and inductor L_r continue to resonate in the two loops shown in Fig. 10, which are the same as mode 1. During this stage, C_2 charges and C_1 discharges, and the voltage of both varies between 0 and V_o nonlinearly as Fig. 11.

Mode 3(t_2-t_3): At t_2, the voltage of C_1 resonates to 0, which provides conduction conditions for D_1, while D_2 is still OFF and the resonant process ends. The current of L_r freewheels linearly through D_1 due to the voltage across C_3 and L_m. When the current of D_1 decreases to 0, mode 3 ends. At t_3, S_1 and S_4 turn OFF, and the driving signals of S_2 and S_3 have not yet arrived, so the system enters the dead zone of the negative half-period.

Since the positive and negative half period of the main converter is symmetrical, based on the volt-second balance of the magnetic inductor L_m, the following relationship can be obtained:

$$(V_{in}G + V_{Cb})\,n + (V_{Cb} - V_{in})\,n = 0. \tag{4}$$

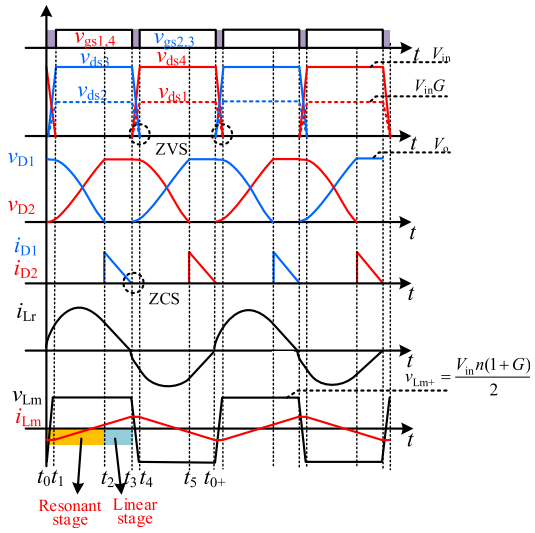

Fig. 11. Waveforms of the main parameters.

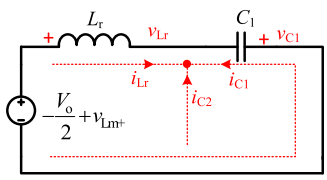

Fig. 12. Equivalent resonant circuit in the positive half-period.

Thus, the voltage of V_{Cb} and $v_{\mathrm{Lm+}}$ can be expressed as (5) and (6), respectively, where the definition of $v_{\mathrm{Lm+}}$ is shown in Fig. 11

$$V_{\mathrm{Cb}} = \frac{V_{\mathrm{in}}\left(1-G\right)}{2} \tag{5}$$

$$v_{\mathrm{Lm+}} = \frac{V_{\mathrm{in}} n\left(1+G\right)}{2}. \tag{6}$$

Besides, the equivalent resonant circuit of the secondary side of the transformer in the positive half-period is shown in Fig. 12, from which the following equations can be obtained:

$$i_{\mathrm{Lr}} = -2i_{\mathrm{C1}} \tag{7}$$

$$v_{\mathrm{Lr}} - v_{\mathrm{C1}} = -\frac{V_{\mathrm{o}}}{2} + v_{\mathrm{Lm+}}. \tag{8}$$

Furthermore, the second-order nonhomogeneous differential equation about v_{C1} is obtained, substituting the initial value $v_{\mathrm{C1}}(t_0) = V_{\mathrm{o}}$ and final value $v_{\mathrm{C1}}(t_2) = 0$, the expression of $v_{\mathrm{C1}}(t)$ and $i_{\mathrm{Lr}}(t)$ in modes 1 and 2 is got as

$$v_{\mathrm{C1}}(t) = \left(\frac{V_{\mathrm{o}}}{2} + v_{\mathrm{Lm+}}\right)\cos\omega t + \frac{V_{\mathrm{o}}}{2} - v_{\mathrm{Lm+}},\ t \in [t_0, t_2] \tag{9}$$

$$i_{\mathrm{Lr}}(t) = \frac{\frac{V_{\mathrm{o}}}{2} + v_{\mathrm{Lm+}}}{Z_{\mathrm{r}}}\sin\omega t, t \in [t_0, t_2] \tag{10}$$

where the resonant angular frequency $\omega = 2\pi f_{\mathrm{r}} = 1/\sqrt{2L_{\mathrm{r}}C_{\mathrm{r}}}$, and the resonant characteristic impedance $Z_{\mathrm{r}} = \sqrt{L_{\mathrm{r}}/2C_{\mathrm{r}}}$.

According to (9), the resonant time t_{r}, i.e., the duration time of modes 1 and 2 can be expressed as

$$t_{\mathrm{r}} = t_2 - t_0 = \frac{\alpha}{\omega} \tag{11}$$

where α is defined as the resonant angle, which is given by

$$\alpha = \arccos\left(\frac{v_{\mathrm{Lm+}} - \frac{V_{\mathrm{o}}}{2}}{v_{\mathrm{Lm+}} + \frac{V_{\mathrm{o}}}{2}}\right). \tag{12}$$

According to the ampere-second balance principle of capacitors, the average current of D_1 is equal to the output current, so (13) is derived

$$\frac{1}{2T_{\mathrm{s}}}\frac{V_{\mathrm{o}}/2 - v_{\mathrm{Lm+}}}{L_{\mathrm{r}}}(t_3 - t_2)^2 = I_{\mathrm{o}}. \tag{13}$$

Then, the diode freewheeling time t_{d} of mode 3 is obtained

$$t_{\mathrm{d}} = t_3 - t_2 = \sqrt{\frac{2L_{\mathrm{r}}I_{\mathrm{o}}}{f_{\mathrm{s}}\left(\frac{V_{\mathrm{o}}}{2} - v_{\mathrm{Lm+}}\right)}}. \tag{14}$$

IV. Parameter Design and Output Regulation Mechanism

A. Parameter Design of C_r and L_r

From the abovementioned analysis, no matter in the positive or negative half period, the working modes of the main converter can be divided into two parts: the resonant stage of inductor L_{r} and capacitors C_1, C_2 and the linear stage of secondary diodes freewheeling, as shown in Fig. 11, so the time relationship of the half switching period is expressed as

$$t_{\mathrm{d}} + t_{\mathrm{r}} = \frac{1}{2}T_{\mathrm{s}}. \tag{15}$$

According to the active power conservation law of the main converter, the following relationship can be obtained:

$$v_{\mathrm{Lm+}}I_{\mathrm{Lr\_avg}} = \frac{V_{\mathrm{o}}^2}{R} \tag{16}$$

where $I_{\mathrm{Lr\_avg}}$ is the average of the absolute value of i_{Lr} over one switching period.

Furthermore, the available C_{r} is required to satisfy

$$C_{\mathrm{r}} = \frac{T_{\mathrm{s}}\left(M-2n\right)M}{2Rn\left(M+2n\right)\left(1-\cos\alpha\right)} \tag{17}$$

where $M = nV_{\mathrm{o}}/v_{\mathrm{Lm+}}$ is the voltage gain of the main converter.

When the main converter voltage gain M, transformer turn ratio n, operating frequency f_{s}, and the system power are determined, the value of the resonant capacitor C_{r} can be obtained. According to (11), (14), and (15), inductor L_{r} can be selected as (18). The relationship between L_{r}, C_{r}, and turn ratio n is shown in Fig. 13

$$L_{\mathrm{r}} = \left[\frac{T_{\mathrm{s}}}{2}\Big/\left(\sqrt{\frac{2T_{\mathrm{s}}M}{R\left(\frac{M}{2}-n\right)}} + \sqrt{2C_{\mathrm{r}}}\arccos\left(\frac{n-\frac{M}{2}}{n+\frac{M}{2}}\right)\right)\right]^2. \tag{18}$$

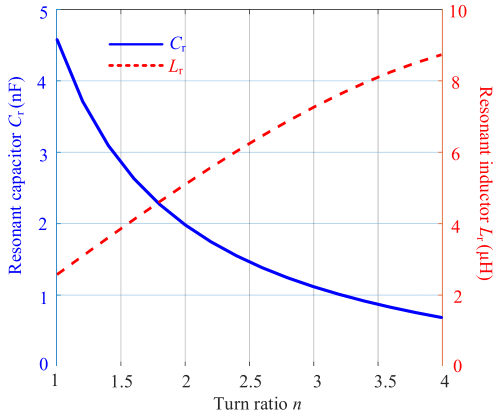

Fig. 13. Relationship between L_r and C_r under different turns ratio n.

Once the transformer design is completed, the turn ratio n is determined, and the appropriate parameter values of L_r and C_r can be obtained according to Fig. 13.

B. Parameter Design of Magnetic Inductor L_m

The magnetic inductor L_m affects the realization of the soft switching as well as the rms current of switches S_1–S_4. During the dead time t_{dead}, i_{Lm} can be regarded as a constant current source i_{Lmmax}, which is given by

$$i_{Lmmax} = \frac{v_{Lm+}}{L_m}\frac{T_s}{4}. \tag{19}$$

Besides, in t_{dead}, the average current of L_r is

$$i_{Lr\_tdead} = \frac{-2C_r\left(\frac{V_o}{2}+v_{Lm+}\right)(\cos\omega t_{dead}-1)}{t_{dead}}. \tag{20}$$

During the dead time, the currents i_{Lm} and i_{Lr} provide the charging and discharging currents for the drain-source capacitors of S_1–S_4 on the primary side. Therefore, in order to complete the charging and discharging processes within t_{dead} so that the drain-source voltages of switches can drop to zero before the next drive signal arrives, it is necessary to satisfy the following requirements:

$$n\times(i_{Lm\,max}-i_{Lr\_tdead}) \geq \frac{4v_{Lm+}C_{oss}}{nt_{dead}}. \tag{21}$$

Furthermore, the available range of magnetic inductor L_m is

$$L_m \leq \frac{nv_{Lm+}T_st_{dead}}{4H} \tag{22}$$

where $H = \frac{4v_{Lm+}C_{oss}}{n} - 4C_rn(\frac{V_o}{2}+v_{Lm+})(\cos\omega t_{dead}-1)$.

C. Voltage and Current Stresses Analysis

1) Voltage Stress Analysis: The voltage stress of S_1, S_2 is the output voltage V_1 of the nonisolated dc–dc voltage regulator as (23) and the voltage stress of S_3, S_4 is the input voltage V_{in}. The voltages of C_1 and C_2 reach the maximum at the end of the resonant stage, respectively, during the positive and negative half period

$$V_{S1,S2} = V_1 \tag{23}$$

$$V_{S3,S4} = V_{in} \tag{24}$$

$$V_{C1max} = V_{C2max} = V_o. \tag{25}$$

2) Current Stress Analysis: ① Magnetic inductor L_m current

The rms value of the magnetic inductor current is

$$i_{Lmrms} = \frac{i_{Lmmax}}{\sqrt{3}} = \frac{v_{Lm+}T_s}{4\sqrt{3}L_m}. \tag{26}$$

② Diodes D_1, D_2 current

The currents of D_1 and D_2 are triangular waves, the average value is the output current I_o, and the peak current is

$$I_{D1pk} = I_{D2pk} = \frac{2I_oT_s}{t_d}. \tag{27}$$

③ Resonant inductor L_r current

During the positive half working period, the inductor L_r current consists of the currents of C_1 and D_1 two parts as

$$i_{Lr} = 2i_{C1} + i_{D1}. \tag{28}$$

The rms currents of D_1 and C_1 during the resonant stage are given by

$$i_{D1rms} = I_{D1pk}\sqrt{\frac{t_d}{3T_s}} \tag{29}$$

$$i_{C1rms} = \sqrt{\frac{1}{T_s}\int_0^{t_r} 4C_r^2\omega^2\left(\frac{V_o}{2}+v_{Lm+}\right)^2\sin^2\omega t dt}. \tag{30}$$

Then, the rms current of L_r is

$$i_{Lrrms} = \sqrt{\frac{2}{T_s}\left(\frac{B}{2}t_r - \frac{B}{4\omega}\sin 2\omega t_r\right) + \frac{2I_{D1pk}^2}{3}\frac{t_d}{T_s}} \tag{31}$$

where $B = 4C_r^2\omega^2(\frac{V_o}{2}+v_{Lm+})^2$.

④ Switches S_1–S_4 current

In the positive half working period, the current of S_1 composes of i_{Lr} and i_{Lm} two parts, and the rms current can be written as

$$i_{S1rms} = \sqrt{(ni_{Lrrms})^2 + (ni_{Lmrms})^2}\Big/\sqrt{2}. \tag{32}$$

According to (26) and (32), the relationship curve of the rms current of L_m and S_1 versus the magnetic inductor L_m is shown in Fig. 14. It reveals that as L_m increases, the rms currents decrease and tend to remain unchanged. Meanwhile, according to (22), an appropriate magnetic inductor can be selected considering the volume of the transformer.

D. Partial Power Voltage Regulation Scheme

According to (6) and (17), the voltage gain M_c of the system after adding the partial power voltage regulator can be obtained

$$M_c = \frac{V_o}{V_{in}} = n\left(1+\frac{f_nQ}{2\pi}\right)(1+G) \tag{33}$$

where the normalized frequency $f_n = f_s/f_r$, the quality factor $Q = R/Z_r$.

The nonisolated dc–dc converter plays the role of voltage regulation. Generally, converters with simple structure, nonisolated

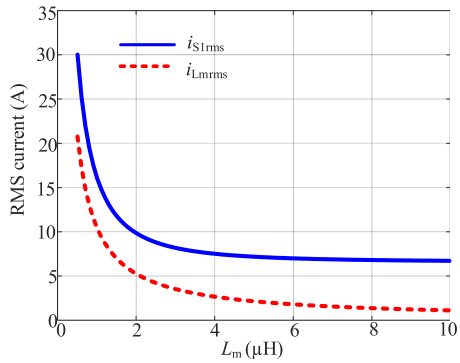

Fig. 14. Relationship curve between i_{S1rms}, i_{Lmrms}, and L_m.

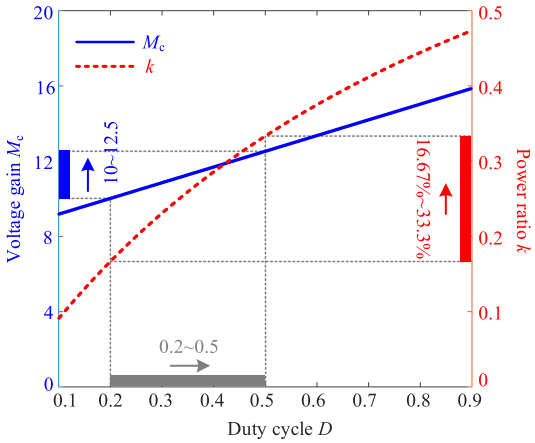

Fig. 15. Voltage gain M_c and the power ratio k versus D.

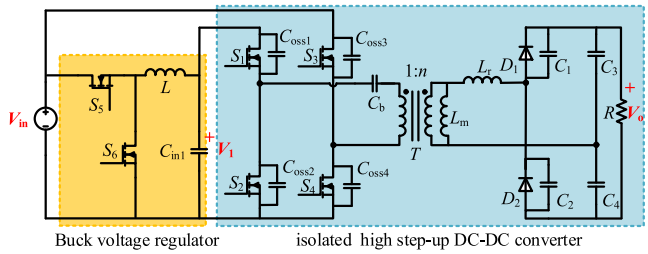

Fig. 16. Proposed isolated high step-up converter with buck voltage regulator.

and easy adjustment are selected, such as conventional buck, boost, and buck–boost converter. However, according to Fig. 8, when the voltage regulator is a step-down converter, the power ratio k is smaller, which is more conducive to improving the system efficiency. Therefore, the buck converter is selected as the voltage regulator here. According to (33), since the main converter operates at the constant frequency, once the component parameters are fixed, the system voltage gain M_c is only related to the voltage gain G of the nonisolated dc–dc converter, which is determined by the switches duty cycle D in this part. When the input voltage V_{in} has a sudden change, the nonisolated dc–dc stage will adjust D through closed-loop feedback control to regulate the output voltage V_o to the reference value. According to (5), the output voltage V_1 of the nonisolated dc–dc stage will be changed by the adjustment of D, and the input voltages of the two bridge arms will be balanced by the capacitor C_b, so the voltage distribution of C_b and V_1 is adjusted with the change of the input voltage V_{in}. The power ratio k is given by (34) when the dc–dc voltage regulator is buck. The relationship between the voltage gain M_c, k, and D is shown as Fig. 15

$$k_{\text{Buck}} = \frac{P_{\text{Buck}}}{P_{\text{total}}} = \frac{D}{1+D}. \tag{34}$$

It reveals from Fig. 15 that when the buck regulator is selected, the duty cycle adjustment range is 0.2–0.5 in order to obtain a voltage gain of 10–12.5, and the power distribution ratio of the Buck regulator is 16.7%–33.3%. The efficiency of the Buck voltage regulator and the main converter are defined as $\eta_{\text{Buck}} = V_1 I_{S1}/V_{in} I_1$ and $\eta_{\text{main}} = P_o/(V_{in} I_{S3} + V_1 I_{S1})$ respectively. Furthermore, the efficiency of the whole system can be estimated as

$$\eta_{\text{total}} = \frac{P_o}{V_{in} I_{in}} = k_{\text{Buck}} \eta_{\text{Buck}} \eta_{\text{main}} + (1 - k_{\text{Buck}})\, \eta_{\text{main}}. \tag{35}$$

When k_{Buck} tends to 1, which is the worst working condition and is not included in the converter design in this article, the system efficiency tends to be equal to the two-stage structure as (36) in this case. Thus, the working efficiency of the proposed converter will be higher than that of the two-stage in the whole working process theoretically. The overall structure of the proposed converter is shown as Fig. 16

$$\eta_{\substack{\text{total} \\ k_{\text{Buck}} \to 1}} = \eta_{\text{Buck}} \eta_{\text{main}}. \tag{36}$$

E. Characteristic Comparison

In this section, some characteristics of the proposed structure are compared with IPOS and the two-stage partial power structure shown in Fig. 3 to further compare the advantages and disadvantages of the three structures. The common feature of the three topologies is that the isolated high step-up dc–dc converter described in Section III is adopted to operate at the unregulated state with the same working frequency. Besides, it is considered that galvanic isolation can be achieved by the three structures, so the isolated voltage regulator is needed for IPOS and the two-stage partial power structure. The conventional flyback converter in [30] is adopted here for the simplicity of topology structure and design. The dynamic voltage regulation of the system can be achieved by PWM of the flyback converter when the input voltage or the load current changes. Based on the above, the voltage and current stress of the switches and magnetic components, and the system voltage gain of the three structures are summarized in Table III.

In Table III, n_1 is the turn ratio between the primary and secondary windings of the flyback voltage regulator, and M is the voltage gain of the isolated high step-up dc–dc converter. D and f_{s1} represent the duty cycle and switching frequency of the

TABLE III
QUALITATIVE COMPARISON OF THREE DIFFERENT PARTIAL POWER STRUCTURES

Properties \ Converter	Proposed	IPOS	Two-stage in Fig. 3
Voltage gain	$\frac{(1+D)M}{2}$	$M+\frac{D}{n_1(1-D)}$	$M+\frac{MD}{n_1(1-D)}$
Voltage stress of S_1 and S_2	$V_{in}D$	V_{in}	$V_{in}\left(1+\frac{D}{n_1(1-D)}\right)$
Voltage stress of S_5 and S_6	V_{in}	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$
Peak current of L_m	$\frac{V_{in}n(1+D)}{8f_sL_m}$	$\frac{V_{in}n}{4f_sL_m}$	$\frac{(1+D/n_1(1-D))V_{in}n}{4f_sL_m}$
Peak current of L	$\frac{I_{in}}{1+D}+\frac{V_{in}(1-D)D}{2Lf_{s1}}$	$\frac{I_{in}}{n_1(1-D)M+D}+\frac{V_{in}D}{2Lf_{s1}}$	$\frac{I_{in}}{n_1(1-D)+D}+\frac{V_{in}D}{2Lf_{s1}}$

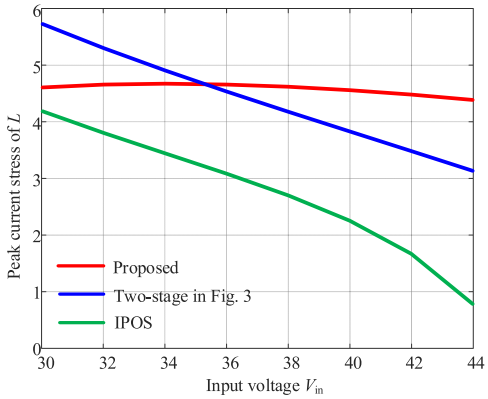

Fig. 17. Relationship between the peak current stress of L and the input voltage V_{in} for the three structures.

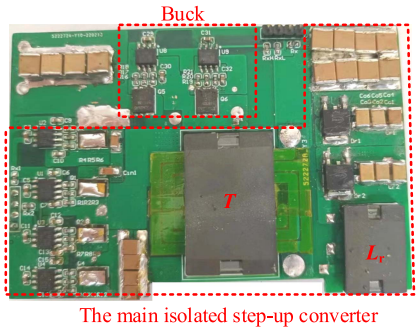

Fig. 18. Picture of the prototype.

voltage regulator. I_{in} refers to the average input current of the system, and L represents the inductor in buck or the magnetic inductor of the flyback converter. It can be seen from Table III that although the proposed structure has the lowest voltage step-up capacity compared with the two others, the voltage stress of switches is the lowest under the same operating voltage, which represents a favorable selection of power switches with smaller on-state resistance and is beneficial to reduce the conduction loss of switches. In addition, it is obvious that according to Table III, the peak current of L_m in the proposed structure is smaller than IPOS and the structure in Fig. 3, which means lower peak current stress and lower switching loss. The relationship between the peak current stress of L and the input voltage V_{in} for the three structures is shown in Fig. 17. It can be seen that the peak current stress of L in IPOS is the smallest. With the decrease of the input voltage, the peak current of L in the proposed structure will be lower than the two-stage partial power structure in Fig. 3.

In addition, since the size of magnetic components accounts for a large proportion of the total volume, a rough qualitative comparison of the power density can be made by the size evaluation of the magnetic components used for the three structures. Compared with the proposed structure, an isolated voltage regulator is needed for the other two structures and an additional transformer is included, resulting in power density sacrifice. Moreover, according to Table III, since the peak current of the magnetic inductor L_m in the proposed structure is smaller than the two others, the effective cross-sectional area of the magnetic core required for the proposed structure is the smallest under the same inductance and peak flux density B_m, which is a benefit to the improvement of the system power density.

V. EXPERIMENTAL RESULTS

In order to verify the abovementioned theoretical analysis, a 1-MHz 32 V–40 V/400 V 0.5 A laboratory prototype with the dimensions of 94.2 mm (length) × 63.2 mm (width) × 1 mm (height) is built, which is shown in Fig. 18. The working state of the buck regulator is independent of the main converter, so the working frequency is set as 100 kHz to reduce the switching losses. The power distribution pie chart of the main converter and the buck voltage regulator under different input voltages are shown as Fig. 19 according to (34). It can be seen that with the increase of V_{in}, D becomes smaller and the power processed by buck is lower, which is conductive to the system efficiency improvement. However, considering the actual circuit loss and the minimum limitation of duty cycle, the duty cycle range of 0.2–0.5 is designed for the system voltage regulation. The parameters and the selection of the main components in the prototype are listed in Table IV.

The test waveforms of the ZVS properties of the main power switches at full load are shown in Fig. 20, where v_{gs} and

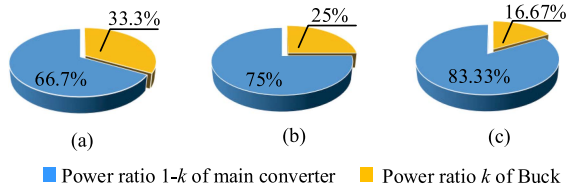

Fig. 19. System power distribution pie chart under different input voltages. (a) $V_{\rm in} = 32$ V. (b) $V_{\rm in} = 36$ V. (c) $V_{\rm in} = 40$ V.

TABLE IV
SPECIFICATIONS AND PARAMETERS OF THE PROPOSED CONVERTER

Electrical specifications	
Input Voltage	32–40 V
Output Voltage	400 V
Output Current	0.5 A
Switching Frequency (the main converter)	1 MHz
Switching Frequency (Buck)	100 kHz
Parameters of main components	
$L_{\rm r}$	7.26 μH
$L_{\rm m}$	10 μH
C_1、C_2	1.1 nF
$C_{\rm b}$、C_3、C_4	10 μF
D_1、D_2	CI08S65E3
S_1–S_4	GS61008T
n	3
Transformer/inductor $L_{\rm r}$ core (3F36)	EI32/EQ20
S_5、S_6	BSC030N08NS5
L (Buck)	20 μH
Dead time $t_{\rm dead}$	40 ns

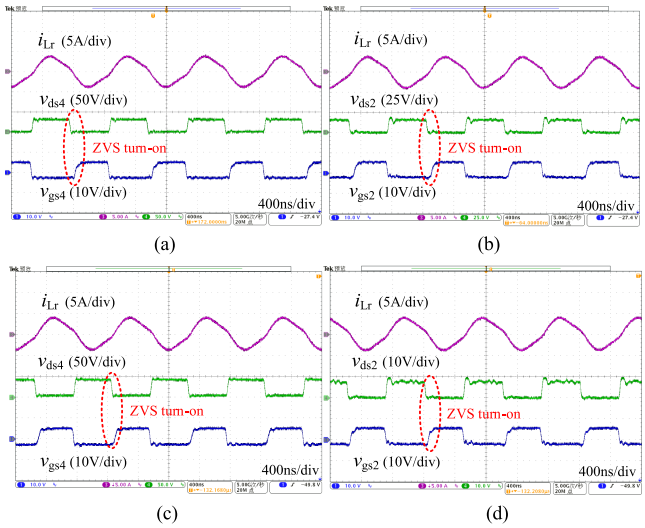

Fig. 20. Soft switching properties test waveforms at full load. (a) $v_{\rm gs4}$, $v_{\rm ds4}$, and $i_{\rm Lr}$ for $V_{\rm in} = 32$ V. (b) $v_{\rm gs2}$, $v_{\rm ds2}$, and $i_{\rm Lr}$ for $V_{\rm in} = 32$ V. (c) $v_{\rm gs4}$, $v_{\rm ds4}$ and $i_{\rm Lr}$ for $V_{\rm in} = 40$ V. (d) $v_{\rm gs2}$, $v_{\rm ds2}$, and $i_{\rm Lr}$ for $V_{\rm in} = 40$ V.

$v_{\rm ds}$ represent the driving voltage and the drain-source voltage of switches, respectively, $i_{\rm Lr}$ refers to the secondary resonant current. As can be observed, the drain-source voltage drops to zero before the arrival of the next driving signal, so the ZVS of the main switches can be realized under the entire working range. Besides, the test waveforms of diodes D_1 and D_2 are shown in Fig. 21, where $i_{\rm D}$ and $v_{\rm D}$ represent the current and voltage of

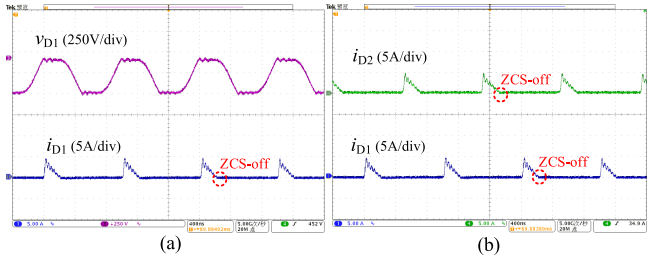

Fig. 21. (a) $v_{\rm D1}$ and $i_{\rm D1}$ for $V_{\rm in} = 32$ V. (b) $i_{\rm D1}$ and $i_{\rm D2}$ for $V_{\rm in} = 32$ V.

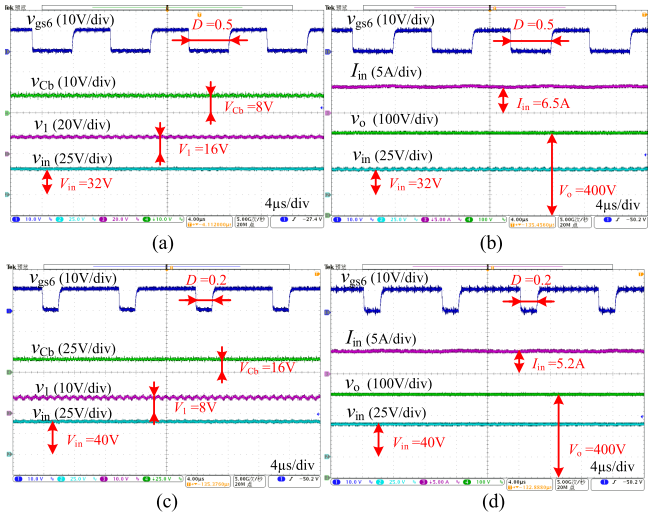

Fig. 22. Steady-state and voltage distribution waveforms. (a), (b) $V_{\rm in} = 32$ V, $I_{\rm o} = 0.5$ A. (c), (d) $V_{\rm in} = 40$ V, $I_{\rm o} = 0.5$ A.

diodes. According to Fig. 21, the ZCS characteristics of D_1 and D_2 are also achieved.

Fig. 22 shows the steady-state test waveforms of the voltage distribution and the driving signal of S_6 when $V_{\rm in} = 32$ V and 40 V at full load. In these waveforms, $v_{\rm gs6}$ is the driving voltage of S_6, $v_{\rm in}$ is the input voltage, $I_{\rm in}$ is the average input current, $v_{\rm o}$ is the output voltage, v_1 refers to the output voltage of the buck converter, and $v_{\rm Cb}$ refers to the voltage of $C_{\rm b}$. The regulation scheme of the duty cycle D of S_5 is given by (33), so as to realize the expected constant dc output voltage. According to the test waveforms, the voltage distribution of v_1 and $v_{\rm Cb}$ changes by adjusting D according to (5) during this process.

Table V gives a comprehensive comparison of the circuit characteristics of the proposed converter and some other high step-up dc–dc converters proposed in recent years. As can be seen from Table V, there are fewer components in [7] and [8], but they all cannot achieve galvanic isolation. The converter proposed in [5] introduces more diodes than other listed converters, and the voltage regulation capability under the fluctuation of input voltage is not verified. The conventional two-stage scheme in [23] can accommodate a wide input voltage range, but the efficiency is sacrificed because both stages transmit all the power.

For a more intuitive comparison, the relationship curves of the normalized main switch voltage stress ($V_{\rm S}/V_{\rm in}$) and the voltage

TABLE V
PROPERTIES COMPARISON BETWEEN THE PROPOSED CONVERTER AND SOME OTHER CONVERTERS WITH HIGH VOLTAGE GAIN

Converter / Properties	proposed	[39]	[23]	[8]	[5]	[7]
Number of components S*/D*/C*/L* or T*	6/2/6/3	6/2/6/2	3/5/3/2	2/3/4/2	2/8/5/2	2/4/1/3
Galvanic isolation	yes	yes	yes	no	no	no
Input voltage	32–40 V	24–37 V	24–48 V	40–48 V	24 V	20–40 V
Output voltage/power	400 V/200 W	240 V/250 W	400 V/1k W	400 V/300 W	432 V/400 W	200 V/200 W
Nominal efficiency	95.3%@200 W	95%@250 W	90.2%@1 kW	~95.1%@300 W	94.55%@400 W	~94.3%@200 W
Partial power processing	yes	yes	no	no	no	no
Switching frequency of the main converter	1 MHz	250 kHz	50 kHz	200 kHz	60 kHz	50 kHz
Voltage gain M	$\frac{(2f_sRnC_r+n)\times}{(1+D)}$	$\frac{2n}{2-D}$	$\frac{n}{2(1-D)}$	$2+n(1+D)$	$\frac{2+nD}{1-D}$	$\frac{1+3D}{1-D}$
Normalized voltage stress of main switch (V_S/V_{in})	1	$\frac{2}{2-D}$	$\frac{1}{1-D}$	1	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$

S: switches; D: diodes; C: capacitors; L: inductors; T: transformers.

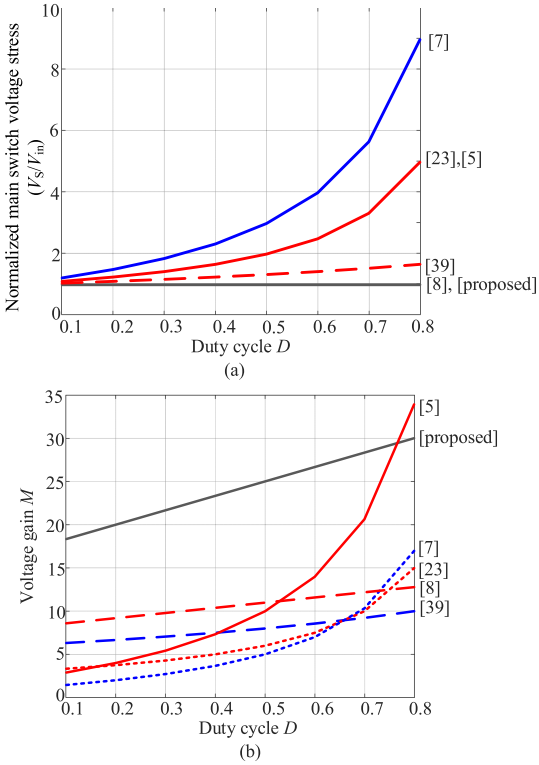

Fig. 23. Performance comparison of the proposed converter and the high step-up converters in Table V. (a) Normalized main switch voltage stress. (b) Voltage gain ($n = 6$).

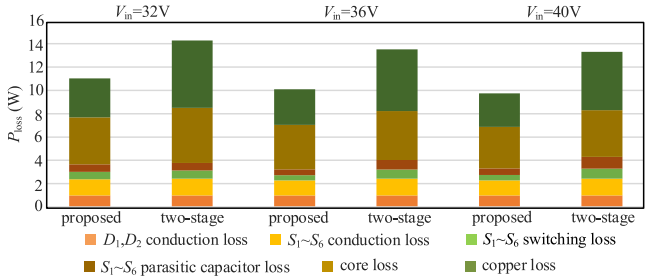

Fig. 24. Comparison of loss distribution between the proposed converter and the conventional two-stage under different input voltages at full load.

gain versus the duty cycle D of the converters in Table V are illustrated in Fig. 23(a) and (b), respectively. It can be seen from Fig. 23 that the proposed converter has advantages in voltage boost capacity with relatively lower voltage stress of the main switch under the adjustable duty cycle in a wide range. In addition, the converter designed in this article also has relatively high measured efficiency by the partial power voltage regulation. Therefore, the proposed converter is more suitable for high step-up applications due to these benefits. However, due to the addition of the partial power dc–dc voltage regulator, the number of components in the proposed converter is slightly more.

The corresponding losses breakdown of the proposed converter and the traditional two-stage converter under different input voltages at full load are shown in Fig. 24, where the losses are calculated according to the theoretical analysis. The two-stage scheme here is the Buck converter cascaded with the main converter proposed in this article. Compared with the two-stage structure dealing with full power, the buck voltage regulator only deals with a small part of the total power in the proposed converter, resulting in less power loss of magnetic components, switches, and higher efficiency under the same working conditions.

The measured system efficiency under different input voltages is shown in Fig. 25. The peak efficiency of the system under 40 V input at full load is 95.3%. According to (35), it can be concluded that as the input voltage increases, the smaller the power ratio k of the buck converter and the higher the system efficiency will be. Besides, the test efficiency comparison curve of the proposed converter, IPOS and the two-stage partial power structure in Fig. 3 under 40 V input is obtained as Fig. 26. The flyback converter is adopted as the voltage regulator in IPOS and the two-stage partial power structure. In both structures, the switching frequency of flyback converter is 100 kHz, which is the same as buck in the proposed converter. The magnetic inductor of the transformer is 80 μH, and the flyback operates at

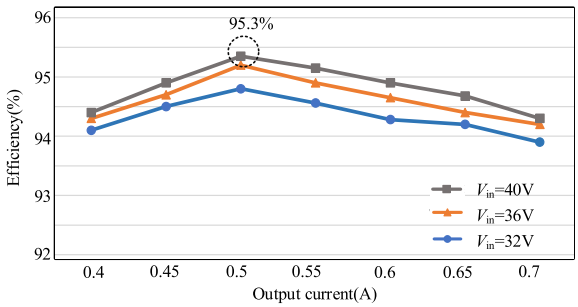

Fig. 25. Efficiency curve under different input voltages.

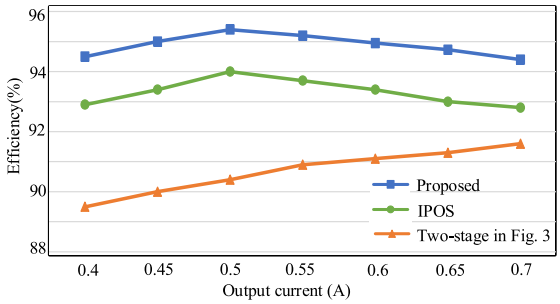

Fig. 26. Comparison of measured efficiency curve of the proposed structure, IPOS and the two-stage partial power structure in Fig. 3($V_{\rm in} = 40$ V).

the CCM state. The turn ratio between the primary and secondary windings of flyback converter is 1:1 and 2:1, respectively. It can be seen from Fig. 26 that compared with the other two converters, the proposed converter performs better efficiency under different loads when $V_{\rm in} = 40$ V.

VI. Conclusion

A partial power processing architecture with different input voltages of the two bridge arms of the full bridge structure is proposed in this article, which features a wide input range, galvanic isolation, fewer components, and low cost. In the proposed structure, the nonisolated dc–dc converter regulates the system output voltage by PWM control, transmitting a small part of the total power, which is conducive to reducing the device stresses and improving the system efficiency. The main isolated dc–dc converter operates at the fixed frequency to achieve constant conversion ratio. An optimal structure is obtained suitable for high step-up applications from the perspective of fewer components, low cost, and better partial power processing capacity. An experimental prototype with 1 MHz switching frequency of 32–40 V input voltage and 400 V output voltage was built. The soft switching properties can be achieved for all the power devices in the main isolated converter, and the resonant tank is located at the secondary side of the transformer, which is conducive to reducing the current stress and ESR losses of the resonant components. Finally, the peak measured efficiency at 40 V input under full load is 95.3%.

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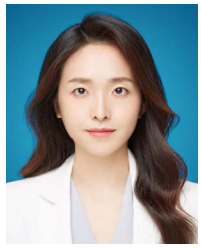

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