Letters

An Improved Asymmetric Modulation of Current-Source Rectifier With CM Filter for Low Voltage Stress on Switching Devices

Haibin Cao, Ping Yang, *Member, IEEE*, Xia Guo, Rui Huang, and Jianping Xu, *Member, IEEE*

***Abstract*—Common-mode (CM) filters are usually utilized in high power density three-phase current-source rectifier (3ph-CSR) to suppress the CM noise in the input currents. However, when CM filters are utilized, the inductor currents at the positive and negative ends of the dc side of 3ph-CSR are unequal, which brings high voltage stress on switching devices. To reduce the voltage stress on the switching devices, an improved asymmetric modulation is proposed in this letter. In the proposed asymmetric modulation, two switching devices are always turned ON in each sector, which clamps the voltage of the switching devices to the peak of the input line voltages. A 1 kW experimental prototype of the 3ph-CSR is built to verify the analysis results.**

***Index Terms*—Asymmetric modulation, three-phase current-source rectifier (3ph-CSR), voltage stress.**

I. Introduction

THREE-PHASE current-source rectifier (3ph-CSR) features low distortion of ac input currents and inherent start-up inrush current limiting capability. The 3ph-CSR, also known as the three-phase buck rectifier (3ph-BR), has been successfully used in more electric aircraft (MEA) [1], [2] and electric vehicle charger [3]. For 3ph-CSR, the high voltage stress on switching devices not only brings high power loss but also makes selection of switching device difficult. Besides, the switching devices with high voltage rating means a high cost of 3ph-CSR. Therefore, some research works on reducing the voltage stress on switching devices have been performed to improve the performance of 3ph-CSR [4], [5], [6], [7].

An improved 3ph-BR with low voltage stress on switching devices is proposed in [4]. The switching devices only need to withstand the input phase voltage. The topology of 3ph-CSR has been modified so that a voltage stress lower than the input phase voltage can be achieved [5]. However, specific modulation is needed together with their topology to reduce voltage stress [4], [5]; the modulation generates two pulse-width driving signals with very small duty ratio, which is difficult to realize, especially when a phase voltage is near to zero. In addition, the topologies in [4] and [5] require an additional diode, which increase the cost and cannot be used in the existing circuit of 3ph-CSR.

The switching loss optimized modulation strategy is widely used in the conventional 3ph-CSRs [6], [7], which makes the switching devices of 3ph-CSR withstand the input line voltage. However, both the current distortion around the boundaries of sectors and the common-mode (CM) noise in the input currents are obvious, which results in a high input current total harmonic distortion (THD) [8], [9].

To eliminate the current distortion around the boundaries of sectors, an asymmetric modulation by applying two asymmetric modulations in different sectors, respectively, has been studied in [8] to achieve extremely low input current THD. For high power density applications, the CM filter is usually utilized to suppress the CM noise [9]. However, when the asymmetric modulation in [8] is applied to 3ph-CSR with a CM filter, the difference of the output inductor currents will appear and causes high voltage stress on switching devices.

To reduce the voltage stress on the switching devices, an improved asymmetric modulation of the 3ph-CSR with CM filter is proposed in this letter. In the proposed asymmetric modulation, two switching devices are always turned ON in each sector, which can clamp the voltage on the switching devices to the input line voltage. When the improved asymmetric modulation is applied to the 3ph-CSR, not only the voltage stress on the switching devices can be reduced but also the low input current THD can be retained.

II. Asymmetric Modulation With High Voltage Stress on Switching Devices

The circuit of 3ph-CSR with CM filter is composed of an input filter unit, six bridge legs, output filter unit, and CM filter unit, as shown in Fig. 1. In Fig. 1, C_{ds1}–C_{ds6} are the parasitic capacitances of switches Q_1–Q_6, respectively. In high power density applications, shield layer is usually adopted to decrease the propagation impedance for the CM noise and to block the

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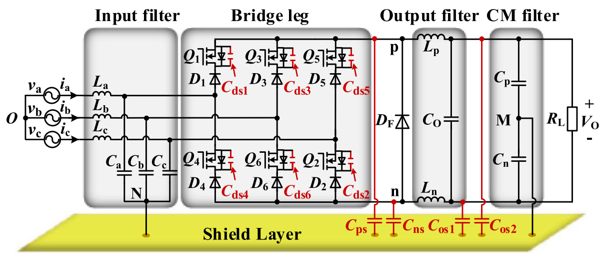

Fig. 1. Circuit model of 3ph-CSR.

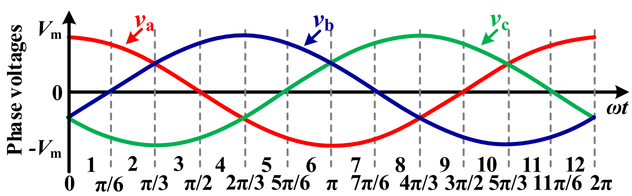

Fig. 2. Three-phase AC input voltages with 12 sectors.

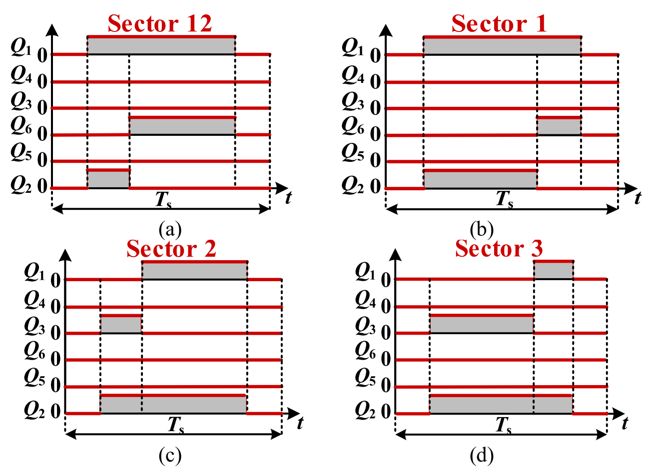

Fig. 3. PWM sequences of the LICT asymmetric modulation in one switching period. (a) Sector 12. (b) Sector 1. (c) Sector 2. (d) Sector 3.

interference between the main power circuit and control circuit. The shield layer produces the distributed capacitances (C_{ps} and C_{ns}, C_{os1} and C_{os2}) between the shield layer and the main power circuit. As distributed capacitances C_{os1} and C_{os2} are much smaller than C_p and C_n, C_{os1} and C_{os2} are not considered.

The asymmetric modulation in [8] can achieve low input current THD (LICT) (called as LICT asymmetric modulation in this letter), which divides 1 ac input cycle into 12 sectors, as shown in Fig. 2. Fig. 3 shows the pulse-width modulation (PWM) sequences of the LICT asymmetric modulation in one switching period in sector 12, sector 1, sector 2, and sector 3. It can be known from Fig. 3(a) and (b) that the duty cycle of Q_1 is larger than that of Q_6 and Q_2, and the duty cycle of Q_1 is symmetrical to the middle of the pulse period in sector 12 and sector 1.

For sector 12, as shown in Fig. 3(a), the duty cycle of Q_2 is smaller than that of Q_6, and Q_2 conducts before Q_6. For sector 1, as shown in Fig. 3(b), the duty cycle of Q_2 is larger than that of Q_6, and Q_2 conducts before Q_6. Thus, the driver signal

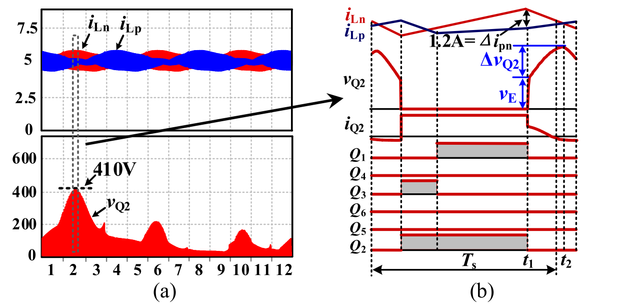

Fig. 4. Simulation waveforms of the output inductor currents and voltage across Q_2 with LICT asymmetric modulation. (a) Output inductor currents and voltage of Q_2 in one ac input cycle. (b) Detailed voltage and current of Q_2 and the driver signals in one switching period in sector 2.

sequences of Q_1, Q_2, and Q_6 does not change in sector 12 and sector 1, and the transition of driver signals between sector 12 and sector 1 is smooth. Similarly, from Fig. 3(c) and (d), the transition of the driver signals between sector 2 and sector 3 is also smooth. Therefore, the input current distortion during the transition from the even sector to odd sector in space vector pulsewidth modulation (SVPWM) can be eliminated [8].

Fig. 4 shows the simulation waveforms of the output inductor currents i_{Lp}, i_{Ln} and the voltage v_{Q2} across Q_2 when the LICT asymmetric modulation is applied. The simulation is performed for the 3ph-CSR when three-phase ac input voltage $V_{\rm in}$ is 115 Vac/400 Hz, switching frequency f_S = 200 kHz, output voltage $V_O = 200$ V, inductors $L_p = L_n = 300\,\mu$H, the distributed capacitance tested in the prototype is $C_{ps} = C_{ns} \approx 500$ pF, the parasitic capacitance of Q_2 from the datasheet of MOSFET is $C_{ds2} = 30$ pF, and the input filter capacitance $C_c = 880$ nF.

Fig. 4(a) shows the output inductor currents i_{Lp}, i_{Ln}, and the voltage v_{Q2} across Q_2 in one ac input cycle. From Fig. 4(a), the voltage stress on Q_2 is 410 V. Fig. 4(b) shows the driver signals and detailed waveforms of i_{Lp}, i_{Ln}, and v_{Q2} in sector 2. From Fig. 4(b), v_{Q2} is expressed as follows:

$$v_{Q2}(t) = v_E + \Delta v_{Q2}(t). \tag{1}$$

In Fig. 4(b), before time t_1, Q_1 and Q_2 are conducted, the voltages across C_{ps} and C_{ns} satisfy $v_{Cps} = v_{Ca} > v_{Cns} = v_{Cc}$, so D_F is turned OFF.

When Q_1 and Q_2 are turned OFF, C_{ps} is discharged by i_{Lp}, C_{ns} is charged by i_{Ln}. v_{Cps} and v_{Cns} will be equal quickly, i.e., $v_{Cps} = v_{Cns} = 0.5(v_{Ca} + v_{Cc})$. Thus, v_E can be expressed as follows:

$$v_E = -v_{Cc} + 0.5(v_{Cc} + v_{Ca}). \tag{2}$$

Then, $v_{Cps} < v_{Cns}$, D_F is turned ON.

From Fig. 4(b), during time interval t_1–t_2, i_{Lp} is not equal to i_{Ln}, which generates three current paths in the 3ph-CSR, as shown in Fig. 5.

It can be known from Fig. 5 that current path 1 is for load current, current path 2 and current path 3 are for the difference current Δi_{pn} between i_{Lp} and i_{Ln}. In current path 2, a part of Δi_{pn} flows through C_{ps} and C_{ns} to shield layer. In current path 3, as the voltage across C_c is minimum among the voltage across C_a, C_b, and C_c in sector 2, the other part of Δi_{pn} (i_{Q2}) flows

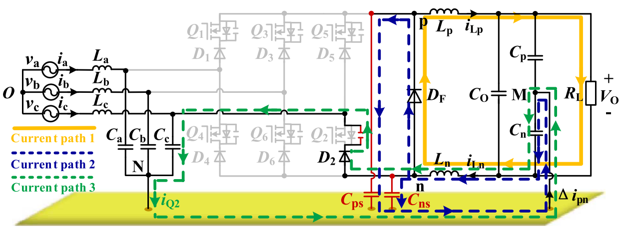

Fig. 5. Current paths of the 3ph-CSR during time interval t_1–t_2 in sector 2 when the LICT asymmetric modulation is applied.

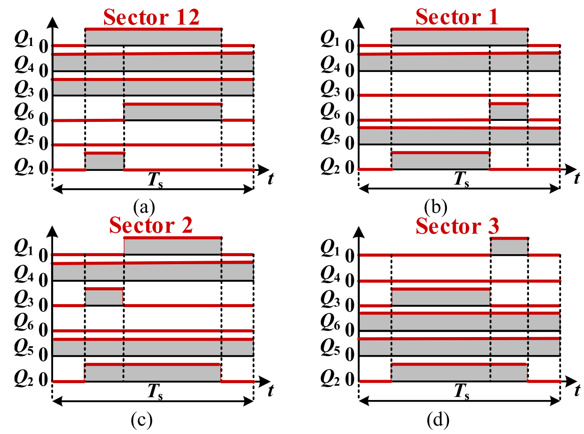

Fig. 6. PWM sequences of the bridge legs in one switching period. (a) Sector 12. (b) Sector 1. (c) Sector 2. (d) Sector 3.

through switch Q_2 and the input filter capacitance C_c to shield layer. The parasitic capacitances C_{ds2} of switch Q_2 is charged, and Δv_{Q2} is generated.

From Fig. 5, during t_1–t$_2$, i_{Q2} can be expressed as follows:

$$i_{Q2}(t) = K\Delta i_{pn}(t) \tag{3}$$

where K is defined as follows:

$$K = \frac{C_c C_{ds2}}{C_c C_{ds2} + (C_c + C_{ds2})(C_{ns} + C_{ps})}. \tag{4}$$

According to the principle of capacitor amp-second balance, Δv_{Q2} is expressed as follows:

$$\Delta v_{Q2}(t) = \frac{\int i_{Q2}(t)dt}{C_2} = K\frac{\int \Delta i_{pn}(t)dt}{C_2}. \tag{5}$$

From (1), (2), and (5), v_{Q2} in sector 2 can be expressed as follows:

$$v_{Q2}(t) = -v_{Cc} + 0.5(v_{Cc} + v_{Ca}) + K\frac{\int \Delta i_{pn}(t)dt}{C_2}. \tag{6}$$

According to (6), with the same parameters as simulation parameters, the peak voltage of Q_2 can be calculated as 410 V, which is consistent with the simulation result. The voltages of other switching devices can be calculated in the same way.

When ac input voltages or ac input frequency increases, Δi_{pn} increases. For the MEA application with input voltage of 90–140 Vac (115 $\pm$ 25 Vac) and ac input frequency of 360–800 Hz, the peak voltage of Q_2 can be higher than 650 V. In the selection of switching devices, the switching device with a voltage rating of 950 V (or higher) need to be considered.

III. Proposed Asymmetric Modulation With LVS on Switching Devices

To reduce the voltage stress on switching devices, an improved asymmetric modulation, called as low voltage stress (LVS) asymmetric modulation, is proposed. Fig. 6 shows the proposed LVS asymmetric modulation in sector 12, sector 1, sector 2, and sector 3. Compared with the LICT asymmetric modulation, the proposed LVS asymmetric modulation has two always conducted switching devices in each sector, e.g., Q_3 and Q_4 are always turned ON in sector 12. Table I presents two always conducted switching devices in different sectors.

Fig. 7 shows the simulation waveforms of the output inductor currents i_{Lp} and i_{Ln}, and the voltage across Q_2 when the proposed LVS asymmetric modulation is applied to 3ph-CSR. From Fig. 7(a), the voltage stress on Q_2 is 282 V. From Fig. 7(b), when

TABLE I
Two Always Conducted Switching Devices in Different Sectors

Sectors	1 and 2	3 and 4	5 and 6	7 and 8	9 and 10	11 and 12
Switches	Q_4 and Q_5	Q_5 and Q_6	Q_1 and Q_6	Q_1 and Q_2	Q_2 and Q_3	Q_3 and Q_4

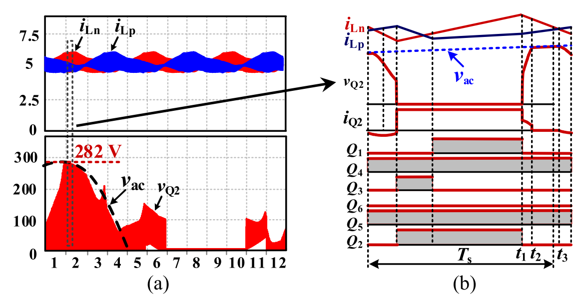

Fig. 7. Simulation waveforms of output inductor currents i_{Lp}, i_{Ln} and the voltage across Q_2 when the proposed LVS asymmetric modulation is applied. (a) Output inductor currents and the voltage of Q_2 in one input ac cycle. (b) Detailed voltage of Q_2 and the driver signals in one switching period in sector 2.

Q_2 is turned OFF and $i_{Ln} > i_{Lp}$ in sector 2, v_{Q2} has two segments during time interval t_1–t_2 and during time interval t_2–t_3, respectively. v_{Q2} increases rapidly during time interval t_1–t_2, and then it is clamped to the input line voltage v_{ac} during time interval t_2–t_3. The two segments of v_{Q2} during time interval t_1–t_2 and time interval t_2–t_3 mean that 3ph-CSR has two operating states during time interval t_1–t_3.

Fig. 8(a) and (b) show three current paths in the time interval t_1–t_2 and time interval t_2–t_3, respectively. From Fig. 8(a), during t_1–t_2, $v_{Q2} < v_{Ca} - v_{Cc}$, D_2 is turned ON. According to current path 3, a portion of Δi_{pn} (i_{Q2}) flows through C_{ds2} and C_c to shield layer, C_{ds2} is charged, v_{Q2} increases until $v_{Q2} = v_{\mathrm{ac}}$.

As shown in Fig. 8(b), during t_2–t_3, $v_{Q2} = v_{\mathrm{ac}}$, D_4 is turned ON, and D_2 is turned OFF. According to current path 3, the current i_{Q4} will flow through Q_4 and C_a to shield layer, not flow through Q_2, v_{Q2} does not increase, i.e., v_{Q2} is clamped to the input line voltage v_{ac}. The voltages across other switching devices are similar.

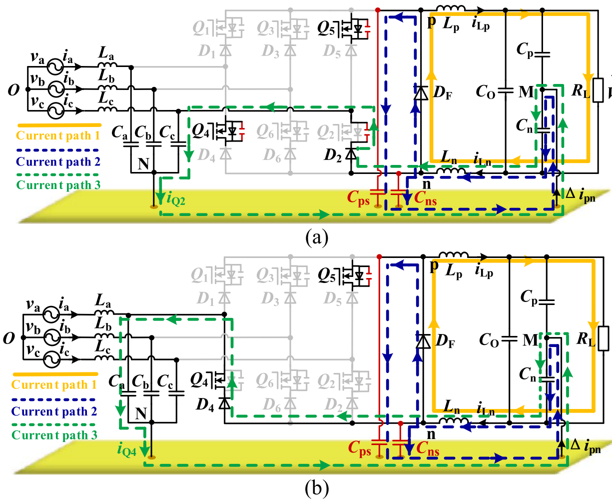

Fig. 8. Current paths of 3ph-CSR with the proposed LVS asymmetric modulation in sector 2 when Q_2 is turned OFF and $i_{Ln} > i_{Lp}$. (a) During time interval t_1–t_2. (b) During time interval t_2–t_3.

For the MEA application, the maximum voltage stress on switching devices is 343 V, which is corresponding to the input line voltage of 140 Vac. The switching devices with a voltage rating of 650 V can be utilized.

IV. Comparative Analysis of Power Loss

The power loss of switching devices mainly includes conduction loss and switching loss. The conduction loss depends on the current flowing through the device. Switching loss depends on the current flowing through the device and the voltage across it during the switching transition. In the following analysis, sector 2 is taken as an example to compare the power loss of the LICT asymmetric modulation and the proposed LVS asymmetric modulation.

A. Analysis of Conduction Loss

1) When Q_2 is Turned ON: For the proposed LVS asymmetric modulation, as shown in Fig. 6(c), the output inductor currents only flow through switching devices Q_1, Q_2, and Q_3, but do not flow through Q_4 and Q_5 [9], i.e., Q_4 and Q_5 do not produce conduction loss. Furthermore, compared with the LICT asymmetric modulation, the switch states of the switching devices Q_1, Q_2, and Q_3 are not changed in the proposed LVS asymmetric modulation in sector 2. Thus, when Q_2 is turned ON, the conduction loss of the switching devices in the proposed LVS asymmetric modulation and the LICT asymmetric modulation is consistent.

2) When Q_2 is Turned OFF: The switching devices Q_1, Q_2, and Q_3 are turned OFF and no conduction loss occurs.

For the LICT asymmetric modulation, as shown in Fig. 5, among the six bridge legs of the 3ph-CSR, only D_2 has a current i_{Q2} flowing through it. It can be known from (3) and (4) that i_{Q2} is very small; thus, the conduction loss of D_2 can be ignored.

For the proposed LVS asymmetric modulation, it can be known from Section III that the 3ph-CSR have two operating states: $v_{Q2} < v_{\mathrm{ac}}$ and $v_{Q2} = v_{\mathrm{ac}}$, as shown in Fig. 8. When $v_{Q2}<v_{\mathrm{ac}}$, as shown in Fig. 8(a), no current flows through the switching devices Q_4 and Q_5; thus, the operating state of 3ph-CSR is the same as that of the LICT asymmetric modulation. When $v_{Q2} = v_{\mathrm{ac}}$, as shown in Fig. 8(b), no current flows through Q_5 and no conduction loss occurs, while almost all of the Δi_{pn} (i_{Q4}) flows through Q_4 and D_4 to C_a because the input filter capacitance C_a is much larger than the distributed capacitances C_{ps} and C_{ns}; thus, Q_4 and D_4 will produce extra conduction loss compared with the LICT asymmetric modulation. This extra conduction loss $P_{\mathrm{loss\_EC}}$ in one switching period can be expressed as follows:

$$P_{\mathrm{loss\_EC}} = \int R_{\mathrm{on}} i_{Q4}^2(t) + V_F i_{Q4}(t) dt \tag{7}$$

R_{on} is the ON-resistance of MOSFET Q_4, and V_F is the forward voltage of diode D_4.

From Fig. 7(b), before $v_{Q2} = v_{\mathrm{ac}}$, Δi_{pn} decreases rapidly. When $v_{Q2} = v_{\mathrm{ac}}$, Δi_{pn} is relatively small, i.e., the current i_{Q4} is relatively small. What is more, the duration of $v_{Q2} = v_{\mathrm{ac}}$ is short, and R_{on} is significantly reduced under the same rating package conditions when the MOSFETs with low voltage rating are used. Thus, from (7), the extra conduction loss $P_{\mathrm{loss\_EC}}$ is small.

Thus, the conduction loss of LVS asymmetric modulation is almost the same as LICT asymmetric modulation. However, the proposed LVS asymmetric modulation can utilize the cost-efficient and low voltage rating MOSFETs with low ON-resistance, and the conduction loss of MOSFETs can be reduced significantly.

B. Analysis of Switching Loss

Compared with the LICT asymmetric modulation, Q_4 and Q_5 are always turned ON in each switching period of sector 2 for the proposed LVS asymmetric modulation; thus, Q_4 and Q_5 do not produce switching loss. The output inductor currents only commutate among the upper bridge leg of phases A and B, the lower bridge leg of phase C, and the freewheeling diodes [5] in sector 2. Thus, for these two modulations, only the switching losses of Q_1–Q_3, D_1–D_3, and D_{F} need to be analyzed and compared.

For the proposed LVS asymmetric modulation and the LICT asymmetric modulation, when Q_2 is turned OFF in sector 2, $v_{Cps} = v_{Cns}$ is approved in the above analysis. To simplify the analysis of switching loss, assuming that v_{Cps} is higher than v_{Cb} because v_{Cb} is relatively small, and the voltage of input filter capacitance is equal to the corresponding input phase voltage, i.e., $v_{Cx} = v_x$ ($x = a, b, c$).

The switching loss of switching devices in 3ph-CSR has been well analyzed [5], [10]. In [5] and [10], the current flowing through the switching device is considered as the output current. The switching loss of the switching devices is in proportional to the voltage across the switching device, and the proportional coefficient is a constant k. Therefore, the calculation of the switching loss in one switching period of sector 2 is shown in Table II.

In Table II, the proportional coefficient of MOSFET (Q_1–Q_6) is k_1, and the proportional coefficient of the diodes (D_1–D_6 and

TABLE II
SWITCHING LOSS IN ONE SWITCHING PERIOD OF SECTOR 2

Switching Devices	LICT asymmetric modulation	LVS asymmetric modulation
Q_1	$k_1I_O(v_a-v_b)+k_1I_O(v_a-v_E)$	$k_1I_O(v_a-v_b)+k_1I_O(v_a-v_E)$
Q_2	$k_1I_O(v_{Cps1}-v_c)+k_1I_O(v_E-v_c)$	$k_1I_O(v_{Cps2}-v_c)+k_1I_O(v_E-v_c)$
Q_3	0	0
D_1	0	0
D_2	0	0
D_3	$k_2I_O(v_{Cns1}-v_b)+k_2I_O(v_a-v_b)$	$k_2I_O(v_{Cns2}-v_b)+k_2I_O(v_a-v_b)$
D_F	$k_2I_O(v_b-v_c)+k_2I_O(v_a-v_c)$	$k_2I_O(v_b-v_c)+k_2I_O(v_a-v_c)$
Total switching loss	$k_1I_Ov_{ab}+k_1I_Ov_{ac}+2k_2I_Ov_{ac}+k_1I_O(v_{Cps1}-v_c)+k_2I_O(v_{Cns1}-v_b)$	$k_1I_Ov_{ab}+k_1I_Ov_{ac}+2k_2I_Ov_{ac}+k_1I_O(v_{Cps2}-v_c)+k_2I_O(v_{Cns2}-v_b)$

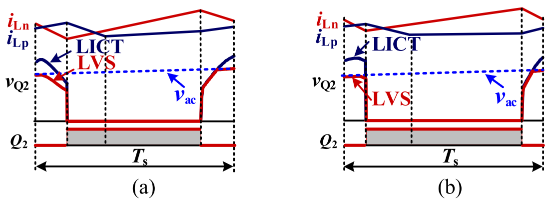

Fig. 9. Simulation results of v_{Q2} of these two modulations in one switching period of sector 2. (a) Close to sector 1. (b) Close to sector 3.

D_F) in series with the MOSFET is k_2. For the LICT asymmetric modulation and the proposed LVS asymmetric modulation, the voltages across C_{ps} and C_{ns} are v_{Cps1} and v_{Cns1} and v_{Cps2} and v_{Cns2}, respectively.

From the above analysis, $v_{Q2} = v_{Cps}-v_c$; thus, the total switching loss $P_{\text{loss\_SW}}$ of these two modulations can be expressed as follows:

$$\begin{aligned} P_{\text{loss\_SW}} &= k_1I_Ov_{ab} + k_1I_Ov_{\text{ac}}+2k_2I_Ov_{\text{ac}} + k_1I_O(v_{Cps} - v_c) \\ &\quad + k_2I_O(v_{Cns} - v_b) \\ &= k_1I_Ov_{ab} + k_1I_Ov_{\text{ac}}+2k_2I_Ov_{\text{ac}} + k_1I_Ov_{Q2\_F} \\ &\quad + k_2I_O(v_{Q2\_F} - v_b) \end{aligned} \tag{8}$$

v_{Q2_F} is the voltage across Q_2 at the time instant when it is about to turn ON.

From (8), under the same input conditions, the difference of the switching loss between these two modulations depends on v_{Q2_F}, the switching loss increases with the increase of v_{Q2_F}.

Fig. 9(a) and (b) show the simulation results of v_{Q2} with these two modulations in sector 2. Fig. 9(a) shows the simulation results close to sector 1, and Fig. 9(b) shows the simulation results close to sector 3.

In Fig. 9(a), the difference of v_{Q2_F} between these two modulations is small, so the switching losses of these two modulations are almost the same. In Fig. 9(b), v_{Q2_F} of the LICT asymmetric modulation is almost equal to its own maximum value, i.e., the voltage stress on Q_2, which is obviously higher than that of the proposed LVS asymmetric modulation, so the switching loss of the LICT asymmetric modulation is higher. Therefore, in sector 2, the switching loss of the LICT asymmetric modulation is higher than that of the proposed LVS asymmetric modulation, and the difference of switching loss between these two modulations mainly depends on the voltage stress on Q_2.

The switching loss in other sectors can be evaluated in a similar way, and the switching loss of the LICT asymmetric modulation is still higher than that of the proposed LVS asymmetric modulation in 12 sectors.

Consider that the difference between the voltage stress on switching devices of the LICT asymmetric modulation and the LVS asymmetric modulation is relatively small when three-phase input voltage V_{in} is 115 Vac/400 Hz, the extra conduction loss produced by these two always conducted switching devices is relatively small; thus, the efficiency of these two modulations will not be significantly different.

However, with the increase of the ac input voltage and ac input frequency, the difference of the voltage stress of the switching device between the LICT asymmetric modulation and the proposed LVS asymmetric modulation becomes larger, and the switching loss of the LICT asymmetric modulation will be obviously higher than that of the LVS asymmetric modulation.

TABLE III
CIRCUIT PARAMETERS OF EXPERIMENTAL PROTOTYPE

Parameters	**Value**
Switching frequency f_S	200 kHz
Output voltage V_O	200 V
Output power P_O	1 kW
Output inductor L_p, L_n	300 μH
Output capacitance C_O	300 μF
CM filter capacitance C_p, C_n	880 nF
Diode D_1– D_6, D_F	IDD08SG60CXTMA2
MOSFET Q_1–Q_6 (LICT)	IPD95R750P7 (950 V)
MOSFET Q_1–Q_6 (LVS)	IPD60R180P7 (650 V)

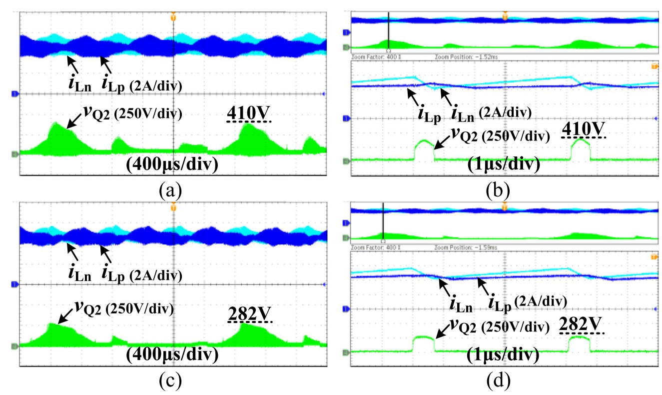

Fig. 10. Experimental results of output inductor currents and voltage across Q_2 when $V_{\text{in}} = 115$ Vac, $f_L = 400$ Hz, and $P_O = 1$ kW with different modulations. (a) Experimental results of the LICT asymmetric modulation. (b) Detailed experimental results of the LICT asymmetric modulation. (c) Experimental results of the LVS asymmetric modulation. (d) Detailed experimental results of the LVS asymmetric modulation.

V. EXPERIMENTAL RESULTS

To verify the analysis results of the proposed LVS asymmetric modulation, a 1 kW experimental prototype of 3ph-CSR with standard full-brick size is developed. The circuit parameters of the experimental prototype are given in Table III. The ac input frequency f_L is 400–800 Hz and voltage V_{in} is 90–140 Vac.

Fig. 10(a)–(d) show the experimental results of the output inductor currents and voltage across Q_2 with different modulations for the ac input of 115 Vac/400 Hz, respectively. Fig. 10(a) shows that with the LICT asymmetric modulation, and Fig. 10(b) is the

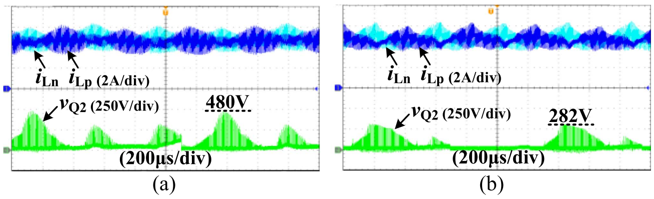

Fig. 11. Experimental results of output inductor currents and voltage across Q_2 when $V_{\rm in} = 115$ Vac, $f_L = 800$ Hz, and $P_O = 1$ kW with different modulations. (a) LICT asymmetric modulation. (b) LVS asymmetric modulation.

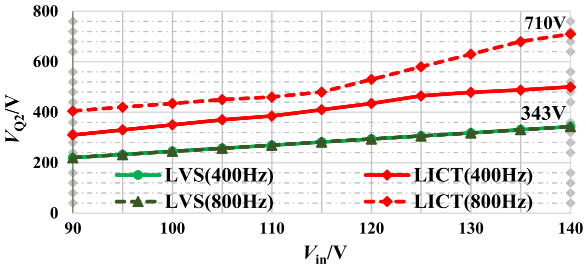

Fig. 12. Voltage stress on Q_2 of the LICT asymmetric modulation and the proposed LVS asymmetric modulation versus input phase voltage with different ac input frequencies when $P_O = 1$ kW.

detailed waveforms of Fig. 10(a) for i_{Lp}, i_{Ln} and v_{Q2} in sector 2. It is known that the voltage stress on Q_2 is approximately 410 V. Fig. 10(c) shows the proposed LVS asymmetric modulation, and Fig. 10(d) shows the detailed waveforms of Fig. 10(c) for i_{Lp}, i_{Ln} and v_{Q2} in sector 2. It is known that the voltage stress on Q_2 is reduced to the input line voltage of 282 V.

Fig. 11(a) and (b) show the experimental results of the output inductor currents and voltage across Q_2 with different modulations for the ac input of 115 Vac/800 Hz, respectively. It is known that with the LICT asymmetric modulation, the voltage stress on Q_2 is approximately 480 V, and with the proposed LVS asymmetric modulation, the voltage stress on Q_2 is reduced to the input line voltage of 282 V.

Fig. 12 shows the voltage stress on Q_2 with the LICT asymmetric modulation and the proposed LVS asymmetric modulation versus input phase voltage with different ac input frequencies. It is known that when the LICT asymmetric modulation is utilized, the voltage stress on Q_2 increases with the increase of the ac input voltages and ac input frequency, which can be up to 710 V when $V_{\rm in} = 140$ Vac and $f_L = 800$ Hz. However, with the proposed LVS asymmetric modulation, the maximum voltage stress on Q_2 is 343 V, which corresponds to the line voltages with $V_{\rm in} = 140$ Vac. Therefore, when the proposed LVS asymmetric modulation is applied, the switching devices with a voltage rating of 650 V can be utilized in 3ph-CSR.

Compared with the LICT asymmetric modulation, the proposed LVS asymmetric modulation has two always conducted switching devices, while the output inductor currents do not flow through these two switching devices [9]. Furthermore, the switch states of other switching devices are not changed for the proposed LVS asymmetric modulation. Therefore, there is no input currents distortion of the 3ph-CSR with the LVS asymmetric modulation during sector transition, and the low input current THD can be achieved. However, the LVS asymmetric modulation has an additional operating state in each switching

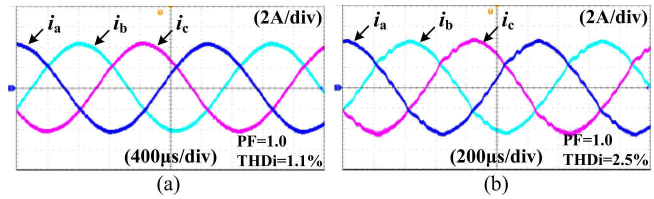

Fig. 13. Experimental results of input currents with the LVS asymmetric modulation when $V_{\rm in} = 115$ Vac and $P_O = 1$ kW for different ac input frequencies. (a) 400 Hz. (b) 800 Hz.

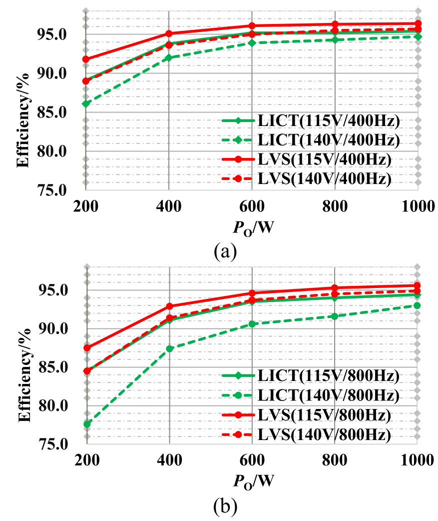

Fig. 14. Experimental results of the efficiency of the LICT asymmetric modulation and the proposed LVS asymmetric modulation versus output power with different ac input frequencies. (a) 400 Hz. (b) 800 Hz.

period, such as that represented in Fig. 8(b). In this additional operating state, there has a current flowing through one of these two always conducted switching devices to the input side, which cause slightly higher input current THD than that of the LICT asymmetric modulation.

Fig. 13(a) and (b) show the experimental results of the input currents of the 3ph-CSR with the proposed LVS asymmetric modulation when ac input frequency $f_L = 400$ Hz and 800 Hz, respectively. The input current THD for ac input frequency $f_L = 400$ Hz and 800 Hz is 1.1% and 2.5%, respectively, i.e., low input current THD can be achieved for ac input frequency $f_L = 400$ Hz and 800 Hz.

Fig. 14(a) and (b) show the experimental results of the efficiency of the LICT asymmetric modulation and the proposed LVS asymmetric modulation in different ac input frequencies, respectively. From Fig. 14(a) and (b), the efficiency of the LVS asymmetric modulation with low voltage rating MOSFETs IPD60R180P7(650 V) is obviously higher than that of the LICT asymmetric modulation with high voltage rating MOSFETs IPD95R750P7(950 V).

For the input voltage 115 Vac/400 Hz, compared with the LICT asymmetric modulation, under full-load condition, the efficiency of the experimental prototype is improved from about 95.4% to 96.4%. For the input voltage 115 Vac/800 Hz, the efficiency of the experimental prototype under full load is improved from about 94.4% to 95.6%.

Furthermore, the efficiency of the 3ph-CSR decreases with the increase of the ac input voltage and input frequency. Under the full-load condition, with the LICT asymmetric modulation, when the input voltage is 115 Vac/400 Hz, the efficiency of the experimental prototype is 95.4%. While when the input voltage is 140 Vac/800 Hz, the efficiency of the experimental prototype is only 93.0%.

Comparing these low voltage rating and high voltage rating MOSFETs, they have similar parasitic parameters. The improvement of efficiency is mainly due to the lower ON-resistance of the low voltage rating MOSFETs and the reduction of the switching loss.

VI. Conclusion

In this letter, an improved asymmetric modulation of 3ph-CSR is proposed to significantly reduce the voltage stress on the switching devices caused by CM filter. Therefore, the low voltage rating MOSFET can be adopted to obtain lower cost and higher efficiency. Moreover, the proposed asymmetric modulation retains the characteristics of low THD of the input currents of LICT asymmetric modulation. Therefore, the proposed modulation with LVS on the switching devices and low THD of the input currents is very suitable for high power density applications.

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