Accurate Modeling and Elimination of Double Vertical Crossing in Multi-Sampled Digital-Controlled Buck Converters

Zhengyuan Zhou, *Student Member, IEEE*, Zeng Liu, *Senior Member, IEEE*, Lulu Guo, Jike Wang, and Jinjun Liu, *Fellow, IEEE*

***Abstract*—The multisampling method is an effective approach to reduce delay in digital controlled power converters. However, this method may deteriorate the dynamic performance of converters due to double vertical crossing (DVC) of modulation signal and carrier signal, which makes the closed-loop regulation lost. This phenomenon is influenced by the operating point, parameters of power stage and control system. Therefore, it is significant to predict and eliminate the DVC for avoiding its negative influences. This article proposes an accurate model of DVC in multisampled digital-controlled buck converters, where the output capacitance and the sampling delay is taken into account. Then, a carrier phase adjusting algorithm is proposed to eliminate DVC. The proposed method features better dynamic performance than existing methods, and it is easier to realize since it keeps switching frequency constant. Finally, the theoretical analysis is validated by the simulation and the experimental results.**

***Index Terms*—Digital control, digital pulse width modulation, multisampling, sampling delay, voltage control.**

I. Introduction

FOR high-power converters with low switching frequency, the dynamic performance of the classical single-update or double-update digital control is not capable of the requirements in applications [1], [2], due to the intrinsic delay of digital pulsewidth modulation (DPWM). The multisampling technique, which can significantly reduce the delay, is introduced by applying sampling and update of modulation signal at multiples of switching frequency in a converter [3]. The increased control frequency enables the closed-loop regulation to reach a higher bandwidth, and thus better dynamic performance can be achieved [4]. Models of this technique have been established and validated through both control theory and nonlinear analysis, indicating that multiupdate PWM is equivalent to double-update PWM with a sampling instant shift [5], [6], [7], [25]. Furthermore, multisampling approaches have been applied to enhance the performance of digital-controlled power converters including dc–dc converters [8], [9], [10], [11], [12], [24], dc–ac converters [13], [14], [15], [16], [17], [18], [19], [25], [26], [27], and motor drives [20], [21].

However, the multisampling approach will also introduce some limitations, and a major one of them is that switching ripple is introduced into the modulation signal, which causes problems in coordination with carrier signal and deteriorate the dynamic performance of converter. The coordination problems include the jitter amplification (JA) and the double vertical crossing (DVC). The JA is a phenomenon that the carrier signal and the modulation signal have one vertical crossing when their derivatives are both positive or both negative, while the DVC is a phenomenon that the carrier signal and the modulation signal with opposite derivatives have two vertical crossings within one switching period.

The JA is reported and analyzed in [23]. It will increase the small-signal gain of the modulation process at the operating point where it happens. Based on the research, an algorithm is proposed to block the jitter by reducing the updating frequency of the modulation signal to twice of the switching frequency after the jitter is recognized in the steady state, and recover the original updating rate when large dynamics happen. On the contrary with the JA, the DVC will decrease the small-signal gain of the modulation process at the operating point where it happens, as a small perturbation in the modulation signal is not able to impact the duty ratio. Modeling of the DVC in a multi-sampled buck converter is first presented in [11], where the control bandwidth is considered as the critical factor to its occurrence. However, the model is not precise, because the influence of the sampling delay and the filter capacitance is not considered. The two coordination problems are unified in [27] with the total delay from the microprocessor, the DPWM, and the equivalent delay of the noise-removing filter. Systems could have DVC with small delay, while large delay could lead to JA. When the total delay is on the border between DVC and JA, both of them can be eliminated.

Dedicated solutions to mitigate the DVC can mainly be classified into two types. The first type, i.e., the filter-based approach,

Manuscript received 8 September 2022; revised 11 January 2023; accepted 9 March 2023. Date of publication 31 March 2023; date of current version 19 May 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 51777160 and in part by the Natural Science Basic Research Program of Shaanxi under Grant 2020JM-060. This paper was presented in part at 35th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, USA, 2020. Recommended for publication by Associate Editor L. Corradini. *(Corresponding author: Zeng Liu.)*

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: zhouzhengyuan@stu.xjtu.edu.cn; zengliu@mail.xjtu.edu.cn; muchenk@stu.xjtu.edu.cn; jike.wang@stu.xjtu.edu.cn; jjliu@mail.xjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3263620.

Digital Object Identifier 10.1109/TPEL.2023.3263620

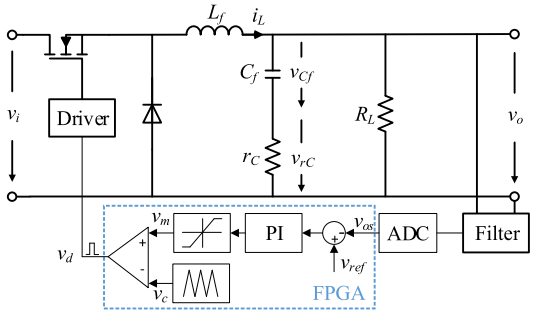

Fig. 1. Power stage and FPGA-based control system for the studied multi-sampled digital-controlled buck converter.

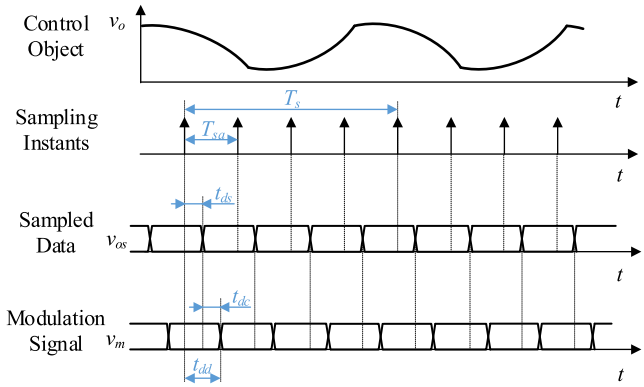

Fig. 2. Digital delay in the control system of the multisampled digital-controlled buck converter.

is to add filters in the regulator to reduce the magnitude of switching frequency components in the modulation signal; while the second type, i.e., the modulation-based approach, is to add an extra component before generating the PWM signal to prevent the DVC. In the filter-based approach, the filter should be designed with as less phase delay as possible so that the advantages of the multisampling method are still available. Various repetitive filters have been proposed considering full ripple removing with simplicity [19], sideband suppression [25], and high-frequency performance [25]. So far, the filter-based approaches have drawn more attention because it is easier to analyze in the frequency domain. However, the mechanism of the DVC is still lack of explanation in the time domain, which is hard to analyze with the filter-based approaches. Thus, detailed analysis in the time domain with the modulation-based approaches is demonstrative and important to the DVC phenomenon. Besides, the extra phase lag introduced by the filters is also a burden to the dynamic performance.

As a modulation-based approach, a phase-locked loop of the sampling frequency is designed to control the crossing point of the carrier and the modulation signal [12]. Thus, the DVC is eliminated since one crossing is controlled to be vertical. The resolution of this method will reduce as the increase of multisampling rate. Besides, this method can only be applied with external ADCs which both the phase of carrier and the sampling instants are adjustable, while with internal ADCs with fixed sampling instants, the method is not available.

To handle the aforementioned issues in the models and the mitigation approaches of the DVC in the multisampled power converters, this article proposes an accurate DVC model derived from the regulator parameters, the shape of the ripple and the working point. The sampling delay and the filter capacitance are important factors to the shape of ripple, and thus the proposed DVC model is more accurate than the existing model. Furthermore, a new modulation-based DVC mitigation approach is proposed by automatically adjusting the phase of the carrier signal to control the crossing point of the carrier and the modulation signal. The system with the proposed method shows better dynamic performance than the system with the simplified repetitive filter (SRF), the full repetitive filter (FRF) and the sampling frequency adjusting method under the same regulator parameters.

The rest parts of this article are organized as follow. Section II introduces the multi-sampled digital-controlled buck converter studied in this article. The model of multi-sampled buck converter is introduced and the theoretical limit of closed-loop bandwidth is verified. In Section III, the accurate model of the DVC is derived. In Section IV, the theoretical analysis and the automatic adjusting algorithm of the carrier signal is presented. Section V validates the theoretical results and the proposed method by simulation and experiments. Finally, Section VI concludes this article.

II. Digital-Controlled Buck Converter Studied

A buck converter with digital control is introduced in Fig. 1. A filter is used to mitigate the high frequency noise in the output voltage v_o. The output voltage v_o is sampled by N times in a switching period with an A/D converter, and then the error between the A/D conversion result v_{os} and the reference value $v_{\rm ref}$ is processed by a PI regulator and an amplitude limiter to produce the modulation signal v_m in each sampling cycle. The PWM signal v_d is generated from the comparison of the modulation signal and the carrier signal v_c, and it controls the power MOSFET via the driver.

A. Small-Signal Model of Multisampled Buck Converters

The major advantage of the multisampling method against the single-sampling method is that the equivalent time delay in the multisampling method is smaller. The time delay in a digital system consists of the modulation delay t_{dm} and the digital delay t_{dd}. In converters with the carriers of the triangular waveforms, the modulation delay is half of the sampling period [5]. The digital delay consists of the conversion delay of A/D converter t_{ds} and the computation time t_{dc}. When the conversion delay is smaller than the expected sampling period, the A/D conversion and the update of modulation signal can be triggered at different time as it is illustrated in Fig. 2 where T_s denotes the switching period, and T_{sa} denotes the sampling period. The controlled object v_o is sampled at each sampling instant, and the sampled data v_{os} is acquired after a conversion delay t_{ds}. The modulation signal v_m is then calculated from the sampled data after computation time t_{dc}. Therefore, the equivalent time delay

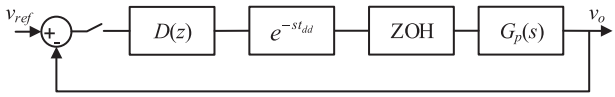

Fig. 3. Block diagram of the loop gain in the multisampled buck converter.

t_d is

$$t_d = t_{dm} + t_{ds} + t_{dc} \tag{1}$$

and the block diagram of the loop gain in the multi-sampled buck converter is derived in Fig. 3 where the power stage

$$G_p(s) = v_i(1 + s/\omega_{esr}) / \left[1 + s/Q\omega_0 + (s/\omega_0)^2\right] \tag{2}$$

is controlled by a discretized PI compensator

$$D(z) = Z\left[K_p(1 + s\tau_i)/s\tau_i\right]. \tag{3}$$

The digital delay t_{dd} is treated as a pure delay process in the forward path, and the modulation delay t_{dm} is presented by the ZOH block to emphasize the stair-like waveform of the modulation signal.

B. Bandwidth Limit of the Digital Compensator

In the buck converter with a PI compensator, the transfer function of the loop gain has three poles and two zeros. At the crossover frequency ω_c, the phase angle of the loop gain is

$$\angle T(j\omega_c) = \angle\left\{Z^{-1}[D(z)] \cdot e^{-st_d} \cdot G_p(s)\right\}|_{s=j\omega_c} \tag{4}$$

replacing $G_p(s)$ and $D(z)$ with (2) and (3), we have

$$\angle T(j\omega_c) = \angle\left\{\frac{v_i K_p}{\tau_i} \cdot \frac{(1 + j\omega_c\tau_i)(1 + j\omega_c/\omega_{esr})e^{-j\omega_c t_d}}{j\omega_c\left[1 - (\omega_c/\omega_0)^2 + j\omega_c/Q\omega_0\right]}\right\}. \tag{5}$$

Finally, with simplification the phase angle is derived

$$\angle T(j\omega_c) = \tan^{-1}(\omega_c\tau_i) + \omega_c t_d - \pi \tag{6}$$

$$\angle T(j\omega_c) = -\pi + \phi \tag{7}$$

where ϕ denotes the phase margin. From (4) we can get the relationship among the time delay, the phase margin and the crossover frequency

$$\omega_c = \frac{\tan^{-1}(\omega_c\tau_i) - \phi}{t_d} \le \frac{\pi/2 - \phi}{t_d}. \tag{8}$$

Equation (8) points out that the control bandwidth of a digital system is limited by the total time delay in the system. The crossover frequency should be set below the limit to make the system stable. The loop gains of multisampled buck converters with 40° phase margin and different multisampling rate is compared in Fig. 4, where the system with higher sampling rate has higher control bandwidth. The bandwidth limitation in multi-sampled systems can be far beyond practical regulator settings. In fact, improper settings will cause the DVC that deteriorates the small-signal dynamic performance, which is not considered in the small-signal model. So, it is significant to investigate the model of DVC phenomenon.

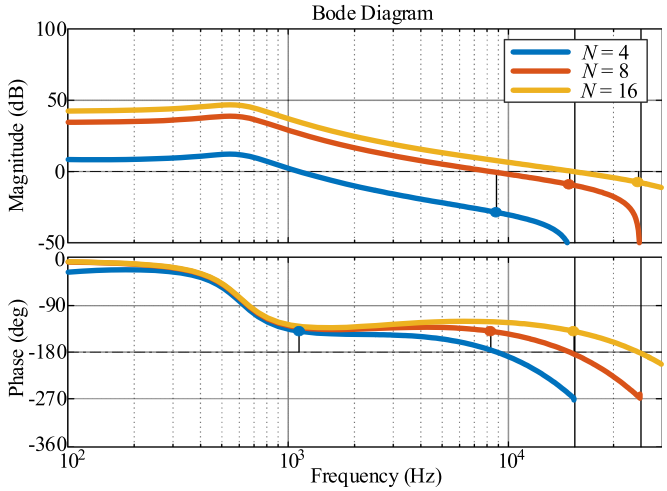

Fig. 4. Bode plots of loop gains in multisampled buck converters with the phase margin of 40° and different multi-sampling rates.

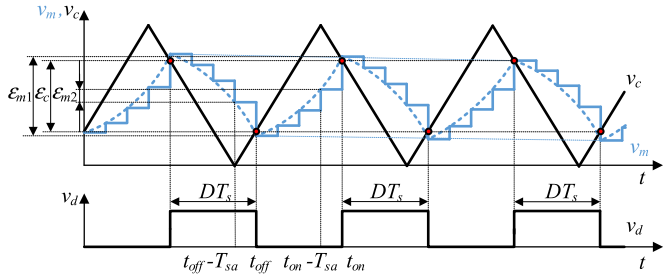

Fig. 5. Typical waveforms of the carrier signal v_c, the modulation signal v_m and the PWM signal v_d when the DVC happens and the perturbated modulation signal v_m is not able to change the pulsewidth. Definition and relationship of the DVC critical variables are noted: the carrier signal difference ε_c, the maximum modulation signal difference ε_{m1} and the minimum modulation signal difference ε_{m2}.

III. Accurate Modeling of Double Vertical Crossing

A. Effect of Double Vertical Crossing

Typical waveforms of the carrier and the modulation signal when the DVC happens are shown in Fig. 5, where the two crossing instants are named $t_{\rm on}$ and $t_{\rm off}$. A small perturbation in the modulation signal can only change the crossing point on the vertical segment of the modulation signal instead of the duty ratio. Hence, the small-signal gain is significantly reduced and the dynamic performance is deteriorated.

B. Accurate Condition of Double Vertical Crossing

The carrier signal value at each crossing instant, i.e., $t_{\rm on}$ or $t_{\rm off}$, lies within a range determined by the values of modulation signal before and after update. So, the condition of the DVC is presented in (9) and (10) with time domain expressions

$$v_m(t_{off}) \le v_c(t_{\rm off}) \le v_m(t_{\rm off} - T_{sa}) \tag{9}$$

$$v_m(t_{\rm on} - T_{sa}) \le v_c(t_{\rm on}) \le v_m(t_{\rm on}) \tag{10}$$

where T_{sa} denotes the sampling period. In order to reduce the amount of inequations, (9) and (10) can be rewritten into (11)

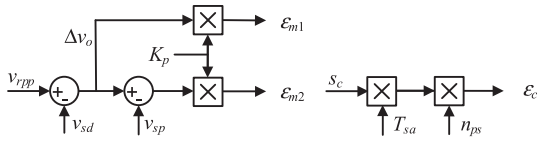

Fig. 6. Calculation principle of the carrier signal difference ε_c, the maximum modulation signal difference ε_{m1} and the minimum modulation signal difference ε_{m2}.

and (12) for simplification

$$v_c(t_{\text{on}}) - v_c(t_{\text{off}}) \le v_m(t_{\text{on}}) - v_m(t_{\text{off}}) \tag{11}$$

$$v_m(t_{\text{off}} - T_{sa}) - v_m(t_{\text{on}} - T_{sa}) \le v_c(t_{\text{on}}) - v_c(t_{\text{off}}). \tag{12}$$

Define the three differences as

$$\begin{cases} \varepsilon_c = v_c(t_{\text{on}}) - v_c(t_{\text{off}}) \\ \varepsilon_{m1} = v_m(t_{\text{on}}) - v_m(t_{\text{off}}) \\ \varepsilon_{m2} = v_m(t_{\text{on}} - T_{sa}) - v_m(t_{\text{off}} - T_{sa}) \end{cases} \tag{13}$$

the inequations can be united as

$$\varepsilon_m 2 \le \varepsilon_c \le \varepsilon_m 1. \tag{14}$$

These three differences defined in (13) are critical variables for describing the DVC phenomenon, and they are illustrated in Fig. 5, where ε_c, ε_{m1}, and ε_{m2} denote the carrier signal difference, the maximum modulation signal difference and the minimum modulation signal difference respectively. Therefore, as (14) indicates, the condition of DVC can be transformed to that the carrier signal difference is within the range of the maximum and the minimum modulation signal difference.

The calculation principle of the three variables is presented in Fig. 6, where v_{rpp} denotes the peak-to-peak value of the output voltage ripple, v_{sd} denotes the voltage difference during the sampling delay, v_{sp} denotes the voltage difference during the sampling period, s_c denotes the carrier signal slope, and n_{ps} denotes the amount of sampling periods with positive slope. Knowledge of the steady-state ripple in the output voltage is essential to derive ε_{m1} and ε_{m2}, and the amount of the sampling period with positive slope is crucial to derive ε_c.

The output voltage of buck converter consists of two parts, i.e., voltage on the filter capacitance v_{Cf} and voltage on the equivalent series resistance (ESR) v_{rC}. The ripple on ESR determines the peak-to-peak value of total ripple. Therefore, the maximum and the minimum modulation signal difference ε_{m1} and ε_{m2} are derived in (15) and (16). The integral part of the controller is neglected because the switching ripple component in the integral part is usually much smaller than the one in the proportional part. Detailed calculations are listed in (17)–(22), and the corresponding variables are shown in Fig. 7

$$\varepsilon_{m1} = K_p \Delta v_o \tag{15}$$

$$\varepsilon_{m2} = K_p(\Delta v_o - v_{sp}) \tag{16}$$

$$\Delta v_o = v_{rpp} - v_{sd} \tag{17}$$

$$v_{rpp} = \frac{T_s v_i D(1-D)}{L} \tag{18}$$

$$v_{sd} = \frac{t_{dd} v_i r_C}{L} + \frac{t_{dd} v_i N D(1-D)(T_s - t_{dd})}{2LC} \tag{19}$$

$$v_{sp} = \Delta v_{rC1} + \Delta v_{rC2} + \Delta v_{Cf1} + \Delta v_{Cf2} \tag{20}$$

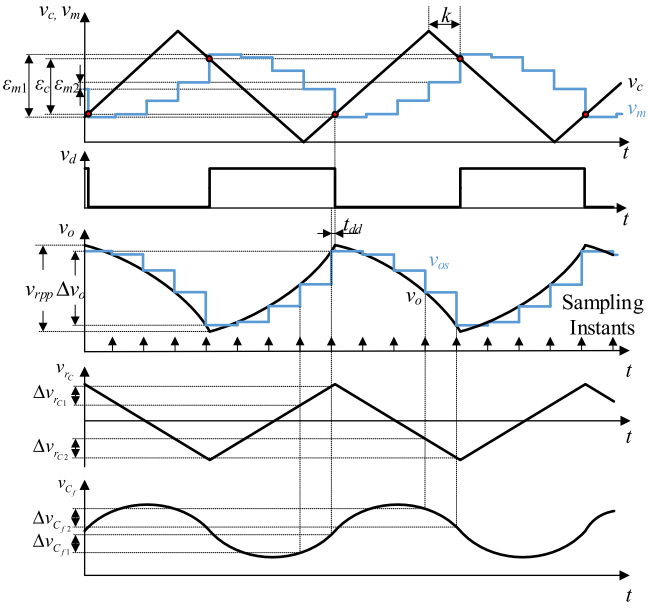

Fig. 7. Specification of the variables in the calculation details to derive ε_c, ε_{m1} and ε_{m2}: v_{rpp}, Δv_o, $\Delta v_{C_{f1}}$, $\Delta v_{C_{f2}}$, $\Delta v_{r_{C1}}$, $\Delta v_{r_{C2}}$, t_{dd}, and k.

$$\Delta v_{r_{C1}} + \Delta v_{r_{C2}} = \frac{T_s v_i r_C}{NL} \tag{21}$$

$$\Delta v_{C_{f1}} + \Delta v_{C_{f2}} = \frac{T_s v_i (1-D)}{2NLC}\left(DT_s - \frac{T_s}{N} - 2t_{dd}\right). \tag{22}$$

The carrier signal difference ε_c is derived in (23), where k denotes the amount of sampling periods between the moments when the carrier signal and the modulation signal reach their maximum values. The three components are corresponding to the variables in Fig. 6

$$\varepsilon_c = s_c \cdot T_{sa} \cdot n_{ps} \tag{23}$$

$$s_c = \frac{2}{T_s} \tag{24}$$

$$n_{ps} = N - DN - 2k. \tag{25}$$

It can be found from (14) that $\varepsilon_c = \varepsilon_{m1}$ and $\varepsilon_c = \varepsilon_{m2}$ are two boundaries for the occurrence of DVC, corresponding to two boundaries of proportional gain of regulator K_p, (26)–(27) shown at the bottom of the next page, where the range of k is

$$0 \le k \le \text{ceil}\left(\frac{N - DN}{2}\right) - 1, k \in \mathbb{N}. \tag{28}$$

The relationship between k and K_p is described by Fig. 8 where the blue areas on the horizontal axis stand for the range of K_p with occurrence of DVC. As the figure indicates, there could be multiple, discontinuous blue areas and the areas are matched with the values of k. In fact, k is not an independent variable. A larger K_p leads to a higher slope of the modulation signal, and thus the crossing point will be closer to the peaks and valleys of carrier signal, which enlarges carrier signal difference ε_c and eventually makes k smaller. Notice when $k = 0$, $\varepsilon_{m1} > 1$

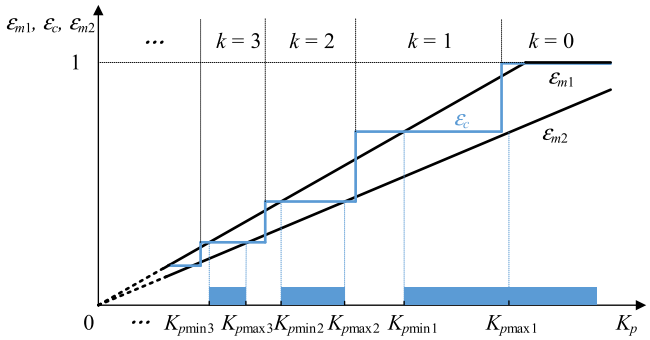

Fig. 8. Relationship among the amount of sample periods between the peak of carrier signal and the peak of modulation signal k, the differences ε_c, ε_{m1}, ε_{m2} and the proportional gain of regulator K_p.

and there will be overmodulation. So, the minimum value of K_p when $k = 0$ is not presented in the figure.

To sum up, the condition of DVC is decided by the multisampling factor N, the working point D, the proportional gain of the regulator K_p, the circuit parameters, and the digital delay t_{dd}. In other converter topologies and feedback variables, the condition of DVC in general presentation (14) and the derivation procedure would be still valid, though the relationship between the modulation signal and the feedback signal (15), (16) would be different. For example, in a voltage-controlled boost converter with inner current loop, the DVC condition should be derived with both the voltage ripple and the current ripple. A desired selection of K_p should be free of DVC under each duty ratio D, but there is no solution to such K_p. In conclusion, the DVC cannot be completely avoided by tuning the proportional gain of the regulator K_p.

IV. Proposed Elimination Approach of Double Vertical Crossing

A. Theoretical Basis

Since tuning the proportional gain of the regulator is not capable of avoiding the DVC, adjusting the carrier signal becomes a possible solution. The idea is originated from (14) where ε_{m1} and ε_{m2} can be modified by the proportional gain K_p, and thus adjusting the carrier signal is equivalent to modifying ε_c. As Fig. 9 indicates, when the carrier signal shifts to left or to right, the value of ε_c will decrease or increase. If the time shift of the carrier signal is defined as t_c and right-shifting as positive, the modified carrier signal difference $\varepsilon_c{}'$ could be presented as

$$\varepsilon'_c = \frac{2}{T_s} \cdot \left[\frac{T_s}{N}(N - DN - 2k) + 2t_c \right]. \tag{29}$$

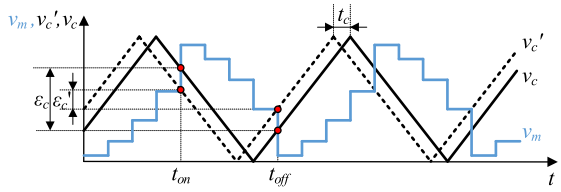

Fig. 9. Regulation of the carrier signal difference from ε_c to $\varepsilon_c{}'$ by adjusting the relative position between the carrier and the modulation signal. The time shift is defined as $t_c$and right-shifting as positive.

Therefore, the conditions of the DVC regarding to the proportional gain are represented as (30) and (31) shown at the bottom of the next page.

When the proportional gain K_p is determined based on the requirements of the system, the time shift of the carrier signal t_c can be adjusted to modify the condition of the DVC, and thus it will be avoided.

B. Principle of the Proposed Algorithm

According to the aforementioned analysis, the solution of t_c does exist, but its analytical expression will be complicated and its result is sensitive to the circuit parameters. So, an automatic adjusting algorithm needs to be designed. The sketch waveforms of the carrier signal and the modulation signal with the proposed approach are illustrated in Fig. 10.

In order to eliminate the DVC, the crossing point is controlled to be at the middle of modulation signal segment. First, the difference Δt from the crossing point t_{cross} to the reference point t_{ref} is measured each switching period. Then, the carrier adjusting magnitude Δv_c is calculated based on Δt. Finally, the carrier signal is set to Δv_c when it reaches zero. Therefore the relative position between carrier and modulation signal can be automatically adjusted to eliminate the DVC. The relationship between Δv_c and Δt is derived in (33), and thus a feedback loop described in (34) can be used to make the crossing point track the middle point. In the equations, t_{cross}, t_{ref}, T_s and Δt are integral multiplications of the digital controller clock cycle T_{clk}. Δv_c is the fixed-point representation of adjusting carrier phase, one LSB of Δv_c denotes $2/T_s$. When the crossing point loop gain K_c is carefully selected, Δt will finally converge to zero

$$\Delta t[n] = t_{\text{cross}}[n] - t_{\text{ref}} \tag{32}$$

$$t_{\text{cross}}[n+1] = t_{\text{cross}}[n] - \frac{T_s}{2}\Delta v_c[n] \tag{33}$$

$$\Delta v_c[n] = \frac{2K_c}{T_s}\Delta t[n]. \tag{34}$$

$$K_{p\max} = \frac{2L(N - DN - 2k)}{v_{\text{i}} T_s r_C \left[(ND - 1 - ND^2) - \frac{Nt_{dd}}{T_s} - \frac{D(1-D)}{2r_C C}\left(T_s - \frac{T_s}{N} - 2t_{dd}\right) \right]} \tag{26}$$

$$K_{p\min} = \frac{2L(N - DN - 2k)}{v_{\text{i}} \left[T_s r_C (ND - ND^2) - Nt_{dd}\left(r_C - \frac{ND(1-D)(T_s - t_{dd})}{2C} \right) \right]} \tag{27}$$

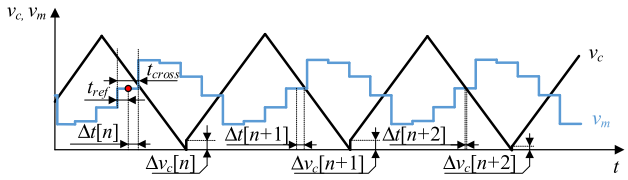

Fig. 10. Waveforms of the carrier and the modulation signal with the proposed adjusting algorithm.

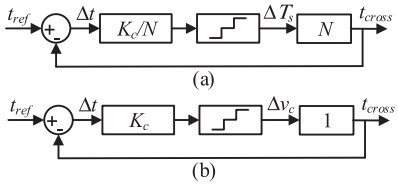

Fig. 11. Simplified control diagram to the crossing point of (a) existing method and (b) proposed method.

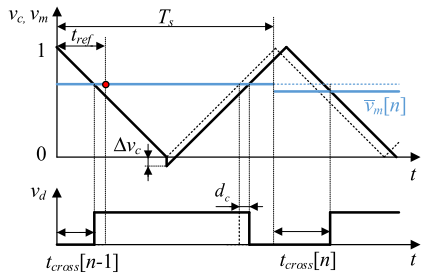

Fig. 12. Waveforms of the carrier signal v_c, the average value of the modulation signal $\bar{v}_m$ and the PWM signal v_d with the proposed algorithm.

The major improvement in the proposed method is the increase of control resolution. As the Fig. 11 indicates, the quantization is made with the production of Δt and K_c/N trimming the sampling interval in the existing method. While in proposed method, it is made with the production of Δt and K_c trimming the carrier phase. The increase in quantization error with multi-sampling factor N is avoided.

C. Parameter Design and Implementation

The design of the crossing point loop gain K_c is based on a simplified model using the proposed algorithm. As the control period of the algorithm is the switching cycle T_s, the model of the power stage is discretized with the same period. The dynamics of the proposed algorithm is illustrated in Fig. 12, where $\bar{v}_m$ denotes the average value of the modulation signal.

As Fig. 12 indicated, the adjustment on the carrier phase Δv_c is equivalent to an extra pulse width d_c in the PWM signal, and the variation in the modulation signal can cause variation in the crossing point t_{cross}. The coupling relationship can be derived in (35) and (36). Therefore, the control diagram of the proposed algorithm is illustrated in Fig. 13

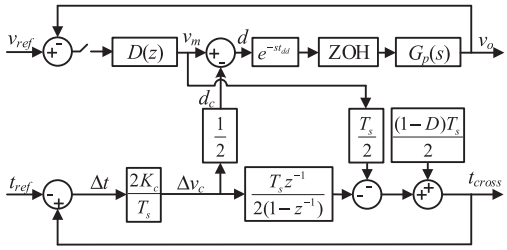

Fig. 13. Block diagram of the system model with the proposed carrier shifting algorithm considering the coupling with voltage control loop.

$$d_c = \frac{\Delta v_c}{2} \tag{35}$$

$$t_{\text{cross}}[n+1] = t_{\text{cross}}[n] - \frac{T_s}{2}\left(\Delta v_c[n] + \bar{v}_m[n+1] - \bar{v}_m[n]\right). \tag{36}$$

Finally, the loop gain of the system with the proposed algorithm T_{cp} is derived in (37) where T_p denotes the loop gain of the original voltage control for the power stage. The design of the crossing point loop gain K_c will be based on the system stability predicted by T_{cp}

$$T_{cp} = K_c\left[\frac{1}{z-1} + \frac{T_p}{2(1+T_p)}\right]. \tag{37}$$

In the stability analysis of the crossing point loop, the voltage loop will be discretized with the same interval. However, the original discretization interval of the voltage loop is the sampling interval T_{sa}, which is smaller and the one for the crossing point loop, i.e., the switching interval T_s. Thus, the larger discretization interval of the voltage loop introduces phase lag in the model. The phase lag will further restrict the control gain which makes the model conservative. So, the actual stability boundary is beyond the predicted one and the design is feasible.

The digital circuit diagram to implement the proposed algorithm is described by Fig. 14. First, detection of the crossing point is performed by a 16-b counter with a 16-b D-flip-flop (DFF). The value of counter is cleared when the AD conversion completes, so the maximum value of counter denotes the sampling cycle. The value of counter is preserved in the DFF at each falling edge of the PWM signal, and the preserved value denotes the crossing point t_{cross}. Then, the adjusting magnitude Δv_c is calculated through an adder, a multiplier, and a limiter. The adjusting magnitude is loaded to the carrier signal counter (CSC) each time when the value of the CSC equals to 0. Next, the

$$K_{p\max} = \frac{2L(N - DN - 2k + 2Nt_c)}{Nv_{\text{i}}r_C\left[T_sD(1-D) - (t_{dd} + T_{sa})\left(1 - \frac{2D(1-D)T_s - t_{dd} - T_{sa}}{2r_CC}\right)\right]} \tag{30}$$

$$K_{p\min} = \frac{2L(N - DN - 2k + 2Nt_c)}{Nv_{\text{i}}\left[T_sr_C(ND - ND^2) - t_{dd}\left(r_C - \frac{(2T_sD(1-D) - t_{dd})}{2C}\right)\right]}. \tag{31}$$

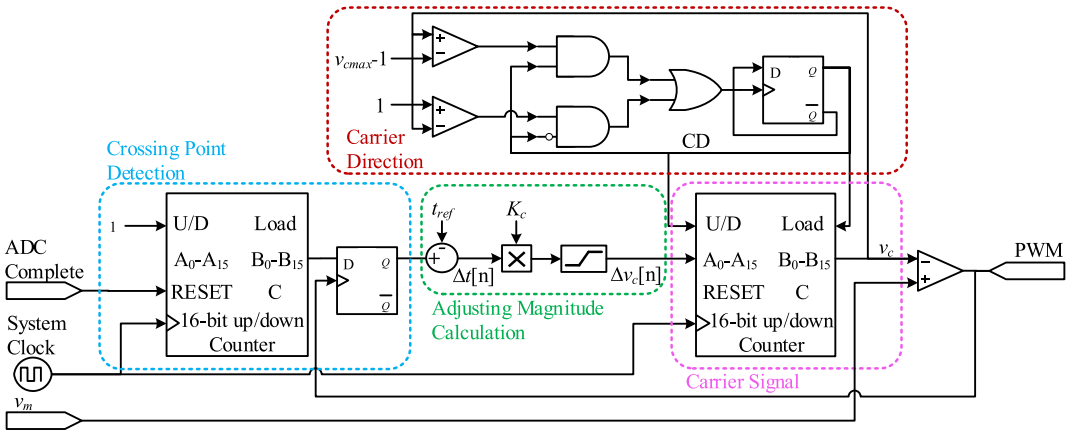

Fig. 14. Digital circuit diagram to implement the proposed algorithm.

TABLE I
PARAMETERS OF THE BUCK CONVERTER STUDIED

Description	Parameter	Value
Input Voltage	V_i	15V
Output Voltage	v_o	4.69V ~ 10.3V
Duty Ratio	D	0.3125 ~ 0.6875
Filter Capacitance	C_f	68μF
Serial Resistance	r_C	2.0Ω
Switching Frequency	f_s	12.5kHz
Multisampling Factor	N	16
System Clock Frequency	f_{clk}	250MHz
Digital Delay	t_{dd}	1μs

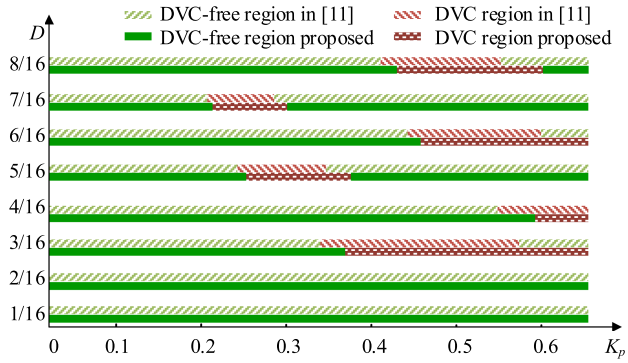

Fig. 15. DVC regions respecting to the proportional gain K_p and the working point D, predicted by the proposed model and the exiting one.

TABLE II
SIMULATION SETTINGS FOR THE DVC CONDITION VERIFICATION

Duty Ratio D	Proportional Gain K_p	Double Vertical Crossing Happens	
		Model in [11]	Proposed model
0.5	0.42	Yes	No
0.5	0.44	Yes	Yes
0.5	0.56	No	Yes
0.5	0.61	No	No

carrier signal is generated by the CSC, and the counting direction of the CSC is switched between increasing and decreasing when its value reaches the maximum value of carrier signal v_{cmax} or 0. Hence, the carrier direction is used to trigger the aforementioned loading of adjusting magnitude Δv_c. Finally, the PWM signal is generated from the comparison result of the carrier signal and the modulation signal.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The multisampled buck converter with parameters in Table I is established in PSIM 9.1. The output voltage is adjustable to demonstrate the DVC phenomenon in different working points. The input voltage is not adjustable because it is a factor that influence the condition of DVC. The serial resistance is larger than typical application to validate the proposed model and compensator. A 12-b DPWM and 10-b ADC is used in the converter. All of the digital signals are in fixed point numbers to simulate the reality.

In Fig. 15, the occurrence of the DVC under different working point D and values of K_p is specified. The settings that the DVC is avoided is illustrated in green, while the settings that DVC happens is illustrated in red. In addition, the proposed prediction result is compared with the result in [11]. As given in Table II, the regulator coefficients are carefully selected so that the two prediction results are different. When the proportional gain K_p is adjusted, the integral gain is adapted to keep the frequency of the pole constant. The simulation waveforms of the carrier and the modulation signal are illustrated in Fig. 16. The sampling is made every 5 μs from the beginning of simulation, while the modulation signal is updated 1μs after. Therefore, the peaks and valleys of the carrier signal are synchronized with the update of the modulation signal to simulate real-time sampling. The prediction made by the proposed model matches with the simulation result better than the traditional model.

It is important to notice that lower ADC resolution brings larger quantization error to the sampled data, which jeopardizes the accuracy of the DVC prediction, especially when the samples fall into the same ADC bin, the magnitude of DVC boundary will be much larger than the predicted one. The DVC boundaries under different ADC resolutions are tested in the simulation, and the results are given in Table III. The waveforms of the output

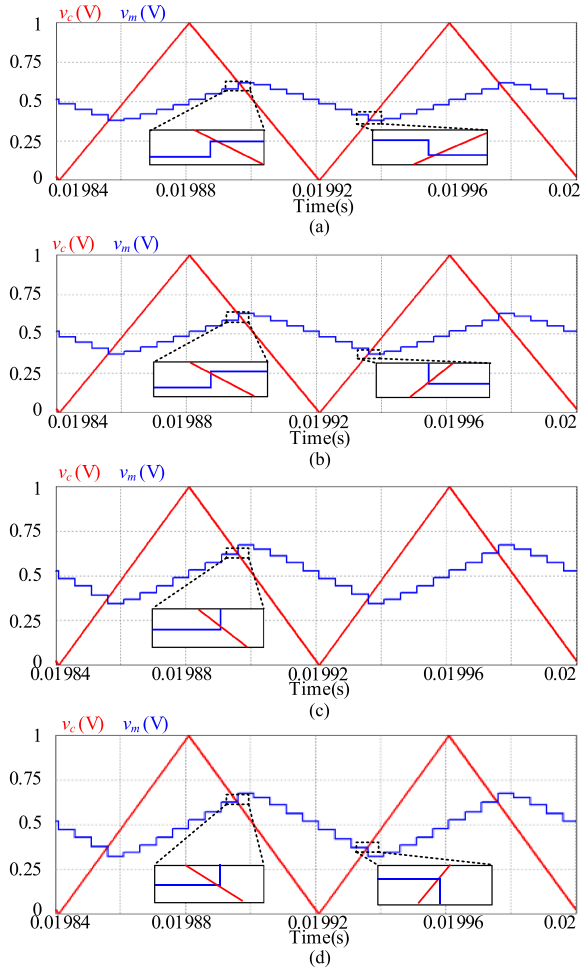

Fig. 16. Simulation waveforms of the carrier and the modulation signal in steady state at working point $D = 0.5$. (a) $K_p = 0.42$, DVC does not happen. (b) $K_p = 0.44$, DVC happens. (c) $K_p = 0.55$, DVC happens. (d) $K_p = 0.61$, DVC does not happen.

TABLE III
SIMULATION RESULTS OF THE DVC BOUNDARIES UNDER DIFFERENT ADC RESOLUTIONS AT $D = 0.5$

ADC Resolution Bits	DVC Boundary
16	[0.44,0.58]
10	[0.44,0.59]
8	[0.48,0.61]
6	[0.37,0.60]

voltage v_o and its sampled value v_{os} are presented in Fig. 17 to highlight how the ADC resolutions influence the sampled data.

Then, the design principle of the crossing point loop gain K_c and effectiveness of the proposed DVC elimination method are investigated, and the system stability boundary of K_c is presented in Table IV with respect to different voltage regulator proportional gain K_p.

The crossing point loop gain K_c is set as 1.26 to demonstrate the validity of the design principle. The simulation verification is performed with the working point $D = 0.3125$ and the reference point $t_{\text{ref}} = 625$. The crossing point t_{cross} is observed in situations that (a) $K_p = 0.3$ without the proposed algorithm, (b) $K_p = 0.3$ with the proposed algorithm, and (c) $K_p = 0.35$ with the proposed algorithm. The simulation results are presented in Fig. 18. The DVC happens in Fig. 18(a) because the proposed algorithm is not adopted, and thus the crossing point t_{cross} will be close to either 0 or the maximum value of the crossing time detection counter. When the proposed algorithm is adopted and the gain K_c is within the stability boundary predicted in Table IV, i.e., 1.27, the crossing point follows the reference point, which indicates that the system is stable and the DVC is eliminated. In Fig. 16(c), the gain K_c is beyond the stability boundary predicted in Table IV, i.e., 1.15, and there is an oscillation in the waveform of the crossing point t_{cross}, showing the system is unstable. Therefore, the stability boundary predicted by the presented simplified model coincide with the simulation result, and the proposed design approach of the gain K_c is validated.

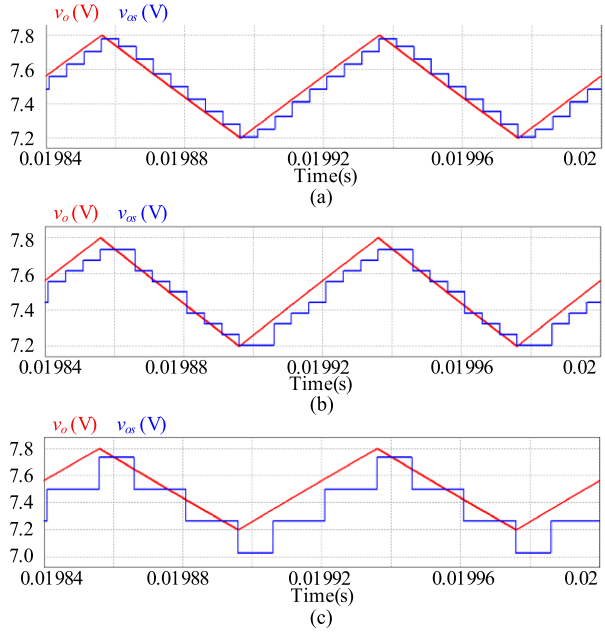

Fig. 17. Simulation waveforms of the output voltage v_o and its sampled value v_{os} at $D = 0.5$ when the sampling resolution is (a) 10 b, (b) 8 b, and (c) 6 b, respectively.

TABLE IV
SYSTEM STABILITY BOUNDARY WITH CONTROL PARAMETER K_c

Voltage Regulator Gain K_p	Stability Boundary of K_c
0.25	1.40
0.3	1.27
0.35	1.15
0.4	1.03
0.45	0.91
0.5	0.80

B. Experimental Results

A buck converter controlled by a MAX 10M40 FPGA is built to validate the theoretical analysis. The converter setup is shown in Fig. 19, where an external A/D converter is embedded in the FPGA-based control board, with other setups including the power supplies, the filter, the driver and the load.

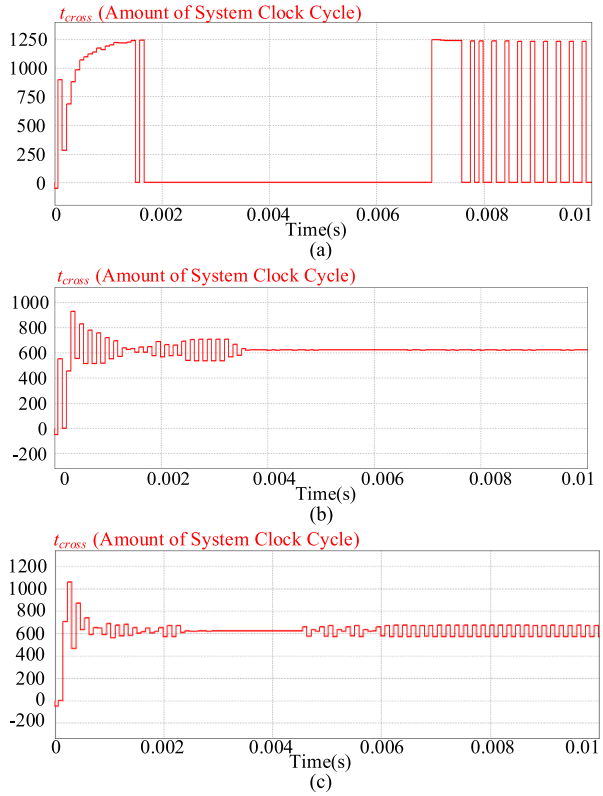

Fig. 18. Simulation waveforms of the crossing point t_{cross} under different situations. (a) $K_p = 0.3$, without the proposed algorithm, DVC happens, t_{cross} unstable. (b) $K_p = 0.3$, $K_c = 1.26$, with the proposed algorithm, t_{cross} stable. (c) $K_p = 0.35$, $K_c = 1.26$, with the proposed algorithm, t_{cross} unstable.

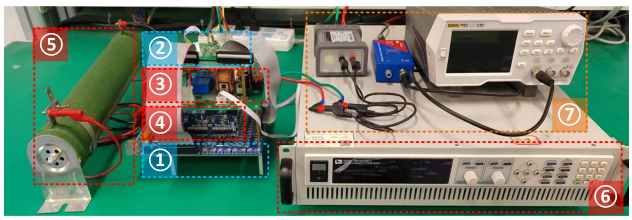

Fig. 19. Photograph of the experimental setup: ① FPGA-based control board, ② filter, ③ power stage, ④ driver, ⑤ resistive load, ⑥ dc voltage source, and ⑦ perturbation source with injector.

First, the load transient performance of the proposed approach is compared with the original multisampling method, the filter-based approaches using SRF, FRF [19], and the sampling frequency adjusting approach (SFA) [12]. The analytical presentation of the digital filters are shown in (38), (39), and the comparison of the loop gains in bode plot with phase margins are shown in Fig. 20. The loop gain of the proposed approach is derived regarding the control diagram in Fig. 13, showing the proposed approach is equivalent to adding an extra pair of low frequency zero and pole. The SRF suffers 40° of phase margin penalty. The waveforms of the output voltage v_o under these five methods with a load step from 0.7 to 1.4 A are shown in Fig. 21. It can be observed that the responses appear to be similar under the original, the FRF approach, the SFA approach, and the proposed approach. But the response of SRF approach is much slower than the former approaches. The reason is that the duty

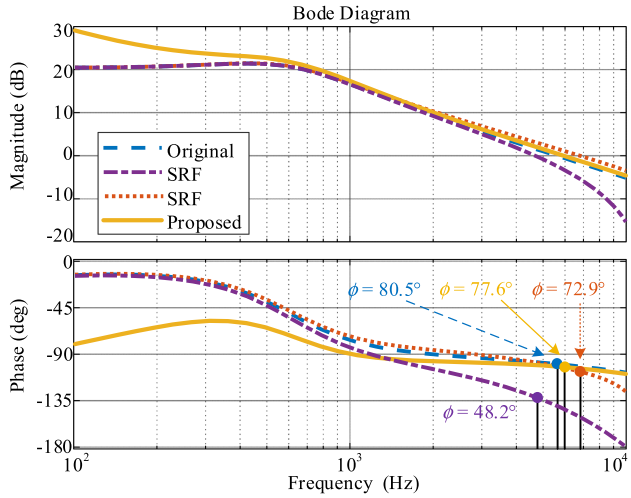

Fig. 20. The bode diagram of the loop gains of the proposed approach, the original multisampling, the SRF, and the FRF.

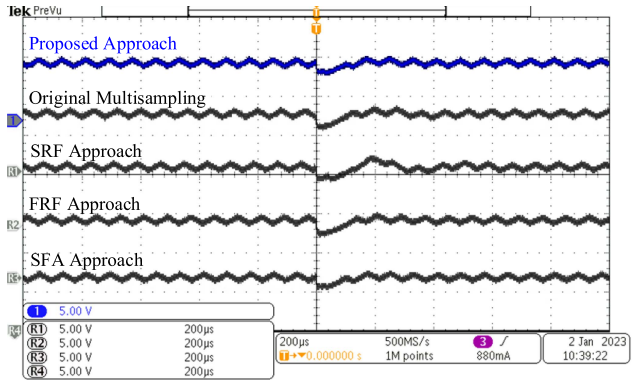

Fig. 21. Experimental waveforms of output voltage v_o with proposed approach (CH1), the original multisampling method (CHR1), filter-based approach using SRF (CHR2), FRF (CHR3), and SFA (CHR4) when load step from 0.7 to 1.4 A. Time: 200μs/div; CH1: 5 V/div, output voltage v_o.

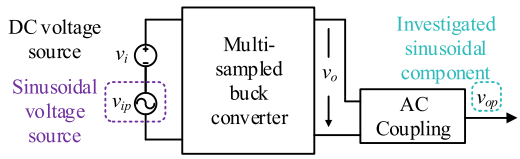

Fig. 22. Circuit diagram of the experiment setup for demonstrating the DVC phenomenon.

ratio is significantly changed during the transient and the DVC is not the critical factor to the response. Instead, the additional phase loss from SRF jeopardized the load transient performance

$$F_{\text{SRF}}(z) = \frac{1 - z^{-N/2}}{2} \tag{38}$$

$$F_{\text{FRF}}(z) = 1.5\frac{1 - z^{-N} + \frac{1}{N}\sum_{n=1}^{N} z^{-n}}{1.5 - z^{-N} + \frac{1}{N}\sum_{n=1}^{N} z^{-n}}. \tag{39}$$

Since it is hard to observe the modulation signal and the carrier signal in the experiment, a sinusoidal voltage source v_{ip} is connected in series with the original dc voltage as Fig. 22 have shown, to demonstrate the deterioration of the control loop due

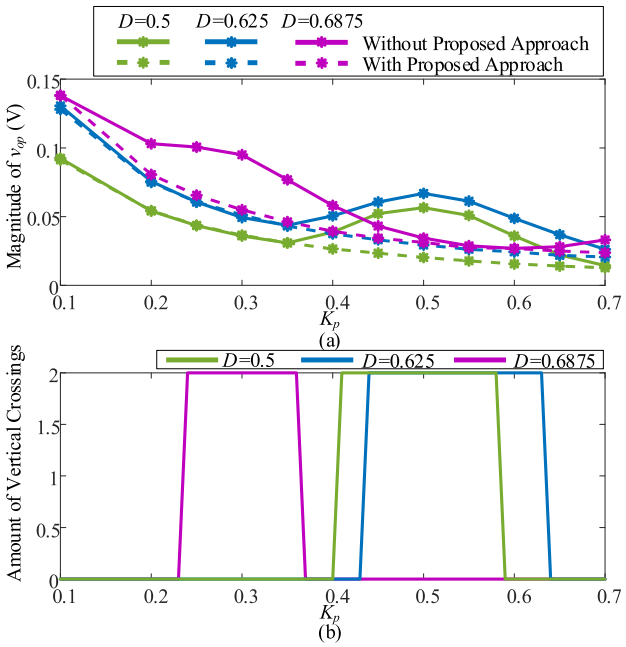

Fig. 23. Experimental test results. (a) Magnitude of the 1 kHz component in the output voltage v_{op} with or without the proposed elimination approach. (b) Estimation on the occurrence of the DVC.

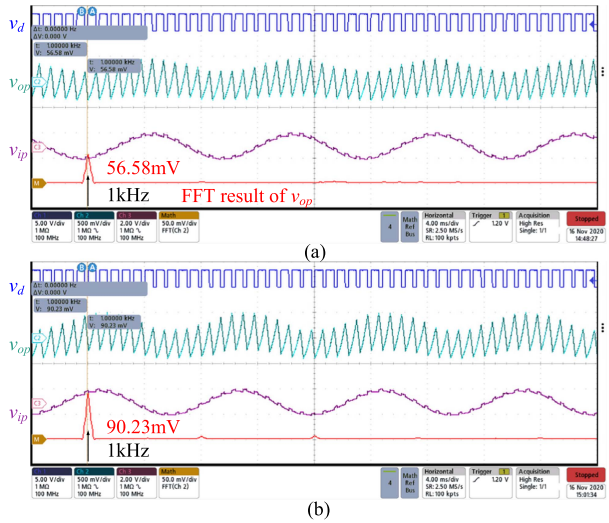

Fig. 24. Experimental waveforms when $K_p = 0.3$, $D = 0.6875$ (a) with and (b) without proposed algorithm: CH1, DC 5 V/div, PWM signal v_d; CH2, AC 500 mV/div, output voltage perturbation v_{op}; CH3, AC 2 V/div, input voltage perturbation v_{ip}; Math, 50 mV/div, FFT result of v_{op}.

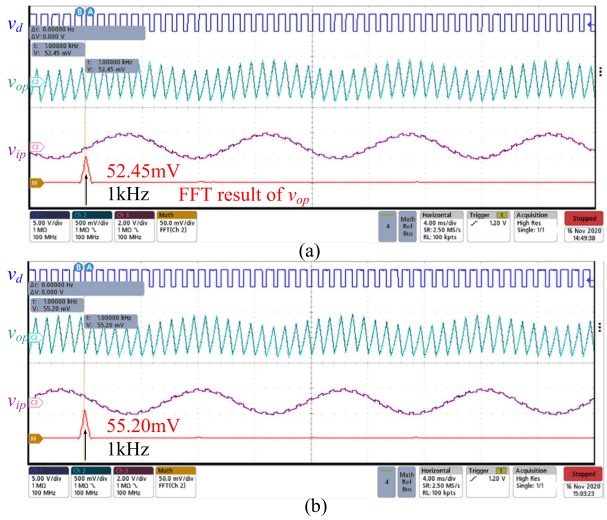

Fig. 25. Experimental waveforms when $K_p = 0.3$, $D = 0.625$ (a) with and (b) without proposed algorithm: CH1, DC 5 V/div, PWM signal v_d; CH2, AC 500 mV/div, output voltage perturbation v_{op}; CH3, AC 2 V/div, input voltage perturbation v_{ip}; Math, 50mV/div, FFT result of v_{op}.

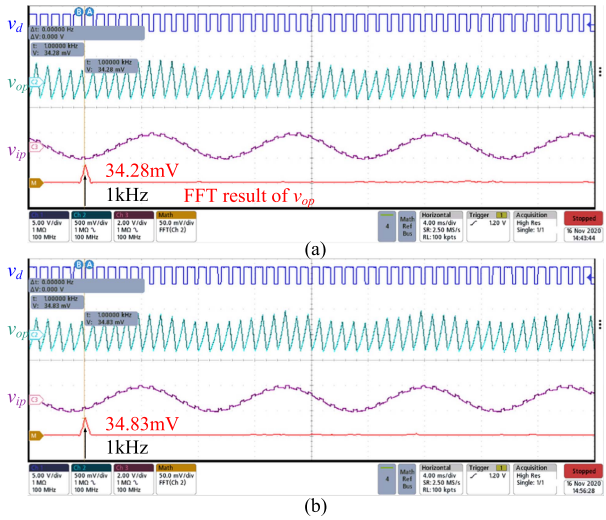

Fig. 26. Experimental waveforms when $K_p = 0.55$, $D = 0.6875$ (a) with and (b) without proposed algorithm: CH1, DC 5 V/div, PWM signal v_d; CH2, AC 500 mV/div, output voltage perturbation v_{op}; CH3, AC 2 V/div, input voltage perturbation v_{ip}; Math, 50 mV/div, FFT result of v_{op}.

to the occurrence of DVC. The frequency of v_{ip} is 1 kHz and its magnitude is 1.2 V. Thus, the magnitude of 1 kHz component of the output voltage v_{op} is investigated when the proportional gain K_p changes from 0.1 to 0.7. If the DVC does not happen, the magnitude will decrease as the regulator proportional gain K_p increases. However, if the DVC happens, the performance of closed-loop regulation will be deteriorated and the magnitude will increase with increase of K_p.

The magnitudes of the 1 kHz component in the output voltage v_{op} are measured with the variation of the proportional gain K_p at different working points, and the results are presented in Fig. 23(a). The estimation on the occurrence of the DVC is originated from the theoretical results in Fig. 15, and it is presented in Fig. 23(b) as the number of vertical crossings n_{vc}. The influence of DVC is obvious, for there is a clear rising in the solid line denoting the magnitude of v_{op} when the estimation of n_{vc} equals to 2. Hence, the experiment results confirm the theoretical prediction by the proposed model of DVC.

Moreover, the results using the proposed elimination algorithm is compared with the results without the algorithm in Fig. 23(a). The rising of v_{op} is avoided when the proposed algorithm is introduced. Detailed waveforms are demonstrated in figures from Figs. 24–27, where the waveforms of v_{op} and the FFT result of v_{op} are compared under four sets of different K_p and D. In cases where DVC is predicted to happen, i.e., as shown in Figs. 21 and 24, the FFT result of v_{op} with the proposed

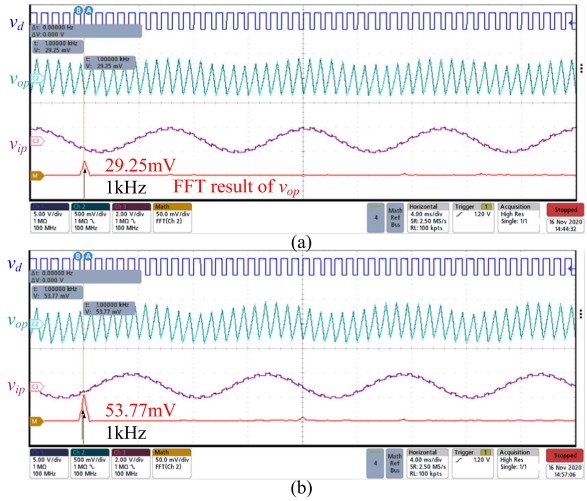

Fig. 27. Experimental waveforms when $K_p = 0.55$, $D = 0.625$ (a) with and (b) without proposed algorithm: CH1, DC 5 V/div, PWM signal v_d; CH2, AC 500 mV/div, output voltage perturbation v_{op}; CH3, AC 2 V/div, input voltage perturbation v_{ip}; Math, 50 mV/div, FFT result of v_{op}.

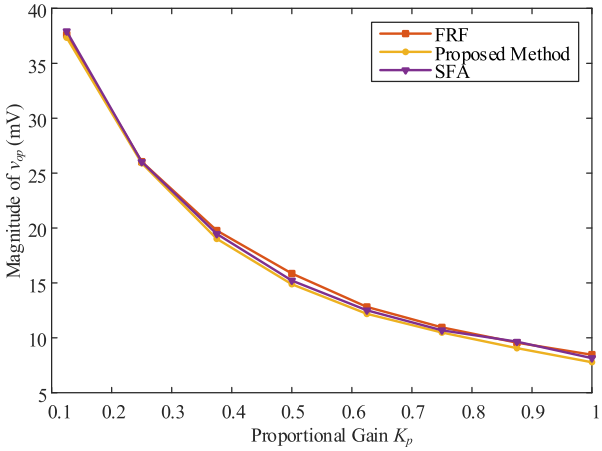

Fig. 28. Experimental test results of the magnitude of the 1 kHz component in the output voltage v_{op} with the proposed approach, the SFA approach, and the FRF approach.

algorithm is smaller than that without the proposed algorithm. In cases where DVC is predicted to not happen, the FFT result of v_{op} with the proposed algorithm is nearly the same with that without the proposed algorithm. The comparison proved that the proposed algorithm can eliminate DVC without introducing extra problems.

Finally, the audio susceptibility at 1 kHz is experimentally tested with the proposed approach, the SFA approach, and the FRF approach to demonstrate their differences. Comparing with the SFA approach, the proposed approach improved the control resolution. As indicated in Fig. 20, the proposed method introduced a pair of zero and pole at low frequency, making the magnitude at 1 kHz higher than the FRF approach. So, the audio susceptibility at 1 kHz of proposed approach is expected to be lower than both of the existing approaches. The test setup is the same as Fig. 22 at steady state duty cycle $D = 0.5$ with 0.1 V-1 kHz perturbation. The test results are presented in Fig. 28, where the proposed method has the best performance. The experimental results validate the theoretical analysis.

VI. Conclusion

This article investigates the phenomenon in multisampled digital-controlled buck converters where the carrier signal and the modulation signal have double vertical crossing in a switching period. First, an accurate model of the DVC phenomenon is derived with geometric approach. The accuracy is enhanced by taking the sampling delay and the filter capacitance into the model. Then, a carrier-adjusting algorithm is proposed to eliminate the DVC phenomenon on the basis of the model previously derived. The proposed method has better dynamic performance than existing methods. Moreover, the proposed method is more preferable because the quantization error is not influenced by the multisampling factor. Finally, the proposed model and elimination approach are validated by simulation and experimental results.

References

[1] H. Fujita, "A single-phase active filter using an H-bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934–941, Apr. 2009.

[2] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4212–4228, Sep./Oct. 2015.

[3] M. Lakka, E. Koutroulis, and A. Dollas, "Development of an FPGA-based SPWM generator for high switching frequency DC/AC inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 356–365, Jan. 2014.

[4] J. Böcker and O. Buchholz, "Can oversampling improve the dynamics of PWM controls?," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2013, pp. 1818–1824.

[5] L. Corradini and P. Mattavelli, "Modeling of multisampled pulse width modulators for digitally controlled DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1839–1847, Jul. 2008.

[6] H. Tian, Y. W. Li, and Q. Zhao, "Multi-rate modeling for low switching frequency VSCs applying multi-sampling control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 5339–5346.

[7] A. K. Singha, S. Kapat, S. Banerjee, and J. Pal, "Nonlinear analysis of discretization effects in a digital current mode controlled boost converter," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 3, pp. 336–344, Sep. 2015.

[8] M. He, J. Xu, Z. Zhou, N. Chen, and G. Zhou, "Digital peak voltage control of buck converter with multi-sample technique," in *Proc. Int. Conf. Commun., Circuits Syst.*, 2007, pp. 1274–1277.

[9] R. Vasconselos and M. Martins, "A hybrid digital control method for synchronous buck converters using multisampled linear PID and V2constant on-time controllers," in *Proc. Braz. Power Electron. Conf.*, 2017, pp. 1–6.

[10] L. Corradini and P. Mattavelli, "Analysis of multiple sampling technique for digitally controlled DC–DC switching converters," in *Proc. 37th IEEE Power Electron. Specialists Conf.*, 2006, pp. 1–6.

[11] L. Corradini, E. Tedeschi, and P. Mattavelli, "Advantages of the symmetric-on time modulator in multiple-sampled digitally controlled DC-DC converters," in *Proc. IEEE Power Electron. Specialists Conf.*, 2007, pp. 1974–1980.

[12] L. Corradini, P. Mattavelli, and S. Saggini, "Elimination of sampling-induced dead bands in multiple-sampled pulse width modulators for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2661–2665, Nov. 2009.

[13] C. Zhou, H.-.. Jiang, and F. Xie, "Control research of NPC three level high-power grid connected inverter based on multi sampling," in *Proc. IEEE 13th Conf. Ind. Electron. Appl.*, 2018, pp. 1386–1389.

[14] J. Kong, J. Lian, Z. Qiu, and G. Chen, "High digitalized resolution and low switching loss for high power electronics converters based on multi-sampling technology," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2009, pp. 2032–2036.

[15] M. Ito, R. Fujiwara, and T. Yokoyama, "3MHz multi sampling dead-beat control of single phase PWM inverter using FPGA based hardware controller," in *Proc. IEEE 2nd Int. Future Energy Electron. Conf.*, 2015, pp. 1–6.

[16] X. Zhang and J. W. Spencer, "Study of multisampled multilevel inverters to improve control performance," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4409–4416, Nov. 2012.

[17] X. Zhang, P. Chen, C. Yu, F. Li, H. T. Do, and R. Cao, "Study of a current control strategy based on multisampling for high-power grid connected inverters with an LCL filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5023–5034, Jul. 2017.
[18] T. B. Lazzarin and I. Barbi, "DSP-based control for parallelism of three phase voltage source inverter," *IEEE Trans. Ind. Inf.*, vol. 9, no. 2, pp. 749–759, May 2013.
[19] L. Corradini, W. Stefanutti, and P. Mattavelli, "Analysis of multisampled current control for active filters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1785–1794, Nov./Dec. 2008.
[20] S. Shang, M. Yang, D. Xu, P. Wang, Z. Lyu, and L. Li, "Enhanced bandwidth of current loop for permanent magnet synchronous motor drives based on FPGA," in *Proc. 21st Int. Conf. Elect. Mach. Syst.*, 2018, pp. 1291–1294.
[21] L. Rovere, A. Formentini, and P. Zanchetta, "FPGA implementation of a novel oversampling deadbeat controller for PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3731–3741, May 2019.
[22] Z. Zhou, J. Wang, Z. Liu, and J. Liu, "Accurate prediction of vertical crossings for multi-sampled digital-controlled buck converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 292–298.
[23] I. Z. Petric, P. Mattavelli, and S. Buso, "A jitter amplification phenomenon in multisampled digital control of power converters," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8685–8695, Aug. 2021.
[24] I. Z. Petric, P. Mattavelli, and S. Buso, "Feedback noise propagation in multisampled DC–DC power electronic converters," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 150–161, Jan. 2022.
[25] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Aliasing suppression of multisampled current-controlled LCL-filtered inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2411–2423, Apr. 2022.
[26] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Line voltage sensorless control of grid-connected inverters using multisampling," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4792–4803, Apr. 2022.
[27] I. Z. Petric, P. Mattavelli, and S. Buso, "Investigation of nonlinearities introduced by multi-sampled pulsewidth modulators," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2538–2550, Mar. 2022.

Zhengyuan Zhou (Student Member, IEEE) received the B.S. degree in electrical engineering in 2018 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in power electronics.

His current research interests include modeling and digital control of power converters.

Zeng Liu (Senior Member, IEEE) received the B.S. degree from Hunan University, Changsha, China, and the M.S. and Ph.D. degrees from Xi'an Jiaotong University (XJTU), Xi'an, China, in 2006, 2009, and 2013, respectively, all in electrical engineering.

He was a Faculty Member in electrical engineering with XJTU, where he is currently an Associate Professor. From 2015 to 2017, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. His research interests include control and stability of power electronics systems with multiple converters for renewable energy and energy storage applications.

Dr. Liu was the recipient of two Prize Paper Awards in IEEE TRANSACTIONS ON POWER ELECTRONICS. He is currently an Associate Editor for the IEEE OPEN JOURNAL OF POWER ELECTRONICS and on the Editorial Board for the ENERGIES, and served as Secretary-General for *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems* and *2020 The 4th International Conference on HVDC*.

Lulu Guo received the B.S. degree in electrical engineering in 2020 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include modeling and control of grid-connected converters in microgrid systems.

Jike Wang received the B.S. degree from Dalian Maritime University, Dalian, China, and the M.S. degrees from Xi'an Jiaotong University, Xi'an, China, in 2018 and 2021, respectively, both in electrical engineering.

Since 2022, he has been an Embedded Software Engineer with the TBEA Xi'an Electric Technology Co., LTD, Xi'an, China. His research interests include energy storage applications and solid-state transformers.

Jinjun Liu (Fellow) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University (XJTU), Xi'an, China, in 1992 and 1997, respectively.

He was a Faculty with Electrical Engineering School, XJTU. From late 1999 to early 2002, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. In late 2002, he was promoted to a Full Professor and then the Head of the Power Electronics and Renewable Energy Center at XJTU, which now comprises more than 20 faculty members and more than 200 graduate students and carries one of the leading power electronics programs in China. From 2005 to early 2010, he was an Associate Dean with the Electrical Engineering School, XJTU, and from 2009 to early 2015, the Dean for Undergraduate Education of XJTU. He is currently a Distinguished Professor of power electronics with XJTU. He coauthored 3 books (including one textbook), published more than 500 technical papers in peer-reviewed journals and conference proceedings, holds more than 70 invention patents (China/US/EU), and delivered for many times plenary keynote speeches and tutorials at IEEE conferences or China national conferences. His research interests include modeling, control, and design methods for power converters and electronified power systems, power quality control and utility applications of power electronics, and micro-grids for sustainable energy and distributed generation.

Dr. Liu was the recipient for many times governmental awards at national level or provincial/ministerial level for scientific research/teaching achievements. He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, the 2016 State Council Special Subsidy Award, the IEEE Transactions on Power Electronics 2016 and 2021 Prize Paper Awards, the Nomination Award for the Grand Prize of 2020 Bao Steel Outstanding Teacher Award, and the 2022 Fok Ying Tung Education and Teaching Award. He was with the IEEE Power Electronics Society Region 10 Liaison and then China Liaison for 10 years, an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS since 2006, 2015–2019 , the Executive Vice President and 2020-2021 Vice President of IEEE PELS. He was on the Board of China Electrotechnical Society 2012-2020 and was elected the Vice President in 2013 and the Secretary General in 2018 of the CES Power Electronics Society. He was 2013–2021 Vice President for International Affairs, China Power Supply Society, and since 2016, the inaugural Editor-in-Chief for *CPSS Transactions on Power Electronics and Applications*. He was elected the President of CPSS in Nov. 2021. Since 2013, he has been the Vice Chair of the Chinese National Steering Committee for College Electric Power Engineering Programs.