A Secondary-Side Phase-Shifted Bidirectional Soft-Switching DC–DC Converter Employing Step Voltage Switching for Eliminating Device Voltage Overshoot

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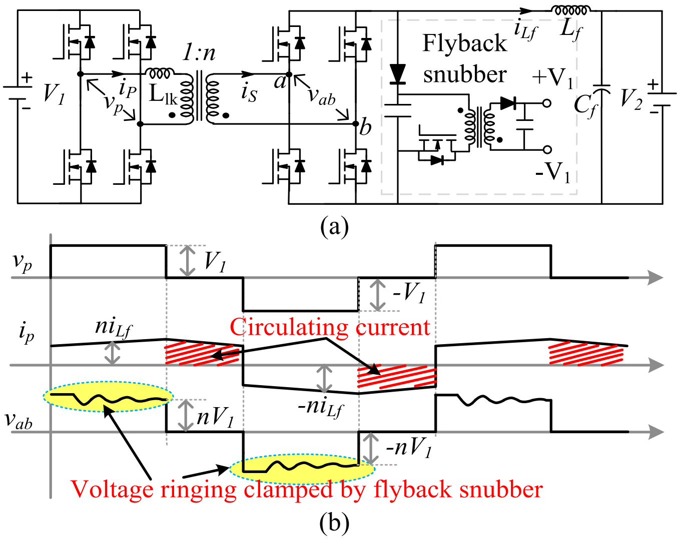
***Abstract*—In this article, we present a modulation strategy for bidirectional power flow for the step voltage switched (SVS) secondary-side phase-shifted (SPS) dc–dc converter that eliminates the device voltage overshoot problem. The voltage overshoot problem arises due to the resonance between the transformer leakage inductance and the output capacitance of the current-fed side metal–oxide–semiconductor field-effect transistor of the converter. Many snubber/clamp circuits were discussed in the literature to suppress this voltage overshoot. However, the power loss in these clamp circuits will affect the converter's efficiency. The bidirectional SVS SPS dc–dc converter presented in this article eliminates the voltage overshoot problem instead of suppressing it and, therefore, nullifies the need for a voltage clamp circuit. And most of all switching devices undergo soft-switching (either zero voltage switching or zero current switching). These factors result in achieving a peak efficiency of 96%. The proposed topology is tested for 1.7 kW at 100 kHz switching frequency with voltage-fed side voltage being 72 V and current-fed side voltage of 400 V. The results obtained prove the feasibility of the proposed work.**

***Index Terms*—Bidirectional, MOSFET's output capacitance, phase-shift full-bridge (PSFB) converters, voltage overshoot, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

ISOLATED bidirectional dc–dc converters are extensively employed in renewable energy systems. These are primarily used to control the power flow between renewable sources, such as photovoltaics, windmills, and many more, and the voltage bus connected to the energy storing elements, such as a battery or supercapacitor. Isolation provides flexibility and safety to the converter. Therefore, the research on isolated bidirectional topologies has increased over the past decade. Among them, full-bridge isolated topologies are immensely used in fuel cells, renewable generating systems, and electric vehicle charging systems [1], [2], [3], [4], [5], [6].



(a)

(b)

Fig. 1. (a) Bidirectional full-bridge DC–DC converter operated with PPS modulation [10] and (b) its key waveforms.

A. Full-Bridge Isolated Bidirectional DC–DC Topologies

Among full-bridge topologies, double full-bridge topologies comprising a current-fed bridge and voltage-fed bridge are implemented in [5], [6], [7], [9], and [11]. The bidirectional full-bridge dc–dc converter presented in [10] and its key waveforms are shown in Fig. 1. This converter operates with primary-side phase-shift (PPS) modulation. It has a simple structure and control; however, it has the following limitations: huge circulating current flow and associated power loss [12], the snubber/clamp circuit requirement to protect the current-fed side MOSFETs from the voltage overshoot, and limited zero voltage switching (ZVS) range at light load conditions [13].

A dual active full-bridge bidirectional isolated dc–dc converter is presented in [2]. This converter has the advantages of soft switching in both the bridges and the absence of the voltage overshoot problem. However, as leakage inductance is a crucial element in energy transfer, it has to be controlled very well; thus, manufacturing the converter in bulk is very difficult [7]. It also has the limitations of high circulating

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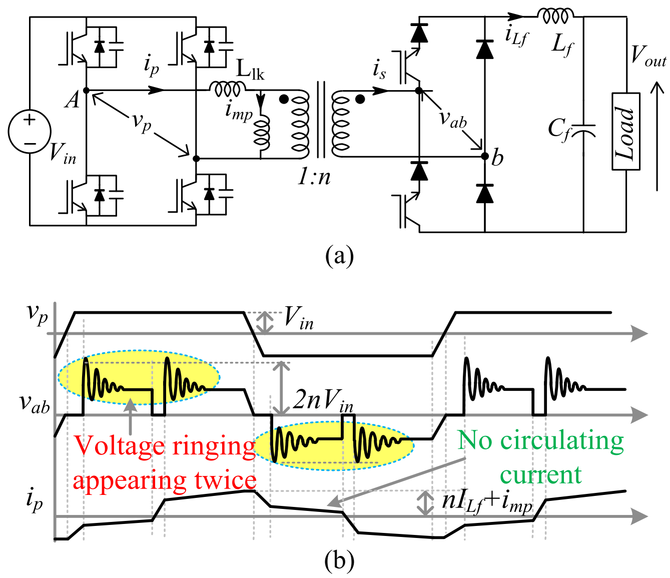


Fig. 2. (a) Unidirectional SPS PWM DC–DC converter [12] and (b) its key waveforms.

conduction losses that significantly affect the efficiency [7]. During the circuit operation, the imminent reactive power flow increases the converter loss and current stress on the switching devices [8].

The circulating current problem in PPS modulated full-bridge converters is addressed by the secondary-side phase-shift (SPS) modulation presented in [12], [14], [15], and [16], and many advanced primary- and secondary-side modulation techniques have taken care of the ZVS range at light load conditions [12], [14], [15], [16], [17].

B. Secondary-Side Phase-Shift Modulated Converters

A unidirectional SPS pulsewidth modulation (PWM) dc–dc converter, presented in [12], and its fundamental waveforms are shown in Fig. 2. From the waveforms, it can be seen that the circulating current is absent in the SPS-modulated full-bridge converters. In addition to the absence of circulating current, soft switching of all the devices would be achieved at all load conditions using the SPS modulation strategy. This modulation strategy can also be implemented in the bidirectional full-bridge converters. For example, it is applied for an IGBT-based isolated bidirectional ac–dc converter by Norrga in [14]. Even though the SPS modulation addresses the circulating current problem, the problem of voltage overshoot still exists in the converter. It appears twice [15] in each switching half-cycle, as shown in Fig. 2. The magnitude of this voltage overshoot is two times the ideal blocking voltage. It will be even more if the reverse recovery of the body diode of the MOSFET is considered [16].

A simple approach to protect the current-fed side MOSFETs from this voltage overshoot is to use a clamp circuit. Many dissipative and regenerative clamp circuits are reported in the literature to suppress the voltage overshoot across the current-fed devices [5], [7], [9], [10], [11], [12], [14], [15], [17], [18], [19], [20], [21], [22], [23], [24]. Apart from using a clamp circuit to suppress the voltage overshoot, some authors have proposed modulation strategies to reduce the magnitude of this voltage overshoot [25], [26], [27], [28], [29], [30]. However, the reduction in the overshoot is not significant, and few of them used a small clamp circuit as backup protection. There will be considerable loss in these clamp circuits when operated at higher voltage levels, whether they are regenerative or dissipative. Hence, there is a need to find a solution for eliminating the voltage overshoot instead of suppressing it such that the need for the voltage clamp would be nullified and the power loss associated with it is eliminated, thus improving efficiency. It also helps in implementing low rating (less expensive) devices on the current-fed side devices and makes transformer design flexible because the effect of leakage inductance on voltage overshoot has already been nullified. A topological solution is provided in [16] to eliminate the voltage overshoot problem in SPS modulation-based dc–ac converter.

C. Three-Legged SPS-Modulated DC–AC Converter That Eliminates the Voltage Overshoot Problem

The basic idea behind the voltage overshoot elimination in this converter is to apply the voltage v_{ab} in two steps with a definite time interval between them instead of applying it in a single step. Hence, it can be called a step voltage switched (SVS) dc–ac converter. This SVS can be achieved by an extra switching leg on the voltage-fed side and splitting the high-frequency transformer $(1{:}\ n)$ into two transformers $(1{:}\ n_1)$ $(1{:}\ n_2)$. Here $n_1 + n_2 = n$ and $n_1 = n_2 = 0.5n$ if silicon carbide (SiC) MOSFETs are used as switching devices on the current-fed side [16]. First, a half-step voltage of $n_1 V_{\rm in}$ $(= 0.5nV_{\rm in})$ is applied. With this voltage being input, the output capacitance of the MOSFETs on the current-fed side bridge and the leakage inductance of the transformer form a resonant circuit. The voltage v_{ab} thus resonates and reaches a peak value of $nV_{\rm in}$, $(= 2n_1 V_{\rm in})$ simultaneously the transformer secondary current i_s reaches the filter inductor current level (i_{Lf}). At this instant, the remaining half voltage $n_2 V_{\rm in}$ is applied. As the voltage across the output capacitance of the MOSFET and leakage inductor current have reached their final steady-state values, there will not be any further resonance. This idea is depicted in Fig. 3.

However, the converter in [16], being a solar microinverter, did not consider the requirements of bidirectional power flow. Here the operation is explained only for forward power flow, i.e., dc to ac. It did not explore how the reverse power flow, i.e., ac to dc, would be achieved. This work aims to develop an SPS modulation strategy for a bidirectional dc–dc converter that also eliminates the voltage overshoot problem. The rest of this article is organized as follows. In Section II, the proposed bidirectional dc–dc converter with SPS modulation and SVS is presented. Basic operating modes describing the elimination of voltage overshoot in the proposed bidirectional converter are presented in Section III-A. A detailed modulated strategy and ZVS analysis during forward and reverse power flow is shown in Sections III-B and III-C, respectively. The symmetry of the SPS-SVS

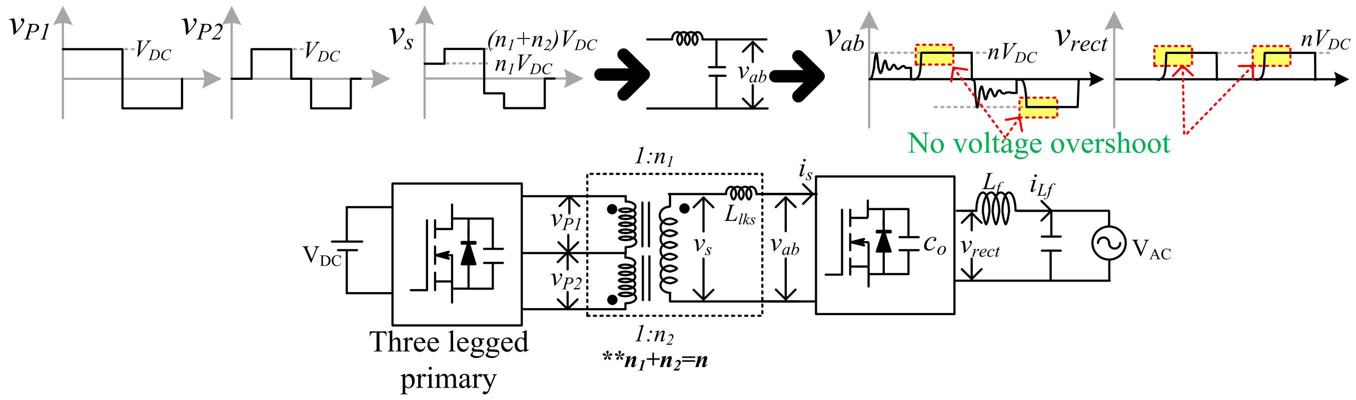


Fig. 3. Illustrating the basic idea behind the voltage overshoot elimination in the SPS-modulated SVS DC–AC converter proposed in [16].

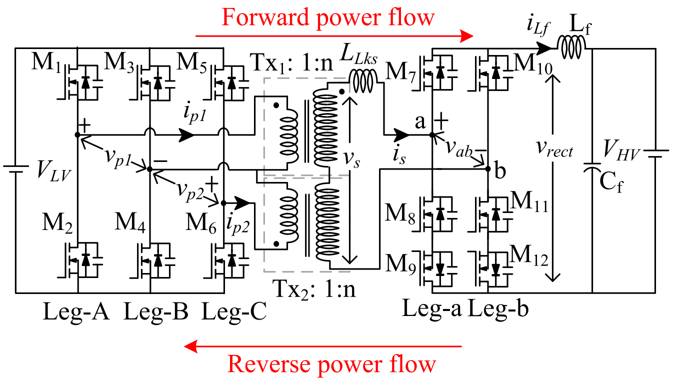


Fig. 4. Proposed SPS-modulated SVS DC–DC bidirectional converter.

modulation strategy during forward and reverse power flow is presented in Section III-D. Experimental results are given in Section IV, and conclusions are given in Section V.

II. PROPOSED BIDIRECTIONAL DC–DC CONVERTER WITH SPS MODULATION AND STEP VOLTAGE SWITCHING

The proposed bidirectional converter is shown in Fig. 4. It has evolved from the conventional phase-shift full-bridge (PSFB) converter [10]. However, unlike conventional PPS modulated PSFB converter, it has adopted SPS modulation to control the output voltage. Therefore, in this topology, the secondary side resembles the secondary side of the unidirectional PWM dc–dc converter presented in [12]. However, to make this topology bidirectional, all the diodes of the SPS PWM dc–dc converter are replaced with MOSFETs and then rearranged for symmetry in the converter structure. It may be noted that compared to PPS modulated PSFB converters, SPS-modulated converters have two additional devices (antiseries) on the secondary side. These antiseries MOSFETs are required in this topology because, unlike PPS control, the secondary-side voltage is not zero in the freewheeling mode, and the devices of only one leg are ON and of the other leg are OFF during this time.

The circulating current problem of the PPS-controlled PSFB converter is solved in this SPS-modulated bidirectional converter. As presented in [12], this topology also has the advantage of soft switching (either ZVS or ZCS) of all the devices over a very wide range of load current [12].

The next significant modification with respect to the PSFB converter is that a third leg (Leg C) has been added to the primary-side bridge to eliminate the problem of voltage overshoot across the secondary-side devices. This three-leg bridge generates a second step voltage waveform at the appropriate instant so that the leakage inductance of the transformer and the device capacitance do not resonate to produce any voltage overshoot. Therefore, this topology is called an SPS-SVS dc–dc bidirectional converter, and the complete modulation scheme is denoted as SPS-SVS modulation in this article.

Even though there are three switching legs on the voltage-fed side, the power will be equally distributed between the two transformers used in the proposed topology. Therefore, two half-bridge legs Leg-A and Leg-C, on the voltage-fed side, carry $^{1}/_{2}$ the load current value compared to the other leg (Leg-B). Thus, despite three switching legs, the voltage-fed side bridge will not have more conduction loss than the conventional PSFB converter. The total KVA rating of the two transformers is equal to that of the single transformer that has been used in a conventional converter. There are other PSFB topologies that propose a three-leg structure for a different purpose, and due to this, there is no detrimental effect on efficiency [31], [32], [33]. The technique to eliminate the voltage overshoot was first proposed in [16], but its application was limited to forward power flow, as discussed in Section I. In this article, a modulation scheme is presented, which maintains the essential features of the modulation scheme presented in [16] but modifies the sequences so that bidirectional power flow between voltage-fed and current-fed sides becomes possible without additional circuit elements. The basic operating modes during forward and reverse power flow operation of the proposed SPS-SVS dc–dc converter and the respective modulation schemes are discussed in the following sections.

III. ANALYSIS OF THE SPS-SVC CONVERTER

A. Basic Operating Modes

Basic operating modes that help in eliminating the voltage overshoot problem in the proposed bidirectional converter

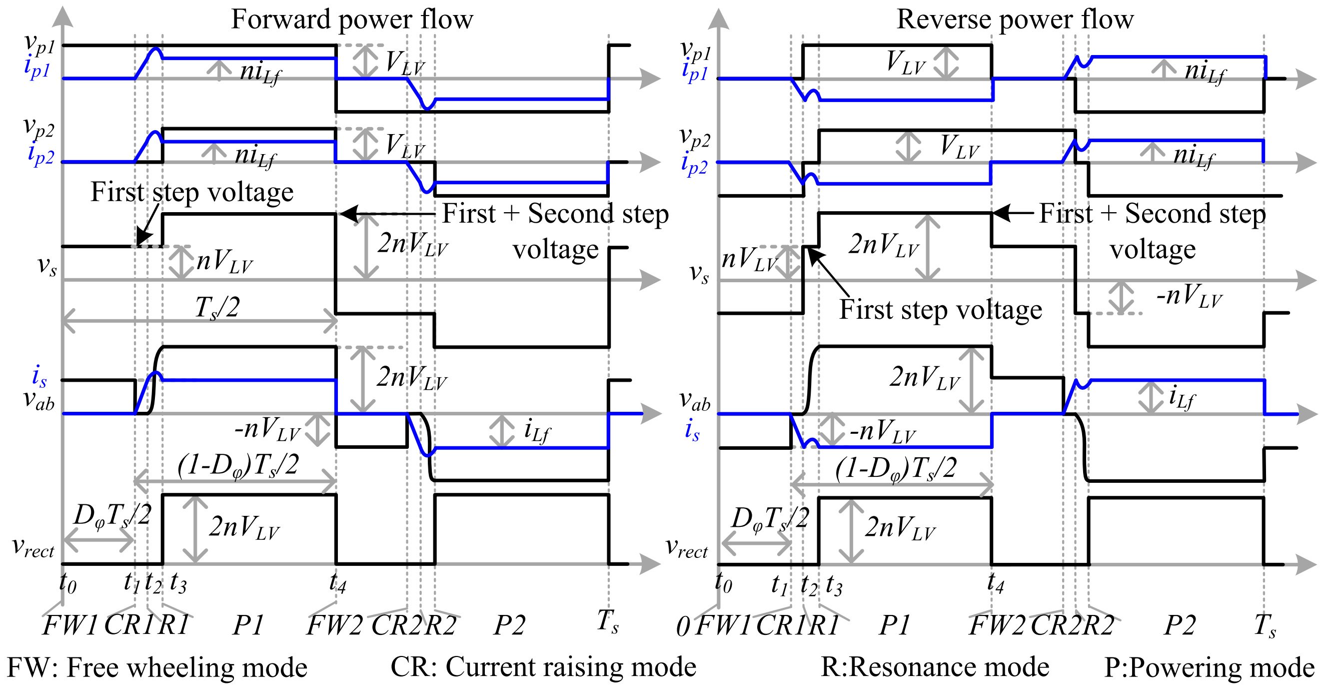


Fig. 5. Basic circuit waveforms of the proposed SPS-SVS bidirectional DC–DC converter during forward and reverse power flow.

are presented in this section. The circuit waveforms of the proposed SPS-SVS dc–dc bidirectional converter are depicted in Fig. 5. In this figure, $D_\varphi T_s/2$ is the phase shift between the current-fed (secondary) side devices. The operation of the proposed converter is divided into four basic modes in each switching half cycle, as shown in Fig. 5, which are as follows.

Freewheeling mode (FW1) (t_0–t_1)*:* In this mode, the filter inductor current freewheels through one of the legs on the current-fed side, and there will not be any power transfer between the voltage-fed side and the current-fed side. Transformer secondary (series-connected) side current (i_s) is zero. The primary of one of the transformers is connected to the V_{LV}, so the reflected voltage on the series-connected secondary (v_s) is equal to nV_{LV} (forward power flow) or $-nV_{LV}$ (reverse power flow).

Current rising mode (CR1) (t_1–t_2)*:* In this mode, the transformer's secondary is effectively shorted, allowing the transformer secondary-side current (i_s) to rise to the filter inductor current level. Current i_s rises in the positive direction in forward power flow as v_s is positive, and it rises in the negative direction in reverse power flow as v_s is negative. The voltage v_{ab} is zero in this mode.

Resonance mode (R1) (t_2–t_3)*:* In this mode, the switching sequence is the same for both forward and reverse power flow. This mode is the starting stage of powering mode. During this mode, the first transformer (Tx_1) primary voltage v_{p1} is equal to V_{LV}. The second transformer (Tx_2) primary voltage v_{p2} is equal to zero, so the reflected voltage on the transformer secondary is nV_{LV}. With this step voltage as input and due to the resonance between the transformer leakage inductance (L_{lks}) and the output capacitance of the MOSFETs on the current-fed side, the voltage v_{ab} starts rising and reaches its peak value ($2nV_{LV}$) at the end of this mode, and at the same instant, the current i_s also resonates and reaches filter inductor current i_{Lf} again.

Powering mode (P1) (t_3–t_4)*:* In this mode also, the switching sequence is the same for both forward and reverse power flow. During this mode, the second step voltage is applied across the transformer secondary by connecting the primary of the other transformer to V_{LV}; hence, the reflected secondary-side voltage(v_s) is $(n+n)V_{LV} = 2nV_{LV}$. As v_{ab} has already reached the voltage level of $2nV_{LV}$ due to resonance, which is the same as the v_s, and the current through another resonating element, i.e., leakage inductor current (i_s) reaches its steady-state value of (i_{Lf}), there will not be any further resonance, and thus, there is no voltage overshoot.

The remaining four modes in the next switching half cycle are similar to those discussed. The circuit equivalents of the four modes discussed are shown in Fig. 6. The complete modulation strategy for implementing these basic modes in the proposed converter is shown in Fig. 7. The detailed analysis of this modulation strategy along with the ZVS/ZCS transitions of the devices is discussed in the section followed. This analysis is based on the following assumptions: Filter inductor current (i_{Lf}) is ripple-free; therefore, it is considered constant in one switching period. The current-fed side devices are SiC MOSFETs; for most SiC MOSFETs, the variation in the output capacitance with respect to drain-to-source voltage is very less when operated at higher voltages [34]. Hence, this output capacitance (C_{os}) is considered constant for the analysis (this has been justified numerically in Section VI). The turns ratio of both the transformers is the same and equal to $1{:}\,n$. The magnetizing inductance is considered very high for the transformers.

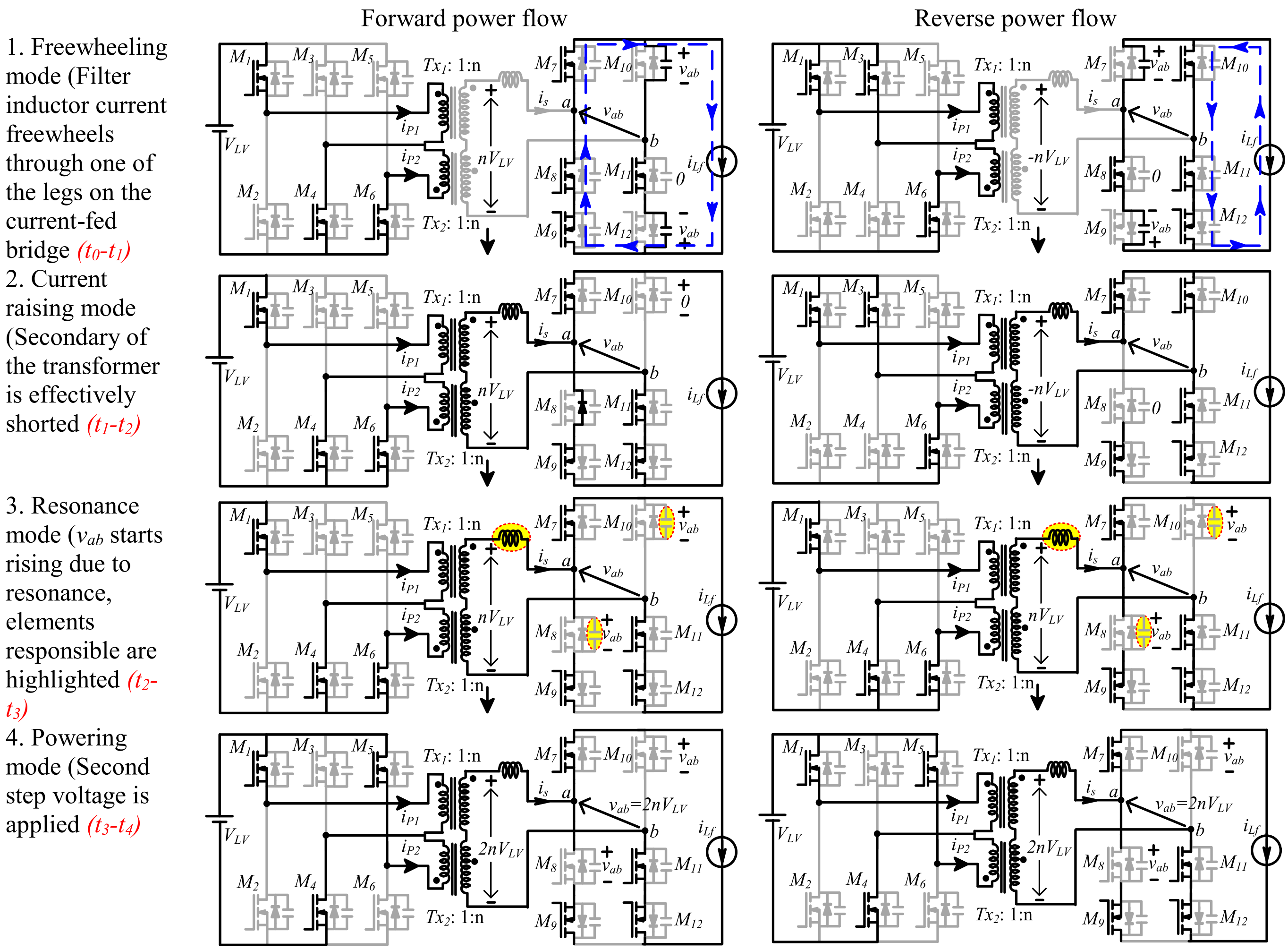


Fig. 6. Illustrating the circuit equivalents of the basic operating modes of the proposed converter during forward and reverse power flow.

B. Detailed Modulation Scheme and Soft-Switching Analysis During Forward Power Flow

Fig. 7(a) shows the modulation strategy during forward power flow operation. Various circuit modes based on the time instants are described as follows.

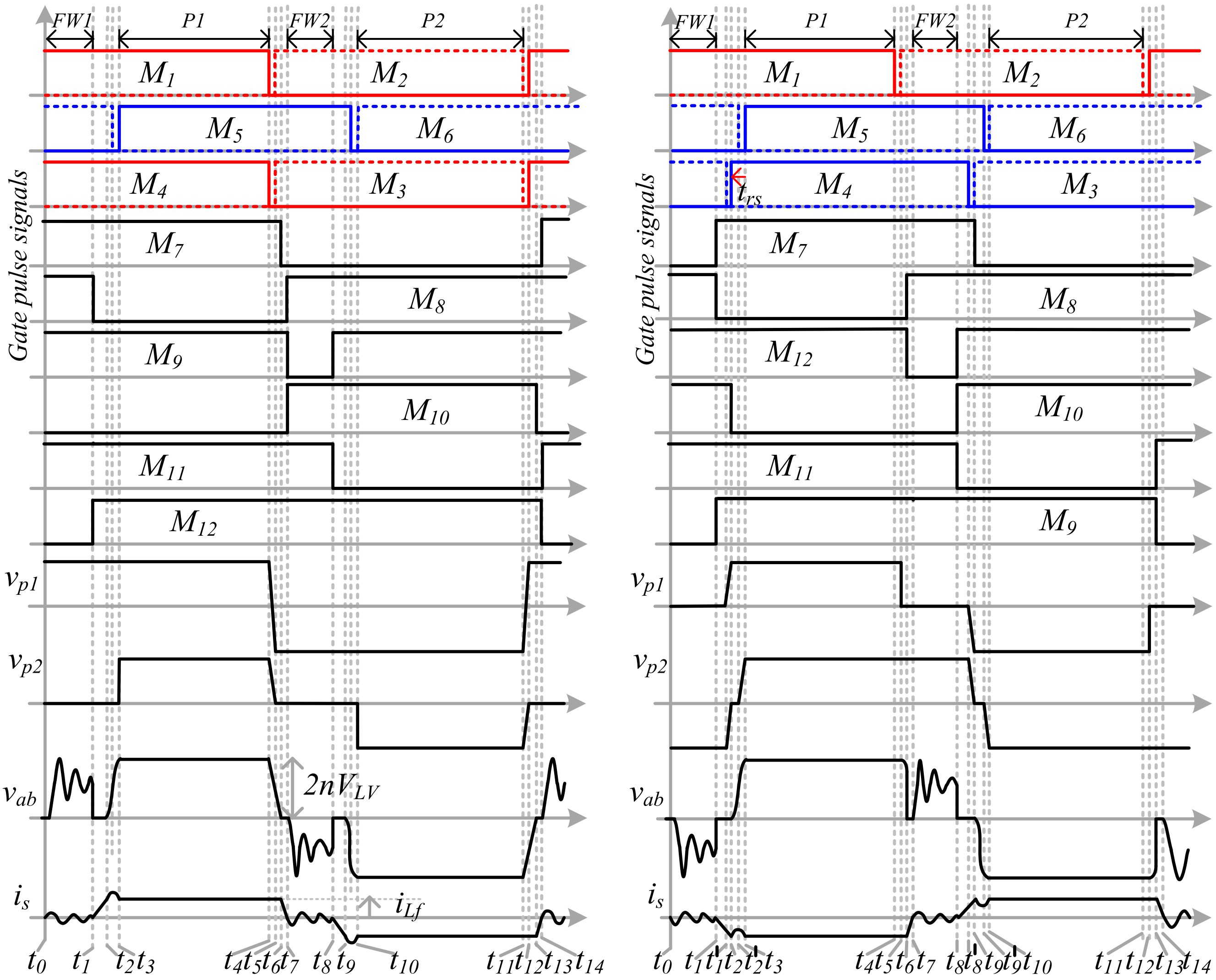
Mode 1 (t_0–t_1) (FW1): In this mode, MOSFETS M_1, M_4, and M_6 of the voltage-fed side are ON, and on the current-fed side, MOSFETS M_7, M_8, M_9, and M_{11} are ON. The primary voltage of transformer Tx$_1$ is $v_{p1} = V_{LV}$, and its reflected secondary voltage is nV_{LV}. This voltage of nV_{LV} has to be blocked by MOSFETS M_{10} and M_{12}. During the charging process of the output capacitances of M_{10} and M_{12}, they form a resonant circuit with the leakage inductance of the transformer (L_{lks}). Resonant equations governing this circuit are given in (1) and (2). Resonance starts with initial values of $v_{ab} = 0$ and $i_s = 0$, and the voltage blocked by MOSFETS M_{10} and M_{12} resonate in this mode as well, but the peak of the voltage according to the (1) would be $2nV_{LV}$ as only a step voltage of nV_{LV} is applied in this mode. Thus, it would not affect the devices on the current-fed side as they are rated for a voltage level of $2nV_{LV}$. The Gate pulse of the MOSFET M_8 is withdrawn at the finishing of this mode.

$$v_{ab}\left(t\right) = nv_{LV}\left(1 - cos\omega_r t\right) \tag{1}$$

$$i_s\left(t\right) = \frac{nv_{LV}}{Z_r}\, sin\omega_r t \tag{2}$$

where resonant frequency $\omega_r = 1/\sqrt{2C_{os}L_{Lks}}$ and resonant impedance $Z_r = \sqrt{L_{Lks}/2C_{os}}$.

Mode 2 (t_1–t_2) (CR1): This mode starts by turning ON MOSFET M_{12}. As no current flows through this MOSFET before this mode, it will turn ON with ZCS. The voltage across the output capacitance of MOSFETS M_{10} and M_{12} discharges through the body channel of MOSFET M_{12}; therefore, v_{ab} becomes zero. As MOSFET M_9 is still ON and the inductor current cannot change its direction immediately, it will force the body diode of the MOSFET M_8 into conduction. With MOSFETS M_{11} and M_{12} also ON, the transformer secondary is effectively shorted; therefore, the secondary-side current or leakage inductor current i_s starts increasing linearly from zero to filter inductor current level i_{Lf} with the slope of nV_{LV}/L_{Lks}. Duty cycle loss occurs in this mode.



$(t_2$-$t_1)$ &$(t_9$-$t_8)$: Current rising mode (CR1)&(CR2)

(a) Forward power flow

$t_{rs}=(t_3$-$t_2)$&$(t_{10}$-$t_9)$: Resonance mode (R1)&(R2)

(b) Reverse power flow

Fig. 7. Illustrating the SPS-SVS modulation strategy for (a) forward power flow and (b) reverse power flow.

The duration of this mode can be calculated as

$$t_2 - t_1 = t_{ir} = L_{Lks}\left(\frac{i_{Lf}}{nV_{LV}}\right). \tag{3}$$

Mode 3 (t_2–t_3) (R1): At time $t = t_2$, with nV_{LV} acting as a source, L_{Lks} along with the paralleled output capacitances of the MOSFETs M_{10} and M_8 form a resonant circuit, with initial conditions of drain-to-source voltages of MOSFETs M_{10} and M_8 being zero, i.e., $v_{ds10}(t_3) = 0$, $v_{ds8}(t_3) = 0$ and leakage inductor current being equal to filter inductor current, i.e., $i_s(t_3) = i_{Lf}$. The resonant equations for this circuit are given as follows:

$$v_{ab}(t) = nV_{LV}(1 - cos\omega_r t) \tag{4}$$

$$i_s(t) = i_{Lf} + \frac{nV_{LV}}{Z_r}\sin\omega_r t. \tag{5}$$

This resonance continues until v_{ab} rises to the peak value of $2nV_{LV}$ and i_s reaches to filter inductor current level (i_{Lf}) again.

The duration of this mode can be found using (6). Gate pulse to the MOSFET M_6 is withdrawn at the finishing of this mode.

$$t_3 - t_2 = \frac{1}{\omega_r}\cos^{-1}\left(1 - \frac{v_{ds10}}{nV_{LV}}\right) = t_{rs}. \tag{6}$$

Mode 4 (P1) (t_3–t_4): This mode starts by turning ON the MOSFET M_5. Thus, the second step voltage is also applied across the transformer secondary, which helps in eliminating the device voltage overshoot, as discussed before in the powering mode *(P1)*.

Mode 5 (t_4–t_5): This mode starts by simultaneously withdrawing the gate pulses to MOSFETs M_1 and M_4. The load current carried by the leakage inductor helps in achieving ZVS of MOSFETs M_2 and M_3. The simplified (multiresonant) circuit of this mode is shown in Fig. 8. The equations related to this circuit can be written based on the equations for the multiresonant

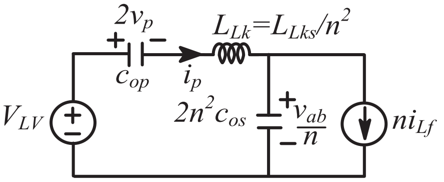


Fig. 8. Resonant circuit formed in mode 5.

circuit given in [35].

$$i_p = ni_{Lf}\cos\omega_{SD}t + \frac{(ni_{Lf})\,C_{op}}{C_{op}+C_D}\,(1-\cos\omega_{SD}t) \tag{7}$$

$$2v_p = \frac{(ni_{Lf})\,t}{C_{op}+C_D} + \frac{1}{\omega_{SD}}\frac{(ni_{Lf})\,C_D}{C_{op}\,(C_{op}+C_D)}\sin\omega_{SD}t \tag{8}$$

$$\begin{aligned} v_{ab} = V_{LV} &+ \left[\frac{1}{C_{op}} - \frac{C_{op}}{(C_{op}+C_D)C_D}\right] \\ &\times \frac{(ni_{Lf})}{\omega_{SD}}\sin\omega_{SD}t - \frac{(ni_{Lf})\ t}{C_{op}+C_D} \end{aligned} \tag{9}$$

where c_{op} = output capacitance of the voltage-fed side MOSFETs, $C_D = 2n^2$ c_{os}, $\omega_{SD} = \sqrt{\frac{1}{L_{Lk}C}}$, and $C = \frac{C_SC_D}{C_S+C_D}$.

Mode 6 (t_5–t_6): This mode starts by turning ON MOSFETs M_2 and M_3. During this mode, the output capacitances of MOSFETs M_8 and M_{10} discharge from $v_{ab}(t_6)$ to zero. The gate pulse of MOSFET M_7 is withdrawn at the end of this mode.

Mode 7 (t_6–t_7): In this mode, the current i_s falls from $i_s(t_7)$ to *0* with a slope of nV_{LV}/L_{lks} following (10). By the finishing of this mode, the gate pulse of M_9 is withdrawn and M_{10} will be ready for ZVS turn ON and M_8 will be ready for ZCS turn ON.

$$L_{Lks}\frac{di_s}{dt} = -nV_{LV}. \tag{10}$$

The remaining modes of operation are similar to the modes discussed.

C. Detailed Modulation Scheme and Soft-Switching Analysis During Reverse Power Flow

Fig. 7(b) shows the modulation strategy during reverse power flow operation. Various circuit modes based on the time instants are described as follows.

Mode 1 (t_0–t_1) (FW1): In this mode, the voltage-fed side MOSFETs M_6, M_3, and M_1 are ON, and on the current-fed side, MOSFETs M_8, M_{10}, M_{11}, and M_{12} are ON. This mode is similar to *mode 1* of forward power flow, except the current i_{Lf} now freewheels through the MOSFET Leg-B instead of Leg-A, and the reflected secondary-side voltage is -nV_{LV} instead of nV_{LV}. The current flowing through MOSFET M_7 is zero in this mode; therefore, it will be ready for ZCS turn ON in the following mode.

Mode 2 (t_1–t_2) (CR1): This mode starts by turning ON the MOSFET M_7. The voltage across output capacitances of the MOSFETs M_7 and M_9 discharges through the body channel of the MOSFET M_7; thus, the voltage across the MOSFET M_9 becomes zero, and so does the voltage v_{ab}. Thus, M_9 turns ON with ZVS, and at the same time, the gate pulse of M_8 is withdrawn. As MOSFET M_{10} is still ON, with MOSFET M_7 turned ON, the transformer secondary is effectively shorted. This mode is similar to *mode 2* of forward power flow, where all bottom devices on the current-fed side are conducting to short the transformer secondary. In contrast, all top devices of the current-fed side are conducting in reverse power flow. As v_s = -nV_{LV} in reverse power flow, i_s rises in the negative direction from zero to filter inductor current level (i_{Lf}) with a slope of -nV_{LV}/L_{Lks}. At the finishing of this mode, the gate pulse to the MOSFET M_{10} is withdrawn. This mode's duration can be found using (3) by replacing nV_{LV} with -nV_{LV}. Here, the leakage inductor current $\mathrm{i_s}$ is forced to rise till the filter inductor current level (i_{LF}) by creating an overlap between M_7 and M_{10}. This overlapping time is calculated online based on (3). From this equation, it is clear that t_{ir} varies proportionally with load current. Hence, even if there is an arbitrary change in load during the transient, there will not be any discontinuity in the inductor current.

Mode 2a (t'_1–t_2): This submode starts by withdrawing the gate pulse of MOSFETs M_3. This mode is similar to *mode 5* in forward power flow. Therefore, M_4 is ready for ZVS turn-ON at the finishing of this mode.

Mode 3 (t_2–t_3) (R1): This mode starts by turning ON the MOSFET M_4 on the voltage-fed side. This mode operation is the same as *mode 3* of the forward power flow.

Mode 3a (t_2—t'_2): This submode starts by withdrawing the gate pulse to MOSFET M_6. Before this mode, as the leakage inductor current i_s is negative, it helps the MOSFET M_5 in achieving the ZVS. When the gate pulse of M_6 is withdrawn, this current discharges the output capacitance of MOSFET M_5 and charges the output capacitance of MOSFET M_6 simultaneously following (11). At the finishing of this mode, MOSFET M_5 will be ready for ZVS turn ON.

$$-C_{op}\frac{dv_{ds5}}{dt} = C_{op}\frac{dv_{ds6}}{dt} = i_{p2} = ni_{lf}. \tag{11}$$

Mode 4 (t_3–t_4) (P1): This mode starts by turning ON the MOSFET M_5. The operation of this mode is similar to *mode 4* of forward power flow. At the finishing of this mode, MOSFET M_1 is turned OFF.

Mode 5 (t_4–t_5): This mode starts by turning OFF the MOSFET M_1 and ends by turning ON the MOSFET M_2. The voltage v_{p1} falls to zero by the end of this mode.

Mode 6 (t_5–t_6): This mode starts by turning ON the MOSFET M_2. As v_{p1} is zero, v_{ab} tends to fall slightly from its level voltage.

Mode 7 (t_6–t_7): This mode starts by turning ON the MOSFET M_8 and turning OFF the MOSFET M_{12}. No current flows through the MOSFET M_8 before this mode, so it will turn ON with ZCS. As M_8 is turned ON, it will create a short on the secondary side with the body diode of M_{12} conducting. Thus, the output capacitances of MOSFETs M_8 and M_{10} discharge to zero so does the voltage v_{ab}, and the current i_s starts rising from i_{LF} to 0 with a slope of nV_{LV}/L_{lks}.

The remaining modes of operation are similar to the modes discussed. The soft switching of the devices during forward and reverse power flow is summarized in Table I. It is given in Table I that two MOSFETs on the voltage-fed side undergo hard turn-ON.

TABLE I
SUMMARY ON SOFT SWITCHING OF THE DEVICES

Switching Device	**Forward power flow (turn ON)**	**Reverse power flow (turn ON)**
M_7, M_{10}	ZVS	ZCS
M_8, M_{11}	ZCS	ZCS
M_9, M_{12}	ZCS	ZVS
M_3, M_4	ZVS	ZVS
M_1, M_2	ZVS	Hard turn on
M_5, M_6	Hard turn ON	ZVS

However, these MOSFETs are required to implement SVS. SVS is absolutely essential to eliminate voltage clamp. The elimination of loss in the voltage clamp (passive or active) is more than compensating for the switching loss of these two MOSFETs. As these MOSFETs are on the low-voltage side, their turn-ON loss will be relatively less.

D. Symmetry of the SPS-SVC Modulation During Forward and Reverse Power Flow

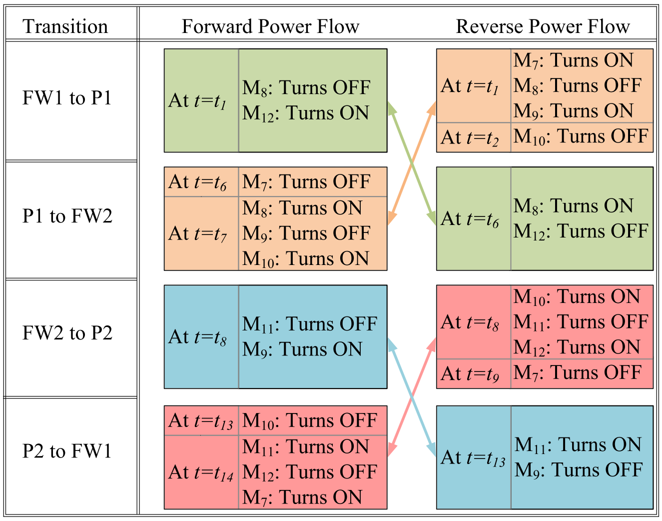
The proposed modulation strategy is essentially symmetric in both directions. The following observations from Fig. 7 help in understanding the symmetry of the proposed modulation.

1) Primary-Side Modulation:

1) In the proposed SPS-SVS modulation scheme, irrespective of the direction of the power flow, the gate pulse of M_5 (top device of Leg-C) is phase-shifted with respect to the gate pulse of M_1 (top device of Leg-A). This phase shift is necessary to control the output voltage of the converter. It broadly divides the entire period into four basic modes of operation (FW1, P1, FW2, and P2), as shown in Fig. 7. It may be noted that these operational modes are identical in both forward and reverse power flow.
2) In the proposed three-leg converter, the gate pulses of the middle-leg (Leg-B) devices, M_3 and M_4, are obtained following a symmetry pattern. M_4 is aligned with the gate pulse of M_1 for the forward power flow and almost aligned with the gate pulse of M_5 for the reverse power flow. The only difference is that, in reverse power flow, the gate pulse of M_4 is slightly advanced (by resonance period t_{rs}) with respect to the gate pulse of M_5 to generate the first step voltage. This two-step application of the input voltage (i.e., $v_{p1}+v_{p2}$) ensures that the voltage across the secondary devices never crosses the level voltage in the reverse power flow mode as well.

This bidirectional converter modulates the primary-side devices as per rules 1) and 2). It is clear that a transition from forward to reverse power flow mode would require only a change in the alignment of the gate pulses of M_4 and M_3.

2) Secondary-Side Modulation: In the secondary-side modulation of SPS-SVS, there is one additional constraint that is taken into consideration. Other than the top devices, M_7 and M_{10}, the pulsewidth of the other devices is modified to get a significant circuit benefit. The modulation does not allow both the series-connected devices to be in the OFF state; otherwise, the voltage across one of the blocking devices may be more than the applied voltage across the combination in the floating state because the blocking voltages appear in opposite directions. This modification extends the ON period of one of the bottom devices of the same leg when both devices are supposed to be OFF to avoid the floating condition of these devices in the OFF state. With this change, the following similarities may be observed from the gate pulses of secondary-side devices shown in Fig. 7(a) and (b).



Transition	Forward Power Flow		Reverse Power Flow	
FW1 to P1	At $t=t_1$	M_8: Turns OFF M_{12}: Turns ON	At $t=t_1$	M_7: Turns ON M_8: Turns OFF M_9: Turns ON
			At $t=t_2$	M_{10}: Turns OFF
P1 to FW2	At $t=t_6$	M_7: Turns OFF	At $t=t_6$	M_8: Turns ON M_{12}: Turns OFF
	At $t=t_7$	M_8: Turns ON M_9: Turns OFF M_{10}: Turns ON		
FW2 to P2	At $t=t_8$	M_{11}: Turns OFF M_9: Turns ON	At $t=t_8$	M_{10}: Turns ON M_{11}: Turns OFF M_{12}: Turns ON
			At $t=t_9$	M_7: Turns OFF
P2 to FW1	At $t=t_{13}$	M_{10}: Turns OFF	At $t=t_{13}$	M_{11}: Turns ON M_9: Turns OFF
	At $t=t_{14}$	M_{11}: Turns ON M_{12}: Turns OFF M_7: Turns ON		

Fig. 9. Illustrating the switching time instants of secondary-side devices.

1) First, it can be seen that M_7 and M_{10} gate pulses (the secondary-side top devices) for reverse power flow are lagging M_7 and M_{10} gate pulses for forward power flow by the freewheeling period (FW), respectively. Second, it may be noted that M_8 and M_{11} (the secondary-side middle devices) gate pulses for reverse power flow are the same as the M_8 and M_{11} gate pulses for forward power flow, respectively. Third, the gate pulses of M_9 and M_{12} (the secondary-side bottom devices) are interchanged when the direction of power flow changes.
Therefore, M_9 and M_{12} gate pulses for reverse power flow are the same as the M_{12} and M_9 gate pulses for forward power flow.
2) It may be noted from Fig. 9 that the instants the secondary-side devices are turned ON or OFF in forward and reverse power flow modes are correlated with each other. For example, to cause a transition from FW1 to P1 in forward power flow mode, at $t = t_1$, M_8 is turned OFF and M_{12} is turned ON, whereas for the transition from P1 to FW2 in reverse power mode, at $t = t_6$, M_8 is turned ON and M_{12} is turned OFF. Similarly, the transition from FW1 to P1 in reverse power flow mode at t_1 and t_2 is correlated with the transition from P1 to FW2 of forward power flow mode at t_5 and t_6 because the same switches change to the inverted state, maintaining the symmetry of the switching instant. Therefore, the proposed SPS-SVS modulation can completely predict the switching signals for reverse

TABLE II
PARAMETERS OF THE PROTOTYPE

Voltage conversion	**72–400 V**
Rated power	1.7 kW
Operating frequency	100 kHz
Filter inductor	1 mH
Low-voltage side devices	200 V, 130 A, 8 mΩ Silicon MOSFETs (IRFP4668PBF)
High-voltage side devices	1.2 kV,31 A,80 mΩ SiC MOSFETs(C2M0080120D)
Controller used to generate gate pulses	FPGA XC3S400 Xilinx control board

TABLE III
TRANSFORMERS DESIGN DATA

Turns ratio	**1:4**
No. of turns winding 1	7
No. of turns winding 2	14+14 (interleaved)
Cores used	EE 42/21/20 N97 cores
Core area	244 mm^2
Leakage inductance	500 nH
AC resistance	23 mΩ

power flow from switching signals for forward power flow.

IV. EXPERIMENTAL RESULTS

The proposed converter is verified experimentally at a peak power of 1.7 kW. The parameters used for the experiment are given in Table II and the design data of the transformers used are given in Table III. From the parameters, it can be observed that, in the proposed converter, the v_{ds} across the current-fed side devices will be equal to 280 V(nV_{LV}) when the first step is applied. After applying the second step voltage, the v_{ds} will be 560 V ($2nV_{LV}$). The variation of C_{os} from 280 to 560 V is <20PF [34]. This variation of < 20 pF in C_{os} will not affect the magnitude of voltage overshoot across the device; hence, it can be considered constant.

The hardware prototype of the proposed converter is shown in Fig. 10. From Figs. 11 and 12, it can be observed the voltage overshoot is absent in the voltage v_{ab} during both forward and reverse power flow.

Soft switching of various devices at rated power (1.7 kW) is shown in Figs. 13 and 14. In these, the ZCS turn ON of MOSFETs M$_8$ and M$_9$ and ZVS turn ON of the MOSFET M$_7$ during forward power flow is shown in Fig. 13(a), (b), and (e), respectively. Similarly, the MOSFET M$_{10}$ also undergoes ZVS turn ON, and MOSFETs M$_{11}$ and M$_{12}$ undergo ZCS turn ON in the next switching half cycle during forward power flow. ZVS turn ON of the voltage-fed side MOSFETs M$_3$ and M$_1$ is shown in Fig. 13(c) and (d), respectively. Similarly, their complementary MOSFETs M$_2$ and M$_4$ also undergo ZVS turn ON during forward power flow.

The ZCS turn ON of the current-fed side MOSFETs M$_{10}$ and M$_{11}$ and the ZVS turn ON of MOSFET M$_{12}$ during reverse power flow are shown in Fig. 14(a)–(c), respectively. Similarly, the MOSFETs M$_7$ and M$_8$ also undergo ZCS turn ON, and MOSFETs M$_9$ undergoes ZVS turn ON in the next switching half cycle during reverse power flow. ZVS turn ON of the voltage-fed side MOSFETs M$_4$ and M$_6$ is shown in Fig. 14(d) and (e), respectively. Similarly, their complementary MOSFETs M$_3$ and M$_5$ also undergo ZVS turn ON during reverse power flow. Transformer primary currents i_{p1} and i_{p2}, along with the transformer secondary current i_s and voltage v_{ab}, are shown in Figs. 15

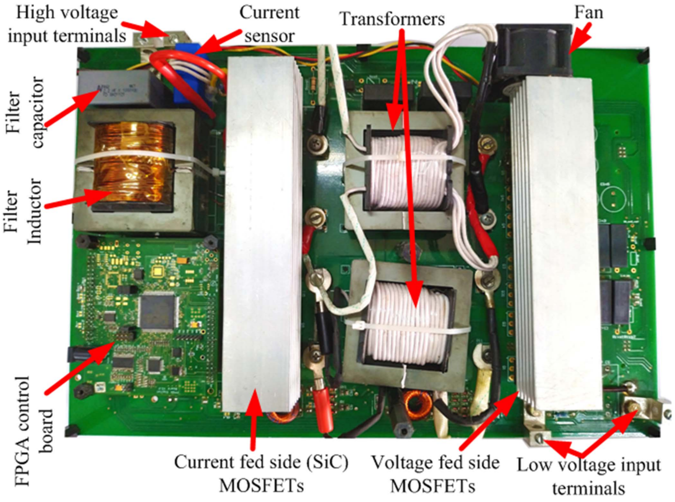


Fig. 10. Hardware prototype of the proposed converter.

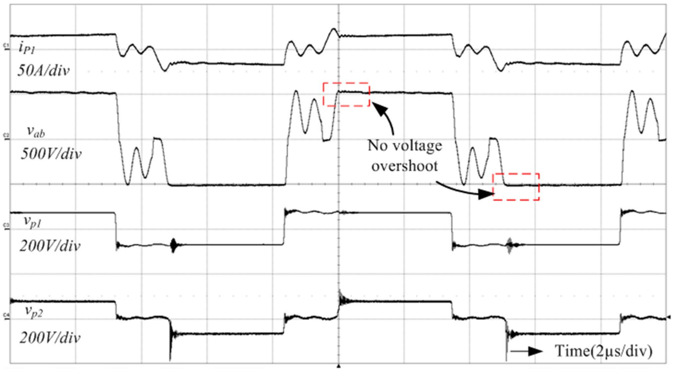


Fig. 11. Experimental result shows the absence of voltage overshoot in v_{ab} during forward power flow at 1.7 kW power.

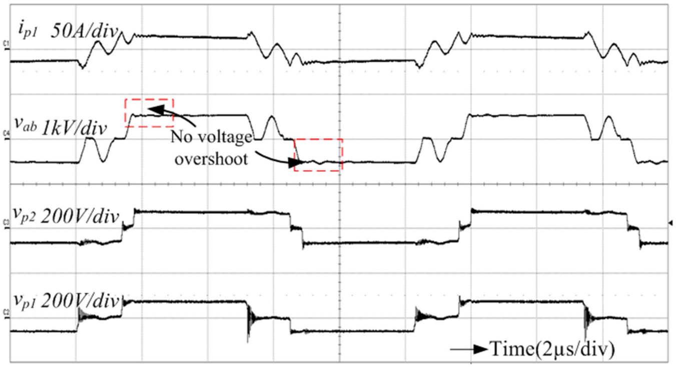
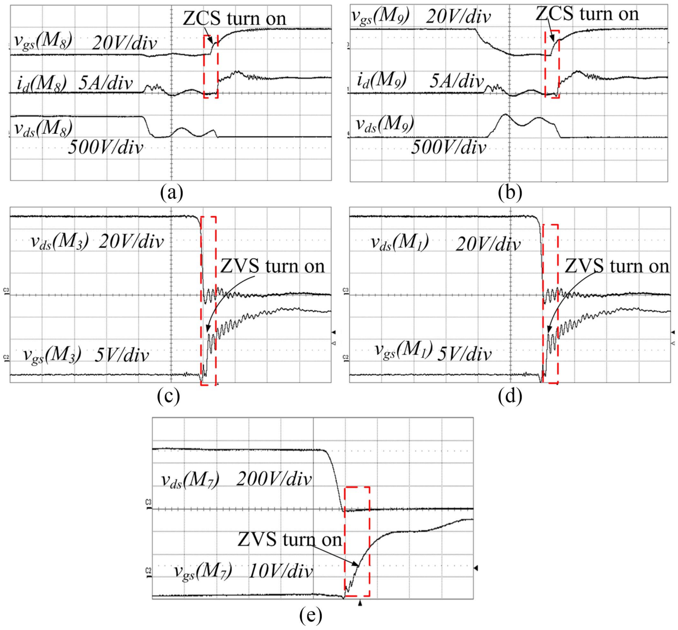


Fig. 12. Experimental result shows the absence of voltage overshoot in v_{ab} during reverse power flow at 1.7 kW power.

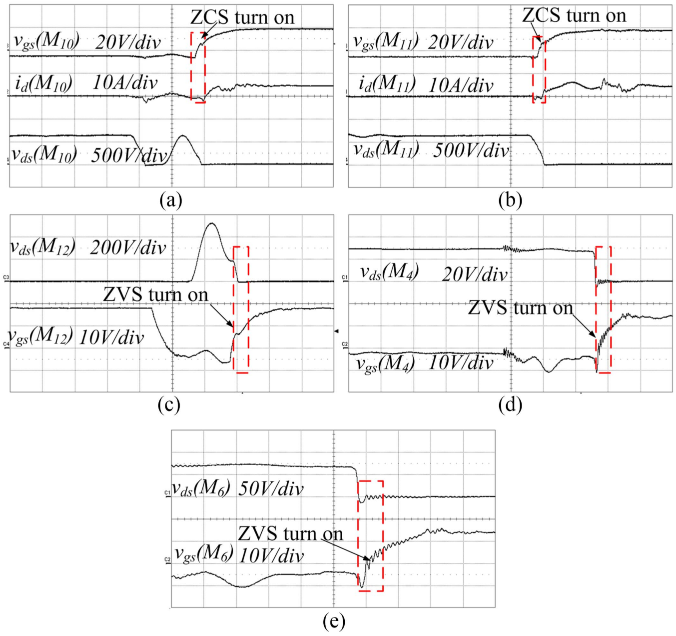


(a) (b)

(c) (d)

(e)

Fig. 13. Experimental result shows soft-switching phenomenon in various MOSFETs during forward power flow at 1.7 kW power.



(a) (b)

(c) (d)

(e)

Fig. 14. Experimental result shows soft-switching phenomenon in various MOSFETs during reverse power flow at 1.7 kW power.

and 16 during forward and reverse power flow, respectively. From these results, it is evident that the circulating current is absent in the proposed converter. The results claiming soft switching at low power at 250 W, i.e.,15% maximum power during both forward and reverse power flow, are shown in Figs. 17 and 18, respectively.

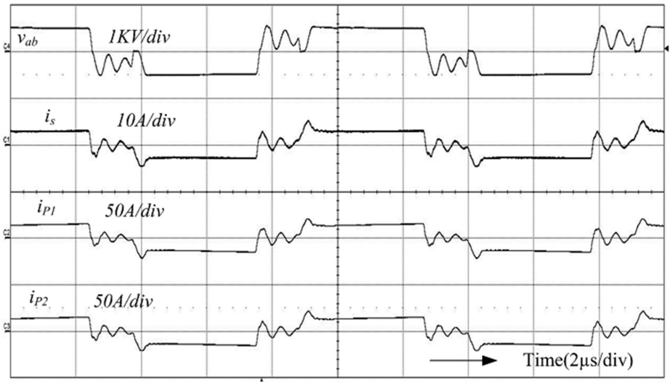


Fig. 15. Experimental result shows all the transformer currents and the voltage v_{ab} during forward power flow at 1.7 kW power.

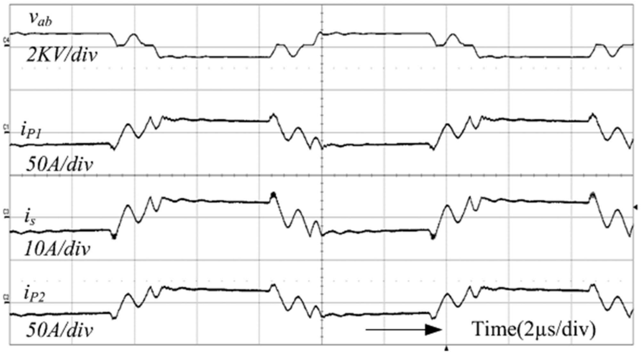


Fig. 16. Experimental result shows all the transformer currents and the voltage v_{ab} during reverse power flow at 1.7 kW power.

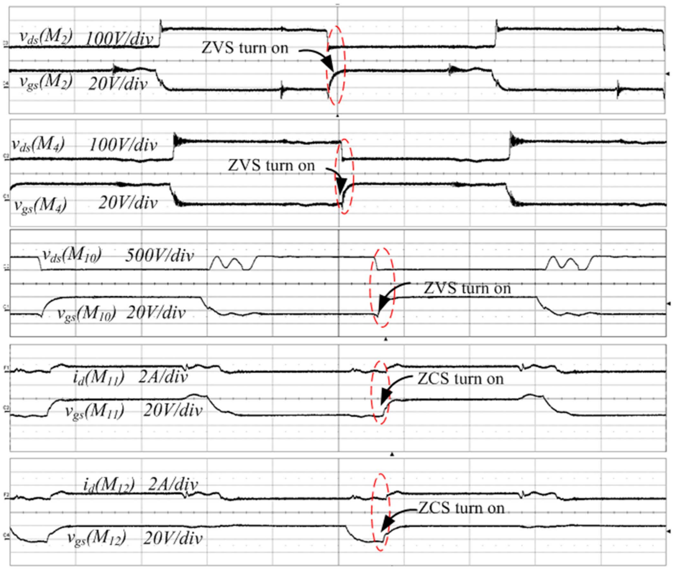


Fig. 17. Experimental result shows soft-switching phenomenon in various MOSFETs during forward power flow at 250 W power.

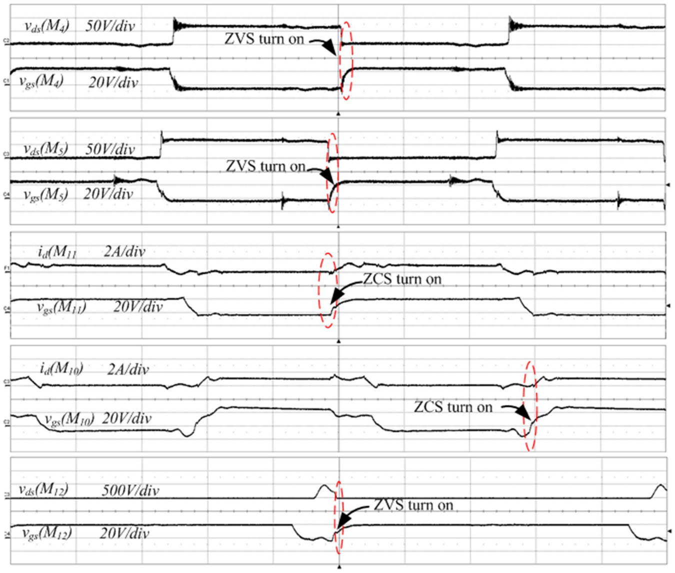


Fig. 18. Experimental result shows soft-switching phenomenon in various MOSFETs during reverse power flow at 250 W power.

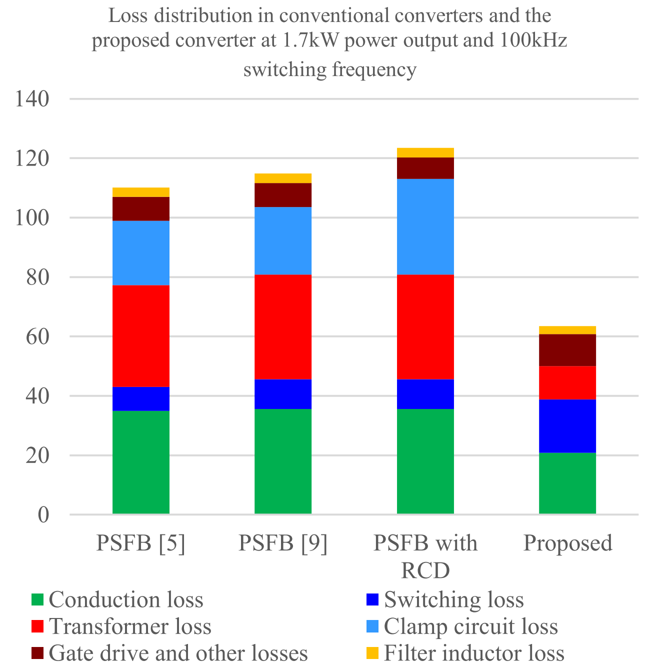


Fig. 19. Power loss distribution in the conventional converter with an active clamp [5], flyback clamp [9], RCD clamp, and the proposed converter at a 1.7 kW power output.

Loss distribution in the proposed converter and the conventional converter with the active clamp [5], flyback clamp [9], and RCD clamp has been calculated through simulations and plotted in Fig. 19. From this figure, it can be observed that the clamp circuit loss (sky blue cube) is absent in the proposed converter. Conduction and transformer losses are significantly less in the proposed converter than in the conventional converters as there is no circulating current in the proposed converter. Switching and gate drive losses are slightly high in the proposed converter, but they are more than compensated by clamp circuit and conduction losses.

The energy loss that occurs in a device during the ZCS transition can be calculated as follows:

Energy loss $= 0.5C_{\rm os}V^2{}_{\rm ds} = 0.5\times\ (90*10^{-12})\ \times\ (560)^2\ =$ $1.4112*10^{-5}$J [where 560 V is the level voltage that will be blocked by the MOSFETs on the current-fed side, and 90 pF is the output capacitance of the current-fed side MOSFETs at $V_{\rm ds}$ $= 560$ V]

Power loss $= 1.4112*10^{-5}\times f_{\rm sw} = 1.4112$ W.

In each switching half cycle, two MOSFETs will undergo ZCS transition so that the total loss will be 2.8224 W. It will be only *0.16%* of the output power (1700 W) and will have a negligible effect on the efficiency.

The proposed converter is operated with a closed-loop current control during the forward power flow. The experimental result in Fig. 20 shows the transient response of the proposed converter when the output current is controlled at 2 A, and the load resistance is changed from 200 to 100 Ω, and vice versa, and the corresponding change in power is from 400 to 800 W, and vice versa. Moreover, it is also operated with closed-loop voltage control during the forward power flow. The experimental result in Fig. 21 shows the transient response of the proposed converter when the output voltage is controlled at 400 V and the load resistance is changed from 200 to 100 Ω, and vice versa, and the corresponding change in power is from 800 to 1600 W, and vice versa. In both cases, the input voltage is maintained at 72 V. From these results, it can be observed that the proposed converter is dynamically fast to respond to load variations, and there is no voltage overshoot problem during the load transition.

The PSFB converter operated with a dissipative RCD clamp and regenerative flyback clamp is compared experimentally with the proposed converter at a switching frequency of 100 kHz and 1.7 kW power output, and the results are tabulated in Table IV.

The efficiency of the proposed bidirectional converter has been compared with the efficiencies of the PSFB bidirectional converter with flyback snubber [9] and PSFB bidirectional converter with active clamp [6] for forward and reverse power flow in Figs. 22 and 23, respectively. It may be observed that the efficiency of the proposed converter is better than the efficiency of the other PSFB converters over the entire output power range for forward power flow. This is true for reverse power flow as well for a range of 800–1700 W. If an RCD clamp is added to the standard bidirectional PSFB, then the efficiency becomes significantly less (about 8% less) compared to the proposed topology, as shown in Fig. 23. There is another point that may be observed. The efficiency of the proposed converter for forward and reverse power flow is almost the same over the entire power range. This is due to the symmetry of the integrated operation of the proposed topology without any additional clamp components—a feature that other topologies do not possess. The following conclusions can be drawn based on the analysis and the experimental results.

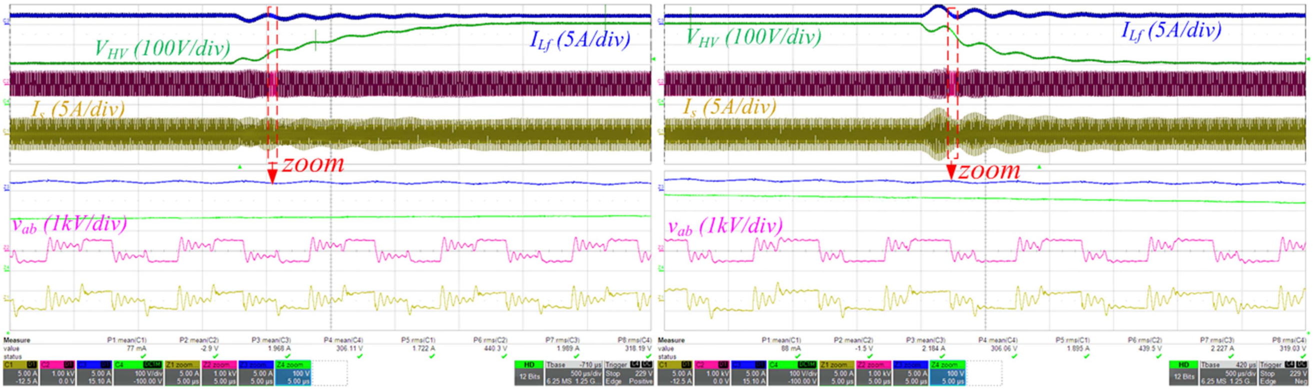


Fig. 20. Experimental result shows the transient response of the proposed converter during forward power flow when the output current is controlled at 2 A, and the load resistance is changed in a step from 200 to 100 Ω, and vice versa. Input voltage is fixed at 72 V.

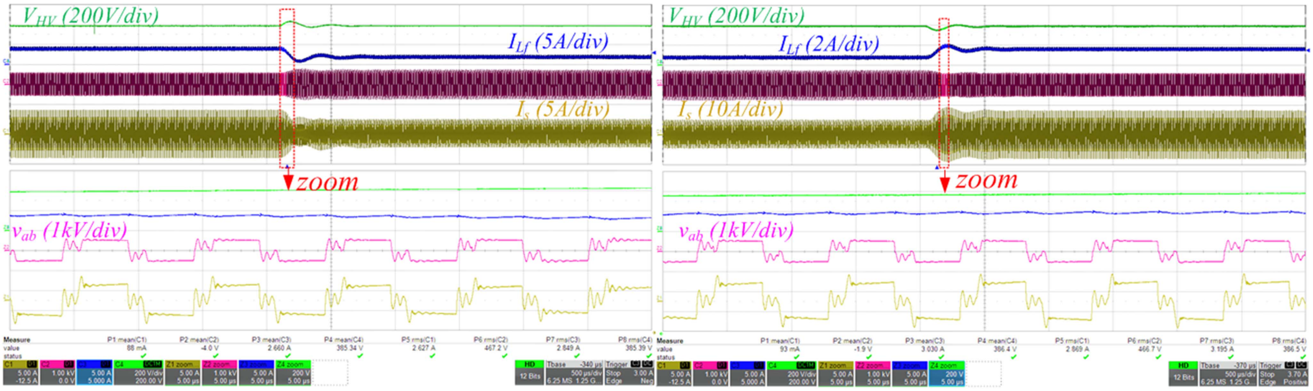


Fig. 21. Experimental result shows the transient response of the proposed converter during forward power flow when the output voltage is controlled at 400 V, and the load resistance is changed in a step from 200 to 100 Ω, and vice versa. Input voltage is fixed at 72 V.

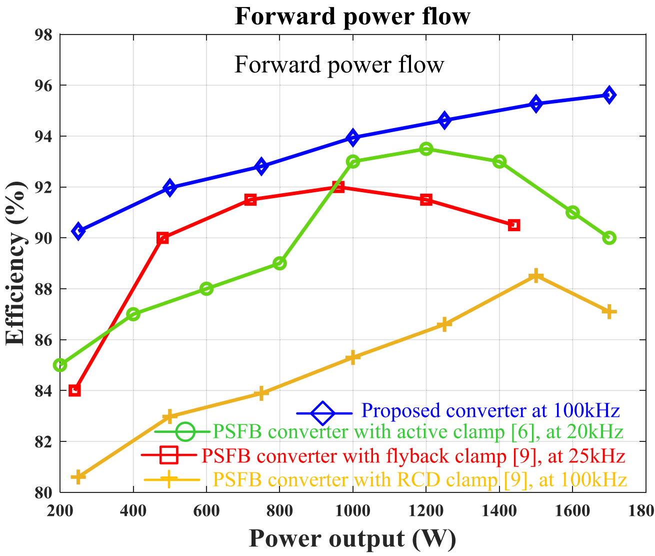


Fig. 22. Conversion efficiency plots of the proposed converter, full-bridge converter with RCD clamp, active clamp [6], and flyback clamp [9] during forward power flow.

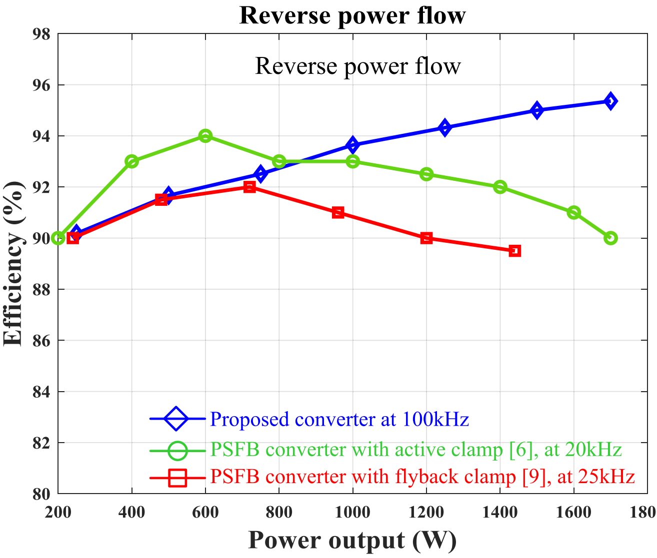


Fig. 23. Conversion efficiency plots of the proposed converter, full-bridge converter with an active clamp [6], and flyback clamp [9] during reverse power flow.

TABLE IV
COMPARISON BETWEEN PSFB CONVERTER WITH CLAMP CIRCUITS AND THE PROPOSED CONVERTER AT 1.7 kW POWER OUTPUT AND 100 kHz SWITCHING FREQUENCY

	Proposed Converter		Conventional converter using active clamp [9] and RCD clamp
RMS currents through voltage-fed side MOSFETs	M1, M2	**I_{p1rms}=12.3 A**	**I_{prms}= 31.1 A**
	M3, M4	**I_{p1rms}+ I_{p2rms}=24.6 A**	**I_{prms}= 31.1 A**
	M5, M6	**I_{p2rms}=12.3 A**	NA
Peak voltage across the current-fed side MOSFETs	**560 V**		**(580–620 V)** It depends on the clamp circuit parameters
Conduction loss in voltage-fed side MOSFETs	**9.68 W**		**29.2 W**
Conduction loss in current-fed side devices	**10.4 W**		**5.78 W**
Switching loss	**18 W**		**2 W**
Transformer losses	**11.23 W**		**34.30 W**
Clamp circuit loss	**0 W**		**21.6 W**
Peak efficiency	**96%**		**91.34% [9]** **88.52%** (RCD)
Power density (W/in^3)	**33.6**		**31.6 [9]** **32.8** (RCD)

V. CONCLUSION

A modulation strategy for bidirectional power flow for the proposed SVS SPS dc–dc converter that eliminates the voltage overshoot problem is presented in this article. It can be observed from the test results that the proposed converter recorded a peak efficiency of 96%, which is at least 4% more than the conventional converter operating with a voltage clamp circuit (at the same operating conditions). The reasons for this improved efficiency are as follows.

1) SVS eliminates the voltage overshoot across the secondary-side devices, which in conventional PSFB converters are suppressed by a voltage clamp (active or passive). Therefore, the proposed solution improves the efficiency as there are no voltage-clamp-related losses.
2) SPS modulation eliminates the circulating current problem in the primary, hence reduced primary device and transformer conduction losses.
3) Except for two low-voltage side devices, all other devices undergo soft switching for a wide output power range.

Apart from this efficiency improvement, the other advantages of the proposed converter are as follows.

1) The transformer design is flexible because the effect of leakage inductance on voltage overshoot has already been nullified.
2) Low-rating (less expensive) devices can be used on the current-fed side of the converter as there is no voltage overshoot.
3) With the elimination of the voltage clamp, the converter circuit is very much simplified, hence a higher power density.
4) Dynamically fast to respond to the load changes when operated in the closed loop.
5) Very little duty cycle loss and can handle a wide variation of duty ratios.

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