ZVS–ZCS High Step-Up/Step-Down Isolated Bidirectional DC–DC Converter for DC Microgrid

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***Abstract*—A soft-switched isolated bidirectional dc–dc converter is proposed for distributed generation systems. Dual coupled inductor-based flyback energy conversion circuit achieves high-voltage step-up/down ratio and high efficiency at lowered duty cycle and, attributes the galvanic isolation. Active switch-based capacitor multiplier cell appreciably reduces voltage stresses on low-voltage (LV) and high-voltage (HV) stage MOSFETS, thereby allowing LV rating devices (small $R_{ds(ON)}$). Active-voltage-clamping type circuit extensively suppresses the voltage spikes across LV-switches caused by leakage inductance. Indeed, this clamp circuitry is formed without any additional switches/diodes, thus, reduces clamp device count. By availing of quasi-resonance, thus, without needing the HV stage snubber, switching voltage spikes are substantially alleviated. Furthermore, this clamp along with quasi-resonance achieves zero-voltage (ZVS) and zero-current (ZCS) switching, over wide-load range, for all switches in both step-up and step-down operations. Reduced voltage stresses, minimized clamp device count, diminished conduction losses, and bidirectional soft-switching performance collectively enhances the efficiency. A 600-W laboratory built set-up working at 75 kHz verifies the viability of the design concept. Measured peak efficiencies in boost and buck stages are 96.65% and 96.58%, respectively.**

***Index Terms*—Active clamp, bidirectional converter, dc–dc converter, high-voltage (HV) conversion gain, switched multiplier cell, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

REMARKABLE progress and advances are being made, and will continue to have, in the dc microgrid technology with the profound innovations and significant contributions of distributed energy generation systems by interfacing efficient dc–dc converters with the high-voltage (HV) step-up/down conversion ratio capability. In Fig. 1, configuration of the renewable energies and battery storage systems with power electronic interfaces in the distributed generation applications is shown [1], [2]. A high step-up highly efficient dc–dc converter is connected as a front-end to deliver the energy generated from the low-voltage (LV) renewable inputs to the high-voltage dc grid [3], [4], [5]. For the better utilization and to overcome the shortage/surplus of the energy generated from the renewable inputs, and thereby improving the performance of the system, an energy storage bank is all-important in the dc microgrid. To integrate low-voltage battery bank (24–48 V) to the high-voltage dc bus (380–400 V), a dc–dc converter need to have the real essences, such as bidirectional power flow, high-voltage step-up/down capability, and high conversion efficiency [6], [7]. In the conventional step-up/down and cascaded converters, to obtain high-voltage conversion gain, the converter should operate at very high duty ratio and/or switch voltage stresses are equal to the dc grid voltage, this entails considerable high conduction and switching losses, resulting in poor conversion efficiency [8].

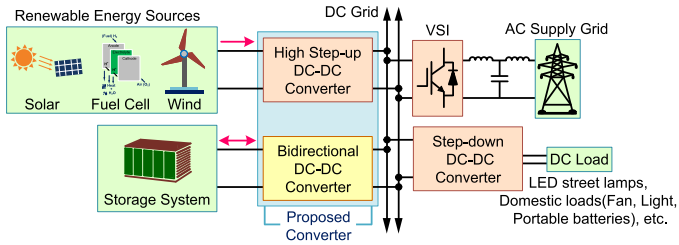

Fig. 1. Typical configuration of a hybrid distributed generating system.

In the development of high-voltage conversion ratio bidirectional converters, built-in transformer, dual active half bridge, and coupled inductor based no - isolated and isolated configurations are of the requisites, because of their simple configuration, winding adjustment, and enlarged voltage gain [9], [10], [11], [12], [13], [14], [15]. Interleaved flyback voltage conversion structure is one of the better alternatives to lower the current ripple at the low-voltage source. However, leakage inductance is the major concern, due to this a clamp circuit is indeed needful [15], [16], [17], [18], [19], [20], [21] against undesired high turn-OFF voltage transients (dv_f/dt) around the low-voltage switch. Severe limitations of RCD clamp are greatly sorted-out by a passive regenerative clamp/snubbers, such as dual-LCD and CD clamp circuits [17], [21]. Adjoining of capacitor and active switch-based voltage multiplier rectifier cells to the coupled inductors will result in further enhancement of voltage conversion gain, reduced switch voltage stress, and improved efficiency [16], [18], and [20]. Furthermore, various techniques are used to improve switching-losses in addition to the eradication of voltage spikes, such as synchronous rectification, quasi-resonance

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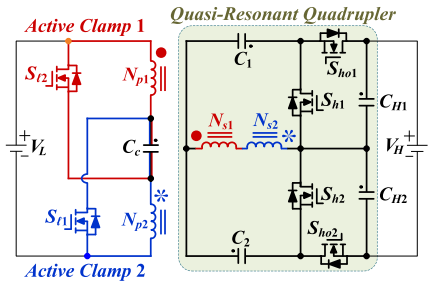


Fig. 2. Proposed isolated high-conversion-gain bidirectional dc–dc converter.

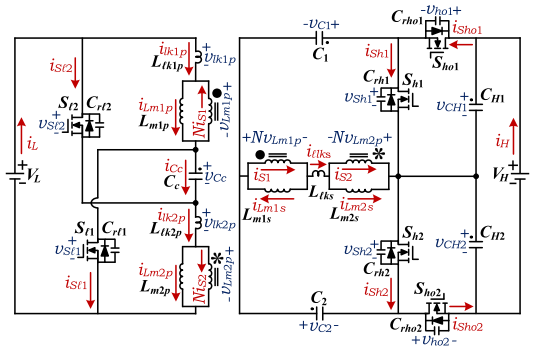


Fig. 3. Equivalent model of proposed converter showing element notations.

principle and also, by forming an active clamp circuit, i.e., insertion of auxiliary switches and reusing leakage inductance, thus soft-switching is employed to the devices in [15], [16], [18], [19], [20], [21], [22], [23], and [24]. Diode operation of a bidirectional converter is actualized by the parasitic *p–n* junction diode(body-diode) of the active switch. However, high reverse recovery time of the internal-diodes resulting in a considerable high switching losses during both the directions of power flow. The aforementioned problem can be appreciably resolved by implementing soft-switching to the body-diodes of the active devices [15]. Galvanic isolation is advisable according to most risk management and battery bank maintenance regulations brought in the grid-connected system. The converters presented in [16], [17], [18] maintain galvanic isolation between battery bank and dc bus and also achieves high conversion ratio with flexible turns ratio using built-in-transformer and flyback transformers by optimizing the components. In [19], T-type neutral clamp circuit with phase-shift power flow control are employed, hence, the converter obtains full range soft-switching and improved efficiency.

This article proposes a novel isolated bidirectional converter with soft-switching for high-voltage step-up/down applications and is shown in Fig. 2. High-voltage conversion gain is achieved in the proposed converter at reduced turns and duty ratios by integrating galvanic isolation structured flyback energy conversion circuit to the resonant switched voltage quadrupler cell. Voltage stresses imposed on LV and HV stage switches are substantially lowered, therefore, low-voltage rated switches can be utilized to mitigate the conduction losses and for the better performance of the converter. Due to the dual flyback energy conversion configuration, the coupled inductors stored energies are nearly equally distributed and continuously transferred to the load throughout the switching cycle. Moreover, the high-gain switched multiplier stands for balanced rectification/inversion due to its inherent voltage balancing property. In addition to this, enormous turn-OFF voltage spikes around mosfets due to parasitic ringing are extensively clipped-off to a secure level using active voltage-clamping-circuit and also reuses the leakage energy. Unlike common switch grounded converters with active clamp circuits (by employing additional/auxiliary switches) at the LV stage, the proposed clamp is realized with optimizing clamp elements and beneficially engaging the leakage inductance. Owing to this, the proposed topology stands for soft-switching in either direction of power flow and minimized switching losses. This further allows high switching frequency operation, which brings-down the size of the magnetic and filtering components. During the power flow from V_L to V_H, zero-voltage switching (ZVS) turn-ON achieved to LV stage switches at-most-load conditions, further, turn-OFF switching currents of the LV switches attains a low peak value. Quasi-resonance operation achieves ZVS turn-ON and zero-current switching (ZCS) turn-OFF for body-diodes of all the HV stage switches. Furthermore, during the power flow from V_H to V_L, negligible turn-ON losses and reduced turn-OFF losses are achieved for all the MOSFETS. The proposed converter avails the key benefits of enhanced voltage conversion gain, reduced switch voltage stresses, smooth switching transitions, compact structured coupled inductors, bidirectional soft-switching, and galvanic isolation.

The rest of this article is organized as follows. Description and operation of the proposed topology are discussed in Section II. Voltage gain derivation and semiconductor stress analysis are presented in Section III. Design guidelines, soft-switching condition, and performance attributes of high-gain bidirectional converters are described in Section IV. Experimental results of the laboratory prototype are demonstrated in Section V. Finally, Section VI concludes this article.

II. Circuit Description and Operation

Fig. 3 illustrates an equivalent circuit model of the proposed ZVS–ZCS high-gain bidirectional converter. The dual coupled inductors are configured as primary and secondary referred equivalent magnetizing and leakage inductances, denoted by $(L_{m1p},\ L_{m2p})$, $(L_{m1s},\ L_{m2s})$, $(L_{lk1p},\ L_{lk2p})$, and $(L_{lks} = L_{lk1s} + L_{lk2s})$, respectively. Primary and secondary winding turns of the coupled inductors denoted as $(N_{p1},\ N_{s1})$ and $(N_{p2},\ N_{s2})$, respectively. During step-up operation (i.e., power flows from V_L to V_H), complementary gating inputs with a sufficient dead-time are given to the low-voltage switches $(S_{l1},\ S_{l2})$ such that the coupled inductors magnetizes alternately in a switching cycle. This ensures continuous and successive rising and falling currents through the magnetizing inductors $(L_{m1p},\ L_{m2p})$, i.e., continuous conduction mode (CCM) operation. Thus, full-wave rectification with low ripple-voltage prevails at the high-voltage side. The body-diodes $(S_{h\_D(1,2)},\ S_{h\_D_{(o1,o2)}})$ of high-voltage switches $(S_{h(1,2)},\ S_{h(o1,o2)})$ together with capacitors $(C_{(1,2)},\ C_{(H1,H2)})$ forms the resonant voltage quadrupler rectifier circuit. The parasitic capacitors of low-voltage and high-voltage switches are (C_{rl1}, C_{rl2}) and $(C_{rh(1,2)}, C_{rh(o1,o2)})$, respectively. During the step-up operation, the leakage inductance L_{lks} together with capacitors C_1, C_2 establishes quasi-resonance for two times in an active switch cycle. Because of this resonating pulse, the body-diodes $(S_{h\_D_{o1}},\ S_{h\_D_2})$ and $(S_{h\_D_1},\ S_{h\_D_{o2}})$, successively and assuredly commutates with zero-current turn-OFF (ZCS) to alleviate the switching losses. The multiplier's

capacitors C_{H1} and C_{H2} are also utilized to diminish ripple in the grid-side voltage source (V_H). Arising of voltage surges across the MOSFETS due to leakage inductance, is an inevitable consequence during switch turn-ON transition. Nevertheless, in the proposed converter, without employing additional switches (auxiliary switches), an active clamping is formed consecutively by the LV switches (S_{l1}, S_{l2}) together with resonant-clamp-capacitor $C_{\mathbf{C}}$.

Indeed, this clamp effectively restrains the large impulse voltages across S_{l1} and S_{l2}. In addition to this, a resonance formed by effectively utilizing the leakage inductances (L_{lk1p}, L_{lk2p}) along with the clamp capacitor $C_{\mathbf{C}}$ achieves, a wide-load-range ZVS (active clamping) for S_{l1} and S_{l2}, thereby, eliminates the turn-ON transition losses. Unlike step-up operation, the gating inputs are withdrawn from the LV side switches (S_{l1}, S_{l2}) during the step-down operation (i.e., power flows from V_H to V_L). Besides, the HV side switches $S_{h(o1,2)}$ and $S_{h(1,o2)}$ conducts alternately by triggering them complementarily. Moreover, body-diodes ($S_{l\_D_1}$, $S_{l\_D_2}$) of S_{l1} and S_{l2} consecutively provides path to transfer the stored energy in coupled inductors to the LV source. During the step-down operation, all the high-voltage switches ($S_{h(1,2)}$, $S_{h(o1,o2)}$) are turned-ON with ZVS and body-diodes ($S_{l\_D_1}$, $S_{l\_D_2}$) of both the low-voltage MOSFETS are switching-OFF under ZCS conditions. Simplified circuit study and analysis of the proposed bidirectional topology is discussed in detail with the following considerations.

1) Instantaneous magnetizing currents of the inductors never attains zero, the converter firmly operates in CCM.
2) ON-state resistance ($R_{ds(\mathrm{ON})}$) of low-voltage and high-voltage MOSFETS are neglected. Meanwhile, their drain to source capacitances are actualized.
3) Voltages across filter and multiplier capacitors remains constant and equal to their applied ideal voltage stresses.
4) Parasitic resistances, i.e., equivalent series resistance (ESRs) of all capacitors and inductor windings and, core losses are neglected.
5) Coupling coefficients of two-winding identical flyback transformers are written as $k = \frac{L_{m1p}}{L_{m1p}+L_{lk1p}} = \frac{L_{m2p}}{L_{m2p}+L_{lk2p}}$ and turns ratios are expressed as $N = \frac{N_{s1}}{N_{p1}} = \frac{N_{s2}}{N_{p2}}$.
6) Leakage inductors accumulates sufficient energy, to fully discharge the parasitic-capacitors of the switches and, consequently turns-ON their body-diodes.

A. Step-Up Stage Operation

During step-up stage (i.e., power flows from V_L to V_H), the converter is merely controlled through complementary switching of LV side switches (S_{l1}, S_{l2}). One complete switch cycle operation of the step-up stage can be sorted-out by the twelve modes. Their subsequent mode of operations and typical switching-waveforms including time intervals are demonstrated in Figs. 4 and 5, respectively.

Mode 1 {$[t_o - t_1]$; Fig. 4(a)}: At time $t = t_o$, low-voltage side switch S_{l2} remains in OFF state whereas, switch S_{l1} commenced in forward conduction, i.e., drain to source. Inductor ($L_{m1p} + L_{lk1p}$) is in storing mode rather, the inductor ($L_{m2p} + L_{lk2p}$) release its energy to the HV stage. Hence, alternately and linearly, the magnetizing currents $i_{L_{m1p}}(t)$ and $i_{L_{m2p}}(t)$ are rising and falling, respectively, and thence, an indication of

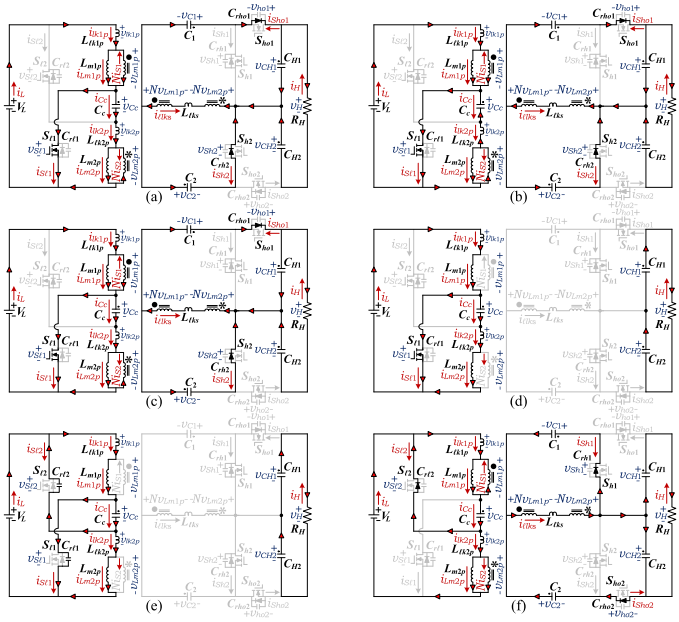


Fig. 4. Step-up stage: Instantaneous modes of operation of the proposed converter. (a) Mode 1 ($t_o t_1$). (b) Mode 2 (t_1 t_2). (c) Mode 3 (t_2 t_3). (d) Mode 4 (t_3 t_4). (e) Mode 5 (t_4 t_5). (f) Mode 6 (t_5 t_6).

the voltage multiplier rectifier cell is i_{lks}, which is due to the resulting induced magnetizing voltage, i.e., $N(v_{L_{m1p}}\ v_{L_{m2p}})$ applied to the series combination of secondary windings. This energy can forward-conduct and reverse-biases the body-diodes ($S_{h\_D_{o1}}$, $S_{h\_D_2}$) and ($S_{h\_D_1}$, $S_{h\_D_{o2}}$), respectively. In addition to this, secondary induced voltage $N(v_{L_{m1p}}$–$v_{L_{m2p}})$ charges the capacitor C_2, discharges C_1 and, also continuously powering the load through filter capacitors C_{H1} and C_{H2}. Also, the body-diode currents exhibits as quasi-sinusoidal nature owing to the resonance between secondary leakage inductance L_{lks} and switched capacitors (C_1, C_2), their current expressions are given by

$$\begin{cases} i_{L_{m1p}}(t) = i_{L_{m1p}}(t_o) + \frac{V_L - V_{lk1p}}{L_{m1p}}(t - t_o) \\ i_{L_{m2p}}(t) = i_{L_{m2p}}(t_o) - \frac{V_{Cc} + V_{lk2p}}{L_{m2p}}(t - t_o) \end{cases} \tag{1}$$

$$\begin{cases} i_{Sh\_D_{o1}}(t) = i_{Sh\_D_{o1}}(t_o) + \frac{V_{x_{o1}}(t)}{Z_{o1}} \sin\left(w_{o1}(t - t_o)\right) \\ i_{Sh\_D_2}(t) = i_{Sh\_D_2}(t_o) - \frac{V_{x_{o2}}(t)}{Z_{o2}} \sin\left(w_{o2}(t - t_o)\right) \end{cases} \tag{2}$$

where $V_{x_{o1}}(t) = N(V_L + V_{C_c}) - V_{CH_1}, Z_{o1} = \sqrt{\frac{p_{o1}}{q_{o1}}}, w_{o1} = \frac{1}{\sqrt{p_{o1}\, q_{o1}}}, p_{o1} = L_{lks}, q_{o1} = C_1; V_{x_{o2}}(t) = N(V_L + V_{C_c}), Z_{o2} = \sqrt{\frac{p_{o2}}{q_{o2}}}, w_{o2} = \frac{1}{\sqrt{p_{o2}\, q_{o2}}}, p_{o2} = L_{lks},$ and $q_{o2} = C_2$.

Mode 2 {$[t_1 - t_2]$; Fig. 4(b)}: At time $t = t_1$, the stored energy of the leakage inductor (L_{lk2p}) reaches zero as $i_{lk2p} = 0$, since then, the static energy of the clamp capacitor $C_{\mathbf{C}}$ begin to feed L_{lk2p}. Due to lossless clamp circuit operation with quasi-resonance, toward end of *Mode* 2, i.e., at $t = t_2$, capacitor $C_{\mathbf{C}}$ is reverse charged and the energy of L_{lk2p} once again becomes zero. A difference in V_L and ($V_{lk2p} + V_{L_{m2p}}$) yields the voltage stress $(V_{Sl2})_{\mathrm{Peak}}$ of S_{l2}. A negative and sinusoidal nature of current (i_{C_c}) through the resonant clamp capacitor can be expressed as

$$i \quad t \qquad \frac{V_{C_c} + V_{L_{m2}}}{} \qquad w \quad t \quad t$$

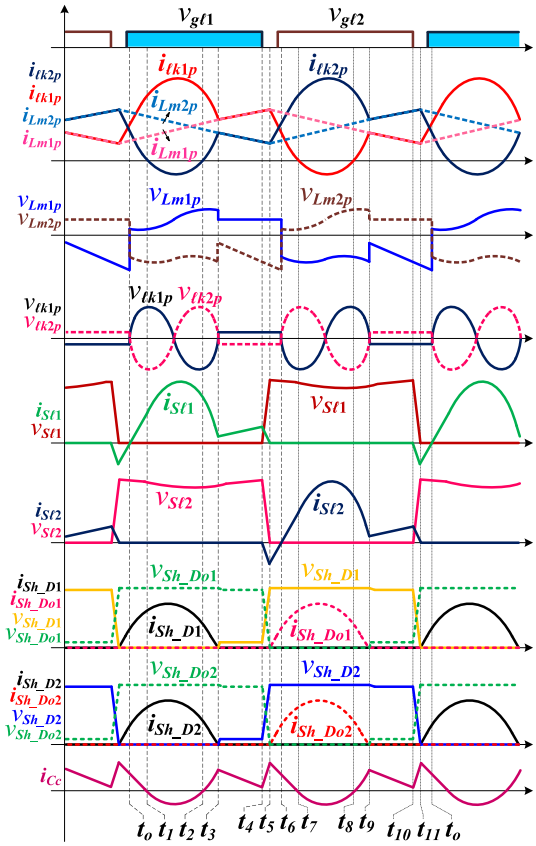


Fig. 5. Step-up operation: Typical switching-waveforms of the converter.

where $Z_{o3} = \sqrt{\frac{L_{lk2p}}{C_{\mathbf{C}}}}$ and $w_{o3} = \frac{1}{\sqrt{L_{lk2p}C_{\mathbf{C}}}}$

Mode 3 {[$t_2 - t_3$]; Fig. 4(c)}: From *Mode* 2 to *Mode* 3 transition, the current $i_{C_c} = i_{lk2p}$ direction gets reversed. At $t = t_2$, negatively polarized clamp capacitor $C_{\mathbf{C}}$ begin to release its static energy to the leakage inductor L_{lk2p}, therefore, i_{lk2p} increases from zero. At the end of this interval, quasi-resonant pulse current ($i_{lks} = i_{Sh\_D_{o1}} + i_{Sh\_D_2}$) reaches zero, thus completing the resonance segment operation of the circuit is completed, and body-diodes $S_{h\_D_{o1}}$ and $S_{h\_D_2}$ commutates under ZCS turn-OFF condition. As yet, $i_{C_c}(t)$ expression remains same as in *Mode* 2. Also, $i_{L_{m1p}}$, $i_{L_{m2p}}$, and $i_{Sh\_D_{(o1,2)}}$ expressions remains same as in *Mode* 1.

Mode 4 {[$t_3 - t_4$]; Fig. 4(d)}: At $t = t_3$, resonating currents $i_{Sh\_D_{(o1,2)}}$ descends to zero, hence, further conduction of body-diodes ($S_{h\_D_{o1}}$, $S_{h\_D_2}$) will not occur as energy or the driving force (i_{lks}) from $N(V_{L_{m1p}} - V_{L_{m2p}})$ is reached zero and the multiplier circuit is in floating state since current (i_{lks}) reversal in the windings is prevented by the flyback transformers. Therefore, body-diodes of all the high-voltage switches are in OFF state and from the very commencement of this interval, the load is merely powered by the filter capacitors C_{H1} and C_{H2}. Leakage currents are same as their respective magnetizing currents and can be written as

$$\begin{cases} i_{lk1p}(t) = i_{L_{m1p}}(t) = i_{L_{m1p}}(t_3) + \frac{V_L}{L_{m1p}+L_{lk1p}}(t - t_3) \\ i_{lk2p}(t) = i_{L_{m2p}}(t) = i_{L_{m2p}}(t_3) - \frac{V_{C_c}}{L_{m2p}+L_{lk2p}}(t - t_3). \end{cases} \quad (4)$$

Mode 5 {[$t_4 - t_5$]; Fig. 4(e)}: At $t = t_4$, the gating inputs are withdrawn from the switch S_{l1}, hence, turned-OFF. However, the output capacitances of S_{l1} and S_{l2}, i.e., (C_{rl1}, C_{rl2}) are forcibly and completely, charged and discharged, respectively, by the clamp circuitry. Thus, ZVS turn-ON action of switch S_{l2} is being commenced. Moreover, from *Mode* 4 to *Mode* 5 transition, the magnetizing energy states of L_{m1p} and L_{m2p} are interchanged, i.e., L_{m1p} energy increases from its minimum energy ($i_{L_{m1p},Min}$) level and L_{m2p} energy decreases from its maximum energy ($i_{L_{m2p},\text{Peak}}$) level; thereby making the driving force (i_{lks}) of the rectifier cell oppositely oriented owing to the polarity reversal of the resulting secondary induced voltage, $N(v_{L_{m1p}} - v_{L_{m2p}})$. Accordingly, voltages of body-diodes ($S_{h\_D_1}$, $S_{h\_D_{o2}}$) of the HV switches falls to zero, hence, turned-ON with ZCS. The time delay of *Mode* 5, i.e., $t_{(4-5)}$ is primarily caused by the internal-capacitances of S_{l1} and S_{l2}, but in fact, due to a quite smaller capacitances, this mode endures for a very short span and is given by

$$\begin{cases} i_{lk1p}(t) - i_{lk2p}(t) = i_{S_{l1}}(t) - i_{S_{l2}}(t) \\ I_{L_{m1p},Peak} - I_{L_{m2p},Min} = C_{rl1}\frac{d(V_{Sl1})}{dt} - C_{rl2}\frac{d(V_{Sl2})}{dt} \\ t_{(4-5)} = (C_{rl1} + C_{rl2})\frac{V_H}{2N} \Big/ \left(\frac{V_L}{2f_{sw}L_{mp}}\right). \end{cases} \quad (5)$$

Mode 6 {[$t_5 - t_6$]; Fig. 4(f)}: Leakage inductor L_{lk1p} acts as an energy repository and by exploiting it, body-diode of switch S_{l2} is turned-ON in this mode; hence, ZVS turn-ON is accomplished for switch S_{l2}. In addition, static energy of switched capacitor C_1 aiding with secondary induced electro motive force (emf) $N(v_{L_{m1p}} - v_{L_{m2p}})$ drives the load. Moreover, capacitor C_2 is charged by the secondary induced emf. Furthermore, a linear rise and fall of the inductor currents ($i_{L_{m2p}}$, $i_{L_{m1p}}$) signifies the magnetizing and demagnetizing states of the two coupled inductors L_{m2p} and L_{m1p}, respectively. The primary winding currents in relation to the switched capacitor cell currents can be written as

$$\begin{cases} i_{lk1p}(t) = i_{L_{m1p}}(t) - N[i_{Sh\_D_1}(t) + i_{Sh\_D_{o2}}(t)] \\ i_{lk2p}(t) = i_{L_{m2p}}(t) + N[i_{Sh\_D_1}(t) + i_{Sh\_D_{o2}}(t)]. \end{cases} \quad (6)$$

In view of a very close resemblance between further *Modes* (7–12) and discussed *Modes* (1–6), their in detail analysis is not discussed.

B. Step-Down Stage Operation

To perform the step-down stage operation (i.e., power flows from V_H to V_L), only HV side switches (S_{ho1}, S_{h2}) and (S_{h1}, S_{ho2}) are driven by the complementary gating inputs and this can be itemized by the 12 modes in one switching period. Fig. 6 portrays an equivalent-circuits corresponding to each of those modes and Fig. 7 demonstrates the typical switching-waveforms.

Mode 1 {[$t_o - t_1$]; Fig. 6(a)}: At the very commencement of this mode, i.e., at time $t = t_o$, the high-voltage multiplier's switches S_{h1} and S_{ho2} carry current from drain to source terminals whereas, their complementary switches S_{ho1} and S_{h2} remain in OFF state. The inductor currents $i_{L_{m2s}}$ and $i_{L_{m1s}}$ increases and decreases linearly, respectively. From this, it can be inferred that L_{m2s} and L_{m1s} are in energy storing and releasing states, respectively. The reflected primary winding voltage, $v_{L_{m1p}}$, (main driving force to feed the LV stage) is adequate to forward and reverse biases body-diode $S_{l\_D_1}$ and $S_{l\_D_2}$, respectively. Furthermore, the resultant secondary

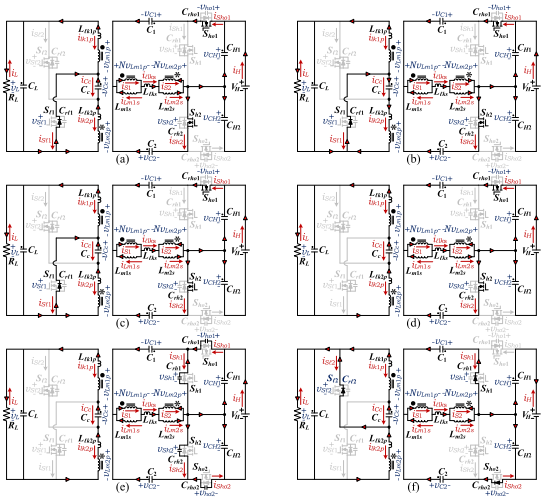


Fig. 6. Step-down stage: Instantaneous modes of operation of the proposed converter. (a) Mode 1 (t_o t_1). (b) Mode 2 (t_1 t_2). (c) Mode 3 (t_2 t_3). (d) Mode 4 (t_3 t_4). (e) Mode 5 (t_4 t_5). (f) Mode 6 (t_5 t_6).

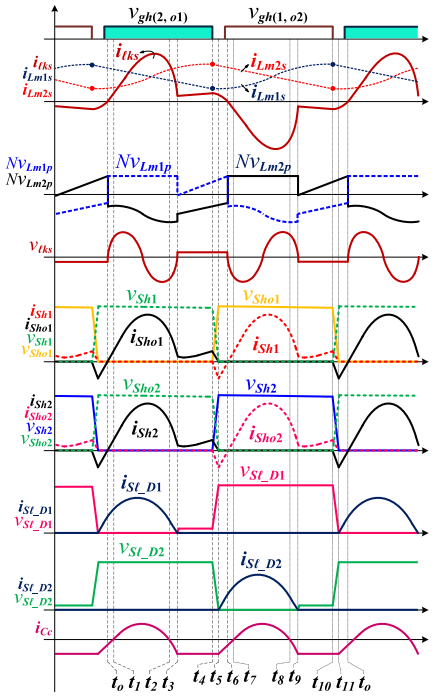


Fig. 7. Step-down operation: Typical switching-waveforms of the converter.

winding voltage $N(v_{L_{m1p}}–v_{L_{m2p}})$ charges and discharges the switched capacitors C_1 and C_2, respectively. Moreover, the LV switch currents are wave-shaped as the sinusoidal. Magnetizing inductor and switch current expressions are given by

$$\begin{cases} i_{L_{m1s}}(t) = i_{L_{m1s}}(t_o) - \frac{N(V_L - V_{lk1p})}{L_{m1s}}(t-t_o) \\ i_{L_{m2s}}(t) = i_{L_{m2s}}(t_o) + \frac{N(V_{C_c} + V_{lk2p})}{L_{m2s}}(t-t_o) \\ i_{Sh_{o1}}(t) = i_{Sh_{o1}}(t_o) - \frac{V_{x_1}(t)}{Z_1}\sin\left(w_1(t-t_o)\right) \\ i_{Sh_2}(t) = i_{Sh_2}(t_o) + \frac{V_{x_2}(t)}{Z_2}\sin\left(w_2(t-t_o)\right) \end{cases} \quad (7)$$

where $V_{x_1}(t) = N(V_L + V_{C_c}) - V_{CH_1}$, $Z_1 = \sqrt{\frac{p_1}{q_1}}$, $w_1 = \frac{1}{\sqrt{p_1 q_1}}$, $p_1 = L_{lks}$, $q_1 = C_1$; $V_{x_2}(t) = N(V_L + V_{C_c})$, $Z_2 = \sqrt{\frac{p_2}{q_2}}$, $w_2 = \frac{1}{\sqrt{p_2 q_2}}$, $p_2 = L_{lks}$ and $q_2 = C_2$.

Mode 2 {[$t_1 - t_2$]; Fig. 6(b)}: At time $t = t_1$, energy of L_{lk2p} becomes zero (i.e., $i_{lk2p} = 0$), from this level, the leakage current rises slowly and sinusoidally as it is energized by resonant clamp capacitor $C_{\mathbf{C}}$, therefore, direction of current into the inductor L_{lk2p} gets reversed. Quite close by this interval ending (i.e., at $t = t_2$), capacitor $C_{\mathbf{C}}$ is oriented toward positive polarity and the energy of L_{lk2p} again attains zero. The resonating current through clamp capacitor, $i_{C_c}(t)$, is expressed as

$$i_{C_c}(t) = -\frac{V_{C_c} + V_{L_{m2}}}{Z_3}\sin\left(w_3(t-t_1)\right) \quad (8)$$

where $Z_3 = \sqrt{\frac{L_{lk2p}}{C_{\mathbf{C}}}}$ and $w_3 = \frac{1}{\sqrt{L_{lk2p} C_{\mathbf{C}}}}$

Mode 3 {[$t_2 - t_3$]; Fig. 6(c)}: During this interval, positively polarized capacitor $C_{\mathbf{C}}$ begin to feed the inductor L_{lk2p}, hence, its current (i_{lk2p}) increases from zero. Also, current through $C_{\mathbf{C}}$ orient toward negative direction and its expression, $i_{C_c}(t)$, can be likewise regarded as in *Mode* 2. In addition, $i_{L_{m1s}}$, $i_{L_{m2s}}$, and $i_{Sh_{(o1,2)}}$ expressions remains same as in *Mode* 1.

Mode 4 {[$t_3 - t_4$]; Fig. 6(d)}: Resonant action of the circuit ends at time $t = t_3$ as the resonant pulse current $i_{Sl\_D_1}$ drops to zero, and body-diode ($S_{l\_D_1}$) of the switch S_{l1} commutates under ZCS condition. During this interval, primary leakage currents (i_{lk1p}, i_{lk2p}) expressions are same as the clamp capacitor current, $i_{C_c}(t)$.

Mode 5 {[$t_4 - t_5$]; Fig. 6(e)}: At $t = t_4$, switches (S_{ho1}, S_{h2}) are turned-OFF by removing their gating inputs. As a consequence, in this mode, parasitic-capacitors $C_{rh(o1,2)}$ and $C_{rh(1,o2)}$ of the HV stage switches are charged and discharged by $N(v_{L_{m1p}}–v_{L_{m2p}})$, respectively. Hence, ZVS turn-ON action of the switches S_{h1} and S_{ho2} are being initiated. From *Mode* 4 to *Mode* 5 transition, both the magnetizing inductors L_{m1s} and L_{m2s} moves into storing and releasing modes, respectively.

Mode 6 {[$t_5 - t_6$]; Fig. 6(f)}: Prior to the commencement of this mode, internal-capacitors of the switches S_{h1} and S_{ho2} are fully discharged. At $t = t_5$, body-diodes ($S_{h\_D_1}$, $S_{h\_D_{o2}}$) of the HV switches are turned-ON under ZCS, hence, their voltages falls to zero. Furthermore, a linear rise and fall of the inductor currents $i_{L_{m1s}}$ and $i_{L_{m2s}}$ denotes the magnetizing and demagnetizing states of L_{m1s} and L_{m2s}, respectively. In light of, a well-likeness between next *Modes* (7–12) and discussed *Modes* (1–6), the remaining half-cycle analysis is not explored here.

III. Steady-State Voltage Gain Analysis and Selection of Semiconductor Devices

A. Step-Up Mode Analysis

All filter and switched capacitors are assumed to be ideal voltage sources; hence, their voltage-ripple is not considered. The low-voltage switches S_{l1} and S_{l2} alternately conducts with time intervals of $D_{l_1} T_S = DT_S$ and $D_{l_2} T_S = (1 - D)T_S$, respectively. Hence, $D_{l2} = 1 - D_{l_1}$. Simplified boost mode voltage gain can be derived from *Mode* 1 and *Mode* 7 of the step-up stage operation of the proposed converter.

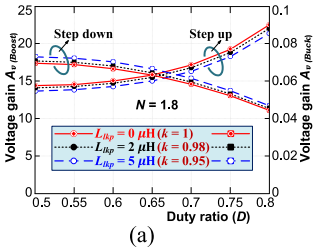


Fig. 8. Magnetic leakage affecting the conversion ratio (A_v) of proposed converter.

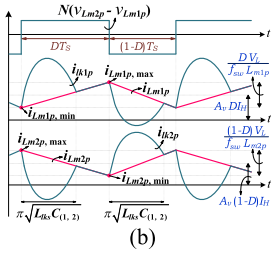


Fig. 9. Theoretical magnetizing and leakage currents of the coupled inductors.

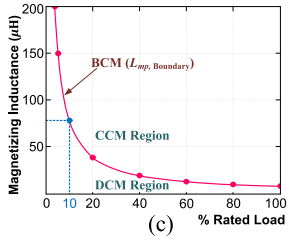


Fig. 10. Magnetizing inductance requirement for CCM operation of the proposed converter.

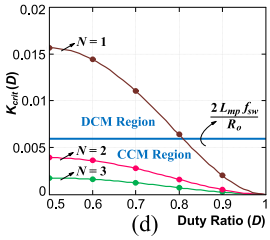


Fig. 11. Different parameters determining CCM region of the converter.

In *Mode* 1 ($t_o - t_1$) of the step-up stage operation, low-voltage switches S_{l1} and S_{l2} are in conduction and blocking states, respectively, thus, inductor L_{m1p} magnetizes (storing energy) and L_{m2p} demagnetizes (releasing energy) simultaneously and their corresponding voltages are given by

$$\begin{cases} V_{L_{m2p}}^{(D_{l_1})} - V_{L_{m1p}}^{(D_{l_1})} = \frac{-V_{C_2}}{N} = \frac{V_{C_1} - V_{CH_1}}{N} \\ V_{L_{m1p}}^{(D_{l_1})} = kV_L \ \& \ V_{L_{m2p}}^{(D_{l_1})} = -kV_{C_c} \end{cases} \tag{9}$$

where N and k are turns ratio and coupling coefficient, respectively.

In *Mode* 7 ($t_6 - t_7$) of the step-up stage operation, i.e., during OFF and ON states of the low-voltage devices S_{l1} and S_{l2}, respectively, L_{m1p} is powering the V_H (demagnetizes) and, L_{m2p} is accumulating the magnetic energy (magnetizes). Voltage equations of L_{m1p} and L_{m2p} are expressed as

$$\begin{cases} V_{L_{m2p}}^{(D_{l_2})} - V_{L_{m1p}}^{(D_{l_2})} = \frac{V_{C_1}}{N} = \frac{V_{CH_2} - V_{C_2}}{N} \\ V_{L_{m1p}}^{(D_{l_2})} = -kV_{C_c} \ \& \ V_{\mathrm{Lm2p}}^{(D_{l_2})} = kV_L. \end{cases} \tag{10}$$

Simplifying (10), one obtains

$$V_{L_{m1p}}^{(D_{l_2})} = kV_L - \frac{V_{C_1}}{N}. \tag{11}$$

From the flux-balancing of magnetizing inductors L_{m1p} and L_{m2p}, multiplier's switched and filter capacitor voltages can be obtained as

$$V_{C_1} = \frac{kNV_L}{D_{l_2}} \ \& \ V_{CH_1} = V_{CH_2} = \frac{V_{C_1}}{D_{l_1}} = \frac{V_{C_2}}{D_{l_2}}. \tag{12}$$

Terminal voltage of the converter at HV side is obtained as

$$V_H = V_{CH_1} + V_{CH_2} = \frac{2kNV_L}{D_{l_1} D_{l_2}}. \tag{13}$$

Boost mode voltage gain, $A_{v(\mathrm{Step-up})}$, of the proposed converter can be expressed as

$$A_{V(Step-up)} = \frac{V_H}{V_L} = \frac{2kN}{D(1-D)}. \tag{14}$$

Using step-up mode gain expression, from (14), converter's HV side bus voltage can be functioned as $V_H = f_n \langle D_{l_1} \times D_{l_2} \rangle$. A minimum bus voltage prevailed at maximum duty ratio product ($D_{l_1} = D_{l_2} = 0.5$) and is given by $V_{H,Min} = 8kNV_L$. Thus, the value of V_H exceeds its V_H, Min when coupled inductors are switched at $D_{l_1} \neq D_{l_2}$. Fig. 8 depicts the effect of leakage inductance (for different coupling coefficients, k) on boost and buck mode voltage gains, i.e., $A_{v(\mathrm{Step-up})}$ and $A_{v(\mathrm{Step-down})}$ of the converter.

During blocking state, all the LV switches (S_{l1}, S_{l2}) and HV switches ($S_{h\_D_{(o1,2)}}$, $S_{h\_D_{(1,o2)}}$) experiences maximum voltage stresses, which are expressed as

$$\begin{cases} (V_{Sl1})_{\mathrm{Peak}} = V_L - V_{L_{m1p}}^{(1-D)} = \frac{DV_H}{2N} \\ (V_{Sl2})_{\mathrm{Peak}} = V_L - V_{L_{m2p}}^{D} = \frac{(1-D)V_H}{2N} \\ \left(V_{Sh\_D_{(o1,2)}}\right)_{\mathrm{Peak}} = \left(V_{Sh\_D_{(1,o2)}}\right)_{\mathrm{Peak}} = \frac{V_H}{2}. \end{cases} \tag{15}$$

From (15), significantly lowered voltage stresses on the low-voltage switches can be noticed with the inclusion of multiplier cell in the proposed converter. Furthermore, by elevating the turns ratio this stress can be reduced. Maximum current stresses of LV devices (S_{l1}, S_{l2}) are expressed as

$$\begin{cases} i_{Sl1,Peak} = A_V(2D-1)I_H + \frac{2NDI_H}{(1-D)f_{sw}\sqrt{L_{lks}C}} \\ i_{Sl2,Peak} = A_V(1-2D)I_H + \frac{2N(1-D)I_H}{Df_{sw}\sqrt{L_{lks}C}} \end{cases} \tag{16}$$

where $C = C_1 = C_2$. The average currents of high-voltage switches, ($S_{h\_D_{(o1,2)}}$, $S_{h\_D_{(1,o2)}}$), are equal to HV bus current I_H, their instantaneous maximum currents are written as

$$\begin{cases} i_{Sh\_D_{(o1,2)},\mathrm{Peak}} = \frac{DI_H}{2(1-D)f_{sw}\sqrt{L_{lks}C}} \\ i_{Sh\_D_{(1,o2)},\mathrm{Peak}} = \frac{(1-D)I_H}{2Df_{sw}\sqrt{L_{lks}C}}. \end{cases} \tag{17}$$

B. Step-Down Mode Analysis

In the entire step-down mode analysis, duty cycles of high-voltage switches S_{ho1} and S_{h2} are considered as $D_{h_1} = 1 - D$ then, duty ratios of the active devices S_{h1} and S_{ho2} becomes $D_{h_2} = D$, therefore, $D_{h_1}T_S + D_{h_2}T_S = T_S$. From *Mode* 1 and *Mode* 7 of the step-down stage operation of the converter, the simplified buck mode voltage gain analysis is as follows.

In *Mode* 1 ($t_o - t_1$) of the step-down operation, the high-voltage active devices (S_{ho1}, S_{h2}) and (S_{h1}, S_{ho2}) are in ON and OFF states, respectively, and their switched inductors magnetizing and demagnetizing voltages ($v_{L_{m1p}}^{D_{h_1}}$ and $v_{L_{m2p}}^{D_{h_1}}$) are expressed as

$$\begin{cases} V_{L_{m1p}}^{(D_{h_1})} = kV_L \ \ \& \ \ V_{L_{m2p}}^{(D_{h_1})} = -kV_{C_c} \\ V_{L_{m2p}}^{(D_{h_1})} - V_{L_{m1p}}^{(D_{h_1})} = \frac{-V_{C_2}}{N} = \frac{V_{C_1} - V_{CH_1}}{N}. \end{cases} \tag{18}$$

In *Mode* 7 ($t_6 - t_7$) of step-down stage operation, during OFF and ON states of the active devices (S_{ho1}, S_{h2}) and (S_{h1}, S_{ho2}),

respectively, the inductor voltage expressions are obtained as

$$\begin{cases} V_{L_{m1p}}^{(D_{h_2})} = -kV_{C_c} \;\; \& \;\; V_{L_{m2p}}^{(D_{h_2})} = kV_L \\ V_{L_{m2p}}^{(D_{h_2})} - V_{L_{m1p}}^{(D_{h_2})} = \frac{V_{C_1}}{N} = \frac{V_{CH_2}-V_{C_2}}{N}. \end{cases} \tag{19}$$

Simplifying (19), one obtains

$$V_{L_{m1p}}^{(D_{h_2})} = kV_L - \frac{V_{C_1}}{N}. \tag{20}$$

From Volt-Sec balancing of the two inductors, switched and filter capacitor voltages are given by

$$V_{C_1} = \frac{kNV_L}{D} \;\&\; V_{CH_1} = V_{CH_2} = \frac{V_{C_1}}{1-D} = \frac{V_{C_2}}{D}. \tag{21}$$

Buck mode voltage conversion gain $A_{v(\text{Step}-\text{down})}$, of the converter is expressed as

$$A_{V(Step-down)} = \frac{V_L}{V_H} = \frac{D(1-D)}{2kN}. \tag{22}$$

The peak voltage stresses in blocking state of the LV stage switches ($S_{l\_D_1}$, $S_{l\_D_2}$) and HV stage switches ($S_{h(o1,2)}$, $S_{h(1,o2)}$) are given by

$$\begin{cases} \left(V_{Sl\_D_1}\right)_{\text{Peak}} = \frac{(1-D)V_H}{2N} \;\&\; \left(V_{Sl\_D_2}\right)_{\text{Peak}} = \frac{DV_H}{2N} \\ \left(V_{Sh_{(o1,2)}}\right)_{\text{Peak}} = \left(V_{Sh_{(1,o2)}}\right)_{\text{Peak}} = \frac{V_H}{2}. \end{cases} \tag{23}$$

From (23), the peak voltage stress across high-voltage switches are much lesser than V_H due to the establishment of voltage quadrupler cell, indeed this stress is 50% of the HV bus voltage (V_H). Peak current stress expressions of LV and HV devices are given by

$$\begin{cases} i_{Sl\_D_1,\text{Peak}} = A_v(1-2D)I_H + \frac{2N(1-D)I_H}{Df_{sw}\sqrt{L_{lks}C}} \\ i_{Sl\_D_2,\text{Peak}} = A_v(2D-1)I_H + \frac{2NDI_H}{(1-D)f_{sw}\sqrt{L_{lks}C}}. \end{cases} \tag{24}$$

Since $C = C_1 = C_2$, the peak currents through HV side switches are expressed as

$$\begin{cases} i_{Sh(o1,2),\text{Peak}} = \frac{(1-D)I_H}{2Df_{sw}\sqrt{L_{lks}C}} \\ i_{Sh(1,o2),\text{Peak}} = \frac{DI_H}{2(1-D)f_{sw}\sqrt{L_{lks}C}}. \end{cases} \tag{25}$$

IV. Design Considerations and Comparison Analysis of Proposed Converter

A. Boundary Condition and Design of Coupled Inductors

As can be seen in Fig. 9, the instantaneous currents of L_{m1p} and L_{m2p} are unidirectional for all time and they never attains zero, thus, the converter operates in CCM. A critical inductance of L_{m1p} and L_{m2p} obtained at boundary conduction mode, i.e., $L_{mp,\text{Boundary}}$, as explained in [8] and [25], determines the minimum load requirement in order to maintain the converter in CCM. At boundary, a minimum current through L_{m1p} and L_{m2p}, at the valley, becomes zero and the corresponding current expressions are given by

$$\begin{cases} i_{L_{m(1p,2p)}}(t) = I_{L_{m(1p,2p)}}^{Avg} - \frac{1}{2}\Delta i_{L_{m(1p,2p)}} = 0 \\ I_{L_{m(1p,2p)}}^{Avg} = I_{lk(1p,2p)}^{Avg} = \frac{I_{L_{m(1p,2p)}}^{Peak}}{2} = \left(\frac{DV_L}{2f_{sw}L_{m1p}} \& \frac{(1-D)V_L}{2f_{sw}L_{m2p}}\right). \end{cases}$$

Mean magnetizing currents also obtains from the lossless gain expression, $\frac{V_H}{V_L} = \frac{I_L}{I_H} = A_v$. Thus, a critical magnetizing inductance value, of the aforementioned twin-structured dual coupled inductors, which assuredly retains the converter in CCM can be derived as

$$\begin{cases} I_{L_{m1p}}^{Avg} = \left(\frac{2N}{1-D}\right)\frac{P_o}{V_H}; \;\; I_{L_{m2p}}^{Avg} = \left(\frac{2N}{D}\right)\frac{P_o}{V_H} \\ \frac{2L_{mp}f_{sw}}{R_{oB}} > \frac{D^2(1-D)^2}{4N^2} = K_{Crit}^{(D)}. \end{cases} \tag{26}$$

The plot of Fig. 10 denotes the magnetizing inductance needed in inverse proportion to the wide range loads. As can be seen, the computed $L_{mp,\text{Boundary}}$ is 77.38 μH at 10% of rated power, $N = 1.8$, $f_{\text{sw}} = 75$ kHz, and $D = 0.5$, with which the measured inductances are obtained as $L_{mp} = L_{m1p} = L_{m2p} = 96.84\ \mu H$. The converter constant ($K_{Crit}^{(D)}$) in relation to turns ratio (N) and duty ratio (D) is depicted with multiple plots in Fig. 11. It is clear that, in the achievement of assured CCM, turns ratio (N) is of the essence, and at higher turns ratios confirmed CCM obtains as can be seen in Fig. 11. On the contrary, winding parasitic effects due to larger turns ratio, higher conduction losses of semiconductors and passive components due to larger duty ratio operation, narrows the CCM region. Nonetheless, at the moderate values of N and D as aforementioned, the prototype's constant is designed as $\frac{2L_{mp}f_{sw}}{R_{oB}} = 0.0061$, which ensures CCM operation of the converter for wide-load range.

B. Selection of Capacitor and Condition for Soft Switching

1) Resonant Clamp Capacitor C_c: In forward conduction of the switch S_{l1}, a resonant ringing with a substantial huge amplitude may occur around the switch S_{l2}, because of the resonance between clamp capacitor $C_{\mathbf{C}}$ and resonant inductor (L_{m2p} + L_{lk2p}). To restrain the undesired surplus oscillations, as described in [22], 50% of the resonant period must be longer than the maximum OFF state time interval of the switch S_{l2} and can be expressed as

$$\pi\sqrt{(L_{m2p}+L_{lk2p})C_{\mathbf{C}}} \gg (1-D)T_S. \tag{27}$$

This can be rewritten as

$$C_{\mathbf{C}} > \frac{(1-D_{Min})^2}{\pi^2(L_{m2p}+L_{lk2p})f^2{}_{sw}}.$$

Likewise, to restrict the undesired ringing across S_{l1}, the following constraint has to be realized:

$$C_{\mathbf{C}} > \frac{D^2{}_{Max}}{\pi^2(L_{m1p}+L_{lk1p})f^2{}_{sw}}.$$

To prevent excessive ringing across both the low-voltage switches S_{l1} and S_{l2}, the clamp capacitor C_c can be realized under the following constraint as

$$C_{\mathbf{C}} > Max\left\{\frac{(1-D_{Min})^2}{\pi^2(L_{m2p}+L_{lk2p})f^2{}_{sw}}, \frac{D^2{}_{Max}}{\pi^2(L_{m1p}+L_{lk1p})f^2{}_{sw}}\right\}.$$

2) ZVS Condition for Low-Voltage MOSFETs: ZVS turn-ON is achieved for the switches (S_{l1}, S_{l2}) by realizing the following key considerations.

1) Both L_{lk1p} and L_{lk2p} acquire plentiful leakage energy to completely evacuate static carriers and make charge free

TABLE I
PERFORMANCE COMPARISON AMONG MAGNETIC COUPLED BASED HIGH-GAIN CONVERTERS

Parameter	Converter in [15]	Converter in [16]	Converter in [17]	Converter in [18]	Converter in [19]	Converter in [27]	Converter in [28]	Converter in [32]	Proposed Converter
$A_{v\,(\text{Step-up})} = \left(\frac{V_H}{V_L}\right)$	$\frac{2N+1}{1-D}$	$\frac{2N}{1-D}$	$\frac{2ND}{1-D}$	$\frac{2N}{1-D}$	$\frac{N+2}{N(1-D)}$	$\frac{N+2}{1-D}$	$\frac{N}{(1-D)^2}$	$\frac{N}{1-2D}$	$\frac{2N}{D(1-D)}$
$A_{v\,(\text{Step-down})} = \left(\frac{V_L}{V_H}\right)$	$\frac{D}{2N+1}$	$\frac{D}{2N}$	$\frac{D}{2N(1-D)}$	$\frac{D}{2N}$	$\frac{ND}{N+2}$	$\frac{D}{N+2}$	$\frac{D^2}{N}$	$\frac{1-2D}{N}$	$\frac{D(1-D)}{2N}$
LV side switch voltage stress	$\frac{V_H}{2N+1}$	$\frac{V_H}{2N}$	$\frac{V_H}{2ND}$	$\frac{V_H}{2N}$	$\frac{NV_H}{N+2}$	$\frac{V_H}{N+2}$	$\frac{V_H}{N}$	$\frac{V_H}{2ND}$	$\frac{DV_H}{2N}$
HV side switch voltage stress	$\frac{2NV_H}{2N+1}$	V_H	$\frac{V_H}{2D}$	V_H	$\frac{2V_H}{N+2}$	$\frac{(N+1)V_H}{N+2}$	V_H	$\frac{V_H}{2D}$	$\frac{V_H}{2}$
Magnetic Cores	3	3	3	3	4	1	2	2	2
Windings	4	4	5	4	5	2	3	3	4
MOSFETs	6	6	4	4	8	4	6	8	6
Diodes	0	0	6	0	0	0	0	0	0
Low-voltage witch clamp	Active clamp	Active clamp	Passive snubber	No clamp	Active clamp	ZVT Snubber	ZVT Snubber	No clamp	Active clamp
Bidirectional soft-switching	Yes	No	No	No	Yes	Partial	Partial	No	Yes
MOSFETs switching	ZVS turn-ON	ZVS turn-ON	Hard switching	ZVS turn-ON	ZVS turn-ON	ZVS turn-ON	ZVS turn-ON	ZVS turn-ON	ZVS turn-ON
Body-diode/diodes switching	ZCS turn-OFF	Hard switching	Hard switching	Hard switching	ZCS turn-OFF	Hard switching	Hard switching	Hard switching	ZVS turn-ON & ZCS turn-OFF
Switching frequency	100 kHz	50 kHz	40 kHz	50 kHz	50 kHz	100 kHz	40 kHz	>100 kHz	75 kHz
Isolation	No	Yes	Yes	Yes	No	No	Yes	Yes	Yes
Full load $\%\eta$ (boost mode)	95.4% (900 W)	93.8% (1.5 kW)	95.5% (400 W)	95.6% (200 W)	96.5% (1 kW)	96% (200 W)	95.4% (500 W)	–	95.8% (600 W)
Full load $\%\eta$ (buck mode)	95.2% (900 W)	94.6% (1.5 kW)	95.4% (400 W)	96.3% (200 W)	96.5% (1 kW)	95.8% (200 W)	94.1% (500 W)	–	95.6% (600 W)

state of the internal-capacitors C_{rl2} and C_{rl1} to forward bias parasitic-diodes of switches S_{l2} and S_{l1}, respectively.

2) Enough dead-time exists between the gating pulses of S_{l1}, S_{l2} to charge and discharge C_{rl1} and C_{rl2} in the consecutive switching transitions.

Currents flowing into the leakage inductors L_{lk1p} and L_{lk2p} at the instants $t = t_4$ and $t = t_{10}$, respectively, are expressed as

$$\begin{cases} I_{lk1p}(t_4) = I_{L_{m1p}}^{Max} = A_V D I_H + \frac{DV_L}{2f_{sw}L_{m1p}} \\ I_{lk2p}(t_{10}) = I_{L_{m2p}}^{Max} = A_V(1-D)I_H + \frac{(1-D)V_L}{2f_{sw}L_{m2p}}. \end{cases} \tag{28}$$

At the instant $t = t_4$, for S_{l1} and S_{l2}, turn-OFF (linear decay of S_{l1} current till it becomes zero) and turn-ON (linear rise of current into internal-diode of S_{l2}) switching instants are being commenced, respectively. Subsequently, energy accumulated in L_{lk1p} is sufficiently large to totally discharge drain to source parasitic capacitor (C_{rl2}) of the switch S_{l2} just prior to its conduction. Furthermore, using (28), ZVS condition for the switch S_{l2} can be expressed as

$$\begin{cases} 0.5L_{lk1p}I_{lk1p(t_4)}^2 \geq 0.5C_{r(eff)}V_{S_{l2}}^2 \\ I_{lk1p}(t_4)\Big|_{\text{ZVS}-(S_{l2})} \geq \frac{\sqrt{(1-2D+2D^2)}V_H}{2N}\sqrt{\frac{C_{r(eff)}}{L_{lk1p}}} \end{cases} \tag{29}$$

where $C_{r(\text{eff})} = C_{rl1} + C_{rl2}$. Similarly, using $I_{lk2p}\ (t_{10})$ from (28), ZVS condition for the switch S_{l1} can be expressed as

$$I_{lk2p}(t_{10})\Big|_{\text{ZVS}-(S_{l1})} \geq \frac{\sqrt{(1-2D+2D^2)}V_H}{2N}\sqrt{\frac{C_{r(eff)}}{L_{lk2p}}}. \tag{30}$$

3) ZCS Condition for High-Voltage MOSFETs: By utilizing the quasi-resonance principle, i.e., a resonance formed between resultant secondary winding leakage inductance (L_{lks}) and switched capacitors C_1 and C_2, internal-diodes ($S_{h\_D_{o1}}$, $S_{h\_D_2}$) of the high-voltage switches (S_{ho1}, S_{h2}) can be turned-OFF with the accomplishment of zero-current-switching. To achieve this, time span of the resonant pulse should be shorter than the minimum ON-state time interval of the switch S_{l1} and is given by

$$(C_1, C_2)\Big|_{\text{ZCS}-(S_{h\_D_{o1}}, S_{h\_D_2})} < \frac{2D_{Min}^2}{\pi^2 L_{lks} f_{sw}^2}.$$

Likewise, ($S_{h\_D_1}$, $S_{h\_D_{o2}}$) are turned-OFF with ZCS by satisfying the following inequality

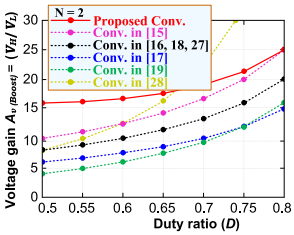
$$(C_1, C_2)\Big|_{\text{ZCS}-(S_{h\_D_1}, S_{h\_D_{o2}})} < \frac{2(1-D_{Max})^2}{\pi^2 L_{lks} f_{sw}^2}.$$

For the successful implementation of ZCS to the internal-diodes of all the high-voltage switches, selection of the capacitors C_1 and C_2 can be made under the following constraint:

$$(C_1, C_2) < Min\left\{\frac{2D_{Min}^2}{\pi^2 L_{lks} f_{sw}^2}, \frac{2(1-D_{Max})^2}{\pi^2 L_{lks} f_{sw}^2}\right\}. \tag{31}$$

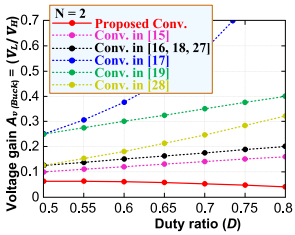
C. Performance Comparison of Proposed Converter

On the basis of key functioning parameters and accomplishments listed in Table I, the proposed converter is compared with high step-up/down bidirectional converters presented in [15], [16], [17], [18], [19]. The proposed converter has a lesser or equal number of magnetic components and semiconductors compared to the other presented converters. By virtue of simple customization of coupled inductor or built-in-transformer's turns ratio, required voltage gain can be acquired in most of the listed converters. In Figs. 12 and 13, comparison plots of voltage conversion gains during both boost ($A_{v(\text{Step}-\text{up})}$) and



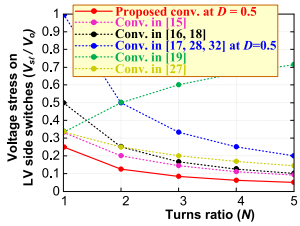
(a)

Fig. 12. Step-up mode: Voltage gain comparison among high conversion ratio bidirectional converters.



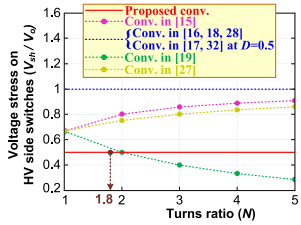
(b)

Fig. 13. Step-down mode: Voltage gain comparison among high conversion ratio bidirectional converters.



(c)

Fig. 14. LV stages MOSFETS normalized voltage stresses versus turns ratio.



(d)

Fig. 15. HV stage MOSFETS normalized voltage stresses versus turns ratio.

buck ($A_{V(\text{Step}-\text{down})}$) modes as the function of duty cycle (D) are depicted. It can be noticed, from Fig. 12, a highest boost mode gain ($\frac{V_H}{V_L}$), from Fig. 13, a lowest buck mode gain ($\frac{V_L}{V_H}$), and from Fig. 14, a reduced voltage stresses on LV side switches are achieved by the proposed converter. Moreover, this stress is substantially lesser than V_H, hence, MOSFETS with low V_{ds} rating (inherits a very low ON-resistance) are availed in LV side switches of the proposed converter.

The turn-OFF voltage spikes across LV MOSFETS are slightly high in [18] due to the absence of clamp circuit, however, a considerable low turn-ON loss is achieved due to synchronous rectification. Furthermore, by employing a lossless dual-LCD clamp, turn-OFF voltage spikes across LV switches are eliminated in [17]. Furthermore, by developing an active clamp circuit, i.e., insertion of auxiliary switches and by engaging leakage inductance, soft-switching is obtained to the MOSFETS in [15], [16], and [19], as a result, switching-losses are lowered in addition to the eradication of voltage spikes. Moreover, without employing additional switches (auxiliary or clamp switches), a more comprehensive solution (an active clamp at LV side) is made with resonance principle and adopted in the proposed converter to alleviate inductive voltage spikes and it results in the improved switching losses of the MOSFETS. Thus, at the very limited leakage inductance and without operating at larger duty ratio, ZVS turn-ON is achieved for both the LV switches below 20% of rated-load and a wide-load-range ZVS turn-ON is obtained for all HV side controlled switches. This will improve the device count of the clamp circuit, switching losses and loss due to converter operating at larger duty cycle. Thus, overall improvement in the efficiency of the proposed converter is obtained. Moreover, owing to the quasi-resonance operation, body-diodes of all the MOSFETS carry sinusoidal wave-shaped currents leads to a very small turn-ON (ZVS) parasitic-diode losses in the proposed converter. Furthermore, guaranteed ZCS turn-OFF of all internal-diodes of the switches in the proposed converter resulting into a lowered body-diode losses compared to those converters. This conveys that the proposed converter achieves bidirectional soft-switching.

Also, voltage stresses of HV side MOSFETS in [16], [17], and [18] are equal to the dc-bus voltage (V_H). Nevertheless, this stress is equal to 50% of V_H in the proposed converter and as can be seen in Fig. 15, the proposed converter obtains a reduced device voltage stress at the designed turns ratio $N = 1.8$. In addition to this, proposed converter and converters in [16], [17], and [18] provide a galvanic isolation, thus, enhances the safety requisites of the system by isolating both the dc buses (i.e., V_L and V_H). By bringing together all the abovementioned merits, the proposed topology is put forwarded for the high step-up/down bidirectional converter applications in energy storage systems to the dc microgrid.

TABLE II
PROPOSED CONVERTER SPECIFICATIONS

Components	Specifications
Power P_o	600 W
Input voltage V_L	26 V
Output voltage V_H	380 V
Switching frequency f_{SW}	75 kHz
Low-voltage side MOSFETS	FDP075N15A
High-voltage side MOSFETS	IXTQ44N50P
Resonant capacitor C_C	0.76 μF, film
Switched capacitors C_1 and C_2	0.52 μF, film
Magnetizing inductances L_{m1p} and L_{m2p}	96.84 μH, EE type
Magnetizing inductances L_{m1s} and L_{m2s}	313.8 μH, Sendust Core
Primary leakage inductances L_{lk1p} and L_{lk2p}	1.86 μH and 1.89 μH
Secondary leakage inductances L_{lk1s} and L_{lk2s}	6.03 μH and 6.14 μH
Switch parasitic capacitors $C_{rl_{(1,2)}}$ and $C_{rh_{(1,2,3,4)}}$	516 pF and 639 pF
Winding turns ratio N	1.8:1
Filter capacitor C_L	2200 μF, electrolytic
Filter capacitors C_{H1} and C_{H2}	94 μF, electrolytic

V. EXPERIMENTAL RESULTS AND DISCUSSION

A 600 W laboratory prototype is built up to validate the design analysis of proposed soft-switched high-gain bidirectional converter. Furthermore, a couple of experiments are carried-out for the power flow in both the directions and, the obtained results are demonstrated and discussed in this section. Voltage conversion gains in both the directions through flyback inductors, multiplier circuit and soft-switching attributes are presented using the built set-up measured at the dc-bus voltages $V_L = 26$ V, $V_H = 380$ V, and designed frequency 75 kHz. Coupled inductors are configured by setting the turns ratio as $N = \frac{N_{s1}}{N_{p1}} = \frac{N_{s2}}{N_{p2}} = 1.8$. In Table II, element ratings and component specifications, which are utilized for implementing the hardware prototype are tabulated.

Fig. 16 shows experimental waveforms of the proposed converter during the step-up operation at rated power $P_o = 600$ W. In Fig. 16(a), currents flowing through low-voltage switches (S_{l1}, S_{l2}) and body-diodes of the high-voltage switches (S_{h1}, S_{ho1})

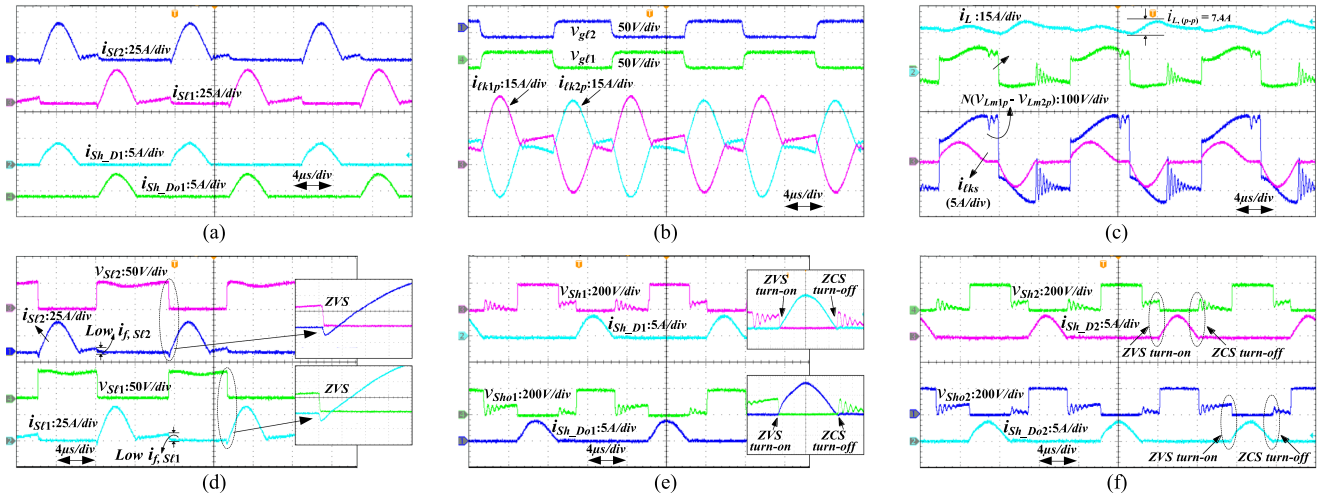


Fig. 16. Step-up operation: Experimental results at full load. (a) Currents through the LV side switches (S_{l1}, S_{l2}) and body-diodes of the HV side switches (S_{h1}, S_{ho1}). (b) Gate pulses of switches S_{l1} (V_{gl1}) and S_{l2} (V_{gl2}) and Primary currents of both the coupled inductors i_{lk1p} and i_{lk2p}. (c) Current (i_L) drawn from LV source, Induced voltage at the secondary winding of the coupled inductor (NV_{Lm1p}), Net voltage appears across series combination of secondary windings $N(V_{Lm1p}–V_{Lm2p})$ and Current through secondary windings (i_{lks}). (d) Voltage stresses and currents through the LV switches S_{l1} and S_{l2} with zoomed ZVS region. (e) Voltage stresses and currents through the body-diodes of the HV side switches S_{h1} and S_{ho1} with zoomed ZVS turn-ON and ZCS turn-OFF regions. (f) Voltage stresses and currents through the body-diodes of the switches S_{h2} and S_{ho2} with highlighted soft – switching portions.

are shown. Fig. 16(b) shows gating inputs of LV switches S_{l1} (V_{gl1}) and S_{l2} (V_{gl2}) and primary winding (leakage) currents of the both coils (i_{lk1p}, i_{lk2p}). In Fig. 16(c), current (i_L) drawn from low-voltage source, induced voltage at the secondary winding terminals of inductor (NV_{Lm1p}), resultant voltage across series combination of secondary winding terminals $N(V_{Lm1p}–V_{Lm2p})$ and their current (i_{lks}) are shown. Due to dual flyback energy conversion with the ensured CCM operation, current ripple obtained at low - voltage source is 7.4 A with a ripple factor of 0.36. Fig. 16(d) depicts the confirmed soft turn-ON of the LV switches S_{l1} and S_{l2} during their turn-ON transitions. This denotes negligible turn-ON losses of the devices. Moreover, while turning-OFF, both the LV switches have very small peak magnitudes of falling currents ($I_{f,S_{l1}}$ and $I_{f,S_{l2}}$), which signifies much lowered turn-OFF losses of the devices. Besides, substantial and harmful inductive switching voltage spikes around the LV MOSFETS because of magnetic leakage, are indeed suppressed below 60 V using voltage-clamp circuit composed by a resonant capacitor along with the LV switches (without any additional or auxiliary switches). Furthermore, reduced voltage stresses ensure small voltage rating semiconductor devices, thus, low conduction losses are prevailed. Both LV and HV stage MOSFET switches, FDP075N15 A, and IXTQ44N50P, are placed onto the fabricated circuit board. Fig. 16(e) apparently shows the sinusoidal nature of currents through the body-diodes ($S_{h\_D_1}$, $S_{h\_D_{o1}}$) of the high-voltage side active devices (S_{h1} and S_{ho1}) and the establishment of ZVS turn-ON and ZCS turn-OFF, owing to an implementation of the quasi-resonance principle in the proposed converter. Also, zoomed view of soft-switching transitions are shown. Moreover, a substantial voltage overshoot around the body-diode, as the result of an undesirable resonant ringing due to parasitic capacitance of the switch is evidently alleviated by utilizing the ZCS technique. Thus, a negligible turn-ON and turn-OFF losses are obtained for all the high-voltage devices in the step-up operation. Fig. 16(f) depicts emphasized ZVS turn-ON and ZCS turn-OFF switching instants of body-diodes ($S_{h\_D_2}$, $S_{h\_D_{o2}}$) of the HV switches (S_{h2} and S_{ho2}). A good compliance is accomplished between experimental waveforms and the operating waveforms illustrated in Section II.

In Fig. 17, experimental results of the proposed converter during the step-down operation at full load, $P_o = 600$ W are shown. In Fig. 17(a), gating inputs of high-voltage side switches S_{h1} (V_{gh1}), S_{ho1} (V_{gho1}), S_{h2} (V_{gh2}), and S_{ho2} (V_{gho2}) are shown. Fig. 17(b) shows currents flowing into all the four HV switches (S_{h1}, S_{ho1}) and (S_{h2}, S_{ho2}). In Fig. 17(c), secondary winding voltages, NV_{Lm1p} and NV_{Lm2p}, of the coupled inductors and their primary leakage currents (i_{lk1p}, i_{lk2p}) are shown. In Fig. 17(d) and (e), the establishment of soft-switching of the HV side switches (S_{h1}, S_{ho1}) and (S_{h2}, S_{ho2}) during their turn-ON transitions are shown, respectively. Reduced peak magnitudes of falling currents ($I_{f,S_{h(1,o1)}}$ and $I_{f,S_{h(2,o2)}}$) ensure lowered turn-OFF switching losses of all the HV devices. This shows that, in the step-down operation, a negligible turn-ON loss and lowered turn-OFF losses are achieved for all HV side active devices. Furthermore, as it can be seen from Fig. 17(d) and (e), a maximum blocking-state voltage stress (from source to drain) imposed on internal-diodes of the high-voltage switches is brought-down to one-half of the grid voltage (V_H). This certainly improved the voltage rating of the HV MOSFETS. Fig. 17(f) shows the establishment of ZVS turn-ON and ZCS turn-OFF of the body-diodes ($S_{l\_D_1}$, $S_{l\_D_2}$) of the low-voltage side active devices (S_{l1}, S_{l2}). Also, highlighted portion of soft-switching transitions are presented. As can be seen in step-up/down experimental waveforms, altogether, soft-switching is achieved for all the LV and HV stage semiconductors in the proposed converter, in either direction, thus, very low-switching losses occurred in the proposed converter. Figs. 18 and 19 show experimental waveforms of the proposed converter during the step-up and step-down operations at P_o =200 W, respectively. In Fig. 18(a), gating-inputs (V_{gl1}, V_{gl2}) and currents (i_{Sl1}, i_{Sl2}) flowing

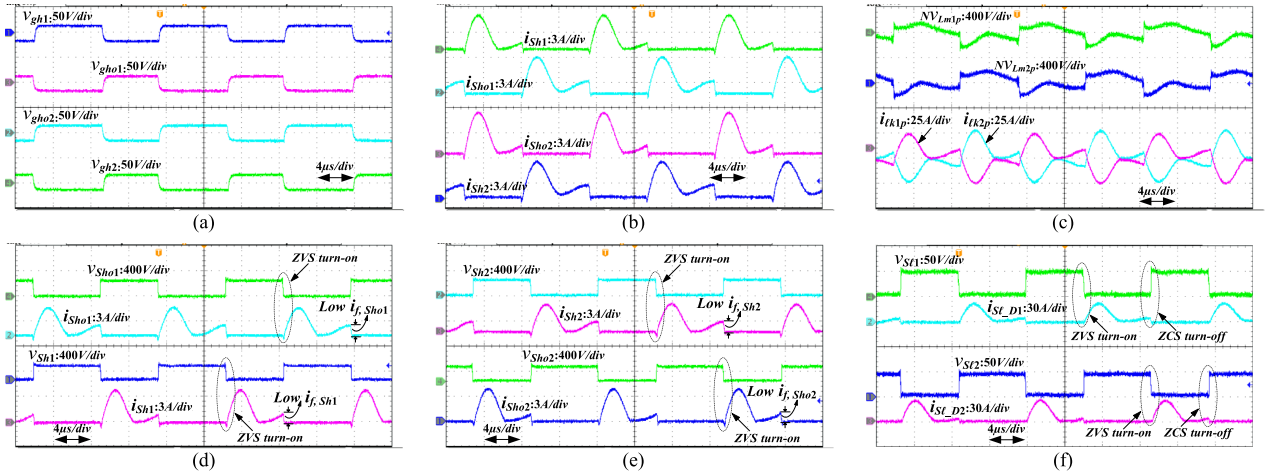


Fig. 17. Step-down operation: Experimental results at full load. (a) Gate pulses of switches S_{h1} (V_{gh1}), S_{ho1} (V_{gho1}), S_{h2} (V_{gh2}), and S_{ho2} (V_{gho2}). (b) Currents through the HV side switches ($S_{h(1,o1,2,o2)}$). (c) Voltages across the secondary windings of the coupled inductors (NV_{Lm1p}, NV_{Lm2p}) and Primary currents of both the coupled inductors i_{lk1p} and i_{lk2p}. (d) Voltage stresses and currents through the HV side switches S_{h1} and S_{ho1} with emphasized ZVS region. (e) Voltage stresses and currents through the HV side switches S_{h2} and S_{ho2} with highlighted ZVS transition. (f) Voltage stresses and currents through the body-diodes of the LV side switches S_{l1} and S_{l2} with emphasized ZVS turn-ON and ZCS turn-OFF transitions.

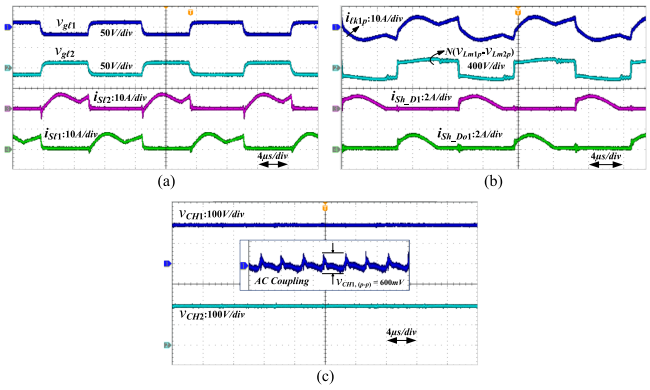


Fig. 18. Step-up operation: Experimental results at 200 W. (a) Gate pulses and currents of the LV side switches (S_{l1}, S_{l2}). (b) Primary current of the coupled inductor (i_{lk1p}), Voltage across series connected secondary windings $N(V_{Lm1p}$ V_{Lm2p}), currents through the HV side switches (S_{h1}, S_{ho1}). (c) Voltage across HV side filter capacitors (V_{CH1}, V_{CH2}).

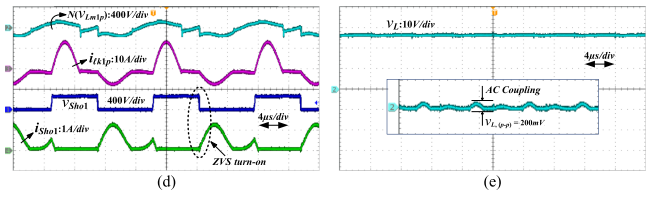


Fig. 19. Step-down operation: Experimental results at 200 W. (a) Voltage across the secondary winding of the coupled inductor (NV_{Lm1p}), Coupled inductor current (i_{lk1p}), Voltage stress and current through the HV side switch S_{ho1} with emphasized ZVS region. (b) Voltage across LV side-filter capacitor (V_L).

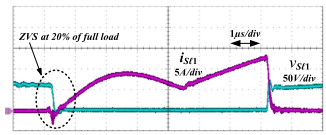


Fig. 20. Step-up mode: ZVS turn-ON of LV switch at 20% of full load.

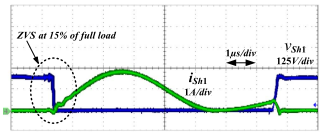


Fig. 21. Step-down mode: ZVS turn-ON of HV switch at 15% of full load.

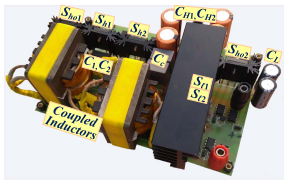


Fig. 22. Experimental prototype of the proposed converter.

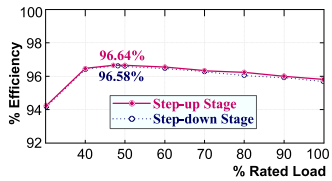


Fig. 23. Measured efficiencies in step-up/down stages of the converter.

through low-voltage switches (S_{l1}, S_{l2}) are shown. Fig. 18(b) shows primary winding current of the coupled inductor (i_{lk1p}), voltage across series combination of secondary winding terminals $N(V_{L_{m1p}} - V_{L_{m2p}})$, and currents through body-diodes of the high-voltage switches (S_{h1}, S_{ho1}). In Fig. 18(c), voltage of HV side filter capacitors (V_{CH1}, V_{CH2}) are shown. Fig. 19(a) shows secondary winding voltage (NV_{Lm1p}) and primary winding leakage current (i_{lk1p}) of the coupled inductor, voltage stress, and current through the HV side switch S_{ho1} with emphasized ZVS region. In Fig. 19(b), voltage of the LV side filter capacitor (V_L) is shown.In Figs. 20 and 21, experimental ZVS turn-ON waveforms of LV and HV stage switches at 20% and 15% of full load, respectively, are shown with an highlighted ZVS portion.Fig. 22 exhibits photograph of the fabricated experimental circuit board. Fig. 23 compares experimental efficiencies in both boost and buck stages of the laboratory prototype from light load to full load and corresponding peak efficiencies are 96.65% and 96.58%. However, the converter retains the efficiency above 95% for wide-ranging loads. InFig. 24, photo of the experimental setup of the proposed converter is shown. In Fig. 25, a schematic control diagram is shown for the proposed converter. Fig. 26 presents the proportion of loss distribution

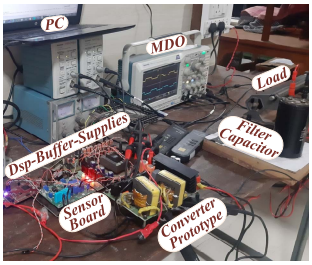


Fig. 24. Photo of experimental setup of the proposed converter.

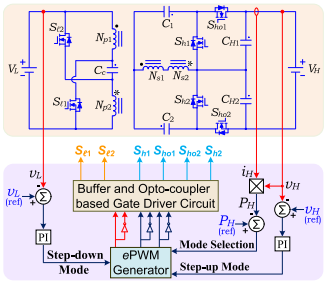


Fig. 25. Schematic control block diagram of the proposed converter.

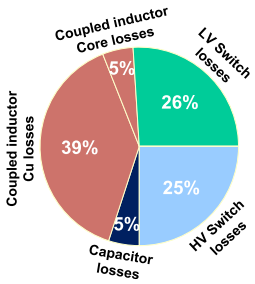


Fig. 26. Loss distribution of the proposed bidirectional converter.

among key elements of the proposed converter under the rated load condition. Both the LV stage MOSFETS of the proposed topology are not at the same reference so, an isolated gate driver is employed. There will be the scope for further reduction in current stresses at the LV stage.

VI. Conclusion

In this article, a novel isolated dual coupled inductors-based topology with switched multiplier cell and soft-switching for bidirectional power flow is proposed for high-voltage step-up/down interfaces in the renewable energy applications. Experimental results for low-side source voltage (V_L) of 26 V and grid voltage (V_H) of 380 V for 600 W laboratory prototype are presented to validate the proposed converter. Enhanced voltage conversion ratio is accomplished with the high-gain multiplier and compact designed coupled inductors at smaller turns and duty ratios. The peak voltage stresses on LV switches are clamped below 60 V. Furthermore, the voltage stress experienced by the HV switch is reduced to 50% of V_H, thus, low-voltage-rating MOSFETS having small $R_{ds(\mathrm{ON})}$ can be used.

Undesired excessive voltage spikes during MOSFET switching transitions are significantly diminished by the clamp circuit constituted by the reduced devices. Smooth switching transitions obtained by waveshaping the currents as sinusoidal by virtue of quasi-resonance. Thereby, ZVS turn-ON (during switch operation, i.e., drain to source) and ZVS turn-ON and ZCS turn-OFF (during body-diode operation, i.e., source to drain) for all the MOSFETS over wide-load range are achieved in both the directions of power flow, and achieving efficiency improvement. Maximum efficiencies in step-up and step-down stages are observed to be 96.65% and 96.58%, respectively. The future studies will be pursued with a model of the multiple different characteristics renewable inputs and battery system with the help of front end dc–dc converters can be integrated to the grid. Furthermore, an experimental setup with a suitable control strategy can be developed for an optimum extent utilization of energy from the renewable inputs and battery system to ensure smooth power flow between the generation and demand during continuous variation of loads connected to the microgrid.

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