Symmetric Circuit Layout With Decoupled Modular Switching Cells for Multiparalleled SiC MOSFETs

Yang He, Junming Zhang, *Senior Member, IEEE*, and Shuai Shao, *Member, IEEE*

***Abstract*—Parallel connection of silicon carbide metal-oxide-semiconductor transistors are widely used in large-current-capacity applications or power modules. However, current imbalance caused by the tolerance of device parameters or asymmetric circuit layout is still a challenge for the reliability of the paralleled devices. The asymmetry of power circuit layout is inevitable when more than two devices are paralleled, which will lead to serious dynamic current imbalance. In this article, an equivalently symmetric power circuit layout based on decoupled paralleled modular switching cells (MSCs) is presented. The current sharing mechanisms of typical asymmetric power circuit layouts are first illustrated. The layout with distributed dc decoupling capacitors turns out to have the potential to modify the current paths but requires further optimization. Based on the mechanisms, the construction of the symmetric layout with the concept of MSC is elaborated by mathematical analysis. DC decoupling capacitors are used to decouple the paralleled symmetric MSCs. Thereafter, the key considerations for the decoupling capacitors are discussed. Experiments are finally carried out to validate the analysis. The test results show that the peak current imbalance is reduced to only 4.1% by the equivalently symmetric power circuit layout, which confirms the effect of decoupled MSCs method.**

***Index Terms*—Decoupling capacitor, dynamic current sharing, paralleled silicon carbide (SiC) metal-oxide-semiconductor transistors (MOSFETs), power circuit layout, symmetric layout.**

I. Introduction

POWER semiconductor devices are the key components in power converters. Silicon carbide (SiC) metal-oxide-semiconductor transistors (MOSFETs) have been attracting a lot of attention recently due to their better performance in switching speed, power loss, and thermal conductivity than that of silicon (Si) devices [1]. For some high-power applications, such as inverters in electric vehicles, power devices of high current ratings are necessary. However, the rating of a single SiC MOSFET chip is usually smaller than those of the Si counterparts like Si insulated gate bipolar transistors because of material defects and yield considerations, which limit the current capacity of commercial SiC MOSFETs. Parallel operation of SiC MOSFETs is widely adopted to enlarge the current capacity [2], [3]. However, the tolerance of device parameters and mismatched circuit parasitic parameters will cause both dynamic and static current imbalances [4]. The current imbalance will further lead to uneven junction temperatures and lower the reliability. Therefore, mitigating current imbalance is necessary to the application of paralleled SiC MOSFETs.

Many research works about the topic of current sharing of paralleled SiC MOSFETs have been reported in recent years. In order to solve the current imbalance problem, analyses of the influences of various parameters on the current sharing are necessary. For static current sharing, the ON-resistance of SiC MOSFET is recognized to be the main factor [4], [5], [6]. Since the load current (inductor current) in a double pulse test (DPT) circuit or a power converter is time-variant, the mismatched parasitic inductances also play an important role in the static current sharing [7], [8], [9]. In [10], it is found that the parasitic inductances and resistances of the common current paths of multiparalleled devices will cause significant static current imbalance. Generally, the static current sharing is more sensitive to circuit parasitic resistances than inductances. The reduction of parasitic resistances is easier than that of parasitic inductances. For dynamic current sharing, the transfer characteristics of the MOSFET, which contain the information of the threshold voltage and transconductance, are reported to be the key factors [4], [5], [6], [11], [12].

There are various dynamic current balancing methods for paralleled devices. The active gate driver (AGD) methods try to eliminate the current imbalance by regulating gate driving signals [13], [14], [15], [16]. However, most of the AGDs require high-bandwidth (BW) current detection and control circuits, which significantly increase the complexity and decrease the reliability. The passive methods use extra passive components, such as coupled inductors, to improve the current sharing of paralleled SiC MOSFETs [17], [18], [19], [20]. However, they are usually bulky and difficult to be extended to the applications of more than two paralleled devices.

Most of the AGDs or passive methods mainly focus on the current sharing influenced by device parameters. The device screening method is a straightforward method to select almost identical devices for parallel applications [11], [12]. However, even if the identical devices are paralleled, the current sharing is still a challenge because of the circuit parasitic parameters.

Due to the high current slew rate, the dynamic current sharing is very sensitive to the parasitic parameters in the power loop,

Manuscript received 4 November 2022; revised 21 January 2023; accepted 11 February 2023. Date of publication 16 February 2023; date of current version 20 April 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 51877193, and in part by the Research Program sponsored by Eaton Corporation. Recommended for publication by Associate Editor D. G. Lamar. *(Corresponding author: Junming Zhang.)*

The authors are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: heyang1201@zju.edu.cn; zhangjm@zju.edu.cn; shaos@zju.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3245680.

Digital Object Identifier 10.1109/TPEL.2023.3245680

especially the power-source inductances [9], [21]. The mismatched power-source inductances influence the gate voltage of the paralleled devices and result in dynamic current imbalance [22].

For the parallel connection of more than two devices, it is very hard to achieve a symmetrical power circuit layout considering the physical arrangement of the paralleled devices. Therefore, the mismatched parasitic parameters caused by asymmetric power circuit layout is also a big challenge for the parallel operation of SiC MOSFETs.

Some power circuit layout optimization methods have been proposed to improve the dynamic current sharing related with circuit parasitic parameters. In [23], the mismatched parasitic inductances of a power module are compensated by adjusting the lengths and joints of bonding wires. The dynamic currents are well balanced but the total loop parasitic inductance will increase with the number of paralleled devices. The mutual magnetic coupling between the current paths is adopted to decrease the parasitic inductances of the commutation loops of the paralleled devices in [24]. However, the differences among the power-source inductances still exist even if the parasitic inductance is very low. Identical equivalent power-source inductances are achieved by additional modification paths (MPs) in [25]. The application of this method is simple and can be extended to multiparalleled devices. However, MPs are based on the Cu clip bonding technology, which might be difficult to be applied in other types of power modules. Meanwhile, the MPs increase the complexity of current loops, which might introduce mutual magnetic coupling and interfere with the accuracy of the equivalent source inductances calculation.

The optimizations of power circuit loop above mainly modify the lengths or structures of the current paths to change the parasitic inductances. The equivalent dynamic current paths can also be changed by decoupling capacitors due to their low impedances at high frequency. In [26], two dc decoupling capacitors are placed on the two sides of the direct bonded copper of a power module, which makes the layout more symmetrical and decreases the current imbalance. However, the axial symmetry of this power circuit layout cannot achieve the symmetry of all paralleled devices, especially when the number of paralleled devices further increases. Literature [27] improves the circuit layout with distributed dc decoupling capacitors mentioned in [3] and achieves good dynamic current sharing. It improves the asymmetric layout of the output nodes of the paralleled switching legs by separation slots. However, the root causes and other layout factors causing current imbalance were not revealed. The separation slots can only be designed by simulations and trial and error. Furthermore, the effects of the decoupling capacitors on current balancing, including the size and capacitance, have not been considered in [27]. A monolithic Si-RC snubber is added in a power module in [22] to change the dynamic current paths and try to decrease the circulating current in the gate loop caused by different power-source voltages. However, the demonstrated current balancing effect is limited because the circulating current cannot be fully eliminated by the RC snubber.

Inspired by the effect of distributed dc decoupling capacitors, an equivalently symmetric layout with the concept of decoupled modular switching cells (MSCs) is proposed in this article. The current sharing mechanisms of both conventional power circuit layout and layout with distributed decoupling capacitors are elaborated to illustrate the key considerations for a symmetric layout. Based on the analysis, the paralleled switching legs are divided into independent MSCs. The internal structures of the MSCs are identical to guarantee the symmetry of the layout. Each MSC is configured with a dc decoupling capacitor bank to decouple the MSC from the other paralleled MSCs. The dynamic commutation current of each MSC only flows through the current paths inside the MSC, which achieves the symmetry of the overall layout. A reasonable capacitance value is analyzed to optimize the sizes and cost of the decoupling capacitors. Modular circuit design guarantees the flexibility and expandability of the MSCs.

The rest of this article is organized as follows. In Section II, the basic influences of asymmetric layout on the dynamic current sharing are first demonstrated with a conventional power circuit layout. Then, the current sharing mechanism of a modified layout with distributed dc decoupling capacitors is analyzed in detail. Based on the analyses in Section II, the concept of MSC is introduced to construct an equivalently symmetric layout in Section III. The mathematical analysis, design of circuit layout, and the key considerations for the decoupling capacitor are presented. The theoretical analyses are verified by experiments in Section IV. Finally, the conclusions are given in Section V.

II. Current Sharing of Asymmetric Circuit Layout

In this section, the mismatched power-source potentials are recognized to be the most important cause of dynamic current imbalance based on the analysis of a conventional power circuit layout. Then, the theoretical analysis and circuit simulations are presented to elaborate the dynamic current sharing mechanism in a layout for paralleled switching legs with distributed decoupling capacitors. The analyses in this section can help reveal the key considerations for a symmetric power circuit layout.

A. Conventional Power Circuit Layout

The conventional connection for paralleled devices is paralleling the devices directly as shown in Fig. 1. Usually, the gates of all paralleled devices are driven by a common gate signal. Limited by the physical positions of paralleled SiC MOSFETs, it is nearly impossible to realize an absolutely symmetric power circuit layout when the number of paralleled devices is more than two, which will cause dynamic current imbalance among the paralleled MOSFETs.

Even if the drain inductances (L_{d1}–L_{d3}) and source inductances (L_{s1}–L_{s3}) are identical for each device, the total parasitic inductance of each device branch is usually different because of the parasitic inductances of common current paths (L_{d12}, L_{d23}, L_{s12}, and L_{s23}), which are usually inevitable due to the physical device positions. In the current rising/falling stage, the voltage drops across the drain inductances are usually small compared with the dc bus voltage, which have very limited effect on the gate-source voltage $v_{\rm gs}$. Therefore, the influence of drain inductances on current sharing is not very significant [4], [9].

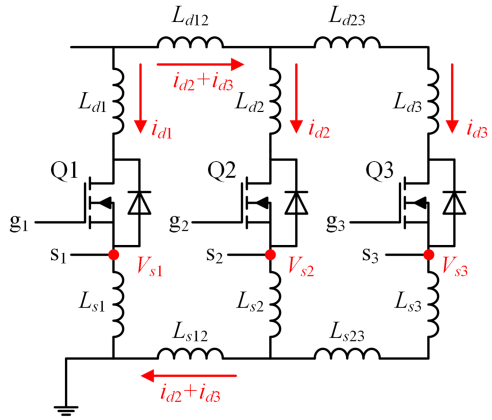


Fig. 1. Schematic of a conventional power circuit layout.

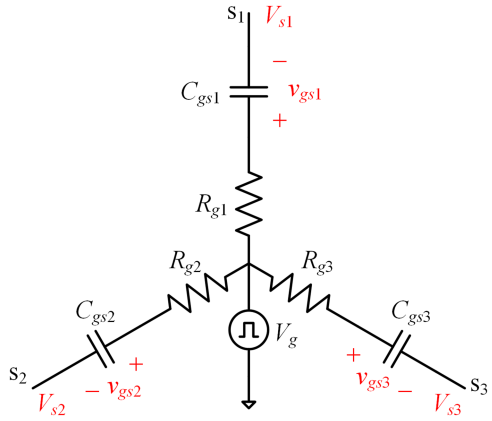


Fig. 2. Simplified network of gate loops.

A simplified network of the gate loops of the paralleled MOSFETs is shown in Fig. 2. To analyze the influences of asymmetric layout on dynamic current sharing, the gate resistances (R_{g1}–R_{g3}), gate-source capacitances ($C_{\rm gs1}$–$C_{\rm gs3}$), and other device parameters are assumed to be identical.

Taking the ground shown in Fig. 1 as the reference point, the potentials of the sources of the MOSFETs can be expressed as

$$\begin{cases} V_{s1} = L_{s1}\dfrac{di_{d1}}{dt} \\ V_{s2} = L_{s2}\dfrac{di_{d2}}{dt} + L_{s12}\dfrac{d(i_{d2}+i_{d3})}{dt} \\ V_{s3} = L_{s3}\dfrac{di_{d3}}{dt} + L_{s23}\dfrac{di_{d3}}{dt} + L_{s12}\dfrac{d\,(i_{d1}+i_{d2})}{dt} \end{cases} \tag{1}$$

where i_{d1}–i_{d3} are the drain currents of the devices. The source currents are assumed to be the same as drain currents.

In Fig. 2, the gate-source voltages ($v_{\rm gs1}$–$v_{\rm gs3}$) of the devices are identical and only dependent on the driver voltage V_g if $V_{s1} = V_{s2} = V_{s3}$. In this case, the device currents are the same. However, according to (1), the potentials of the sources are different due to the additional voltage drops on L_{s12} and L_{s23} even if $L_{s1} = L_{s2} = L_{s3}$. Therefore, the differences among V_{s1}, V_{s2}, and V_{s3} will influence $v_{\rm gs1}$–$v_{\rm gs3}$ and finally cause current imbalance. The higher the source potential is, the lower the gate charging current is. As a result, the gate-source voltage and the related drain current of the device with the highest source potential are the lowest. In a word, $i_{d1} > i_{d2} > i_{d3}$ because $V_{s1} < V_{s2} < V_{s3}$. Even when the devices are identical, the physical positions of the switches can cause current imbalance.

In Fig. 1, the source potentials can be identical by adjusting the values of parasitic inductances. However, the only way is to increase the parasitic inductances of Q_1 and Q_2 to match the highest parasitic inductance of Q_3. The parasitic inductances of the paralleled devices will increase remarkably since there always exists the highest parasitic source inductance restricted by the physical placement of devices. The increase of parasitic inductances will cause more severe oscillation, which is not preferred. Therefore, other methods to equivalently achieve symmetric layout are required.

B. Power Circuit Layout for Paralleled Switching Legs With Distributed Capacitors

Decoupling capacitors, which are widely used in circuit design, can change the equivalent transient current loop due to their low impedances in a certain frequency range. Distributed dc decoupling capacitors have been adopted in some research works to improve the symmetry of the layout of paralleled MOSFETs [3], [27]. However, the degree of symmetry is still highly related with the layout design. Until now, the key considerations for a symmetric layout with distributed decoupling capacitors have not been fully revealed. Mismatched parasitic inductances and current imbalance are still common if the circuit layout is improper. A printed circuit board (PCB) layout for four paralleled SiC MOSFETs switching legs with distributed decoupling capacitors for DPT is shown in Fig. 3, which is taken as an example here to illustrate this phenomenon. The high side device and low side device in TO-247-4 packages of each switching leg are placed together. The dc decoupling capacitors are arranged in a distributed way, which are divided into four groups and located near the four switching legs. Therefore, the structures of four paralleled switching legs and their decoupling capacitors are identical. The decoupling capacitors are connected to the dc positive bus and negative bus via two large copper planes to reduce the conduction loss. The output nodes are connected in a symmetrical way as recommended by [27]. Multilayer ceramic capacitors (MLCCs) are used here to minimize the commutation loops because of their compact sizes and low equivalent series inductances (ESLs).

In order to better illustrate the layout, one of the four paralleled switching legs and the corresponding group of decoupling capacitors are picked out. The simplified current paths and components of a single switching leg are shown in Fig. 4. The current paths of dc positive bus, dc negative bus, and the middle point of the switching leg are marked by different colors. The green dots represent the electrical nets where the paralleled switching legs are electrically connected side by side. In this group of decoupling capacitors, the capacitors are labeled as $C_{\rm dec1}$, $C_{\rm dec2}$, $C_{\rm dec3}$, and $C_{\rm dec4}$. The parasitic inductances of the commutation loop of a switching leg are divided into several parts for further illustration, which are listed in Table I.

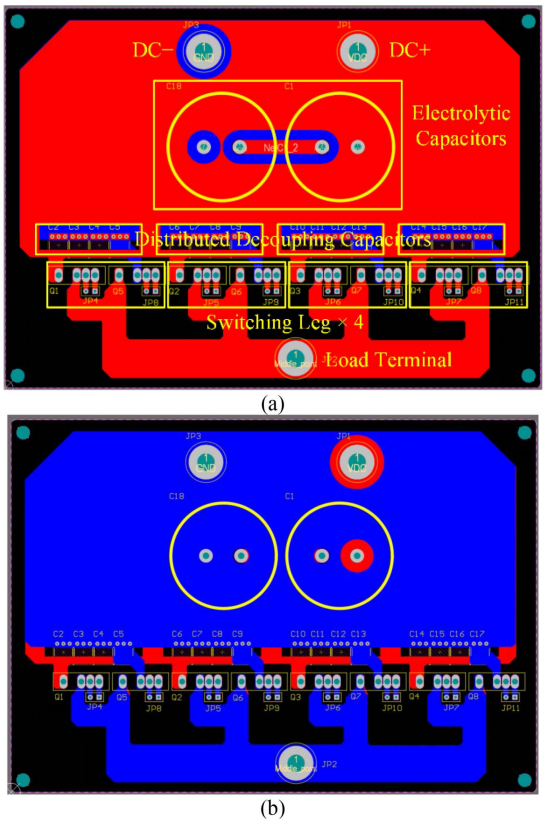


Fig. 3. PCB layout for paralleled switching legs with distributed decoupling capacitors. (a) Top layer. (b) Bottom layer.

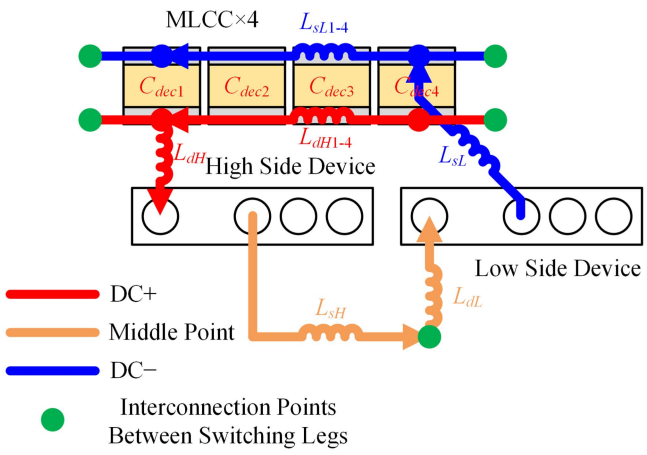


Fig. 4. Simplified current paths of a single switching leg.

TABLE I
MEANINGS OF PARASITIC INDUCTANCES

Symbols	Meanings
L_{dH}	From positive of C_{dec1} to drain of high side device
$L_{dH1\text{-}4}$	From positive of C_{dec4} to positive of C_{dec1}
L_{sH}	From source of high side device to middle point connection
L_{dL}	From middle point connection to drain of low side device
L_{sL}	From source of low side device to negative of C_{dec4}
$L_{sL1\text{-}4}$	From negative of C_{dec4} to negative of C_{dec1}

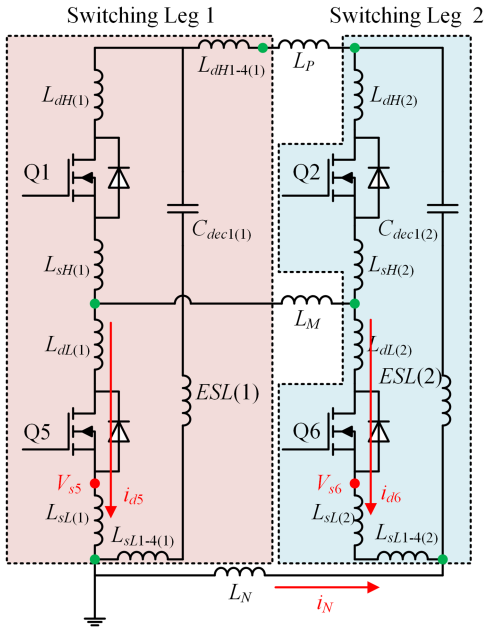


Fig. 5. Schematic of two paralleled switching legs with only C_{dec1}.

From left to right, consider only the first two switching legs in Fig. 3 are paralleled. The asymmetry of this layout is analyzed in the following part. Based on Fig. 4, the schematic of two paralleled switching legs is shown in Fig. 5, and only C_{dec1} of each switching leg is considered.

In Fig. 5, the dc power supply and load inductor in the DPT circuit are not shown since only dynamic commutation process is considered in this analysis. The subscripts "(1)" and "(2)" at the end of component names are used to indicate whether the components belong to switching leg 1 or 2. L_P, L_M, and L_N are the parasitic inductances of the interconnection traces of dc positive bus, middle point, and dc negative bus between two paralleled switching legs, respectively. The interconnection points are also represented by green dots in Fig. 5. In the analysis of this article, the low side devices are referred as the devices under test (DUTs) and the high side devices serve as freewheeling diodes. i_{d5}, i_{d6}, and i_N are the currents of Q_5, Q_6, and L_N, respectively. With the reference ground shown in Fig. 5, the source voltages of Q_5 and Q_6 are expressed as

$$\begin{cases} V_{s5} = L_{sL}\dfrac{di_{d5}}{dt} \\ V_{s6} = L_{sL}\dfrac{di_{d6}}{dt} + L_{sL1-4}\dfrac{di_{d6}}{dt} - L_N\dfrac{di_N}{dt} \end{cases}. \tag{2}$$

According to (2), V_{s6} is dependent on the current flowing through the interconnection trace (i_N), which can be regarded as the circulating current between the two paralleled switching legs. In order to derive the expression of i_N and compare the values of V_{s5} and V_{s6}, the circuit in Fig. 5 is split into two circuits as shown in Fig. 6. The commutation loops of two switching legs are analyzed independently.

In Fig. 6(a), $i_{d5(1)}$ and $i_{d5(2)}$ flow through the capacitor branches of the first and the second switching legs, respectively.

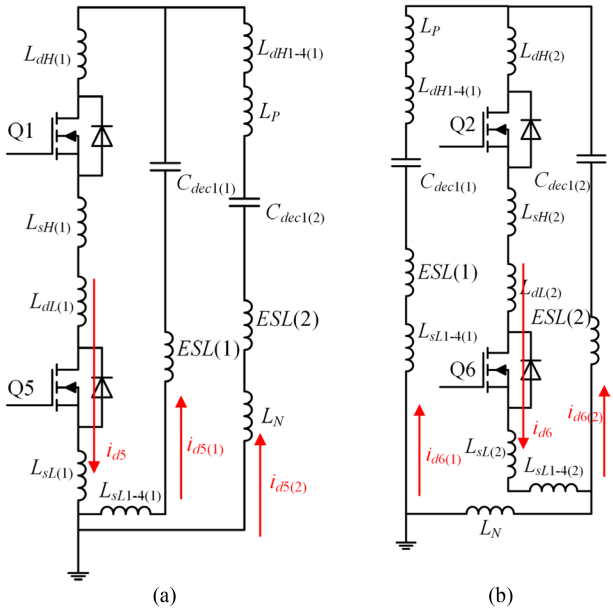


Fig. 6. Split circuits of two paralleled switching legs with C_{dec1}. (a) First switching leg. (b) Second switching leg.

Symbols in Fig. 6(b) are similar to those in Fig. 6(a). At the equivalent frequency of the transient current, the impedances of decoupling capacitors are low enough to be ignored since the capacitances are large. Therefore, the current sharing of capacitor branches can be expressed as

$$\begin{cases} i_{d5(2)}(s) = \dfrac{L_{sL1-4} + \mathrm{ESL}}{L_{dH1-4} + L_{sL1-4} + L_P + 2\mathrm{ESL} + L_N} i_{d5}(s) \\ i_{d6(1)}(s) = \dfrac{\mathrm{ESL}}{L_{dH1-4} + L_{sL1-4} + L_P + 2\mathrm{ESL} + L_N} i_{d6}(s) \end{cases}. \tag{3}$$

Considering the superposition of the circuits shown in Fig. 6, the current of L_N in Fig. 5 can be expressed as

$$i_N = i_{d5(2)} - i_{d6(1)}. \tag{4}$$

Assuming i_{d5} is equal to i_{d6} and substituting (3) and (4) into (2), the voltage difference between the sources of Q_5 and Q_6 is derived as

$$V_{s6} - V_{s5} = \frac{L_{dH1-4} + L_{sL1-4} + L_P + 2\mathrm{ESL}}{L_{dH1-4} + L_{sL1-4} + L_P + 2\mathrm{ESL} + L_N} L_{sL1-4} \frac{di_{d6}}{dt}. \tag{5}$$

It is obvious that V_{s6} is higher than V_{s5}, which will cause current imbalance ($i_{d5} > i_{d6}$). This is inconsistent with the assumption that i_{d5} is equal to i_{d6}. Therefore, it is impossible that device currents are balanced in the circuit shown in Fig. 5.

The analysis above only considers the effect of C_{dec1}. The effects of the rest of the decoupling capacitors can be analyzed by the same methodology. For simplicity, the analysis is not repeated in this article. The results are the same ($V_{s5} < V_{s6}$ and $i_{d5} > i_{d6}$). The main reasons for current imbalance can be summarized as follows:

TABLE II
EXTRACTED PARASITIC INDUCTANCES

Symbols	Values
L_{dH}	1.2 nH
$L_{dH1\text{-}4}$	3.3 nH
L_{sH}	3.2 nH
L_{dL}	4.4 nH
L_{sL}	3.2 nH
$L_{sL1\text{-}4}$	2.7 nH
L_P	4.7 nH
L_M	24.8 nH
L_N	3.6 nH

1) There still exists circulating current between the switching legs ($i_N \neq 0$), which means the voltage drop on the interconnection trace (L_N) will influence the source voltages of DUTs.
2) The equivalent source parasitic inductances (between the sources of DUTs and the interconnection points) of Q_5 and Q_6, which are L_{sL} and $L_{sL} + L_{sL1\text{-}4}$, respectively, as shown in Fig. 5, are different due to asymmetric interconnection points for decoupling capacitors.

The reasons summarized above lead to unequal source potentials of the DUTs, which are the root causes of the current imbalance. Therefore, the circuit shown in Fig. 5 is essentially an asymmetric layout, even though the structure of each switching leg shown in Fig. 4 is identical.

Meanwhile, the analysis above has not considered the situation where four switching legs are paralleled. Actually, since the physical location relationship between Q_5 and Q_6 is the same as those between Q_6 and Q_7 or between Q_7 and Q_8, the current relationships are also the same. Therefore, the results based on two paralleled switching legs can be extended to four paralleled switching legs. The currents of devices located on the left side of the PCB are higher than those of devices located on the right side.

C. Simulation of the PCB Layout for Paralleled Switching Legs With Distributed Capacitors

To support the analysis above, DPT circuit simulations are carried out in Pspice based on the layout shown in Fig. 3. The circuit parasitic parameters of the layout (as the equivalent circuit shown in Fig. 5) are extracted by Ansys Q3D and listed in Table II. Since the conventional circuit layout shown in Fig. 1 has been widely analyzed in previous research works, it is not simulated in this article. The spice models of the SiC MOSFET C3M0032120K and SiC Schottky barrier diode (SBD) C3D30065D provided by Cree are used in the simulations.

First, two paralleled switching legs as shown in Fig. 5 are simulated. The simulation diagram is shown in Fig. 7. The dc bus voltage is 400 V. The dc bus capacitance C_{dc} is 110 μF. The load inductance L_{load} is 0.1 mH. The decoupling capacitance is 100 nF. The ESL of the decoupling capacitor is 1 nH. The external gate resistance (R_{g1}, R_{g2}) is 20 Ω. The source resistance (R_{s1}, R_{s2}) is 1 Ω.

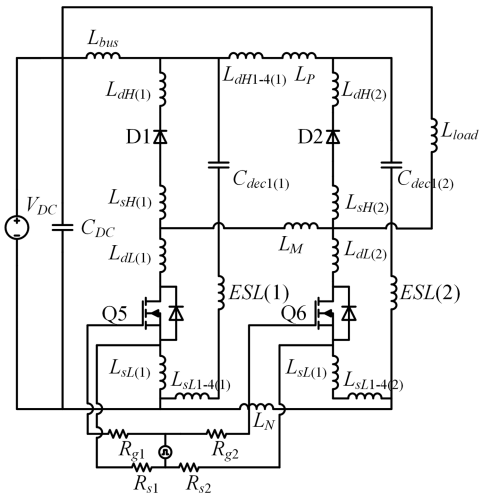


Fig. 7. Simulation model of two paralleled switching legs.

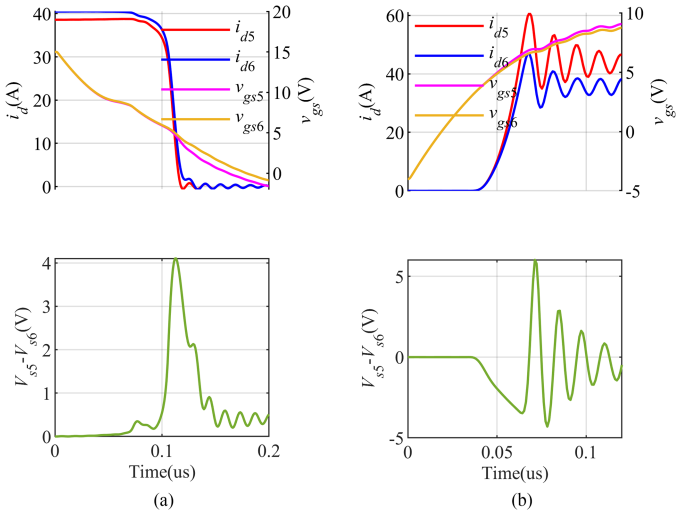


Fig. 8. Simulation results of two paralleled switching legs. (a) Turn-OFF waveforms. (b) Turn-ON waveforms.

The simulation results are shown in Fig. 8. As shown in Fig. 8(a) and (b), i_{d5} is lower/higher than i_{d6} in the turn-OFF/turn-ON transient because v_{gs5} is lower/higher than v_{gs6}. The source voltage difference (V_{s5}–V_{s6}) are also shown in Fig. 8. It can be seen that V_{s5} is higher/lower than V_{s6} in the turn-OFF/turn-ON transient, resulting in the difference between gate-source voltages. The simulation results coincide well with the theoretical analysis.

Thereafter, the parallel of four switching legs with their decoupling capacitors shown in Fig. 3 are also simulated. All the parasitic parameters are extracted by Q3D. To keep the same average device current, the load inductance is changed to 0.05 mH. Other simulation settings are the same as those shown in Fig. 7. The simulation results are shown in Fig. 9. The current sharing in the switching transient validates the analysis given in Section II-B.

As a summary, the conventional power circuit layout shown in Fig. 1 is asymmetric because of the physical positions of the devices. Significant dynamic current imbalance is caused

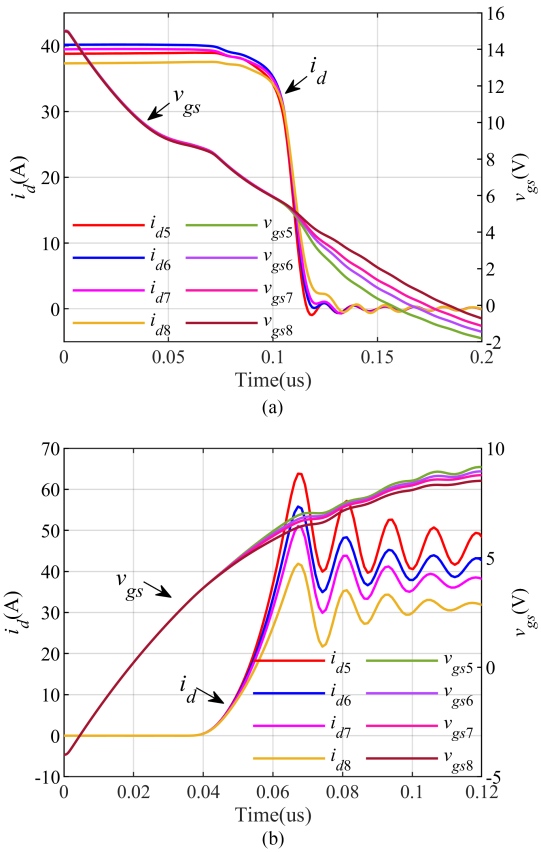


Fig. 9. Simulation results of four paralleled switching legs. (a) Turn-OFF waveforms. (b) Turn-ON waveforms.

by the different source voltages across the mismatched power-source inductances. Additional low-impedance transient current paths are provided by distributed dc decoupling capacitors in the layout shown in Fig. 3. However, the symmetry of the layout cannot be guaranteed only by additional decoupling capacitors. The dynamic current sharing is still highly related with the circuit layout. Further analysis and design considerations are necessary to achieve an equivalently symmetric layout.

III. Decoupled Modular Switching Cells

As has been analyzed in Section II, the layout for paralleled switching legs with distributed decoupling capacitors is also asymmetric with the side-by-side connection of switching legs. According to the main reasons for current imbalance summarized in Section II-B, i.e., circulating current between paralleled switching legs and different equivalent source parasitic inductances caused by asymmetrical interconnection points of decoupling capacitors, a decoupled MSC method is introduced to solve these problems.

A. Theoretical Analysis

In order to guarantee the symmetry of circuit layout, modular design can be adopted. An MSC, which is composed of a switching leg and a decoupling capacitor bank, is shown in Fig. 10. L_{CP} and L_{dP} are, respectively, the parasitic inductances

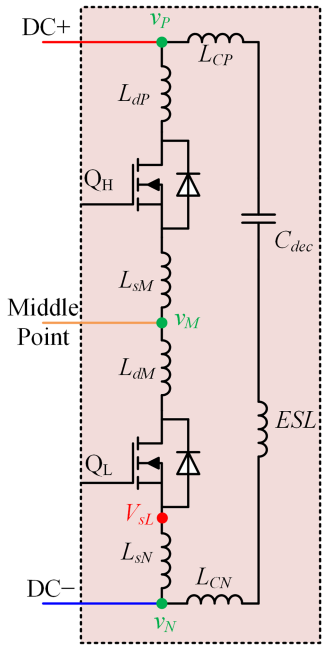


Fig. 10. Schematic of an MSC.

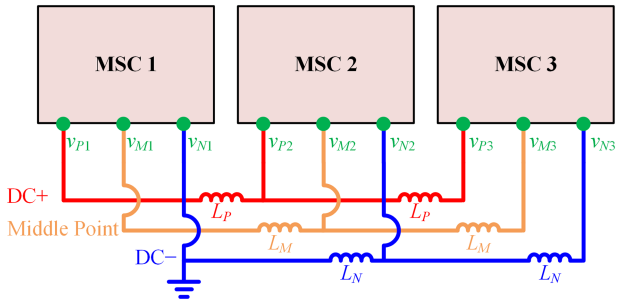


Fig. 11. Parallel connection of three MSCs.

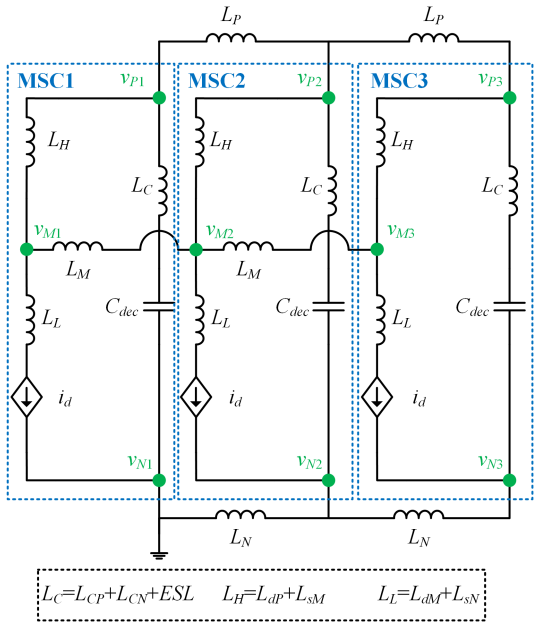


Fig. 12. Equivalent circuit of three paralleled MSCs.

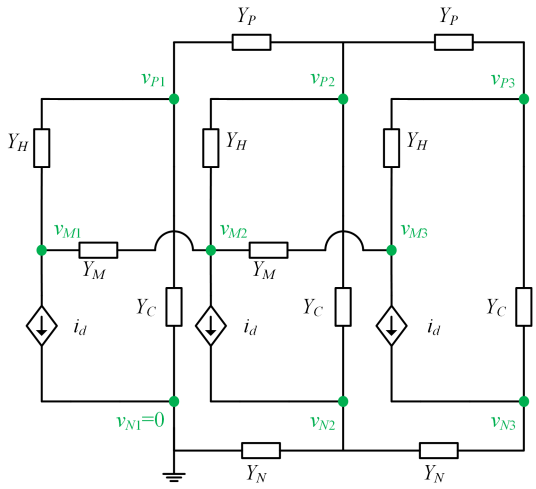


Fig. 13. Simplified equivalent circuit.

of the traces from the decoupling capacitor and the drain of high side device to dc+. L_{sM} and L_{dM} are, respectively, the parasitic inductances of the traces from the source of high side device and the drain of low side device to the middle point. L_{sN} and L_{CN} are the parasitic inductances of the traces from the source of low side device and the decoupling capacitor to dc−. v_P, v_M, and v_N, are respectively, the potentials of dc+, middle point, and dc−. V_{sL} is the source voltage of the DUT.

The parallel connection of three MSCs is shown in Fig. 11 as an example. The internal structures of MSCs are identical, and the relative positions of the interconnection points (green dots) are also identical. Therefore, the equivalent source inductance of the DUT in each MSC (L_{sN}) is also identical. The second main reason for current imbalance summarized in Section II-B is avoided.

In the current rising or falling stages of the switching process, the MOSFETs can be modeled as voltage controlled current sources (VCCSs). Meanwhile, the freewheeling diodes are in the conduction state. Assuming the currents of all paralleled MOSFETs are balanced, the equivalent circuit of the layout in Fig. 11 is shown in Fig. 12. Since each MSC is identical, the parameters shown in Fig. 12 for each MSC are also the same. The series inductances of VCCSs i_d can be ignored. Substituting the inductances and capacitances by their admittances, the equivalent circuit can be further simplified as the circuit shown in Fig. 13. It can be found that the interconnection points are equipotential for three paralleled MSCs. From mathematical perspective, the matrix equation of the circuit is

$$\mathbf{YV} = \mathbf{I} \tag{6}$$

where $\mathbf{Y}$ is the admittance matrix, $\mathbf{V}$ is the node voltage matrix, and $\mathbf{I}$ is the branch current matrix. The matrices are expressed as follows (7)–(9), shown at the bottom of the next page.

The node voltage matrix can be solved as

$$\mathbf{V} = \begin{bmatrix} -i_d/Y_C \\ -i_d/Y_C \\ -i_d/Y_C \\ -i_d(Y_C+Y_H)/(Y_CY_H) \\ -i_d(Y_C+Y_H)/(Y_CY_H) \\ -i_d(Y_C+Y_H)/(Y_CY_H) \\ 0 \\ 0 \end{bmatrix}. \tag{10}$$

Equation (10) indicates that the potentials of the interconnection points of dc+(v_{P1}–v_{P3}), middle point(v_{M1}–v_{M3}), and dc− (v_{N1}–v_{N3}) are, respectively, identical as long as the internal impedances are identical. Therefore, the circulating currents between the paralleled MSCs are eliminated. There is no current flowing through the interconnection traces (L_N), which means the first main reason causing current imbalance summarized in Section II-B is eliminated. In Fig. 10, the source voltages of the low side devices in three paralleled MSCs can be expressed as

$$V_{sL1} = V_{sL2} = V_{sL3} = L_{sN}\frac{di_d}{dt}. \tag{11}$$

The source voltages are identical and only depend on the internal parasitic inductances of a single MSC. As a consequence, the MSCs are well decoupled from each other and the circuit layout is equivalently symmetric. Moreover, this layout can be extended to more paralleled devices by simply increasing the number of MSCs.

B. PCB Layout for Paralleled Modular Switching Cells

Based on the theoretical analysis above, the PCB layout for four paralleled identical MSCs is shown in Fig. 14. A four-layer PCB is preferred to achieve a symmetrical PCB layout. Fig. 14(a) and (b) is, respectively, observed from the first layer and the fourth layer. The internal dynamic commutation loop of each MSC is connected in the first and second layers. The MSCs are electrically interconnected in the third and fourth layers by dc positive bus, dc negative bus, and middle point. The current paths in the third and fourth layers conduct the static currents when MOSFETs are fully ON. The connections to the dc power supply and load inductor are also in these two layers. It can be found that the dynamic current paths are separated from the static current paths by the multilayer PCB. In the first and second layers, the dynamic current paths of the MSCs are identical and independent, which guarantees consistency of the internal structures of the MSCs.

The diagram of the current commutation loop of a single MSC is shown in Fig. 15. The loop is designed to have minimized parasitic inductance for good decoupling performance. Therefore, no resistive damping is needed. The decoupling capacitance can be increased by paralleling capacitors if necessary. The interconnection points of the MSC are located at the pins of the power devices, which can guarantee their relative positions in different MSCs are identical to avoid the reasons for current imbalance summarized in Section II.

In this article, the PCB layout of paralleled discrete devices is demonstrated. Actually, the concept of MSC and the arrangement of the devices can also be applied in the design of a power module.

C. Simulation of the PCB Layout for Paralleled MSCs

The simulation model for the layout shown in Fig. 14 is built in Pspice to verify the theoretical analysis. The circuit diagram is shown in Fig. 16. The internal circuit of a single MSC is the same as the circuit shown in Fig. 10, where the high side devices are replaced by SiC SBDs in the simulation. P1–P4, M1–M4, and N1–N4 are the dc+, middle point, and dc– terminals of the MSCs, respectively. The parasitic parameters of the layout are also extracted by Q3D and used in the simulation model, which are listed in Table III. Other simulation settings are the same as those discussed in Section II-C.

The simulation results are shown in Fig. 17. It can be seen that the gate-source voltages of the paralleled devices are almost identical, which is different from the results in Fig. 9. Therefore, the dynamic current imbalances in both turn-ON and turn-OFF transients are mitigated, which validates the symmetry of circuit layout presented in Fig. 14.

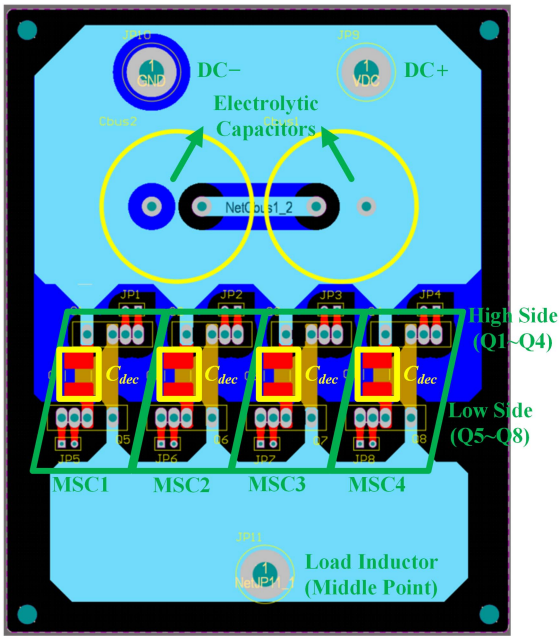
D. Design Considerations for the Decoupling Capacitor

The decoupling capacitor is the key component in the MSC, which provides the dynamic current path of the switching leg in

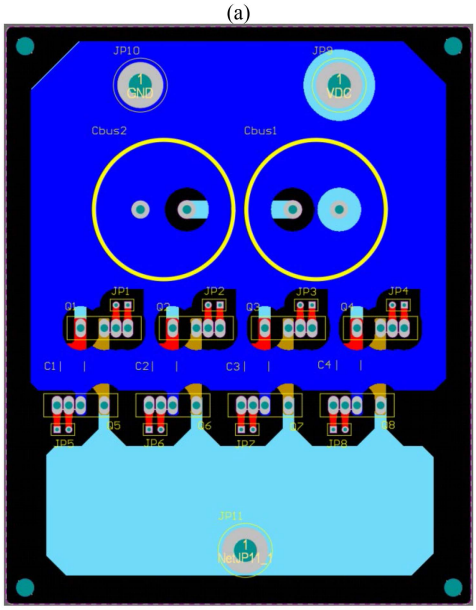
$$\mathbf{Y} = \begin{bmatrix} Y_C+Y_H+Y_P & -Y_P & 0 & -Y_H & 0 & 0 & 0 & 0 \\ -Y_P & 2Y_P+Y_C+Y_H & -Y_P & 0 & -Y_H & 0 & -Y_C & 0 \\ 0 & -Y_P & Y_C+Y_H+Y_P & 0 & 0 & -Y_H & 0 & -Y_C \\ -Y_H & 0 & 0 & Y_H+Y_M & -Y_M & 0 & 0 & 0 \\ 0 & -Y_H & 0 & -Y_M & 2Y_M+Y_H & -Y_M & 0 & 0 \\ 0 & 0 & -Y_H & 0 & -Y_M & Y_H+Y_M & 0 & 0 \\ 0 & -Y_C & 0 & 0 & 0 & 0 & Y_C+2Y_N & Y_N \\ 0 & 0 & -Y_C & 0 & 0 & 0 & -Y_N & Y_C+Y_N \end{bmatrix} \tag{7}$$

$$\mathbf{V} = \begin{bmatrix} v_{P1} & v_{P2} & v_{P3} & v_{M1} & v_{M2} & v_{M3} & v_{N2} & v_{N3} \end{bmatrix}^{\mathrm{T}} \tag{8}$$

$$\mathbf{I} = \begin{bmatrix} 0 & 0 & 0 & -i_d & -i_d & -i_d & i_d & i_d \end{bmatrix}^{\mathrm{T}}. \tag{9}$$



(a)



(b)

Fig. 14. PCB layout of paralleled MSCs. (a) First layer. (b) Fourth layer.

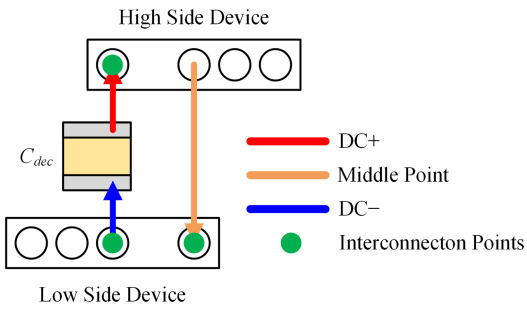


Fig. 15. Diagram of the commutation loop of a single MSC.

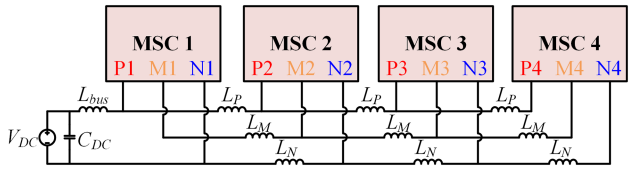


Fig. 16. Simulation model of paralleled MSCs.

TABLE III
EXTRACTED PARAMETERS OF PARALLELED MSCS

Symbols	Values
L_{dP}	6.5 nH
L_{sM}	5.5 nH
L_{dM}	4.4 nH
L_{sN}	2.7 nH
L_{CP}	1.6 nH
L_{CN}	1.7 nH
L_P	8.2 nH
L_M	12.9 nH
L_N	7.2 nH

the MSC. Generally, the MLCC is preferred for this decoupling capacitor due to its compact size and very good high-frequency characteristics. Theoretically, the larger the decoupling capacitance is, the better the decoupling effect is. However, the capacitances of MLCCs have their limitations. A suitable capacitance is usually preferred since more paralleled capacitors also require larger space and higher cost in practical applications. To optimize the design of the decoupling capacitors, it is necessary to analyze the influence of the decoupling capacitance.

1) Capacitor Voltage Fluctuation: The dynamic current of a single MSC should only flow through its decoupling capacitor during the switching transient, and it should not flow to other MSCs or the dc bus to achieve good dynamic current balancing, which is illustrated in Fig. 18. Therefore, the impedance of the decoupling capacitor branch should be much lower than that appeared on the dc bus. The decoupling capacitance for a single MSC should be large enough to lower its impedance. The trace connecting the decoupling capacitor to the MOSFET should also be carefully designed to minimize its parasitic inductance, and no additional resistive damping is added in the decoupling capacitor branch in order to minimize its impedance.

The commutation loop of a single MSC is illustrated by Fig. 19, where C_D, C_{gd}, C_{gs}, and C_{ds} are the junction capacitances of the SBD and MOSFET, respectively. It is clear that a minimized L_C helps to improve the decoupling performance. In the layout shown in Fig. 15, L_C is very small as given in Table III.

It is necessary for the decoupling capacitors to hold the dc voltages of paralleled MSCs in a short period. The decoupling capacitances will influence the fluctuation of the capacitor voltage. Taking the turn-ON process as an example, the decoupling capacitors are discharged by the dynamic currents of MSCs, which lead to decreased dc voltages. The equivalent circuit of this process is shown in Fig. 20.

Since the voltages of the decoupling capacitors in all paralleled MSCs are usually the same, the circuit shown in Fig. 20 considers all paralleled MSCs together. In Fig. 20, $V_{\rm dc}$ is the

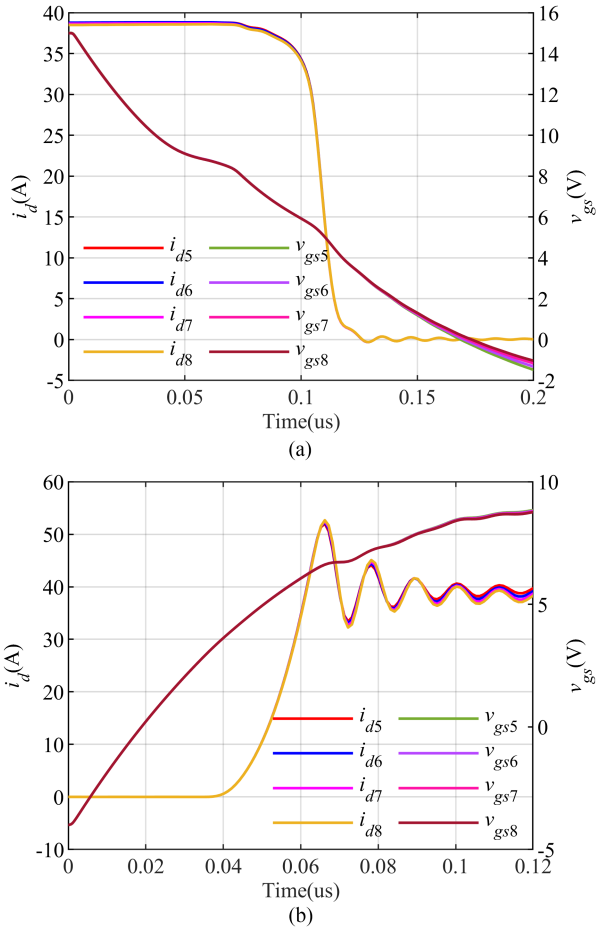


Fig. 17. Simulation results of paralleled MSCs.

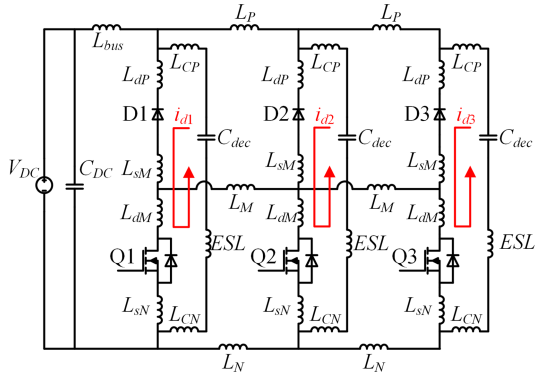


Fig. 18. Commutation loops of MSCs in the switching transient.

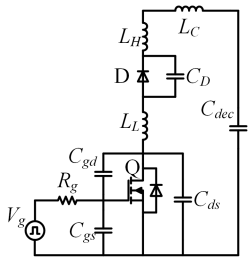


Fig. 19. Commutation loop of a single MSC.

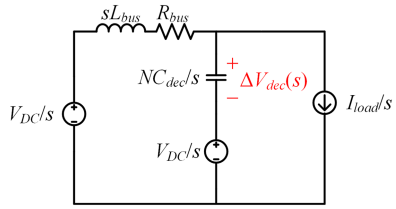


Fig. 20. Equivalent circuit considering voltage drop in turn-ON process.

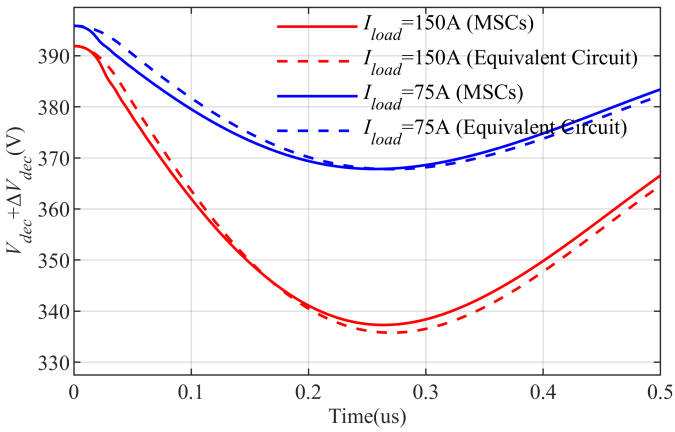


Fig. 21. Simulation results of the fluctuation of DC voltage.

voltage of dc power supply. $L_{\rm bus}$ and $R_{\rm bus}$ are the equivalent parasitic inductance and resistance of the dc bus and the dc capacitor, respectively. N is the number of paralleled MSCs. $C_{\rm dec}$ is the decoupling capacitance in a single MSC. The voltage source in series with the decoupling capacitance is the initial voltage of the decoupling capacitors. $I_{\rm load}$ is the load current of the paralleled MSCs, which is also the sum of static currents of the MSCs. In the freewheeling stage, the load current only flows inside the MSCs. When the paralleled MOSFETs are turned ON, the load current begins to flow through the decoupling capacitors, which is equivalently represented by the step current source. To simplify the analysis, the parasitic parameters shown in Fig. 19, like L_L, L_H, L_C, and ESR, are neglected in Fig. 20 because they are usually very small compared with the decoupling capacitance and bus parasitic inductance $L_{\rm bus}$. The variance of the dc voltage of decoupling capacitance can be expressed as

$$\Delta V_{\rm dec}(s) = \frac{sNL_{\rm bus}C_{\rm dec} + NR_{\rm bus}C_{\rm dec}}{s^2L_{\rm bus} + sR_{\rm bus} + NC_{\rm dec}} \frac{I_{\rm load}}{s}. \qquad (12)$$

The expression of $\Delta V_{\rm dec}(s)$ in time-domain is rather complex, which is not given here. The simulation results of the equivalent circuit under different load currents are shown in Fig. 21(dashed lines). To verify the effectiveness of the simplifications above, the simulation results of the circuit shown in Fig. 16 under the same operation conditions are also shown in Fig. 21 (solid lines), which include all the parasitic parameters. In the simulation, $R_{\rm bus}$ and $L_{\rm bus}$, which include the parsitics of PCB traces and the dc capacitor, are considered in the circuit shown in Fig. 16 and the parameters are $L_{\rm bus} = 45$ nH, $R_{\rm bus} = 160$ mΩ, $C_{\rm dec} = 100$ nF, $N = 4$. Other parasitic parameters are the same as those discussed in Section III-C. The same parameters are used

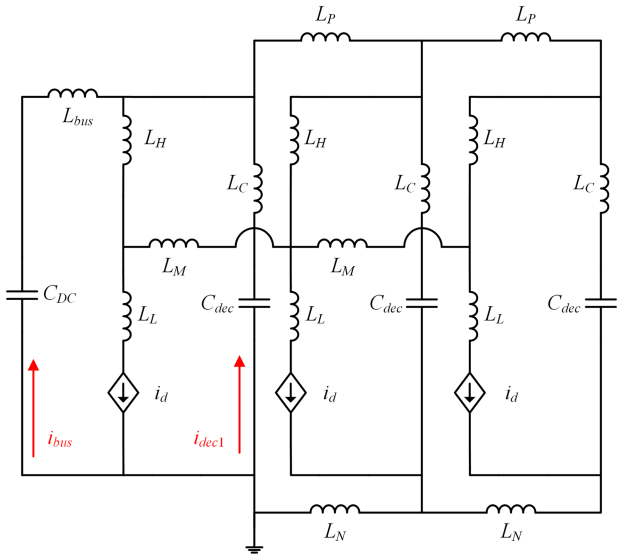


Fig. 22. Equivalent circuit of paralleled MSCs considering the DC bus.

in the equivalent circuit for comparison. As shown in Fig. 21, the simulation results of the equivalent circuit match well with those of the circuit considering all the parasitic parameters.

It can be found that the peak voltage drops of the decoupling capacitance with the given parameters are around tens of volts. Further decreasing the capacitance of decoupling capacitors will result in significant fluctuation of the capacitor voltage, which will influence the stability of the dc voltage and is not preferred. Meanwhile, the fluctuation of the decoupling capacitor voltage is also related with the load current according to (12). Therefore, the capacitance should increase with the load current to maintain a low variation of the dc voltage. As a rule of thumb, the voltage variation should be kept less than 10% of bus voltage to avoid potential oscillation, and the capacitance can be selected.

2) Current Sharing Performance: In the MSCs, the effect of decoupling capacitors is providing low-impedance branches to decouple the commutation currents. However, this effect might be limited by the decoupling capacitance. In the former analysis of this article, the branch of dc bus is ignored, which is based on the assumption that the impedances of decoupling capacitors are much lower than that of dc bus. If the decoupling capacitance is too small, the commutation currents cannot be fully decoupled and will partially flow through the dc bus, which will break the symmetry of the circuit and cause current imbalance. The equivalent circuit of paralleled MSCs considering the dc bus is shown in Fig. 22.

The equivalent parasitic inductance of the dc bus ($L_{\rm bus}$) includes both the ESL of the dc capacitor and the parasitic inductances of the PCB traces. The dc capacitance is usually very large, whose impedance is approximately zero in the frequency range of the switching process. Therefore, the dynamic current sharing of the dc bus and the decoupling capacitor can be expressed as

$$\frac{|i_{\rm bus}|}{|i_{\rm dec1}|}=\frac{\left|sL_C+\frac{1}{sC_{\rm dec}}\right|}{|sL_{\rm bus}|}. \tag{13}$$

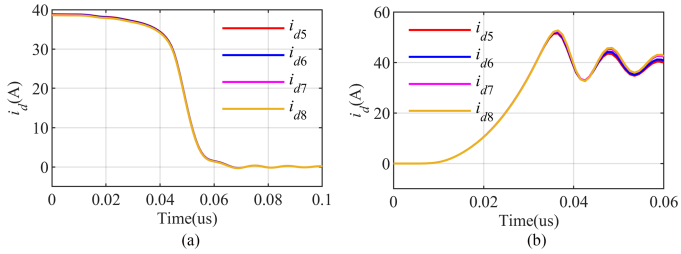


Fig. 23. Simulation results considering the tolerance of decoupling capacitances.

According to [28], the BW of the rising edge of the turn-ON current of a MOSFET can be expressed as

$$\text{BW}=\frac{0.35}{t_r} \tag{14}$$

where t_r is the rising time of the MOSFET. Considering t_r is 40 ns, BW is about 8.75 MHz. At this frequency, the impedance amplitude of 45 nH $L_{\rm bus}$ is equal to that of 7.35 nF $C_{\rm dec}$. To achieve a better decoupling effect, the capacitance should be at least 10 times larger. According to the analysis above about the fluctuation of capacitor voltage, relatively low variations of the dc voltage can be maintained only when the decoupling capacitance is 100 nF or higher, which is much larger than 7.35 nF. Therefore, the impedance of $C_{\rm dec}$ in (13) can be ignored.

According to (13), the parasitic inductance L_C in the capacitor branch also influences the current sharing. If L_C is too large, the current through the dc bus cannot be ignored any more. The current sharing performance of the paralleled SiC MOSFETs will be deteriorated. As discussed above, the L_C should be as small as possible. From engineering point of view, L_C should be less than one tenth of $L_{\rm bus}$ to achieve a good decoupling performance according to (13). For the PCB layout shown in Fig. 14, using an MLCC decoupling capacitor, the parasitic inductances (L_{CP} and L_{CN}) are only 1.6 and 1.7 nH, respectively, and the $L_{\rm bus}$ is 45 nH.

3) Tolerance of Decoupling Capacitances: For practical capacitors, the tolerance of the capacitances can be up to 10%–20%, which means the decoupling capacitances in the MSCs might be different. Theoretically, this tolerance will not influence the proper operation of the MSCs. As has been discussed before, the decoupling capacitance is large enough so that its impedance is ignored compared with the parasitic inductances in the circuit. For example, the decoupling capacitances of four MSCs are set as 80, 90, 110, and 120 nF in the simulation circuit shown in Fig. 16. The simulation results are shown in Fig. 23. It is clear that the dynamic current sharing is almost not affected by the tolerance of the decoupling capacitances.

4) Power Losses of Decoupling Capacitors: Since the dynamic current during switching transient flows through the decoupling capacitor in an MSC, it will cause power loss due to the ESR. To avoid potential thermal stress, there is a maximum allowable ripple current for a certain capacitor. It can also be analyzed by the circuit shown in Fig. 20. For the turn-ON transient, the decoupling capacitors are discharged by the commutation currents and then charged by the dc bus voltage.

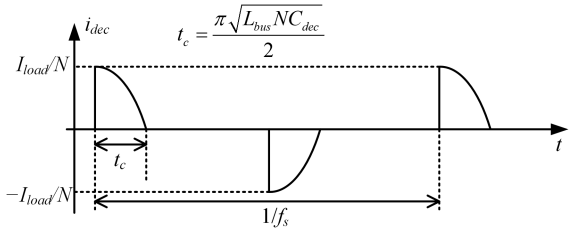


Fig. 24. Simplified waveform of the current through a decoupling capacitor.

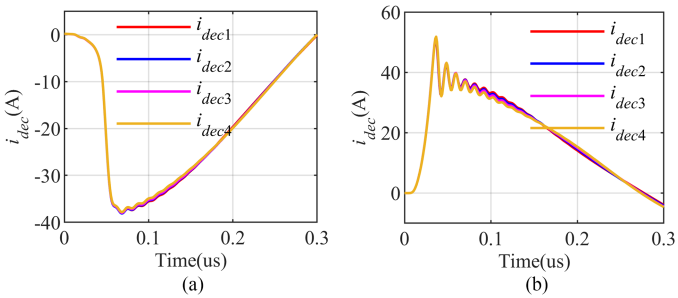


Fig. 25. Currents through decoupling capacitors. (a) In the turn-OFF transient. (b) In the turn-ON transient.

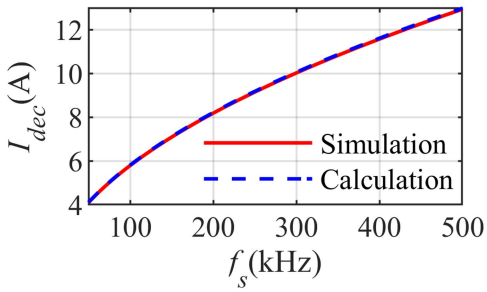


Fig. 26. Comparison of the calculation and simulation of rms capacitor current.

It can be approximately regarded as the resonance between $L_{\rm bus}$ and $NC_{\rm dec}$. The turn-OFF transient is similar to the turn-ON transient. The current waveform of each decoupling capacitor can be approximately illustrated by Fig. 24. The rising time of the commutation current is ignored since it is very short compared with the resonant period. One-fourth of the resonant period is considered in each switching transient for simplicity considering the damping of $R_{\rm bus}$. The rms current of each decoupling capacitor can be expressed as

$$I_{\rm dec} = \frac{I_{\rm load}}{\sqrt{2}N}\sqrt{\pi f_s \sqrt{L_{\rm bus}NC_{\rm dec}}} \tag{15}$$

where f_s is the switching frequency.

The currents through the decoupling capacitors in the simulation circuit are shown in Fig. 25. The load current is around 160 A. Other simulation settings are the same with those discussed in Section III-D-2. The rms current of a single capacitor is calculated based on the simulation results, and it is compared with the calculation results using (15), as shown in Fig. 26. It is clear that the calculation results based on (15) match well with the simulation results.

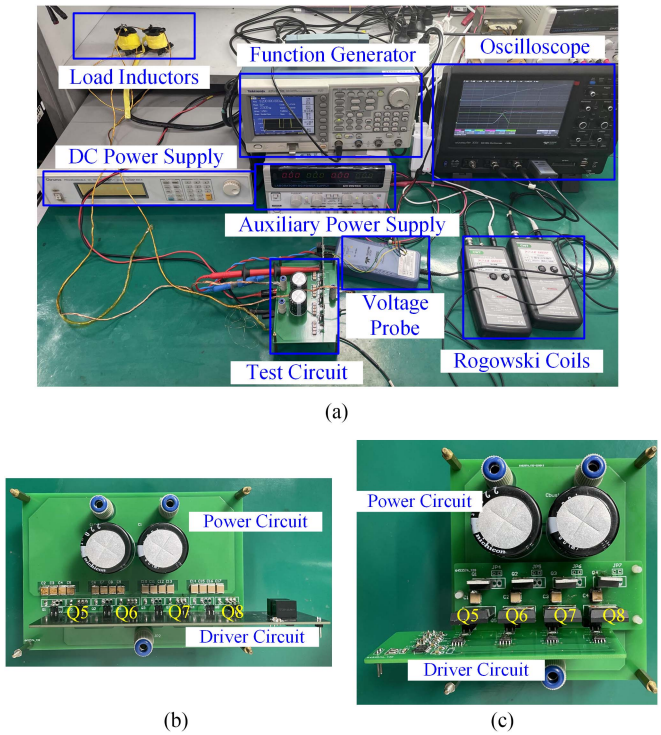


Fig. 27. Hardware setup. (a) Experimental platform. (b) Test circuit of the paralleled switching legs with distributed decoupling capacitors. (c) Test circuit of the layout of paralleled MSCs.

Then, the power loss of the ESR of a decoupling capacitor can be calculated. The temperature rise can be estimated properly. If the ripple current through the capacitor exceeds its maximum current rating, paralleling more capacitors is an effective way.

IV. Experimental Validation

In this section, DPTs are conducted under 400 V dc bus voltage to verify the theoretical analyses in Sections II and III. The experimental results of paralleled switching legs with distributed decoupling capacitors shown in Fig. 3 and the proposed paralleled MSCs shown in Fig. 14 are presented and compared. To save the cost, two double-layer PCBs are stacked to achieve a four-layer PCB layout as shown in Fig. 14. Rogowski coils from PEM (30 MHz, 300 A) are used to measure the device currents. Two 50 μH air-core inductors are series connected as the load inductor. The hardware setup is shown in Fig. 27.

The parasitic parameters of two different layouts have been listed in Tables II and III in previous sections. The key components used in the DPT test circuits are listed in Table IV. For the PCB layout shown in Fig. 3, there are four decoupling capacitors for each switching leg. For the proposed MSC method shown in Fig. 14, only one decoupling capacitor is used for a single MSC, a 220 nF/1 kV/X7R capacitor is adopted. The part numbers of the capacitors are shown in Table IV.

The power devices for two different circuit layouts are the same. For simplicity, the high side devices are replaced by SiC SBDs, which serve as freewheeling diodes. The low side SiC MOSFETs are selected and screened in advance to ensure they

TABLE IV
KEY COMPONENTS USED IN DPT TEST CIRCUITS

Components	Parameters
Electrolytic capacitors	LGU2W221MELB (Nichicon) 450 V, 220 μF
Decoupling capacitors (Fig. 3)	FV55X104K102EGG (PSA) 1 kV, 100 nF, X7R
Decoupling capacitors (Fig. 14)	FV55X224K102EHG (PSA) 1 kV, 220 nF, X7R
SiC SBDs	CSD10060A (Cree)
SiC MOSFETs	C3M0032120K (Cree)

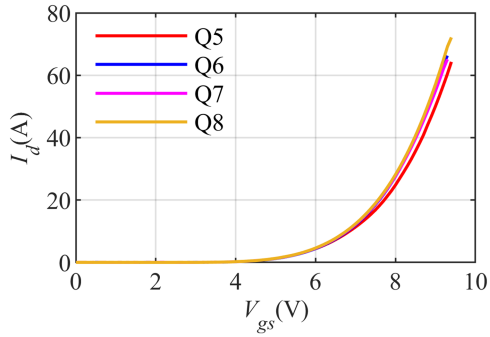


Fig. 28. Transfer curves of SiC MOSFETs.

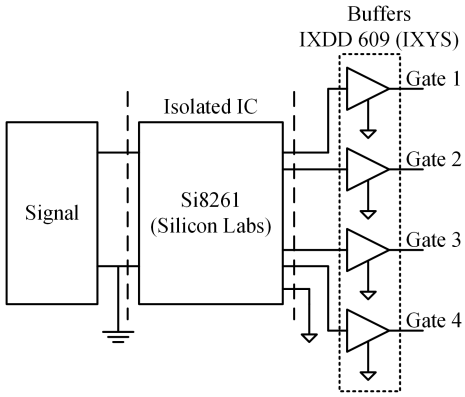


Fig. 29. Diagram of the gate driver circuit.

have similar parameters. The transfer curves of these MOSFETs are measured at 20 V v_{ds} by the curve tracer Keysight B1505A, which are shown in Fig. 28. In Fig. 28, the devices are almost identical.

The gate driver circuits for two different layouts are also the same. The diagram of the gate driver circuit is shown in Fig. 29. A single isolated driver IC is used to isolate the gate drive signals. In order to guarantee the consistency of the gate loops of the paralleled devices, four buffer stages after the isolated IC are adopted to drive the MOSFETs. In this article, the gate resistances are 20 Ω and the driver voltage is +15/−5 V.

A. Experimental Results of Paralleled Switching Legs With Distributed Decoupling Capacitors

The dynamic current sharing of the four paralleled DUTs is first measured with the layout for paralleled switching legs with distributed decoupling capacitors. The experimental results are shown in Fig. 30.

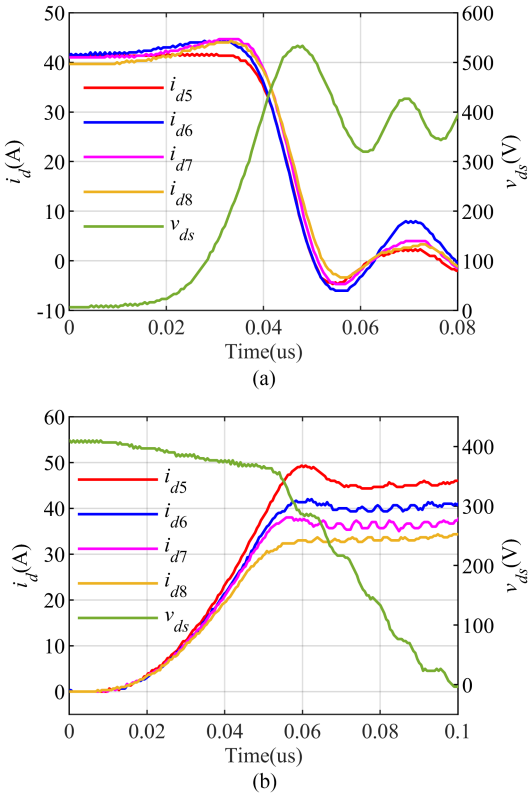


Fig. 30. Experimental results of the paralleled switching legs with distributed decoupling capacitors. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

TABLE V
PEAK CURRENTS AND SWITCHING LOSSES OF PARALLELED SWITCHING LEGS WITH DISTRIBUTED DECOUPLING CAPACITORS

$i_{d5\max}$	$i_{d6\max}$	$i_{d7\max}$	$i_{d8\max}$	i_{avg}	$\Delta i_{d\max}$	$\Delta i_{d\max}/i_{avg}$
49 A	42 A	38 A	33 A	40.5 A	16 A	39.5%
E_1	E_2	E_3	E_4	E_{avg}	$\Delta E_{\max}$	$\Delta E_{\max}/E_{avg}$
820 μJ	785 μJ	747 μJ	708 μJ	765 μJ	112 μJ	14.6%

In Fig. 30(a), the waveforms of the turn-ON currents of paralleled MOSFETs confirms the analysis in Section II ($i_{d5} > i_{d6} > i_{d7} > i_{d8}$). The peak turn-ON currents and the total switching losses are summarized in Table V. The peak current of Q_5 is about 49 A, while the peak current of Q_8 is only 33 A. The ratio of the current difference between Q_5 and Q_8 to the average peak current is up to 39.5%. The current imbalance caused by the circuit layout for paralleled switching legs with distributed decoupling capacitors is very significant due to its inherent asymmetry. The current imbalance in the turn-ON process is more significant than that in the turn-OFF process because of the current overshoots in the turn-ON process.

The switching losses of the devices with this layout are also mismatched due to the mismatched dynamic current. The switching loss imbalance is dominated by the turn-ON losses. Q_5 has the highest turn-ON loss because it has the largest current, while Q_8 has the lowest turn-ON loss. The maximum total switching loss imbalance is 14.6%.

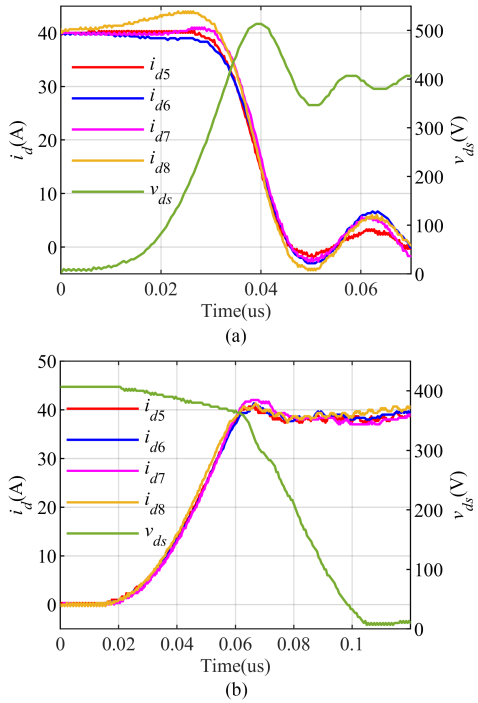


Fig. 31. Experimental results of the paralleled MSCs. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

TABLE VI
PEAK CURRENTS AND SWITCHING LOSSES OF PARALLELED MSCS

$i_{d5\max}$	$i_{d6\max}$	$i_{d7\max}$	$i_{d8\max}$	i_{avg}	$\Delta i_{d\max}$	$\Delta i_{d\max}/i_{avg}$
40.3 A	41 A	42 A	41 A	41.1 A	1.7 A	4.1%
E_1	E_2	E_3	E_4	E_{avg}	$\Delta E_{\max}$	$\Delta E_{\max}/E_{avg}$
783 μJ	785 μJ	801 μJ	815 μJ	796 μJ	32 μJ	4.0%

B. Experimental Results of Paralleled MSCs

The dynamic current sharing of the DUTs using paralleled MSCs method is also measured. The waveforms of the experiments are shown in Fig. 31.

It is obvious that the dynamic current sharing performance is significantly improved with the paralleled MSCs method. The mismatched peak turn-ON currents and total switching losses are listed in Table VI. The maximum current imbalance is only 4.1%. The current deviation during the turn-OFF transient is quite small compared with that during the turn-ON transient. In Figs. 30(b) and 31(b), the current through Q_8 is slightly increased at the beginning of the turn-OFF transient in both cases, and the maximum amplitudes are almost the same. One possible reason is that the transconductance of Q_8 is slightly larger as shown in Fig. 28. For the proposed MSCs approach, the currents of other devices during the turn-OFF transient are also well balanced, which also proves that the proposed method is effective to improve the current balancing in the turn-OFF transient.

Compared with the layout for paralleled switching legs with distributed decoupling capacitors, the switching losses are more even due to the better dynamic current sharing. The maximum switching loss difference is reduced from 112 to 32 μJ. The switching loss imbalance is only 4% in the proposed MSC method.

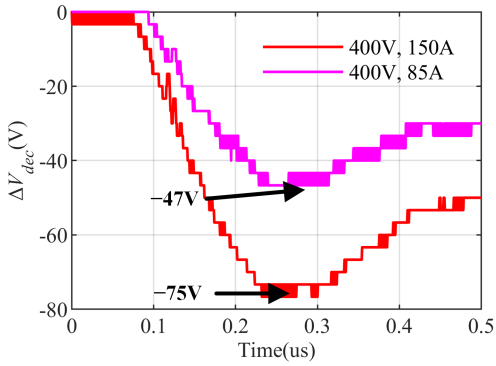


Fig. 32. Variations of DC voltage of MSC.

C. Decoupling Capacitor Voltage Fluctuation of MSCs

As has been discussed in Section III, the decoupling capacitance will influence the capacitor voltage fluctuation. The variations of decoupling capacitor voltage of the MSC in the turn-ON process are measured under different load currents. The test results are shown in Fig. 32.

The capacitance of the MLCC is affected by the dc bias voltage. The voltage rating of the MLCC used in the experiments is 1 kV. Therefore, the capacitance of the MLCC in the experiments is actually lower than the nominal value. The experimental results are similar to the simulation results shown in Fig. 21. The discrepancy might result from the inaccurate parasitic parameters of the components and dc bus.

Considering the stability of the dc voltage of the MSCs, it is recommended that more decoupling capacitors are paralleled to maintain the dc voltage. The waveforms also confirm that the voltage fluctuation is dependent on the load current. Higher load current also requires higher decoupling capacitances to maintain a reasonable voltage drop.

V. CONCLUSION

In this article, the root cause of current imbalance for paralleled SiC MOSFETs application even with the matched devices is analyzed. An equivalently symmetric power circuit layout of paralleled SiC MOSFETs is proposed based on the decoupled MSCs structure, which achieves good dynamic current sharing performance. DC decoupling capacitors, which can modify the dynamic current paths, are utilized to achieve symmetric commutation loops of paralleled devices. The current sharing of a power circuit layout for paralleled switching legs with distributed dc decoupling capacitors is analyzed. It is confirmed by experiments that significant current imbalance (39.5%) and switching loss imbalance (14.6%) will occur with this layout due to its inherent asymmetry. Based on the current sharing mechanism, independent symmetric MSCs method are proposed to construct a symmetric power circuit layout. The experimental results show the current sharing and switching loss sharing are significantly improved with the equivalently symmetric layout.

The maximum current imbalance degree and switching loss imbalance degree are only 4.1% and 4.0%, respectively. The proposed layout composed of paralleled MSCs can be easily extended to any number of paralleled devices and is simple to implement.

REFERENCES

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] A. Avron, "About the SiC MOSFETs modules in telsla model 3," pntpower, 2018. [Online]. Available: https://www.pntpower.com/tesla-model-3-powered-by-st-microelectronics-sic-mosfets/

[3] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm3 on-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419–431, Mar. 2017.

[4] H. Li et al., "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[5] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1478–1483.

[6] A. Raciti, M. Melito, M. Nania, and G. Montoro, "Effects of the device parameters and circuit mismatches on the static and dynamic behavior of parallel connections of silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1846–1852.

[7] S. Ding, P. Wang, W. Wang, D. Xu, and F. Blaabjerg, "Current sharing behavior of parallel connected silicon carbide MOSFETs influenced by parasitic inductance," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 2846–2852.

[8] R. M. Burkart, A. Bahmani, F. Kieferndorf, F. Grecki, K. Park, and F. Canales, "In-Depth analysis of static current sharing of hard-paralleled 1.7kV 700A SiC MOSFET linpak power modules," in *Proc. 20th Int. Symp. Power Electron.*, 2019, pp. 1–6.

[9] C. Zhao, L. Wang, and F. Zhang, "Effect of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with kelvin-source connection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7392–7404, Jul. 2020.

[10] Y. He, X. Wang, J. Zhang, S. Shao, H. Li, and C. Luo, "Analysis on static current sharing of N-Paralleled silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5590–5596.

[11] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "New screening method for improving transient current sharing of paralleled SiC MOSFETs," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 1125–1130.

[12] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "Chips classification for suppressing transient current imbalance of parallel-connected silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3963–3972, Apr. 2020.

[13] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1563–1569.

[14] J. Ao, Z. Wang, J. Chen, L. Peng, and Y. Chen, "The cost-efficient gating drivers with master-slave current sharing control for parallel SiC MOSFETs," in *Proc. IEEE Transp. Electrific. Conf. Expo, Asia-Pacific*, 2018, pp. 1–5.

[15] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Feb. 2021.

[16] X. Wang, Y. He, J. Zhang, S. Shao, H. Li, and C. Luo, "An active gate driver for dynamic current sharing of paralleled SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5407–5411.

[17] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with Aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.

[18] Y. Mao, Z. Miao, C. Wang, and K. D. T. Ngo, "Passive balancing of peak currents between paralleled MOSFETs with unequal threshold voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3273–3277, May 2017.

[19] Y. Mao, Z. Miao, C. Wang, and K. D. T. Ngo, "Balancing of peak currents between paralleled SiC MOSFETs by drive-source resistors and coupled power-source inductors," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8334–8343, Oct. 2017.

[20] Z. Miao, Y. Mao, G. Lu, and K. D. T. Ngo, "Magnetic integration into a silicon carbide power module for current balancing," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11026–11035, Nov. 2019.

[21] Z. Zeng, X. Zhang, and X. Li, "Layout-Dominated dynamic current imbalance in multichip power module: Mechanism modeling and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11199–11214, Nov. 2019.

[22] J. Lv, C. Chen, B. Liu, Y. Yan, and Y. Kang, "A dynamic current balancing method for paralleled SiC MOSFETs using monolithic Si-RC snubber based on a dynamic current sharing model," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13368–13384, Nov. 2022.

[23] C. Zhao, L. Wang, F. Zhang, and F. Yang, "A method to balance dynamic current of paralleled SiC MOSFETs with kelvin connection based on response surface model and nonlinear optimization," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2068–2079, Feb. 2021.

[24] F. Yang et al., "Interleaved planar packaging method of multichip SiC power module for thermal and electrical performance improvement," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1615–1629, Feb. 2022.

[25] L. Wang et al., "Cu clip-bonding method with optimized source inductance for current balancing in multichip SiC MOSFET power module," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7952–7964, Jul. 2022.

[26] M. Wang, F. Luo, and L. Xu, "A double-end sourced wire-bonded multichip SiC MOSFET power module with improved dynamic current sharing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1828–1836, Dec. 2017.

[27] J. Qu, Q. Zhang, X. Yuan, and S. Cui, "Design of a paralleled SiC MOSFET half-bridge unit with distributed arrangement of DC capacitors," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10879–10891, Oct. 2020.

[28] H. Li, "Parallel connection of silicon carbide MOSFETs for multichip power modules," Ph.D. thesis, Dept. Energy Tech., Aalborg Univ., Aalborg, Denmark, Nov. 2015.

Yang He received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with the Zhejiang University, Hangzhou, China.

His research interests include applications of wide bandgap power devices and parallel connection of SiC MOSFETs.

Junming Zhang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Zhejiang University, Hangzhou, China, in 1996, 2000, and 2004, respectively.

He is currently a Professor with the College of Electrical Engineering, Zhejiang University. From 2010 to 2011, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, Michigan State University, East Lansing, MI, USA. His research interests include power electronics system integrations, power management, and high-efficiency converters.

Prof. Zhang is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and *CPSS Transactions Power Electronics and Application*.

Shuai Shao (Member, IEEE) received the B.S. degree in electrical engineering from the Zhejiang University, Hangzhou, China, in 2010, and the Ph.D. degree in electrical and electronic engineering from the University of Nottingham, Nottingham, U.K., in 2015.

In 2015, he joined the College of Electrical Engineering, Zhejiang University, as a Lecturer. In January 2020, he was promoted as an Associate Professor. He has authored/coauthored more than 50 peer-reviewed journal and conference papers. His research interests include solid-state transformers, bidirectional dc–dc converters, and fault detection in power converters.

Dr. Shao was a Guest Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and *CES Transactions on Electrical Machines and Systems*.