Single-Phase Five-Level Multiswitch Fault-Tolerant Inverter

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***Abstract*—A novel fault-tolerant (FT) multilevel inverter (MLI) to deal with both open- and short-circuit faults on the single and multiple switches is presented in this article. It is formed by combining the main circuit and a redundant unit. With the help of a redundant unit, the proposed MLI preserves the same output power under any fault conditions as that of healthy mode. In addition, the inverter has equal efficiency under healthy and faulty scenarios for the given operating conditions. The redundant unit of the proposed FTMLI reduces the current stress on the main circuit switches under overload conditions. To validate the capabilities of the proposed MLI in tolerating the different faults, various simulation and experimental studies are carried out, and the corresponding results are presented in this article. The superior features, such as low device count, higher efficiency, and lower total blocking voltage, make the proposed MLI a reliable candidate for emergency loads. To showcase the better performance of the proposed topology over other recent topologies, comprehensive evaluation and comparisons in terms of component count and functionality are presented.**

***Index Terms*—Fault-tolerant (FT), multilevel inverter (MLI), pulsewidth modulation (PWM), switch faults, total blocking voltage (TBV).**

I. Introduction

THE multilevel inverters (MLIs) featuring high-quality output, reduced device stress, lower electromagnetic interference (EMI), and higher efficiency are continuously gaining importance in various medium- and high-power applications, such as HVdc systems, FACTS, electric vehicles, electric aircraft, and pump drives [1], [2], [3], [4]. In addition, MLIs are very much popular in applications where EMI reduction is of primary importance [5], [6]. In recent times, MLIs are also popularly being used in single-phase systems, such as distributed generation systems [7], electric vehicle chargers [8], high-frequency power distribution systems [9], and power supply for plasma dielectric barrier discharge devices [10]. Despite the advantages, the MLIs with higher device count significantly affect the system's reliability as the semiconductor devices are more prone to faults [11]. Sometimes the faults on the semiconductor switches may lead to a complete shutdown of the entire system, which causes enormous revenue loss. Furthermore, mission critical applications, such as aircraft, remote military secured systems, offshore wind energy systems, and ship propulsion systems [12], require a reliable inverter that ensures continuity of power supply even under fault conditions. In this regard, the researchers have been developing new fault-tolerant (FT) MLI topologies to address the different types of faults and preserve the continuous power supply. The various FT methods based on the hardware redundancy and control techniques for the power converters are presented in [13]. Among the different methods, the redundant parallel unit method [14] offers better performance and reliability.

Chen et al. [15] proposed an FT solution to the traditional flying capacitor MLI by using redundant switching states and modified control signals. However, the switches nearer to the dc bus cannot sustain the faults, causing a complete shutdown of the inverter. In [16], an FT method using four relays in each module is presented for the cascaded H-bridge (CHB) MLI to tolerate the faults on the switches. The incorporation of relays in the inverter makes the whole system bulky and costly. In addition, it has the drawback of high voltage stress across the healthy switches during postfault operation. A new hybrid topology [17] consisting of a cross-coupled CHB unit is developed to overcome the above drawbacks. However, this topology requires more switching devices. A single-phase five-level FT inverter [18] with a minimum number of devices is proposed for the standalone PV generation systems. Partial fault tolerance and reduced output power during the postfault operation are the main limitations of the above inverter. A hybrid MLI topology [19] derived from the combination of half-bridge leg, flying capacitor (FC) leg, and redundant leg has been introduced to overcome the above problem. This topology with an equal number of switches in both the main unit and redundant leg can tolerate the open-circuit (OC) faults on the single and multiple switches. In addition, it delivers the rated output power during fault conditions. Nevertheless, these features are obtained at the cost of a higher device count in the redundant leg. In continuation to the above topology, a resilient MLI structure with fewer number of switches in the redundant leg is proposed in [20]. The clamping diodes employed in the above structure increase the conduction losses. A new reconfigurable FTMLI that combines the T-type module and neutral point clamped (NPC) unit proposed in [21] provides the complete solution to the switch faults at various locations. The utilization of the bidirectional switches in the

Manuscript received 22 July 2022; revised 11 December 2022 and 2 February 2023; accepted 14 March 2023. Date of publication 20 March 2023; date of current version 20 April 2023. Recommended for publication by Associate Editor A. Ioinovici. *(Corresponding author: Sankar Peddapati.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3259722.

Digital Object Identifier 10.1109/TPEL.2023.3259722

redundant leg adds higher cost and complexity to the inverter. To overcome the above problem, an efficient five-level FT topology [22] without bidirectional switches is introduced. In addition to the FT characteristics, it has an overload capability feature, i.e., reducing the burden on the switching devices under overload conditions. Two new topologies [14], [23] based on the full-bridge NPC inverter and redundant leg are proposed for tolerating both OC and short-circuit (SC) faults on single and multiple switches. The main limitations of these topologies are increased device count and higher total bocking voltage (TBV). A new five-level reconfigurable MLI with single- and multi-switch FT capability using less number of switches is presented in [24]. However, it requires an enormous number of diodes, leading to higher conduction losses in the system. In addition, it cannot completely provide fault tolerance to the multiple switch failure cases. Two new nine-level switched capacitor-based FT MLI topologies [25], [26] can effectively tolerate both OC and SC faults on the single and multiple switches. The presence of the flying capacitors drastically reduces the reliability of the inverter as they have a higher probability of failure after the semiconductor switches [8]. In addition, the topology [26] uses bidirectional switches, which results in increased conduction losses of the inverter. A reliable five-level inverter for a linear generator-based wave power generation system is presented in [27]. This inverter ensures the uninterruptable tapping of wave power under a single-switch and some multiswitch fault conditions only. The other type of MLI topologies, such as modular MLIs [28], [29], incorporates the FT features by using redundant submodules. However, they employ a vast number of switching devices that ultimately increase the cost and complexity of the system. The increased number of flying capacitors and dc-link capacitors in the FT topology [30] significantly reduces the reliability of the entire system. A recently proposed generalized MLI incorporates the FT features without using any capacitors and bidirectional switches. However, it has the drawbacks of limited FT capability and inability to deliver the rated power for most of the multiswitch fault conditions [31].

In order to address the above issues, a novel FT single-phase five-level inverter with the following key features is proposed in this article:

1) low switch count;
2) OC and SC FT capability for single- and multiswitch faults;
3) ability to deliver rated output power under various fault conditions;
4) increased overload capability;
5) higher efficiency during healthy and faulty conditions.

II. Working of the Proposed FTMLI

A. Topology Description

The schematic diagram of the proposed FTMLI consisting of the main circuit and redundant unit is shown in Fig. 1. The main unit comprises of eight switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8 that generate the five-level output voltage under fault-free conditions. On the other hand, the redundant unit made of four switches R_1, R_2, R_3, and R_4 tolerates the various OC and SC

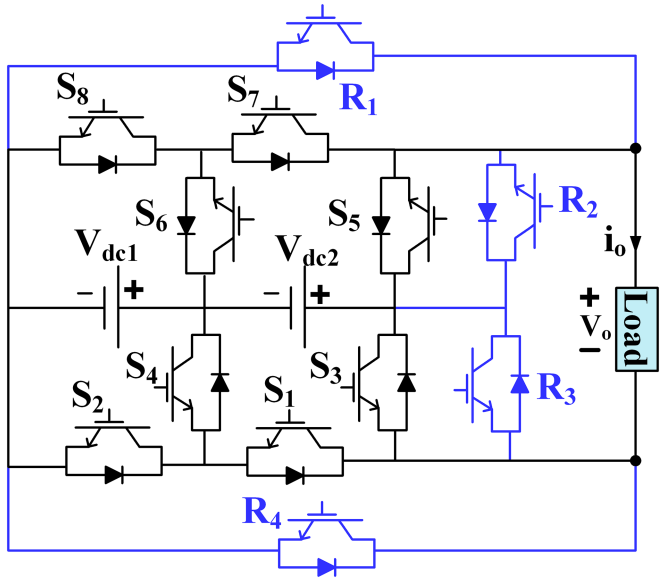


Fig. 1. Schematic diagram of the proposed FTMLI.

faults of the main circuit. The voltage and current ratings are the crucial parameters for selecting the semiconductor switches of the inverter. In the proposed topology, the switches S_1, S_2, S_4, S_6, S_7, and S_8 of the man unit operate at a higher frequency and should block half of the total input voltage. The remaining switches, S_3 and S_5, operate at the low (fundamental) frequency and should block total input voltage. So, the switches S_3 and S_5 can be implemented using low-frequency semiconductor devices. The current rating for all the switches presented in the main unit of the proposed inverter is equal to the rated load current (I_o) except for the switches S_4 and S_6. The switches S_4 and S_6 must carry half of the rated load current ($I_o/2$). Equations (1) and (2) summarize each main unit switch's voltage and current ratings

$$V_{S_1} = V_{S_2} = V_{S_4} = V_{S_6} = V_{S_7} = V_{S_8} = V_{\rm dc}, \quad V_{S_3} = V_{S_5} = 2V_{\rm dc} \tag{1}$$

$$I_{S_1} = I_{S_2} = I_{S_3} = I_{S_5} = I_{S_7} = I_{S_8} = I_o, \quad I_{S_4} = I_{S_6} = \frac{I_o}{2}. \tag{2}$$

The voltage and current ratings for the redundant switches are as follows:

$$V_{R_1} = V_{R_2} = V_{R_3} = V_{R_4} = 2V_{\rm dc} \tag{3}$$

$$I_{R_1} = I_{R_2} = I_{R_3} = I_{R_4} = I_o. \tag{4}$$

In this work, all the switches are realized using the same IGBT, which can withstand the highest voltage stress, i.e., total input voltage and highest current stress I_o.

B. Healthy Case (HC)

The main circuit of the proposed MLI with two dc sources $V_{\rm dc1}$ and $V_{\rm dc2}$ generates the five-level load voltage waveform

TABLE I
SWITCHING STATES OF THE MAIN CIRCUIT UNDER HEALTHY CONDITION (1 = SWITCH ON AND 0 = SWITCH OFF)

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	State number	Voltage level	Voltage magnitude
1	1	0	0	1	0	0	0	P_1	V_1	$+2V_{dc}$
1	0	0	1	1	0	0	0	P_2	V_2	$+V_{dc}$
1	1	0	0	0	1	1	0	P_3		
0	0	1	0	1	0	0	0	Z_1	V_3	0
1	0	0	1	0	1	1	0	Z_2		
1	1	0	0	0	0	1	1	Z_3		
0	0	1	0	0	1	1	0	N_1	V_4	$-V_{dc}$
1	0	0	1	0	0	1	1	N_2		
0	0	1	0	0	0	1	1	N_3	V_5	$-2V_{dc}$

consisting of $\pm 2V_{dc}$, $\pm V_{dc}$, and zero-voltage levels under healthy conditions. The different switching combinations to generate the five-level output voltage are given in Table I. It shows that the voltage levels $+V_{dc}$, 0, and $-V_{dc}$ have redundant states, providing the FT ability to the proposed topology. The switching states P_1, P_2, Z_1, N_1, and N_3 are selected to generate five-level output under normal operating conditions as these states contain the minimum number of conducting devices resulting in lower conduction losses.

C. Faulty Case

The operation of the main circuit is sensitive to the failure of the switching devices. Table II presents the effect of the single- and multiswitch OC and SC faults on the output voltage levels of the main circuit. It can be seen that the OC fault on the switches causes the loss of one or more voltage levels at the load terminals, and also, in most of the faulty cases, the output power during postfault state is not restored to the prefault state. On the other hand, the SC fault can generate the corresponding voltage levels. However, to avoid the short circuiting of the dc sources, the conduction path of other voltage levels, which includes the complementary switch of the faulty, should be made inactive and, in turn, results in reduced output power. The degraded performance of the inverter during postfault state is not suitable for most of the applications, such as motor drives, renewable energy systems, uninterruptible power supplies (UPSs), and electric vehicles [32]. The severity of the loss of voltage levels in the main circuit is more when multiple switches undergo simultaneous fault. One such scenario is the simultaneous OC fault on the switches S_1 and S_3 that causes loss of all voltage levels and shut down of the inverter. To resolve the above issues, a redundant unit is connected across the load terminals, as shown in Fig. 1.

The addition of the redundant unit Incorporates the following features to the main circuit:

1) single- and multiswitch OC FT capability;
2) single- and multiswitch SC FT capability;
3) capability to maintain the prefault output power during postfault state;
4) maintain the same efficiency under pre- and postfault states;
5) improved reliability.

TABLE II
AVAILABLE VOLTAGE LEVELS UNDER FAULTY CONDITIONS WITHOUT REDUNDANT UNIT

Faulty switches	Status of output voltage levels under OCF condition						Status of output voltage levels under SCF condition					
	V_1	V_2	V_3	V_4	V_5	1[a]	V_1	V_2	V_3	V_4	V_5	1[a]
S_1	X	X	√	√	√	X	√	√	√	√	X	X
S_2	X	√	√	√	√	X	√	√	√	√	√	√
S_3	√	√	X	X	X	X	X	X	√	√	√	X
S_4	√	X	√	√	√	√	X	√	√	√	√	X
S_5	X	X	X	√	√	X	√	√	√	X	X	X
S_6	√	√	√	X	√	√	√	√	√	√	X	X
S_7	√	√	√	X	X	X	X	√	√	√	√	X
S_8	√	√	√	√	X	X	√	√	√	√	√	√
S_1S_2	X	X	√	√	√	X	√	√	√	X	X	X
S_1S_3	X	X	X	X	X	X	X	X	X	X	X	X
S_1S_4	X	X	√	√	√	X	X	√	√	√	X	X
S_1S_5	X	X	X	√	√	X	√	√	X	X	X	X
S_1S_6	X	X	√	X	√	X	√	√	√	X	X	X
S_1S_7	X	X	√	X	X	X	X	√	√	√	X	X
S_1S_8	X	X	√	√	X	X	√	√	√	√	X	X
S_2S_3	X	√	X	X	X	X	X	X	√	√	√	X
S_2S_4	X	X	√	√	√	X	X	X	√	√	√	X
S_2S_5	X	X	X	√	√	X	√	X	√	X	√	√
S_2S_6	X	√	√	X	√	X	√	√	√	√	X	X
S_2S_7	X	√	√	X	X	X	X	√	√	√	√	X
S_2S_8	X	√	√	√	X	X	√	X	√	X	√	√
S_3S_4	√	X	X	X	X	X	X	X	√	√	√	X
S_3S_5	X	X	X	X	X	X	X	X	√	X	X	X
S_3S_6	X	X	√	√	√	X	X	X	√	√	X	X
S_3S_7	√	√	X	X	X	X	X	X	X	√	√	X
S_3S_8	√	√	X	X	X	X	X	X	√	X	√	X
S_4S_5	X	X	X	√	√	X	X	√	√	X	X	X
S_4S_6	√	X	√	X	√	√	X	√	√	√	X	X
S_4S_7	√	X	√	X	X	X	X	X	√	√	√	X
S_4S_8	√	X	√	√	X	X	X	√	√	√	√	X
S_5S_6	X	X	X	X	√	X	√	√	√	X	X	X
S_5S_7	X	X	X	X	X	X	X	X	X	X	X	X
S_5S_8	X	X	X	√	X	X	√	√	√	X	X	X
S_6S_7	√	√	√	X	X	X	X	√	√	√	√	X
S_6S_8	√	√	√	X	X	X	√	√	√	X	X	X
S_7S_8	√	√	√	X	X	X	X	X	√	√	√	X
$S_1S_2S_3$	X	X	X	X	X	X	X	X	X	X	X	X
$S_1S_2S_4$	X	X	√	√	√	X	X	X	X	X	X	X
$S_1S_2S_5$	X	X	X	√	√	X	X	X	X	X	X	X
$S_1S_2S_6$	X	X	√	X	√	X	√	√	X	X	X	X
$S_1S_2S_7$	X	X	√	X	X	X	X	√	√	X	X	X
$S_1S_2S_8$	X	X	√	√	X	X	√	X	√	X	X	X
$S_2S_3S_4$	X	X	X	X	X	X	X	X	√	√	√	X
$S_2S_3S_5$	X	X	√	√	X	X	X	X	√	X	X	X
$S_2S_3S_6$	X	√	X	√	X	X	X	X	√	√	X	X
$S_2S_3S_7$	X	√	X	X	X	X	X	X	X	√	X	X
$S_2S_3S_8$	X	X	√	√	X	X	X	X	√	X	√	X
$S_3S_4S_5$	X	X	√	√	X	X	X	X	√	X	X	X
$S_3S_4S_6$	√	X	√	X	X	X	X	X	√	√	X	X
$S_3S_4S_7$	√	X	X	X	X	X	X	X	X	√	√	X
$S_3S_4S_8$	√	√	X	X	X	X	X	X	√	X	√	X
$S_4S_5S_6$	X	X	√	X	√	X	X	√	√	X	X	X
$S_4S_5S_7$	X	X	X	X	X	X	X	X	X	X	X	X
$S_4S_5S_8$	X	√	X	X	X	X	X	√	√	√	√	X
$S_5S_6S_7$	X	X	X	X	X	X	X	X	X	X	X	X
$S_5S_6S_8$	X	X	X	X	X	X	√	√	√	X	X	X
$S_6S_7S_8$	√	√	√	X	X	X	√	√	√	X	X	X

1[a]: Post fault output power = pre fault output power

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter/component	Value/rating
IGBT Switch: FGA15N120ANTD	1200 V, 15 A
Controller	SPARTAN6 FPGA
Optocoupler	TLP250
Input DC Sources	$V_{dc1} = V_{dc2} = 24$ V
Output frequency	$f_o = 50$ Hz
Switching frequency	$f_s = 5$ kHz
Modulation index	$m_a = 0.9$
Load resistance	R = 25 Ω
Load inductance	L = 25 mH

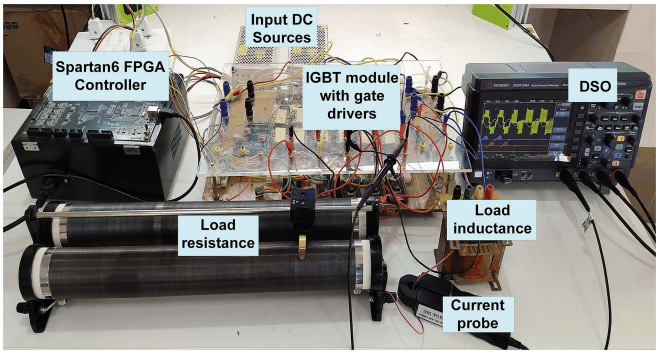


Fig. 2. Hardware setup of the proposed system.

III. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed FTMLI under various switch OC and SC fault conditions has been validated through simulation and experimental studies. Table III list out the parameters considered in simulation and experimental studies. The hardware setup of the proposed system consisting of the IGBT module with gate drivers, SPARTAN6 FPGA controller, and *R–L* load is depicted in Fig. 2. Here, modulation strategies, such as level-shifted carrier pulsewidth modulation (PWM) and space vector modulation, can be used; but the former is employed for the proposed converter as it is simple and reliable. The flowchart that indicates the steps involved in implementing the conventional level-shifted carrier PWM (LSCPWM) control strategy using the SPARTAN6 FPGA controller to generate the switching pulses is shown in Fig. 3. Here, the modulation index (m_a), switching frequency (f_s), and output frequency (f_o) are given to the microcontroller and are programmed to generate the PWM pulses using LSCPWM technique. The fault detection (FD) algorithm employed in the controller detects the faults on the switches, and accordingly gate pulses to the switches are generated as per the switching, as given in Table IV. Eight different fault cases, which includes both OC and SC faults on single as well as multiple switches, are considered to verify the working of the proposed topology. In this work, the OC fault on the switch is emulated by withdrawing gate pulses to it, whereas the SC fault is emulated by providing a continuous gate pulse to it. However, the FD can be carried out by using the smart gate drivers (SGD), such as TLP5214/TLP5212/TLP5222 with DESAT protection feature. The SGD continuously monitors the collector to emitter voltage (V_{CE}) of the switch through DESAT

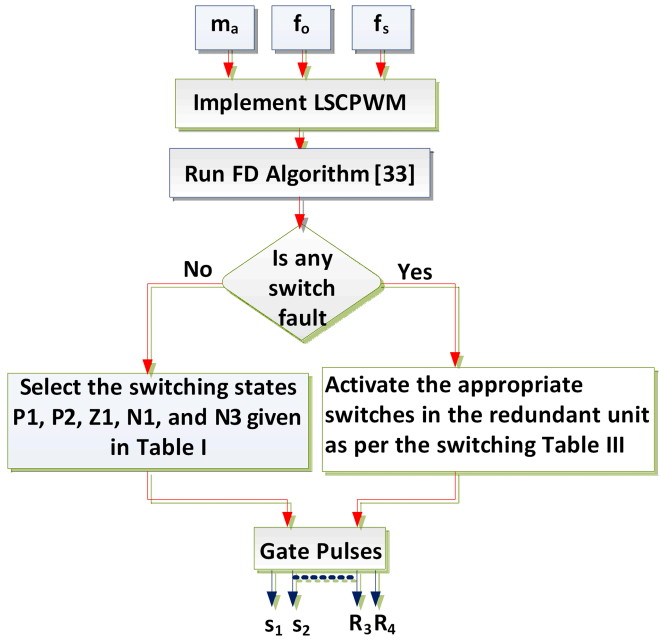


Fig. 3. Flowchart for generating the switching pulses under healthy and faulty conditions.

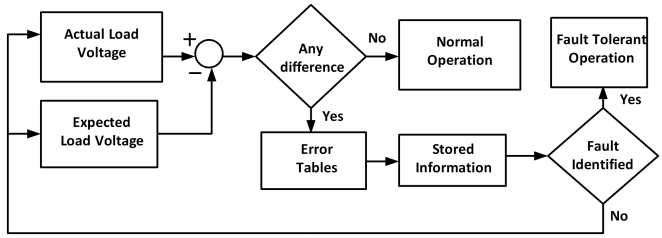


Fig. 4. Block diagram of the FD method based on the waveform analysis.

pins. Under healthy condition, the value of $V_{CE(sat)}$ is low; however, in the event of SC fault, the $V_{CE(sat)}$ increases to beyond its threshold value. Once the fault is identified by the SGD, it sends the fault signal to the controller. However, the FD methods given in [33] can be used to identify the OC fault on the switches, as shown in Fig. 4. Here, the error, which is the difference between the actual and expected load voltage, is initially stored for each switch failure case in the microcontroller as a lookup table. Then, the actual output voltage measured from the sensor is compared with the expected load voltage for one complete cycle. The combination of mismatches between the measured and anticipated voltage levels from the lookup table is used to identify the specific switch failure in real time. Then, the converter is reconfigured by providing the control signals to switches in providing alternative conduction path as per Table IV.

A. OC Fault Analysis

Five different cases, such as one single-switch fault (S_1), one antiparallel diode fault of the switch S_7 (S_{d7}), and three multiswitch fault cases (S_4S_6, $S_2S_4S_8$, and $S_1S_4S_6S_8$), are considered for the OC FT analysis of the proposed topology.

TABLE IV
SWITCHING SCHEME OF THE PROPOSED FTMLI UNDER VARIOUS FAULT CONDITIONS

Faulty switches	Conducting switches for the voltage levels				
	$+2V_{dc}$	$+V_{dc}$	0	$-V_{dc}$	$-2V_{dc}$
$S_1/S_2/S_4/S_1S_2/S_1S_4/S_2S_4$	S_5R_4	$S_6S_7R_4$	S_3S_5	$S_3S_6S_7$	$S_3S_7S_8$
S_3	$S_1S_2S_5$	$S_1S_4S_5$	S_5R_3	$S_6S_7R_3$	$S_7S_8R_3$
S_5/S_3S_5	$S_1S_2R_2$	$S_1S_4R_2$	R_2R_3	$S_3S_6S_7$	$S_3S_7S_8$
S_6/S_3S_6	$S_1S_2S_5$	$S_1S_4S_5$	S_5R_3	$S_1S_4R_1$	$S_7S_8R_3$
S_7	$S_1S_2S_5$	$S_1S_4S_5$	S_3S_5	$S_1S_4R_1$	S_3R_1
S_8	$S_1S_2S_5$	$S_1S_4S_5$	S_3S_5	$S_3S_6S_7$	S_3R_1
$S_1S_3/S_2S_3S_4$	S_5R_4	$S_6S_7R_4$	S_5R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_1S_5/S_2S_5/S_1S_4S_5$	R_2R_4	$S_6S_7R_4$	S_3R_2	$S_3S_6S_7$	$S_3S_7S_8$
S_1S_6/S_1S_7	S_5R_4	-	S_3R_2	-	S_3R_1
S_1S_8	S_5R_4	$S_6S_7R_4$	S_3S_5	$S_3S_6S_7$	S_3R_1
S_2S_3	S_5R_4	$S_1S_4S_5$	S_5R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_2S_6/S_2S_7/S_2S_8$	S_5R_4	$S_1S_4S_5$	S_3S_5	$S_1S_4R_1$	S_3R_1
S_3S_4	$S_1S_2S_5$	$S_6S_7R_4$	S_5R_3	$S_6S_7R_3$	$S_7S_8R_3$
S_3S_7/S_3S_8	$S_1S_2S_5$	$S_1S_4S_5$	S_5R_3	$S_1S_4R_1$	R_1R_3
S_4S_5	$S_1S_2R_2$	$S_6S_7R_4$	S_3R_2	$S_3S_6S_7$	$S_3S_7S_8$
S_4S_6	$S_1S_2S_5$	-	S_3S_5	-	$S_3S_7S_8$
$S_4S_7/S_4S_6S_7/$ $S_4S_6S_8/S_4S_7S_8$	$S_1S_2S_5$	-	S_3S_5	-	S_3R_1
S_4S_8	$S_1S_2S_5$	$S_6S_7R_4$	S_3S_5	$S_3S_6S_7$	S_3R_1
S_5S_6	$S_1S_2R_2$	$S_1S_4R_2$	S_3R_2	$S_1S_4R_1$	$S_3S_7S_8$
$S_5S_7/S_5S_6S_7/$ $S_5S_6S_8/S_5S_7S_8/S_6S_7S_8$	$S_1S_2R_2$	$S_1S_4R_2$	S_3R_2	$S_1S_4R_1$	S_3R_1
S_5S_8	$S_1S_2R_2$	$S_1S_4R_2$	S_3R_2	$S_3S_6S_7$	S_3R_1
$S_6S_7/S_6S_8/S_7S_8$	$S_1S_2S_5$	$S_1S_4S_5$	S_3S_5	$S_1S_4R_1$	S_3R_1
$S_1S_2S_3$	S_5R_4	$S_6S_7R_4$	S_5R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_1S_2S_4$	S_5R_4	$S_6S_7R_4$	S_3S_5	$S_3S_6S_7$	$S_3S_7S_8$
$S_1S_2S_5/S_2S_4S_5$	R_2R_4	$S_6S_7R_4$	S_3R_2	$S_3S_6S_7$	$S_3S_7S_8$
$S_1S_2S_6/S_2S_4S_6$	S_5R_4	-	S_3S_5	-	$S_3S_7S_8$
$S_1S_2S_7/S_1S_4S_6/S_1S_4S_7/$ $S_1S_6S_7/S_1S_6S_8/S_1S_7S_8/$ $S_2S_4S_7$	S_5R_4	-	S_3S_5	-	S_3R_1
$S_1S_2S_8/S_1S_4S_8/S_2S_4S_8$	S_5R_4	$S_6S_7R_4$	S_3S_5	$S_3S_6S_7$	S_3R_1
$S_1S_3S_4$	S_5R_4	$S_6S_7R_4$	S_5R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_1S_3S_5$	R_2R_4	$S_6S_7R_4$	R_2R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_1S_3S_6$	S_5R_4	-	S_5R_3	-	$S_7S_8R_3$
$S_1S_3S_7$	S_5R_4	-	S_5R_3	-	R_1R_3
$S_1S_3S_8$	S_5R_4	$S_6S_7R_4$	S_5R_3	$S_6S_7R_3$	R_1R_3
$S_1S_5S_6/S_1S_5S_7$	R_2R_4	-	S_3R_2	-	S_3R_1
$S_1S_5S_8$	R_2R_4	$S_6S_7R_4$	S_3R_2	$S_3S_6S_7$	S_3R_1
$S_2S_3S_5$	R_2R_4	$S_1S_4R_2$	R_2R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_2S_3S_6/S_2S_3S_7/S_2S_3S_8$	S_5R_4	$S_1S_4S_5$	S_5R_3	$S_1S_4R_1$	R_1R_3
$S_2S_5S_6$	R_2R_4	$S_1S_4R_2$	S_3R_2	$S_1S_4R_1$	$S_3S_7S_8$
$S_2S_5S_7$	R_2R_4	$S_1S_4R_2$	S_3R_2	$S_1S_4R_1$	S_3R_1
$S_2S_5S_8$	R_2R_4	$S_1S_4R_2$	S_3R_2	$S_3S_6S_7$	S_3R_1
$S_2S_6S_7/S_2S_6S_8/$ $S_2S_7S_8$	S_5R_4	$S_1S_4S_5$	S_3S_5	$S_1S_4R_1$	S_3R_1
$S_3S_4S_5$	$S_1S_2R_2$	$S_6S_7R_4$	R_2R_3	$S_6S_7R_3$	$S_7S_8R_3$
$S_3S_4S_6/S_3S_4S_7$	$S_1S_2S_5$	-	S_5R_3	-	R_1R_3
$S_3S_4S_8$	$S_1S_2S_5$	$S_6S_7R_4$	S_5R_3	$S_6S_7R_3$	R_1R_3
$S_3S_5S_6/S_3S_5S_7/S_3S_5S_8/$ $S_3S_6S_7/S_3S_6S_8/S_3S_7S_8$	$S_1S_2R_2$	$S_1S_4R_2$	R_2R_3	$S_1S_4R_1$	R_1R_3
$S_4S_5S_6$	$S_1S_2R_2$	-	S_3R_2	-	$S_3S_7S_8$
$S_4S_5S_7$	$S_1S_2R_2$	-	S_3R_2	-	S_3R_1
$S_4S_5S_8$	$S_1S_2R_2$	$S_6S_7R_4$	S_3R_2	$S_3S_6S_7$	S_3R_1

1) OC Fault on Switch S_1*:* From Table II, it can be observed that the OC fault on the switch S_1 would result in loss of voltage levels $+2V_{dc}$, and $+V_{dc}$. The simulation and experimental results of the proposed FTMLI for the switch S_1 OC fault condition are shown in Fig. 5. It can be seen that the OC fault is created at $t = 0.004$ s in the simulation study by withdrawing gate pulses to it. During the postfault state, the switch R_4 of the redundant unit is triggered to generate the five-level output voltage at the load terminals. From Fig. 5, it can be seen that the experimental

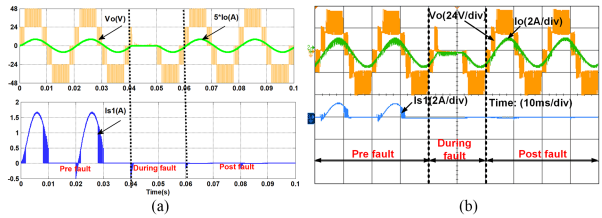


Fig. 5. (a) Simulation and (b) experimental results under S_1 OC fault condition.

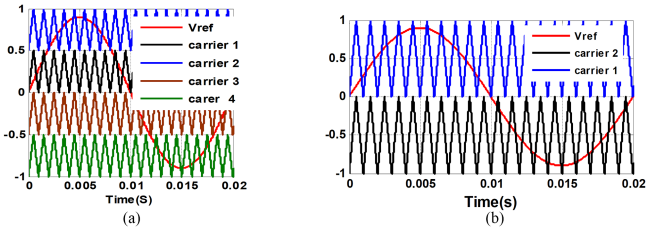


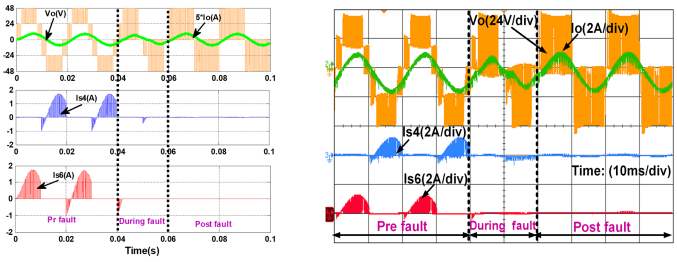
Fig. 6. Carrier signals under (a) healthy condition and (b) S_4S_6 OC fault conditions.

results are well matched with the simulation results. It is clear from Table IV that the number of conducting devices remains the same in both pre- and postfault states. As a result, the efficiency of the proposed FTMLI under healthy and faulty conditions remains the same. In all simulation results, to increase the current visibility along with the voltage, the output current is scaled up by a factor of 5.

2) Simultaneous OC Fault on Switches S_4 *and* S_6*:* Under this simultaneous fault condition, the voltage levels $+V_{dc}$ and $-V_{dc}$ are not possible to generate at the output. During the postfault state, the output voltage consisting of the levels $+2V_{dc}$, 0, and $-2V_{dc}$ is produced at the load terminals. In this fault scenario, even after reconfiguration, the voltage levels $+V_{dc}$ and $-V_{dc}$ are not possible to generate at the output. However, with the possible voltage levels ($+2V_{dc}$, 0, and $-2V_{dc}$), the rated output power can be maintained. Here, the control strategy requires modifications in the carrier signals to generate the above load voltage waveform. The carrier signals required to implement the control strategy under healthy and S_4S_6 fault conditions are shown in Fig. 6. From the figure, it can be noticed that the number of carriers and their positions are different for the considered fault condition.

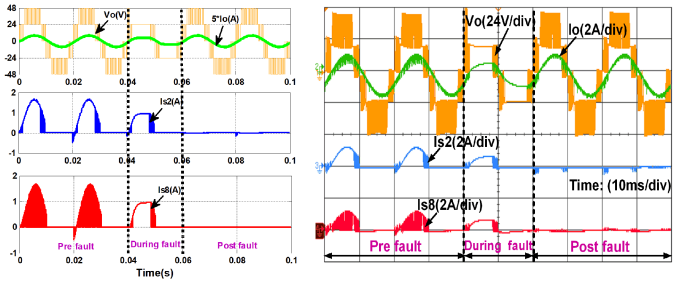
The simulation and experimental results of the proposed topology under OC fault on the switches S_4 and S_6 are shown in Fig. 7. Although the proposed topology generates the three-level waveform, the prefault output power is delivered to the load in this scenario.

3) Simultaneous OC Fault on Switches S_2*,* S_4*, and* S_8*:* One of the important features of the proposed topology is the ability to tolerate the simultaneous OC fault on three switches, which are not found in many FTMLI topologies. The OC fault on the switches S_2, S_4, and S_8 is considered to validate the above feature. In the simulation study, the OC fault is created by removing the gate pulses to the above switches at $t = 0.04$ s. At



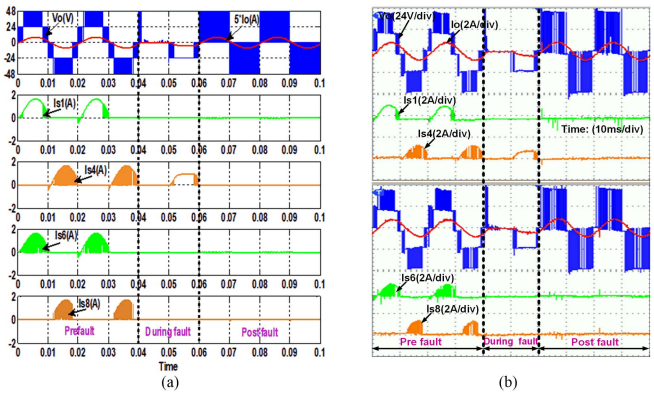
(a) (b)

Fig. 7. (a) Simulation and (b) experimental results under simultaneous OC fault on S_4 and S_6.



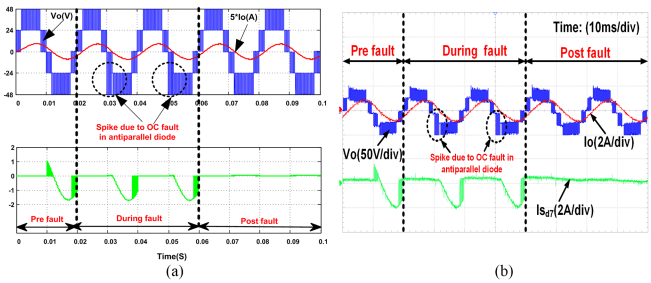
(a) (b)

Fig. 8. (a) Simulation and (b) experimental results under simultaneous OC fault on S_2, S_4, and S_8.



(a) (b)

Fig. 9. (a) Simulation and (b) experimental results under simultaneous OC fault on S_1, S_4, S_6, and S_8.



(a) (b)

Fig. 10. (a) Simulation and (b) experimental results under OC fault on S_{d7}.

this instant, the upper voltage levels $+2V_{\rm dc}$ and $-2V_{\rm dc}$ cannot be produced at the output waveform. In order to generate the above voltage levels, the switches R_1 and R_4 from the redundant unit are activated at $t = 0.06$ s. The corresponding simulation and experimental results for this fault condition are depicted in Fig. 8. The figure shows that upon the activation of appropriate redundant unit switches, all five voltage levels are generated in the postfault state. Hence, it can be concluded that the proposed FTMLI can tolerate the simultaneous OC fault on three switches with an equal number of conducting switches in both pre- and postfault states. As a result, the efficiency of the proposed topology remains the same in both states.

4) Simultaneous OC Fault on Switches S_1, S_4, S_6, *and* S_8: Under this simultaneous fault condition, the voltage levels $+V_{\rm dc}$ and $-V_{\rm dc}$ are impossible to generate at the output. However, the remaining voltage levels, such as $+2V_{\rm dc}$, 0, and $-2V_{\rm dc}$, can be generated at the output by using the redundant unit switches. During the reconfiguration state, the redundant switch R_4 is turned ON to generate the $+2V_{\rm dc}$ level, and the $-2V_{\rm dc}$ level is generated by turning ON the switch R_1. Even though the output voltage has three levels, the rated power is still delivered to the load under this fault condition. The same control strategy employed in the simultaneous fault on S_4 and S_6 is utilized for this fault condition. The simulation and experimental results for this fault condition are shown in Fig. 9. The figure shows that the proposed topology can tolerate the simultaneous OC fault on the four switches, which is not found in any recently developed FT topologies.

5) OC Fault on Antiparallel Diode of Switch S_7: The OC fault on the antiparallel diode will have either of the following two effects on the output waveform. First, the antiparallel diode provides the path for the load current in case of inductive loads, and the OC fault on it causes the spike in the output voltage; the other impact of the diode fault is missing voltage levels at the output. However, the location of the OC fault on antiparallel diode requires an additional sensor [34], and FD becomes challenging in the proposed converter. Here, to verify the FT capability of the proposed inverter, the OC fault on the antiparallel diode (S_{d7}) of the switch S_7 is emulated, and the corresponding redundant switching states are activated as per Table IV. The simulation and experimental studies are carried out with a load of $R = 20\ \Omega$ and $L = 50$ mH for the above case study and the corresponding results are shown in Fig. 10. It can be seen that the OC fault on S_{d7} produces a spike during the $-V_{\rm dc}$ level of the output voltage. During the postfault state, the gate pulses are withdrawn to the switch S_7 and the redundant switch R_1 is activated to eliminate the voltage spike in the output voltage. This case study also reveals that the proposed FT inverter can work for predominant inductive loads also.

B. SC Fault Analysis

The effect of the SC fault on the semiconductor device is severely compared with the OC fault. Here, three different case studies are considered to evaluate the performance of the proposed FTMLI for tolerating the SC fault on the switches and antiparallel diodes.

1) SC Fault on Switch S_6: During the SC fault on the switch S_6, turning ON its complementary switch S_8 for generating the

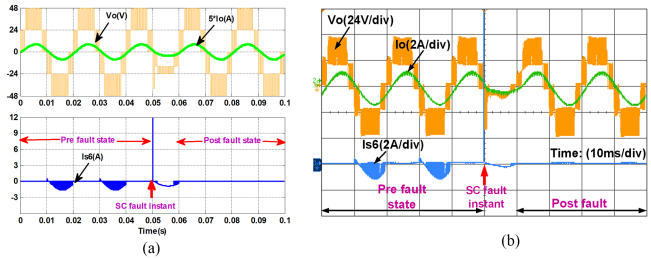


Fig. 11. (a) Simulation and (b) experimental results under S_6 SC fault.

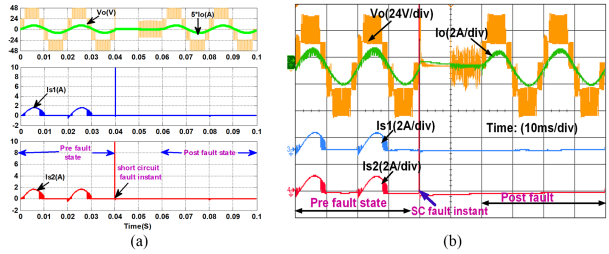


Fig. 12. (a) Simulation and (b) experimental results for simultaneous SC fault on S_1 and S_2.

voltage levels $-V_{\rm dc}$ and $-2V_{\rm dc}$ causes an SC of the input dc voltage source $V_{\rm dc1}$. As a result, a higher magnitude of current flows, and thereby, the SC fault is converted into OC fault. Fig. 11 shows the simulation and experimental results for the S_6 SC fault condition. At the SC fault instant, a large spike is observed in the switch S_6 current (Is_6), which is due to the short circuiting of the input dc source $V_{\rm dc1}$; consequently, SC fault is converted into an OC fault. The switch R_1 from the redundant unit is activated during the postfault state to generate the prefault voltage levels, as seen in Table IV.

2) SC Fault on Switches S_1 *and* S_2*:* The case study of SC fault on switches S_1 and S_2 is taken to verify the FT characteristics of the proposed topology for simultaneous SC fault on the two switches. Under this fault case, the two input dc sources are short circuited when the switch S_3 is turned ON to generate the 0, $-V_{\rm dc}$, and $-2V_{\rm dc}$ voltage levels. The simulation and experimental results of the proposed topology for S_1 and S_2 simultaneous SC fault conditions are shown in Fig. 12. The figure reveals that, during the faulty instant, a higher amount of current is flowing through the switches S_1 and S_2 due to the short circuiting of the two input dc sources; consequently, SC fault is converted into an OC fault. The switches R_3 and R_4 from the redundant unit are activated during the postfault state to generate the prefault voltage levels, as seen in Table IV.

3) SC Fault on Antiparallel Diode of Switch S_5*:* The SC fault on the antiparallel diode produces a similar effect as that of SC fault on its corresponding switch and is identified through smart gate drive circuit. To test the capability of the proposed inverter in tolerating the SC fault on the antiparallel diode of a switch, fault on the antiparallel diode (S_{d5}) of S_5 is chosen. During the SC fault on S_{d5}, turning ON the switches S_6 and S_7 for generating the voltage level $+V_{\rm dc}$ causes an SC of the input dc source $V_{\rm dc2}$. As a result, a higher magnitude of current flows, and thereby, the SC fault is converted into OC fault. The simulation and experimental studies are carried out with a load of $R = 20\ \Omega$ and $L = 50$ mH for the above case study and the results are shown in Fig. 13.

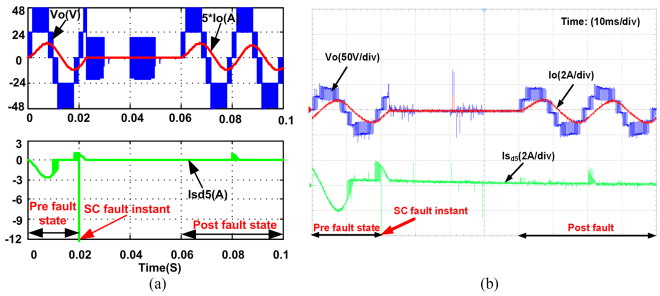


Fig. 13. (a) Simulation and (b) experimental results under S_{d5} SC fault.

TABLE V
THD OF THE OUTPUT VOLTAGE AND CURRENT FOR THE PROPOSED INVERTER

No of levels	Voltage THD		Current THD	
	Without filter	With filter	Without filter	With filter
5-level	33.51%	2.30%	2.30%	0.91%
3-level	64.39%	3.15%	1.72%	0.36%

At the SC fault instant, a large spike is observed in the diode current (Is_{d5}), which is due to the short circuiting of the input dc source $V_{\rm dc2}$; consequently, SC fault is converted into an OC fault. The switch R_1 from the redundant unit is activated during the postfault state to generate all the prefault voltage levels.

From the above OC and SC fault analysis, it can be noted that the proposed topology can sustain all types of OC and SC faults on the single and multiple switching devices. This shows that the proposed topology is highly reliable for emergency applications.

The total harmonic distortion (THD) of the output voltage under healthy and faulty conditions for the proposed topology is not under the limits of IEEE-519 rules. However, the dominant harmonics appears at higher frequency (i.e., f_s) of the inverter; hence, by employing a small-size filter ($L = 3$ mH and $c = 4\ \mu$F [17]), the THD of the output voltage can be decreased to the acceptable limits of the IEEE-519 standards. Table V summarizes the proposed inverter's THD values of the output voltage and current. The table presents that the THD of both output voltage and current is below the limits of the IEEE-519 standards.

IV. Comprehensive Evaluation

A. Power Loss and Efficiency Analysis

The evaluation of the power losses, such as conduction and switching losses, is needed to obtain the efficiency and reliability of the inverter. The conduction losses are occurred due to the internal resistance and forward voltage drop across the semiconductor devices. On the other hand, the switching losses arise due to the transition of the switches between ON and OFF states. Among the above two types of losses, the conduction losses greatly influence the efficiency of the inverter, and these losses mainly depend on the number of conducting devices at a

TABLE VI
PARAMETERS FOR POWER LOSS AND EFFICIENCY ANALYSIS

Parameter/Component	Value
IGBT	IGW100N60H3_IGBT
Diode	IGW100N60H3_Diode
Input DC Sources	$V_{dc1} = V_{dc2} = 100$ V
Output frequency	$f_o = 50$ Hz
Switching frequency	$f_s = 5$ kHz
Load resistance	R = 25 Ω
Load inductance	L = 25 mH

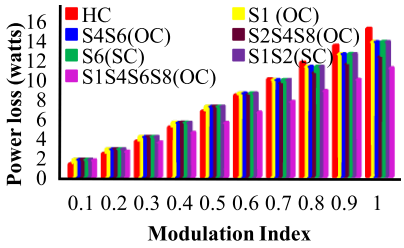


Fig. 14. Power losses of the proposed FTMLI under healthy and various fault conditions.

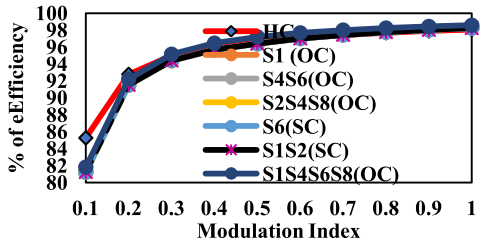


Fig. 15. Efficiency curves of the proposed FTMLI healthy and various fault conditions.

given time. In the proposed FTMLI, the maximum number of conducting switches before the fault and after the fault is three only, which is less than most recently proposed topologies. The power loss and efficiency of the proposed topology are obtained using PLECS simulation software. The power loss and efficiency analysis are carried out with the parameters given in Table VI. Figs. 14 and 15 show the power losses and efficiency of the proposed topology under HC and different fault conditions. It can be seen that the power loss and efficiency of the proposed topology under healthy and faulty conditions for different modulation indices remain the same.

This is because the same number of switches are conducted in both pre- and postfault states. This indicates that the proposed FTMLI is highly efficient for a wide range of modulation indices (m_a) under healthy and faulty conditions.

B. Switching Device Power (SDP) Rating

The SDP of a semiconductor device quantifies its voltage and current stress [35], and it is defined as the product of the peak inverse voltage (PIV) across the switch (V_p) and peak current flowing through the switch (I_p). The total SDP rating of the inverter is obtained by adding the SDP of all the switches

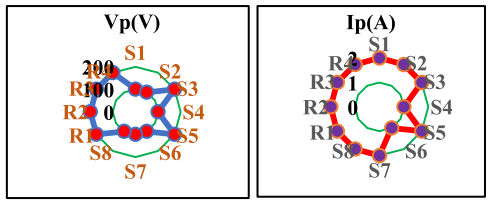


Fig. 16. (a) PIV across the switches. (b) Peak current flowing through the switches.

presented in the topology

$$\text{SDP}_{\text{switch}} = V_p \times I_p \tag{5}$$

$$\text{SDP}_{\text{Inverter}} = \sum_{k=1}^{N} V_{pk} \times I_{pk} \tag{6}$$

where N denotes the number of switching devices of the topology. With the above equations, the total SDP rating of the proposed FTMLI is calculated for the following parameters: $V_{\text{dc1}} = V_{\text{dc2}} = 100$ V, $m_a = 0.9$, $f_s = 5$ kHz, and $R = 100\ \Omega$. The PIV across each switch and peak current flowing through the switches is shown in Fig. 16. From the figure and (2), the total SDP rating of the proposed topology is obtained as 3400 VA, which is less in comparison with the newly developed inverters. The lower SDP rating indicates that the proposed topology is cost effective.

C. Overload Capability

The overload capability of the inverter is determined by the thermal constraints of the switching devices during the operation [32]. In the proposed FTMLI, the semiconductor switches S_3 and S_5 are dissipating more power loss during healthy conditions as these switches are conducting more time than the remaining switches. The dominant losses of the switching devices will reduce the overload capability of the inverter. This problem can be overcome in the proposed topology with the help of a redundant unit. In the proposed topology, the power losses of the switches S_3 and S_5 are reduced by providing the parallel path to the overload current with the help of redundant switches R_2, R_3, and R_4. Considering the instant at which the voltage level is $+2V_{\text{dc}}$, the load current sharing capability of the proposed topology using redundant unit is given in Fig. 17. In order to validate the overload capability, feature of the proposed FTMLI and simulations are performed with the parameters given in Table III. Fig. 18 shows the simulation results in which the redundant switches R_2 and R_4 are activated at $t = 0.06$ s. The current flowing through the switch S_5 is reduced to half after the activation of redundant switches. From the above analysis, it can be noted that the proposed topology can reduce the current stress of the main circuit switches under healthy conditions.

V. COMPARATIVE ANALYSIS

This section presents the comparisons of the different five-level FTMLI topologies in terms of components count and functionality, which are shown in Table VII. The topologies

TABLE VII
COMPARISONS WITH RECENT FTMLI TOPOLOGIES

S. No.	18	19	20	21	22	23	24	36	37	Proposed
1	2	1	1	1	1	2	2	1	1	**2**
2	0	1	1	1	1	0	0	3	2	**0**
3	6	6	8	8	8	8	10	6	8	**8**
4	10	12	12	14	14	14	12	12	14	**12**
5	6	0	2	2	2	4	0	0	6	**0**
6[a]	3	3	4	4	3	4	5	3	4	**3**
6[b]	5	4	3	5	4	3	5	4	4	**3**
7	19	20	18	22	23	22	18	16	22	**18**
8	3800	4000	3600	3600	4300	4400	3900	3000	4600	**3400**
9	25.6	19.1	20.5	30.3	20.1	24.2	32.5	20.5	29.7	**17.51**
10	97.5	98.1	97.9	97.1	98.1	97.6	96.8	98.1	97.1	**98.3**
11	√	√	√	√	√	√	√	√	√	√
12	√	X	√	X	X	√	X	√	√	√
13	X	√	√	√	√	√	√	X	√	√
14	X	X	√	X	X	√	X	X	√	√
15	X	√	√	X	√	√	√	√	√	√

1- No of DC sources; 2- No of capacitors; 3- No of power switches without FT ability; 4- No of power switches with FT ability; 5- No of diodes; 6[a]-Turn ON devices before fault; 6[b]- Turn ON devices after fault; 7- TBV(*V_{dc}); 8-SDP rating in terms of VA; 9-power loss in watts; 10- % Efficiency at 1KW; 11- Single switch OC FT ability; 12- Single switch SC FT ability; 13- Multi switch OC FT ability; 14- Multi switch SC FT ability; 15- Overload capability

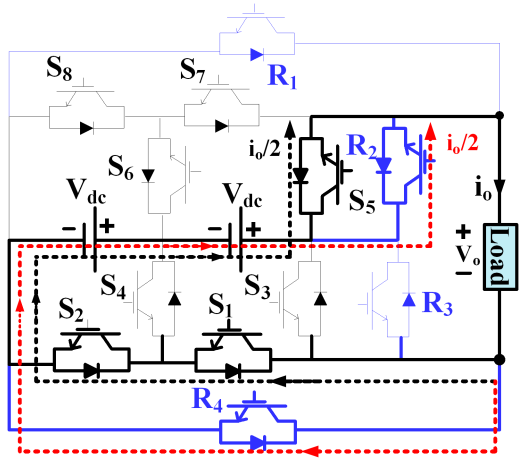


Fig. 17. Load current sharing of the proposed FTMLI during $+2V_{dc}$ level generation.

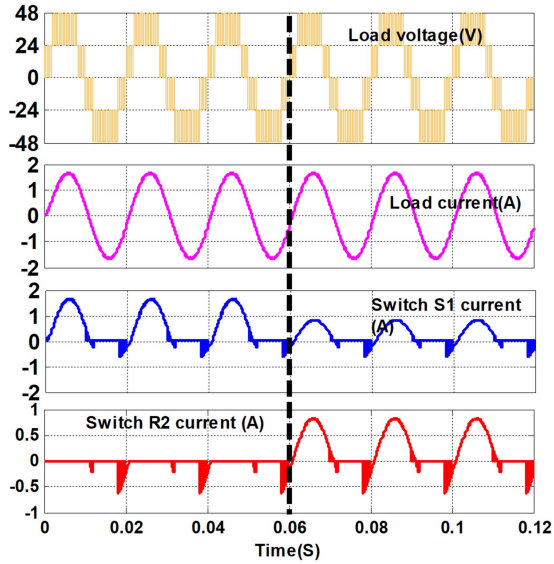


Fig. 18. Simulation results of the proposed FTMLI under overload condition.

[19], [20] and the proposed topology employ 12 switches only, which are less compared to all the topologies given in Table VII except the topology proposed in [18]. However, the topology [18] requires a more significant number of clamping diodes and a bulky transformer. The topology [20] also requires two clamping diodes, whereas the proposed topology does not employ any diodes. Another significant parameter that shows the competitiveness of the MLI topology in terms of device count for generating higher or lower voltage levels is the level-switch ratio (LSR), which can be obtained using the following relation:

$$\text{LSR} = \frac{N_L}{N_{\text{sw}}} \tag{7}$$

where N_L denotes the number of voltage levels, and N_{sw} indicates the switching devices of the topology. The LSR of FT topologies possessing slightly lower and higher output voltage levels is computed using the above relation and is presented in Table VIII. For a fair comparison, the converters with the ability to deliver the rated power during the postfault state are considered. The higher value of LSR indicates that the inverter topology requires fewer switching devices for generating the

TABLE VIII
LSR AND FT ABILITY FOR DIFFERENT TOPOLOGIES

Parameter	[32]	[38]	[PT*]	[17]	[39]	[40]
No of levels (N_L)	3	3	**5**	7	7	9
No of switches (N_{sw})	8	8	**12**	16	14	18
LSR(N_L/N_{sw})	0.37	0.37	**0.43**	0.43	0.5	0.5
Two switch FT ability	√	X	√	X	√	√
Three switch FT ability	X	X	√	X	X	X

*PT – Proposed topology

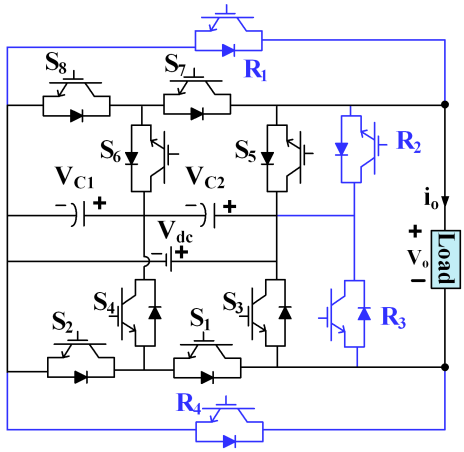


Fig. 19. Schematic diagram of the proposed inverter with single DC source.

TABLE IX
SWITCHING SCHEME OF THE PROPOSED INVERTER WITH SINGLE DC SOURCE

State number	Conducting switches	Voltage level	Status of the capacitors
P_{U1}	$S_1S_2S_5$	$+V_{dc}$	No effect
P_{L1}	**$S_1S_2S_6S_7$**	**$+0.5V_{dc}$**	**C_1- Charging, C_2- Discharging**
P_{L2}	**$S_1S_4S_5$**	**$+0.5V_{dc}$**	**C_1- Discharging, C_2- Charging**
Z_1	S_3S_5	0	No effect
Z_2	$S_1S_4S_6S_7$		
Z_3	$S_1S_2S_7S_8$		
N_{L1}	**$S_3S_6S_7$**	**$-0.5V_{dc}$**	**C_1- Discharging, C_2- Charging**
N_{L2}	**$S_1S_4S_7S_8$**	**$-0.5V_{dc}$**	**C_1- Charging, C_2- Discharging**
N_{U1}	$S_3S_7S_8$	$-V_{dc}$	No effect

required output voltage levels. From Table VIII, it can be noticed that the LSR value for the proposed FTMLI is high compared with the articles presented in [32] and [38] and low compared with the articles presented in [39] and [40]. However, the topologies [39], [40] cannot tolerate simultaneous faults on the three switches. Furthermore, the topologies [17], [38] does not have the two and three switch simultaneous FT capability. In contrast, the proposed topology can tolerate the simultaneous fault on any number of switches of the main unit. Hence, it can be concluded that the proposed FTMLI is competitive with device count and FT ability.

One important parameter that influences the efficiency of the inverter is the number of turn ON devices at a given instance. The higher number of conducting devices indicates more power loss and low efficiency. In the proposed FTMLI, the number of conducting devices before and after fault is only three, less than the topologies presented in Table VII. Hence, the power loss and efficiency are better in the proposed topology. The power loss and efficiency of the proposed inverter at 1 kW output power rating are obtained as 17.51 W and 98.3%. Table VII presents that the power losses are low for the proposed topology, and hence, efficiency is high compared with the remaining topologies. On the other hand, the topology [24] exhibits higher power loss as it employs more conducting devices; hence, the efficiency is low compared with all the topologies.

The other important parameters that significantly decide the cost of the inverter are TBV and SDP rating. The TBV is obtained by the summation of the PIV across all the switches of the inverter, and for the proposed topology, it is equal to $18V_{\rm dc}$. The procedure, as given in Section IV, is adopted for obtaining the SDP rating for each topology, as presented in Table VII. The table presents that TBV and SDP ratings for the proposed topology are low compared with the remaining topologies. Lower values of TBV and SDP ratings indicate that the implementation cost of the proposed FTMLI is low.

The functionalities, such as OC and SC FT capabilities, on both single and multiple switches are the indications of a reliable inverter. It can be noted that all the compared topologies, as given in Table VII, are capable of tolerating the single-switch OC fault. However, the topologies [19], [21], [22], [24] cannot tolerate the multiple device faults and SC faults. The works reported in [18] and [36] addresses single-switch SC faults but unable to tolerate faults on multiple devices. However, the proposed topology and the topologies [20], [23], [37] can tolerate all types of single- and multiswitch faults. However, the topologies [23], [37] have higher TBV and SDP ratings than the proposed topology. Furthermore, the proposed topology has the overload capability to reduce the current stress on the main circuit switches, which is not possible in topologies [18], [21].

The comparative analysis shows that the proposed MLI requires two sources but is highly competitive over other topologies in terms of efficiency, device count, and functionalities, such as single- and multiswitch OC and SC fault tolerance. With the above features, the proposed topology is a suitable candidate for UPS systems and multistring inverters used in interfacing different renewable energy sources to the microgrid.

VI. REALIZATION OF THE PROPOSED INVERTER USING A SINGLE DC SOURCE

The schematic diagram of the proposed inverter with a single dc source and two dc-link capacitors (C_1 and C_2) is shown in Fig. 19. The two dc-link capacitors are connected across the dc source such that their voltages are balanced to half of the dc source voltage ($V_{\rm dc}$). The switching scheme of the proposed inverter with a single dc source for generating the five-level output voltage is shown in Table IX. By properly utilizing the switching states, the self-balancing of the capacitors can be obtained. The switching state P_{L1} charges the capacitor C_1 and discharges the capacitor C_2. On the other hand, the switching state P_{L2}, in contrast to the P_{L1}, discharges C_1 and charges C_2. Likewise, the voltage level $-0.5V_{\rm dc}$ can be generated using either N_{L1} or N_{L2} switching states. The switching state N_{L1} discharges C_1 and charges C_2. However, the switching state N_{L2} has the opposite effect on the capacitor voltages, as seen in Table IX. The voltage across the capacitor is said to be balanced when the average value of the capacitor current over one cycle is zero. This can be achieved in the proposed inverter by PWM-based capacitor voltage balance technique; wherein, both states P_{L1} and P_{L2} and N_{L1} and N_{L2} are appropriately

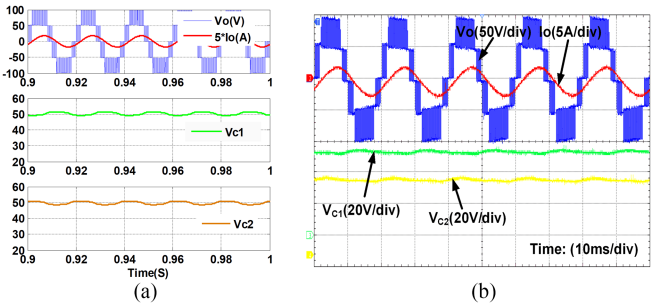


Fig. 20. (a) Simulation and (b) experimental results of the proposed inverter with single DC source.

used in the voltage levels $0.5V_{\rm dc}$ and $-0.5V_{\rm dc}$, respectively, to balance the capacitor voltages. The capacitor voltage balancing in the proposed inverter is verified by performing the simulation and experimental studies. The parameters considered in the both simulation and experimental study are $V_{\rm dc} = 100$ V, $C_1 = C_2 = 2200$ μF, $f_s = 5$ kHz, $m_a = 0.9$, $R = 20$ Ω, and $L = 50$ mH.

The simulation and experimental results of the load voltage and current, and voltage across the capacitors (V_{C1} and V_{C2}) are shown in Fig. 20. From the figure, it can be observed that the proposed inverter generates the five-level output voltage waveform by maintaining the balanced voltage across the capacitors. However, addressing the capacitor voltage issue with the occurrence of switch faults is challenging and requires new control scheme, which is considered for future scope, and hence, the fault case studies of the proposed inverter with single dc source are not reported in this article.

VII. Conclusion

An improved single-phase FTMLI structure with minimum number of components is presented in this article. The proposed five-level inverter obtained from the combination of the main circuit and redundant unit handles both OC and SC faults on single and multiple switches. The working of the proposed topology under various fault conditions is verified by conducting simulation and experimental studies. The redundant unit not only helps in achieving fault tolerance but also ensures the increased overload capability of the proposed topology. The efficiency of the proposed topology does not deteriorate under any fault conditions. Moreover, it delivers the equal rated output power to the load under pre and postfault states. The comparative analysis reveals that the proposed topology is superior in terms of device count, power loss, efficiency, TBV, and SDP ratings over other prominent FT topologies.

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