SR Control With Zero Current Detection Delay Compensation for GaN CRM Totem-Pole PFC Rectifier

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***Abstract*—An synchronous rectifier (SR) control with zero current detection (ZCD) delay compensation is proposed to reduce the high reverse inductor current and input current distortion caused by the ZCD delay in critical mode totem-pole power factor correction (PFC). The basic idea of the proposed control is to calculate the SR turn-OFF instant considering the ZCD delay. Accurate operation model in VOT control is analyzed with ZCD delay compensation to realize the proposed control. A prototype of 2 kW GaN CRM totem-pole PFC converter is built to verify the proposed control. The total harmonic distortion (THD) with full load decreases to 3% by mitigating the current distortion caused by the ZCD delay, 1.6% lower than that before compensation. The high reverse inductor current near the zero-crossing of input voltage is avoided since the length of the zero-current platform is shortened by 87.5%. The prototype achieves 99% efficiency at full load (2 kW) and a power density of 120 W/inch^3.**

***Index Terms*—Critical conduction mode (CRM), synchronous rectifier (SR), total harmonic distortion (THD), totem-pole power factor correction (PFC), zero current detection (ZCD) delay.**

I. Introduction

HIGH-EFFICIENCY power factor correction (PFC) is required in telecommunication, servers, and electric vehicle [1], [2], [3]. Compared with other PFC topologies, the totem-pole PFC converters have a compact structure since fewer power devices. The emerging 650-V gallium-nitride (GaN) devices feature lower conduction resistance $R_{\mathrm{ds(on)}}$, lower junction capacitance C_{oss}, and especially zero reverse recovery charge Q_{rr}. Those advantages make totem-pole PFC topology efficient and practical with much-reduced conduction loss, switching loss, and reverse recovery loss [4], [5]. The totem-pole PFC with critical conduction mode (CRM) operation has attracted more attention because of the capability of zero voltage switching (ZVS) [6], [7].

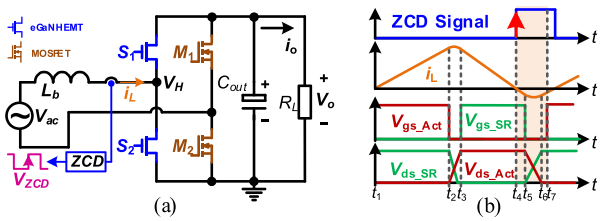

Fig. 1. Totem-pole PFC topology in CRM. (a) Topology of Totem-pole PFC. (b) Waveform of ZVS realization.

Fig. 1 shows the totem-pole PFC topology in CRM. Referring to Fig. 1(a), S_1 and S_2 are GaN HEMTs operating at high frequency, and M_1 and M_2 are MOSFETs operating at line frequency. L_b is the boost inductor. The inductor current i_L in L_b is detected by the zero current detection (ZCD) circuit to confirm the zero-crossing time. Before the active switch (S_1 or S_2, depending on the polarity of input voltage v_{ac}) turns ON, the inductor L_b resonates with the device junction capacitances of S_1 and S_2, and the drain-source voltage of the active switch decreases to zero, then the active switch can achieve ZVS. However, the ZVS of the active switch is inherent only when $v_{ac} \leq 0.5\ V_o$. When $v_{ac} > 0.5\ V_o$, ZVS cannot be passively achieved due to insufficient energy stored in the inductor L_b, resulting to partial hard switching loss [8], [9]. From Fig. 1(b), during t_4–t_5, to achieve full-line-cycle ZVS, when $v_{ac} > 0.5\ V_o$, the SR needs to conduct extended. Thus, the negative inductor current has enough energy to decrease the drain-source voltage of the active switch to zero before it turns ON and realizes ZVS [10].

A control strategy based on a digital controller has the characteristic of operation adaptability and computational flexibility and is preferred in the control of CRM totem-pole PFC [11]. Typically, the input current of the totem-pole PFC can be regulated by hysteresis current control [12], time-based current control [13], or hybrid current control [14]. Time-based current control is more straightforward, and variable on-time (VOT) control is widely used [15], [16]. For the time-based current control, a ZCD circuit is needed to generate a ZCD signal which is used

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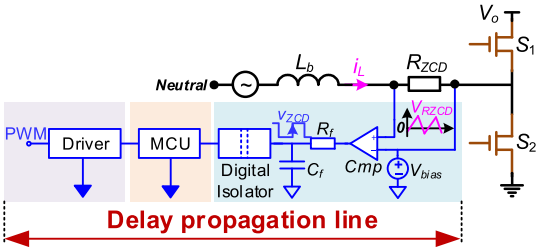


Fig. 2. ZCD circuit based on sensing resistor.

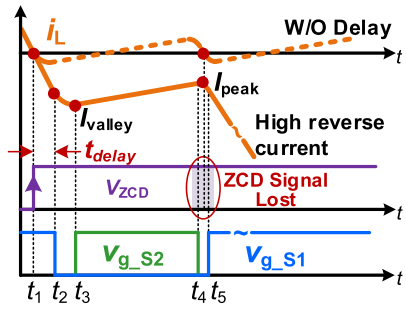


Fig. 3. Mechanism of the high reverse inductor current near the zero-crossing of input voltage.

to synchronize the controller timer, and the digital controller determines the drive signals based on ZCD signal [17], [18].

In the conventional VOT control, the turn-ON instant and turn-OFF instant of the power switches is triggered based on the ZCD signal [19]. However, due to the parasitic parameters, the sampling time, and the digital controller processing time, there exists a signal propagation delay in ZCD circuit (hereinafter referred to as $t_{\rm delay}$). Various causes of ZCD signal time error are discussed, with signal propagation delay identified as the dominant mechanism [18], [19]. The delay of the ZCD signal makes the input line currents deviate from normal operation in steady state, and suffer from two distinct distortion mechanisms: the ac line zero-crossing reverse high current near the zero-crossing and the low-frequency line-cycle current distortion. Some ZCD delay compensation methods have been proposed for CRM boost PFC [17], but it is not suitable for the CRM totem-pole PFC converter. It should be noted that the negative effect of the high reverse inductor current caused by the ZCD delay has not been discussed on the current distortion effect.

The contribution of this article is to propose an SR control with ZCD delay compensation to reduce the distortion in the inductor current, avoid destructively high reverse inductor current caused by the ZCD delay in CRM totem-pole PFC and improve THD and efficiency.

II. Problem of Input Current in CRM Totem-Pole PFC Rectifier Due to ZCD Signal Delay

The ZCD signal propagation delay $t_{\rm delay}$ is decided by the ZCD circuit, driver circuit, and MCU. Fig. 2 shows a typical ZCD circuit based on the sensing resistor, including the sensing resistor $R_{\rm ZCD}$, *RC* filter, the comparator *Cmp*, the digital isolator, MCU, and the drive circuit.

In the practical application, the measured $t_{\rm delay}$ is around 120 ns. It is equivalent to say that the turn-ON instant of S_1/S_2 has 120-ns delay referenced to the inductor current positive-to-negative ZCD signal.

A. Problem 1: High Reverse Current in Inductor

Near the zero-crossing of the input voltage, the ZCD delay $t_{\rm delay}$ could cause a high reverse inductor current due to the extreme inductor current slew rate. Taking the input voltage positive half cycle as example. The slew rate k_i of inductor current during a switching cycle is

$$k_i = \begin{cases} \frac{v_{ac}}{L_b} & \text{if} \quad S_2\text{on} \\ \frac{v_{ac}-V_o}{L_b} & \text{if} \quad S_1\text{on} \end{cases} \tag{1}$$

k_i varies with the input voltage $v_{\rm ac}$. Near the zero-crossing point of $v_{\rm ac}$, $k_i \approx 0$ when S_2 (the active switch) turns ON. When S_1 (the SR) on, the k_i reaches the maximum slew rate.

Fig. 3 shows the mechanism of high reverse inductor current near the zero-crossing point of $v_{\rm ac}$. With $t_{\rm delay}$, S_1 (SR) extends a conduction time $t_{\rm delay}$ during $t_1 \sim t_2$. i_L keeps decreasing with maximum slew rate and reaches larger $|I_{\rm valley}|$. In this case, during $t_3 \sim t_4$, when S_2 turns ON, i_L could not rise above zero due to the extremely small raise rate. Then, i_L misses the chance downward through the zero after t_5, the ZCD signal lost, and S_1 loses the trigger signal to turn OFF, making i_L keep increasing reversely with maximum slew rate and causing high reverse current. Assume that the dc-bus voltage $V_{\rm o}$ is 400 V. When the single control period of digital controller $T_{\rm dsp}$ is 5 μs and the inductance L_b is 70 μH, the $\Delta i_{L\cdot\rm down}$ that i_L decreases in one cycle will be

$$\Delta i_{L\_\rm down} = V_o \cdot \frac{T_{\rm dsp}}{L_b} = 28 \text{ A}. \tag{2}$$

Even worse, once the ZCD signal lost, i_L increases reversely in the following switching cycles. Therefore, the uncontrolled high reverse inductor current i_L could damage power devices in several switching cycles.

A. Problem 2: Distortion of Inductor Current

The ZCD delay $t_{\rm delay}$ causes the inductor current i_L to deviate from the normal trajectory and results to larger current ripple and RMS value. Fig. 4 shows the distortion of inductor current in VOT control caused by the ZCD delay. Compared with the ideal case, $I_{\rm valley}$ decreases due to the over-conduction of SR caused by the ZCD delay. In VOT control, to keep the output power unchanged, the outer loop PI controller will extend the active switch conduction time $T_{\rm AC\_ON}$ to increase the inductor peak current. In a steady state, the extended conduction part of the active switch conduction time $T_{\rm AC\_ON}$ is a constant value [17]. When $v_{\rm ac} > 0.5\ V_{\rm o}$ [see Fig. 4(a)], with the extended conduction part in the $T_{\rm AC\_ON}$, $I_{\rm peak}$ is higher in the case of $t_{\rm delay}$. However, when $v_{\rm ac} \leq 0.5\ V_{\rm o}$ [see Fig. 4(b)], although $T_{\rm AC\_ON}$ is increased

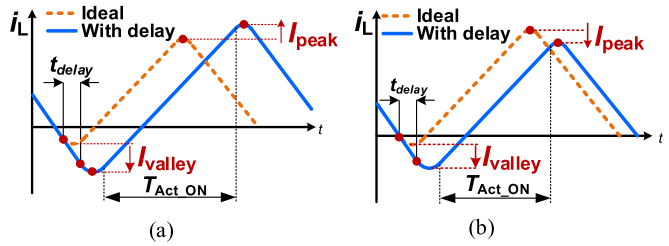


Fig. 4. Distortion of Inductor current caused by ZCD delay. (a) $v_{ac} > 0.5\ V_o$. (b) $v_{ac} \leq 0.5\ V_o$

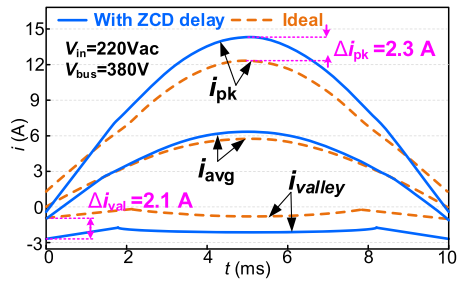


Fig. 5. Comparison of inductor currents between the ideal case and the case with ZCD delay.

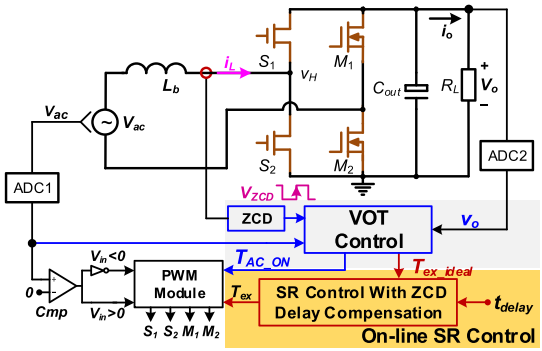


Fig. 6. Diagram of proposed SR control.

by the PI controller, the extended conduction part is not adequate to maintain the same peak current. Hence, with $t_{\rm delay}$, $I_{\rm peak}$ is higher when $v_{\rm ac} > 0.5\ V_{\rm o}$ and slightly lower when $v_{\rm ac} \leq 0.5$.

Fig. 5 illustrates the impacts of the ZCD time delay on the input current in an example CRM PFC converter operating at 2 kW with 120 ns ZCD delay. The inductor current is distorted with larger current ripple. The current ripple increases, resulting to additional turn-OFF loss and conduction losses, and a worse THD.

III. Proposed SR Control With Compensation of Zero Current Detection Delay

This section takes a single-phase CRM totem-pole PFC rectifier as an example to illustrate the proposed SR control. Fig. 6 shows the diagram of the proposed control. Based on the ZCD signal, the active switch's conduction time $T_{\rm AC\_ON}$ and the ideal SR extended conduction time $T_{\rm ex\_ideal}$ is obtained by the DSP real-time calculation in VOT control. Then, the ideal SR conduction time $T_{\rm ex\_ideal}$ is compensated depending on the actual ZCD delay by the proposed SR control, and the corrected SR conduction time T_{ex} is sent to the PWM module to drive the SRs.

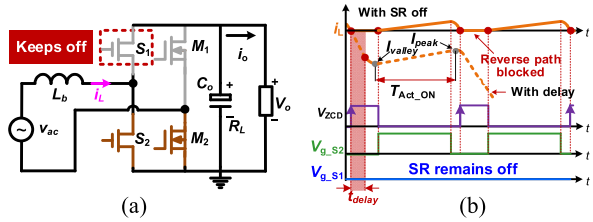


Fig. 7. Avoid high reverse inductor current near the zero-crossing of the input voltage. (a) Block OFF the reverse current path. (b) Key waveforms.

A. Basic Idea

The basic idea of the proposed control is calculating the accurate SR turn-OFF instant by compensating the error from ZCD delay, to reduce the distortion of input current and avoid the high reverse inductor current. Near the zero-crossing of the input voltage, the SR is OFF to avoid the uncontrolled high reverse inductor current; during the full-line-cycle, the SR turn-OFF instant is recalculated by compensating the error from ZCD delay to minimize the distortion of input current.

B. Avoid High Reverse Current in Inductor

To avoid the high reverse inductor current caused by the ZCD delay near the zero-crossing of input voltage, SR is controlled to be OFF to block OFF the reverse inductor current before ZCD signal lost and a too-large reverse inductor current generating. A positive line frequency cycle is taken as example.

Fig. 7 shows the proposed SR control near the zero-crossing of the input voltage. Referring to Fig. 7(a), near the zero-crossing of the input voltage, before the delay of the ZCD signal causes the inductor current fails to raise above zero in the next period, the SR S_1 keeps OFF while the active switch operates normally. From Fig. 7(b), after the SR keeps OFF, the reverse path of the inductor current $i_{\rm L}$ is blocked OFF, then the maximum slew rate of the inductor current ($V_{\rm o}/L_b$) will not be a problem. There will be no uncontrolled reverse high inductor current flowing through the SR S_1, as the dash line in Fig. 7(b). In this way, the high reverse inductor current is avoided and switch current stress is decreased. Meanwhile, the active switch S_2 remains on status, so the inductor current still can flow positively. There will be no long zero-current platform that impairs the THD of the input current.

The delay time of the ZCD that decreases $I_{\rm peak}$ to zero is defined as the tolerance time $t_{\rm tor}$. If the measured ZCD delay time $t_{\rm delay}$ is longer than $t_{\rm tor}$, $I_{\rm peak}$ in Fig. 3 can be lower than zero, then the ZCD signal loses; otherwise, the ZCD signal exists. Therefore, the tolerance time $t_{\rm tor}$ is the condition to predict whether the ZCD signal loses or not. The tolerance time

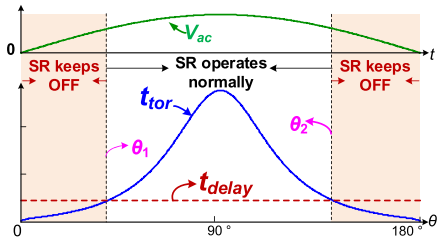


Fig. 8. SR operation status based on tolerance time $t_{\rm tor}$.

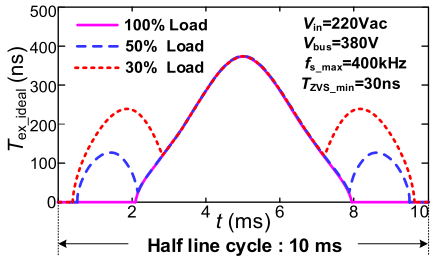


Fig. 9. Extended SR conduction time under different loads.

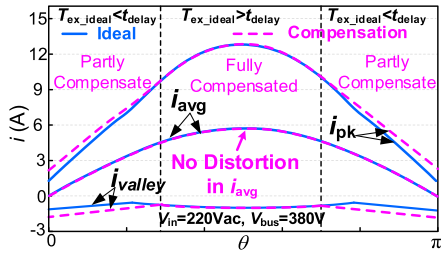


Fig. 10. Full load inductor current waveform after ZCD delay compensation.

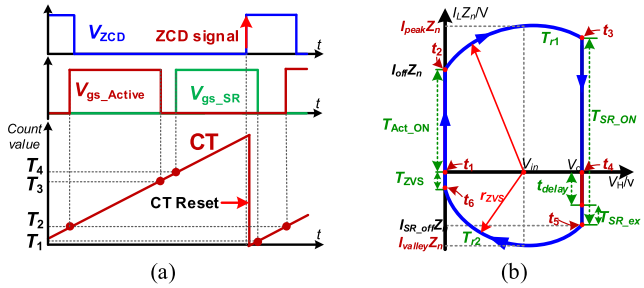


Fig. 11. Key parameters determine drive signals. (a) Key waveform. (b) State trajectory in VOT control.

$t_{\rm tor}$ is

$$t_{\rm tor} = \frac{v_{\rm in} \cdot T_{\rm Act\_ON}}{V_o - v_{\rm in}}. \tag{3}$$

Based on the tolerance time $t_{\rm tor}$ and the ZCD delay time $t_{\rm delay}$, the DSP determines whether the SR needs to be turned OFF. Fig. 8 shows the variation of $t_{\rm tor}$ in the positive half cycle of input voltage. When $t_{\rm tor} > t_{\rm delay}$, even with ZCD delay, $I_{\rm peak}$ is higher than zero, and the ZCD signal exists. Therefore, when the input voltage phase θ is between θ_1 and θ_2, the SR operates normally. Outside this interval, the SR keeps OFF to block OFF the reverse inductor current.

C. Mitigation of Inductor Current Distortion

To reduce the distortion of input current caused by ZCD delay, the ideal extended conduction time $T_{\rm ex\_ideal}$ (see Fig. 6) of the SR is compensated. Since the ZCD delay increases the extended conduction time of the SR, the ZCD delay time $t_{\rm delay}$ can be subtracted from the ideal extended conduction time $T_{\rm ex\_ideal}$ of the SR, so that the overall extended conduction time $T_{\rm SR\_ex}$ remains unchanged

$$T_{\rm SR\_ex} = T_{\rm ex\_ideal} - t_{\rm delay}. \tag{4}$$

Fig. 9 shows the ideal *SR* extending conduction time $T_{\rm ex\_ideal}$ under full load, 50% load, and 30% load, respectively. When $T_{\rm ex\_ideal}$ is smaller than $t_{\rm delay}$, it cannot be directly compensated by (4). In this case, lets $T_{\rm SR\_ex}$ be 0, and the actual extended conduction time of the SR is $t_{\rm delay}$.

Fig. 10 shows the waveform of full-load inductor current after ZCD delay compensation. Based on the ZCD delay compensation, the average value of inductor current $i_{\rm avg}$ remains unchanged in the ideal trajectory and the input current is not distorted. In the region where $T_{\rm ex\_ideal}$ is larger than $t_{\rm delay}$, the ZCD delay $t_{\rm delay}$ is fully compensated and the inductor current ripple does not increase. In the region where $T_{\rm ex\_ideal}$ is smaller than $t_{\rm delay}$, the current ripple slightly increases, but the average inductor current $i_{\rm avg}$ remains the same.

D. Benefits of the Proposed SR Control

The benefits of the proposed control are as follows.

1) The high reverse inductor current is eliminated, and long zero-current platform is avoided because when the SR OFF, the active switch remains on status.
2) The distortion of the input current is relieved, because the accurate SRs' turn-OFF instant is calculated to reduce the reverse conduction time of the inductor current.
3) The loss reduction is achieved. The turn-OFF loss of the active switch and the conduction loss of switches and inductor are reduced in the steady state. Because the peak value of the inductor current is decreased.

IV. Realization of the Proposed SR Control Based on Digital Controller

A. Key Parameters Calculation

Fig. 11 shows the way that the drive signals determined in the digital controller. A positive line frequency cycle is taken as example. In Fig. 11(a), CT is the inner counter of the digital controller which is reset by ZCD signal. T_1, T_2, T_3, and T_4 are comparison value used to compared with the count value in CT to determine the turn-OFF instant of SR, turn-ON instant of the active switch, turn-OFF instant of the active switch, and turn-ON instant of SR. When inductor current i_L decreases to zero, the ZCD signal is triggered and produces a rising edge. After a ZCD delay, CT is reset and begins to count over again, and enters the next switching cycle. Fig. 11(b) is the state trajectory

TABLE I
CALCULATION OF THE KEY PARAMETERS

Description	Comparison value calculated in digital controller
Active switch turns on	$T_2 = T_{SR\_ex} + T_{r2}$
SR turns on	$T_4 = T_{Act\_ON} + T_{r1}$
Active switch turns off	$T_3 = T_{SR\_ex} + T_{r2} + T_{ZVS} + T_{Act\_ON}$
SR turns off	$T_1 = T_{SR\_ex}$

considering the resonance between the inductor and the eGaN HEMTs' junction capacitances. The variables used to calculate T_1, T_2, T_3 and T_4 are shown in Fig. 11(b). The relation between those variables and T_1, T_2, T_3, T_4 is given in Table I.

The required process variables in Table I are calculated below.

1) Extended Conduction Time of SR T_{SR_ex}*:* According to Fig. 11(b), $I_{\mathrm{SR\_off}}$, I_{on} and I_{valley} satisfy

$$I_{SR\_off} = -\sqrt{I_{valley}^2 - \left(\frac{V_o - v_{in}}{Z_n}\right)^2} \tag{5}$$

$$I_{on} = -\sqrt{I_{valley}^2 - \left(\frac{v_{in}}{Z_n}\right)^2}. \tag{6}$$

Combing these two equations, the inductor current I_{on} can be expressed by $I_{\mathrm{SR\_off}}$

$$I_{on} = -\sqrt{\frac{V_o(V_o - 2v_{in})}{Z_n^2} + I_{SR\_off}^2}. \tag{7}$$

Similarly, $I_{\mathrm{SR\_on}}$, I_{off}, and I_{peak} satisfy

$$I_{SR\_on} = \sqrt{-\left(\frac{V_o - v_{in}}{Z_n}\right)^2 + I_{peak}^2} \tag{8}$$

$$I_{off} = \sqrt{I_{peak}^2 - \left(\frac{V_{in}}{Z_n}\right)^2}. \tag{9}$$

I_{valley} is solved as

$$I_{valley} = -\frac{r_{ZVS}}{Z_n}. \tag{10}$$

According to (5) and (10), $I_{\mathrm{SR\_off}}$ can be derived as

$$I_{SR\_off} = \frac{-\sqrt{r_{ZVS}^2 - (V_o - v_{in})^2}}{Z_n}. \tag{11}$$

The resonance radius r_{ZVS} increases to

$$r_{ZVS} = (V_o - v_{in})\sqrt{1 + \frac{T_{SR\_ex}^2}{2L_bC_{oss}}}. \tag{12}$$

The ideal extended conduction time $T_{\mathrm{ex\_ideal}}$ regardless the ZCD delay can be obtained by submitting (11) into (12)

$$\mathrm{T}_{ex\_ideal} = \frac{\sqrt{r_{ZVS}^2 - (V_o - v_{in})^2} \cdot \sqrt{2L_bC_{oss}}}{V_o - v_{in}}. \tag{13}$$

The extended conduction time $T_{\mathrm{SR\_ex}}$ considered the ZCD delay can be obtained

$$\mathrm{T}_{SR\_ex} = \begin{cases} \mathrm{T}_{ex\_ideal} - t_{delay} & \text{if } \mathrm{T}_{ex\_org} > t_{delay} \\ 0 & \text{if } \mathrm{T}_{ex\_org} \le t_{delay} \end{cases}. \tag{14}$$

2) Active Switch Conduction Time T_{Act_ON}*:* The t_1 is the moment when the inductor current increases to zero. At t_1, Active switch S_2 is on, i_L increases from zero

$$i_L(t) = \frac{v_{in}}{L_b}(t - t_1) + i_L(t_1). \tag{15}$$

According to (15) and (8), the peak current I_{peak} is

$$I_{peak} = \sqrt{\left(\frac{v_{in}}{L_b}\mathrm{T}_{\mathrm{Act\_ON}}\right)^2 + \left(\frac{v_{in}}{Z_n}\right)^2}. \tag{16}$$

Ignoring the resonance of interval 2 and interval 5, submitting and (16) into (15), the active switch conduction time $T_{\mathrm{Act\_ON}}$ is obtained

$$\begin{cases} T_{on\_cnst} = \frac{2L_bP_o}{V_{in\_rms}^2} \cdot T_{on\_var} = \frac{r_{ZVS}L_b}{Z_n v_{in}} \\ \mathrm{T}_{\mathrm{Act\_ON}} = T_{on\_cnst} + T_{on\_var} = \frac{2L_bP_o}{\eta V_{in\_rms}^2} + \frac{r_{ZVS}L_b}{Z_n v_{in}} \end{cases}. \tag{17}$$

$T_{\mathrm{Act\_ON}}$ includes the constant conduction time $T_{\mathrm{on\_cnst}}$ and variable conduction time $T_{\mathrm{on\_var}}$, where $T_{\mathrm{on\_cnst}}$ can be obtained by the voltage loop while $T_{\mathrm{on\_var}}$ needs to be calculated in real-time.

3) SR Conduction Time T_{SR_ON}*:* According to the voltage-second principle, combined with (13) and (17), the SR conduction time $T_{\mathrm{SR\_ON}}$ can be obtained

$$\mathrm{T}_{SR\_ON} = \mathrm{T}_{Act\_ON}\frac{v_{in}}{V_o - v_{in}} + \mathrm{T}_{SR\_ex}. \tag{18}$$

4) ZVS Margin T_{ZVS} *of the Active Switch:* Before S_2 turns ON, inductor current i_L flows through S_2 via the reverse conduction mechanism of GaN. To decrease reverse conduction loss, S_2 should turn ON at t_6. Then, inductor current i_{L1} increases

$$i_L(t) = \frac{v_{in}}{L_b}(t - t_6) + i_L(t_6). \tag{19}$$

According to (19) and (10), the T_{ZVS} can be derived

$$\mathrm{T}_{ZVS} = \frac{L_b}{v_{in}} \cdot \frac{\sqrt{r_{ZVS}^2 - v_{in}^2}}{Z_n}. \tag{20}$$

5) Resonance Time T_{r1} *and* T_{r2}*:* The resonance time T_{r1} and T_{r2} can be derived as

$$T_{r1} = \frac{\pi}{\omega_r} - \frac{\cos^{-1}}{\omega_r}\left(\left(1 + \frac{V_o - v_{in}}{v_{in}}\right) \cdot \left(\left(\frac{Z_nT_{Act\_ON}}{L_b}\right)^2 + 1\right)^{-0.5}\right) \tag{21}$$

$$\mathrm{T}_{r2} = \frac{\pi - \cos^{-1}\left(\frac{V_o - v_{in}}{r_{ZVS}}\right) - \cos^{-1}\left(\frac{1}{k_{ZVS}}\right)}{\omega_r} \tag{22}$$

where resonance coefficient k_{ZVS} is defined as the ratio of r_{ZVS} to V_{in}. When the SR switch is not extended to conduct, the k_{ZVS} reaches the minimum value $k_{\mathrm{min}} = (V_o\text{-}v_{\mathrm{in}}) / v_{\mathrm{in}}$.

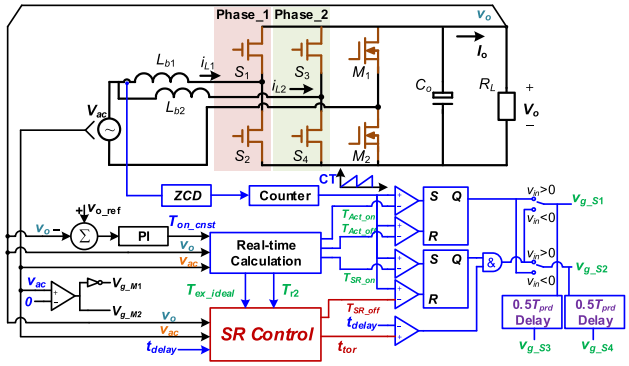


Fig. 12. Diagram of proposed SR control in two-phase interleaving CRM totem-pole PFC rectifier.

B. Realize the Proposed Control in Digital-Based Two-Phase Interleaving CRM Totem-Pole PFC Rectifier

In this article, a two-phase interleaved totem-pole PFC is adopted. Fig. 12 gives the detailed digital control for the two-phase interleaved CRM totem-pole PFC converter with the proposed control. The open-loop interleaving method is adopted. MCU ECAP module detects switching period $T_{\rm prd}$ of the high-frequency switches in phase-1, then with half switching period delay (0.5 $T_{\rm prd}$), the driving signal of S_1 and S_2 are transmitted to S_3 and S_4, respectively.

All the control functions of the proposed control are realized in a 100 MHz MCU TMS320F280049C from Texas Instruments. The main interrupt service routine is triggered by a 15 μs CPU timer.

V. Parameter Design of Two-Phase Interleaved Totem-Pole PFC Converter

A. Inductor Design and Optimization

There is a tradeoff between the loss and core volume when optimizing the inductor. Different boost inductances from 20 to 80 μH are considered. With different inductance, the inductor is designed with different size magnetic cores (PQ20 – PQ40). The DMR95 Mn-Zn ferrite cores from DMECG are selected, and 0.1 $\times$ 300 litz wire is used. The generalized Steinmetz equation is used to calculate the core loss, and squared-field-derivative (SFD) method is used to estimate the winding loss. Based on the analytical loss models, the converter efficiency considering different boost inductances is projected.

Using the above evaluation method, Fig. 13 shows the estimated converter efficiency and core volume at different inductances. With the inductance range from 60 to 80 μH, core PQ35 and 70 μH is the optimized choice to balance efficiency and volume.

B. Bus Capacitor Design

According to the requirement of output voltage ripple $V_{\rm ripple}$ is 40 V, the bus capacitor should be

$$C_{\rm o} \geq \frac{P_o}{\eta_0 \cdot \omega_{\rm line} \cdot V_o \cdot V_{\rm ripple}} = 442\ \mu{\rm F}. \tag{23}$$

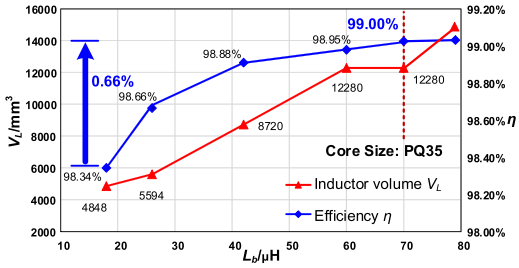


Fig. 13. Efficiency and inductor volume with different inductor, $V_{\rm in}$ = 240 Vac, V_o = 380 V, and P_o = 2 kW.

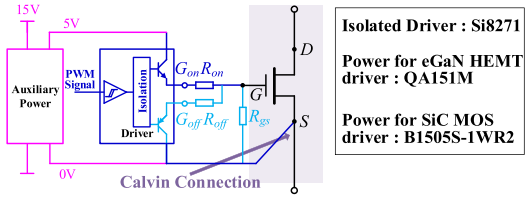


Fig. 14. Drive circuit.

TABLE II
Key Parameters of Prototype

Parameter	Symbol	Value
AC line voltage	V_{in}	220 Vac~265 Vac
DC-link voltage	V_o	380 V~480 V
Rated power	P_o	2 kW
Buck-boost inductance	L_{b1}/ L_{b2}	70 μH
DC-link capacitance	C_{bus}	540 μF
Switches frequency	$f_{\rm sw}$	200 kHz -400 kHz

So, two 600-V 270-μF LGN2X101MELC30 electrolytic capacitors are paralleled to be the bus capacitor.

C. Drive Circuit

The drive circuit is provided in Fig. 14. The driving method of the high frequency switch and the line frequency switch are the same expect the auxiliary power supply.

In summary, Table II gives the key parameters of the two-phase interleaved CRM totem-pole PFC converter.

VI. Experimental Results and Discussion

A. Experimental Prototype

A prototype is built and illustrated in Fig. 15. The rated power is 2 kW and the power density is 120 W/in^3. Table II already shows the key parameters, and Table III gives the power device parameters.

B. Phase Interleaving and Full-Line ZVS

For the proposed converter, the two inductors of the interleaving CRM PFC are very close as 71.2 and 69.5 μH respectively, with an error of 17% and 0.7% compared to the design theoretical value of 70 μH.

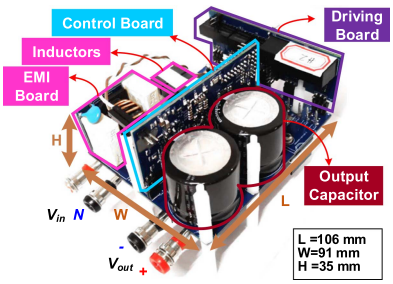
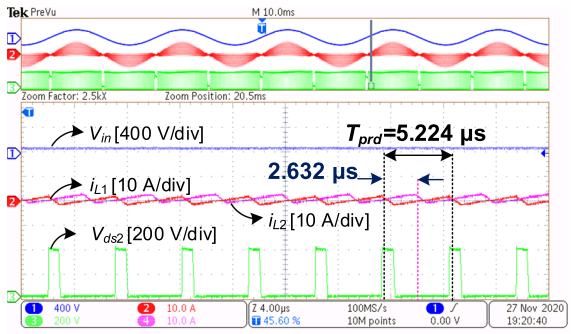


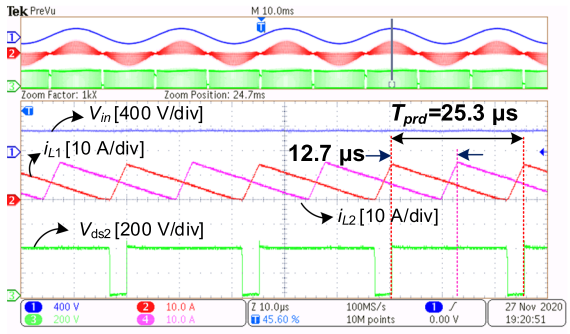
Fig. 15. Photograph of prototype.

TABLE III
POWER DEVICES PARAMETERS

	eGaN HEMT (GaN Systems) S_1 - S_4	SiC MOSFET (Infineon) M_1, M_2
Part No.	GS66508T	IMW65R027M1H
V_{DS}	650 V	650 V
I_D	30 A	47 A
$R_{DS(on)}$	75 mΩ	30 mΩ
C_{oss}	80 pF	278 pF



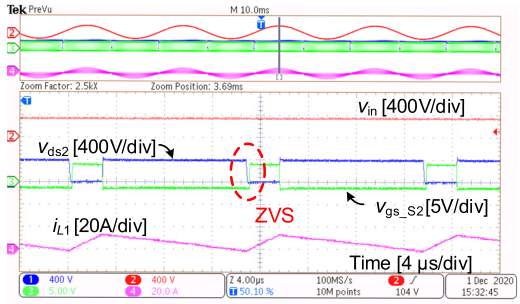
(a)



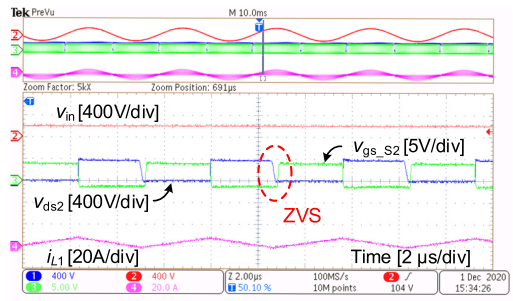
(b)

Fig. 16. Waveforms of the interleaving method, $V_{\rm in} = 220$ Vac, $V_o = 380$ V, $P_o = 2000$ W. (a) Phase of the input voltage is 15°. (b) Phase of the input voltage is 90°.

Fig. 16 is the waveforms of the interleaving method when the output voltage phase is 15° and 90°. From Fig. 16, the phase difference between the two inductor currents is 180°. There are no issues with open-loop phase interleaving method in the proposed converter.



(a)



(b)

Fig. 17. Experimental waveforms of full-line-cycle ZVS, $V_{\rm in} = 220$ Vac, $V_{\rm o} = 380$ V, $P_{\rm o} = 2$ kW. (a) $V_{\rm in} < 0.5\ V_{\rm o}$. (b) $V_{\rm in} \geq 0.5\ V_{\rm o}$.

Fig. 17 shows waveforms ZVS of full-line cycle with the proposed control. The minimum ZVS turn-ON time margin is set as 30 ns. From Fig. 17(a) and (b), the ZVS in full-line cycle can be realized.

C. Zero Current Platform Near the Zero-Crossing Point

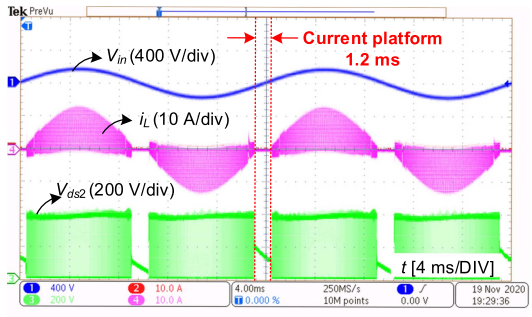
Fig. 18 compares the zero-current platform between the conventional VOT control and the proposed SR control. In conventional VOT control, the zero current platform is long as 1.2 ms. With the proposed control, when the SR OFF to prevent the PFC from a high reverse inductor current, the active switch remains on status, and the zero current platforms is long as 0.15 ms, leading to a reduction of 87.5%. The distortion of input current is mitigated.

D. Distortion of Input Current

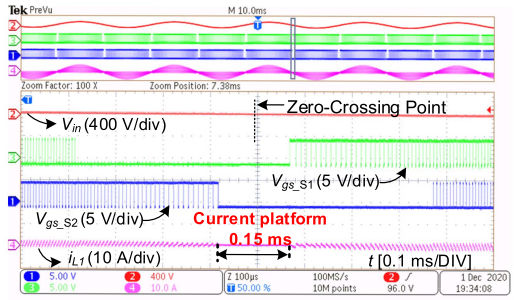
Fig. 19 compares the experimental waveforms without and with ZCD delay compensation. Without compensation, the input current has obvious distortion, and the peak-to-peak value of the inductor current is 16.2 A. After compensation, the input current has no obvious distortion, and the peak-to-peak value of the inductor current decreases to 14.1 A (a reduction of 12.9%).

Fig. 20 is the THD with conventional strategy and proposed control. From Fig. 20(a), THD is 4.791% with conventional VOT control. In Fig. 20(b), as the distortion of input current is reduced with proposed control, the THD decreases to 3.164 (a reduction of 34%).

Fig. 21 shows the comparison of the input current THD in the VOT and proposed SR control. The THD of the input current at 2.2 kW load in the case of the proposed control is 3%, which is

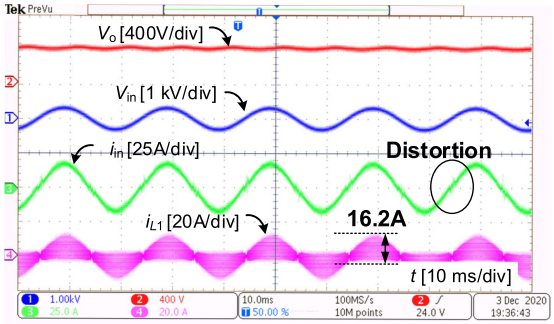


(a)

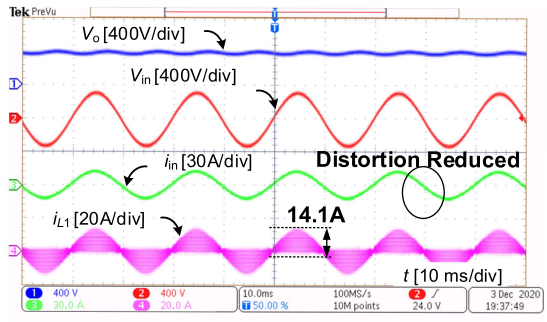


(b)

Fig. 18. Zero current platform comparison between conventional strategy and proposed control, $V_{\text{in}} = 220$ Vac, $V_o = 380$ V, $P_o = 2$ kW. (a) Conventional VOT control. (b) Proposed SR control.

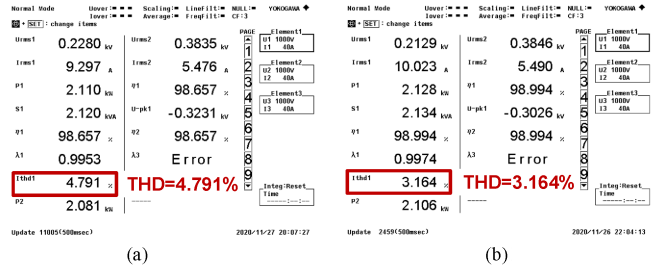


(a)



(b)

Fig. 19. Comparison of experimental waveforms without and with ZCD delay compensation, $V_{\text{in}} = 220$ Vac, $V_o = 380$ V, $P_o = 2$ kW. (a) Without compensation. (b) With compensation.



(a) (b)

Fig. 20. THD of conventional strategy and proposed control. (a) Conventional VOT control. (b) Proposed SR control.

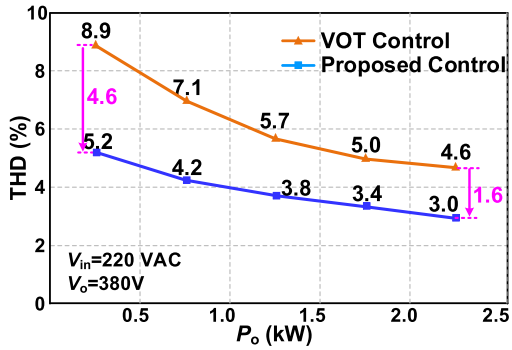


Fig. 21. Comparison of the input current THD.

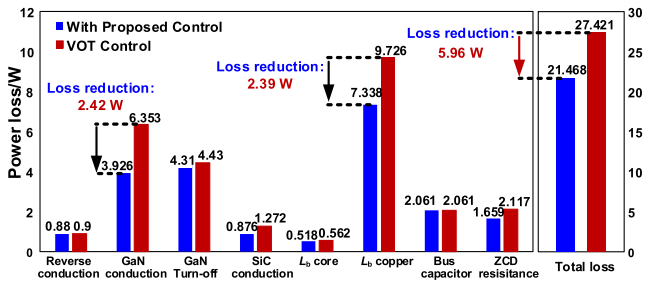


Fig. 22. Power loss breakdown, $V_{\text{in}} = 220$ Vac, $V_o = 380$ V, $P_o = 2$ kW.

1.6% lower than that in VOT control. THD of the input current at 500 W load with the proposed control is 5.2%, a reduction of 3.7% compared with the case in VOT control.

Fig. 22 compares the power loss breakdown between the proposed control and traditional VOT control. The results are obtained by calculation and the total loss is measured experimentally. The total loss of the converter decreases by 5.73 W (21%). So, the full load PFC efficiency increases to 99.00% from 98.7%.

E. Efficiency Analysis

Fig. 23 shows the efficiency of the prototype in this article and the prototype in [3] and [21]. With the proposed control, the inductor current peak-to-peak value is reduced, thus the eGaN HEMTs' conduction loss, the line-frequency switches' loss, and

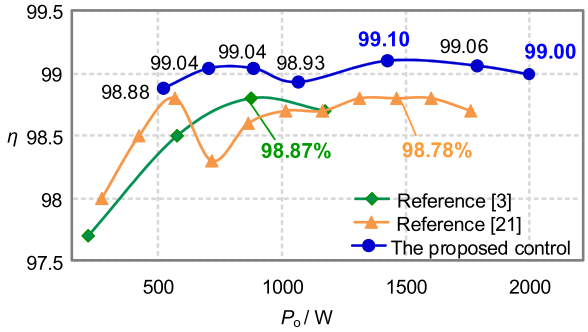
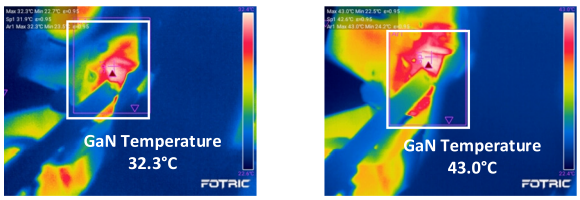


Fig. 23. Efficiency comparison, $V_{\text{in}} = 220$ Vac, $V_o = 380$ V.



(a) (b)

Fig. 24. Thermal images, $V_{\text{in}} = 220$ Vac, $V_o = 380$ V, and $P_o = 2000$ W.

the inductor copper loss are all reduced. The peak efficiency of the prototype is 99.10%, and the efficiency at 2 kW is 99.00%.

Fig. 24 shows the thermal images of GaN HEMTs in the two-phase CRM totem-pole PFC converter. The maximum temperature is 32.3 °C with fan cooling (35 W and 3500 r/min) and 43.0 °C with air cooling, respectively.

VII. Conclusion

To reduce the current distortion and avoid high reverse inductor current due to the delay of ZCD signal, an SR control with ZCD delay compensation is proposed for CRM totem-pole PFC rectifiers. The basic idea is to calculate the accurate SR turn-OFF instant considering the ZCD delay. The accurate operation model in VOT control is analyzed with ZCD delay compensation. The proposed control is able to reduce the distortion in the inductor current, avoid destructively high reverse inductor current caused by the ZCD delay and improve THD and efficiency.

To verify the proposed control, a prototype of a 2 kW 400 kHz GaN CRM two-phase interleaved totem-pole PFC converter is built. Compared with the conventional VOT control, the proposed control can avoid the destructively high reverse inductor current while decreasing the zero-current platform of the inductor current from 1200 to 150 μs (a reduction of 87.5%). In addition, as the ZCD delay is compensated in full-line cycle, the distortion of the inductor current is reduced and the inductor current peak-to-peak value is decreased from 16.2 to 14.1 A (a reduction of 12.9%) at 2 kW. Finally, The THD of full load in the case of the proposed control decreases to 3% from 4.6%, a reduction of 34%. The peak efficiency of the 2 kW PFC prototype reaches 99.10% at 1.5 kW, and 99.00% at 2 kW.

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