Letters

Objective-Based Low-Frequency Parasitic Inductance Characterization Method for Power Semiconductor Package With High Power and Switching Speed

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***Abstract*—Characterizing package parasitic inductance is significant for package design, dynamic characteristic evaluation, thermal management, and insulation breakdown protection. As package parasitic inductances become smaller and the switching speed of the power semiconductor becomes higher, traditional and widely-used double pulse tests based on the "$L = V/(di/dt)$" and "$L = 1/(4\pi^2 f^2 C)$" present more critical drawbacks in accuracy and adaptability. This letter proposes a novel method called objective-based low-frequency-range parasitic inductance characterization to accurately obtain the parasitic inductance of semiconductor packages. The proposed method directly extracts the package inductances instead of the current commutation loop and can be carried out under low bus voltage and low frequency. Thus, the proposed method features higher robustness, adaptability, and accuracy. Experimental results in the commercial silicon carbide power device/module validate the feasibility and superiority of the proposed method.**

***Index Terms*—Double pulse test, package and integration, parasitic inductance, power semiconductor, wide band gap semiconductor.**

I. Introduction

THE advancement of power semiconductor technology has promoted the development of power electronic equipment to higher power density and switching speed. Furthermore, the advanced package technologies apparently reduce the package parasitic inductances of devices/modules to ensure their high efficiency and safe operation at higher switching speeds [1], [2], [3], [4], [5], [6]. However, these changes make it challenging to accurately characterize package parasitic inductances and bring obstacles to the experimental verification of package design, switching loss estimation in thermal management, insulation protection, and EMC design.

The double pulse test (DPT) is a widely preferred method for silicon-based power semiconductors to characterize the package parasitic inductances. Several industrial or international standards, such as IEC 60747-15 [7], AQG 324 [8], and JEDEC JEP173 [9], adopt the DPT method to obtain the package parasitic inductances. However, traditional DPT methods cannot match the development trend of power devices. It has become a focus of attention when the switching speed and power density of semiconductor devices/modules become higher. The traditional DPT has the following features, which introduce errors.

1) The DPT's result is not the object— "the package parasitic inductances of semiconductor device/module," but the DPT's whole current commutation loop (CCL). The obtained parasitic inductances consist of the device under test (DUT), the extraneous inductances derived from the extraction fixture, and the equivalent series inductance (ESL) of decoupling capacitors. Extraneous parasitic parameters are large enough compared to the DUT and challenging to be obtained by experiments.
2) Power semiconductors are developing towards higher power density and switching speed while the package parasitic inductances become smaller than the traditional package technology. Silicon carbide (SiC) and gallium nitride (GaN) power devices/modules, which are representative of wide band gap (WBG) semiconductors, usually have package parasitic inductances of less than 10 nH. However, the extraneous parasitic inductances introduced by the extraction fixture may be larger than that of the DUT. Considering that the obtained result of traditional DPT is CCL's parasitic inductances, the errors introduced by backward parasitic inductance characterization method are non-negligible compared with the actual parasitic inductance value, and this phenomenon must be seriously concerned.
3) The traditional DPT measurement progress involves uncertain vital parameters. One method uses the ratio of turn-OFF voltage overshoot to current change rate, i.e., $L_{\text{loop}} = V_{\text{overshoot}}/(di_{\text{D}}/dt)$. The unfavorable characteristics of electrical probes (such as delay time, low bandwidth, large volume, and nonisolation function) and differences between $\Delta i_{\text{D}}/\Delta t$ and di_{D}/dt (corresponding to the maximum voltage overshoot under high-speed switching) cause unavoidable uncertain errors. The other method is obtained by "$L = 1/(4\pi^2 f^2 C^*)$" where the f is

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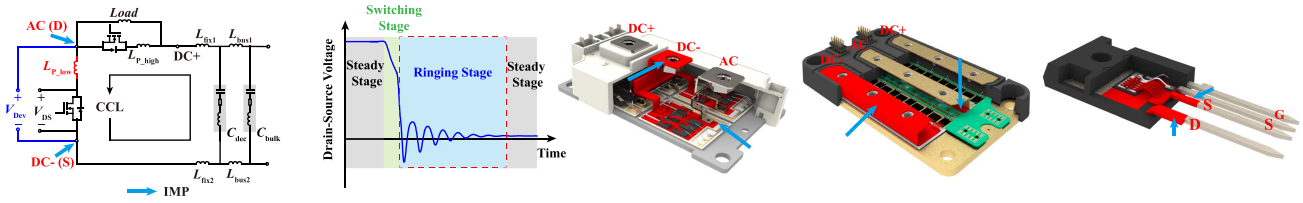

Fig. 1. Illustration for IMP. (a) DPT's equivalent circuit at the turn-ON transients. The IMP's parasitic inductance of low-bridge is $L_{\mathrm{P\_low}}$, highlighted by RED. (b) Drain-source measured voltage V_{Dev} at the turn-ON process. (c) 62 mm-package SiC power module and its IMP. The parasitic inductance of the highlighted RED part is approximately equal to $L_{\mathrm{P\_low}}$. (d) HM2-package low-inductance SiC power module and its IMP. (e) TO-247-package SiC power discrete device and its IMP.

ringing frequency; the C^* consists of the device's output capacitances C_{oss} and package parasitic capacitances. The C_{oss} is nonlinear and often offered by the datasheet, which is obtained under a specific and unitary test condition, while it cannot be directly used for characterization under actual conditions. Package parasitic capacitances are rather complex and challenging to obtain via experiments. The mentioned two capacitors are uncertain and cause unavoidable errors.

This letter, therefore, proposes the objective-based low-frequency-range parasitic inductance characterization (OLFPIC) method in Section II and presents its superior characteristics in Section III with experimental validation, from which a conclusion can be reached in Section IV.

II. Basic Concept and Method

A. Inductance-Included Measurement Position

The OLFPIC method is based on the inductance-included measurement position (IMP), which needs to be more noticed. Take SiC MOSFET as the DUT, the measured drain-source voltage V_{Dev} differs from the bare die's drain-source voltage V_{ds}. The primary source of deviations is that the IMP contains the package parasitic inductances L_{P}, which introduces the extra oscillation at the ringing stage. Fig. 1 shows the IMP's low-bridge package parasitic inductances $L_{\mathrm{P\_low}}$ in the half-bridge power module. More explanations can be found in [3]. Solving this defect is to change the package structure, such as the direct electrode measurement position [3]. However, the IMP widely exists in the commercial (such as the SiC package of TO series, 62 mm, CREE 45 mm, and HM2) and lab-made power devices/modules.

Furthermore, "the L_{P} of IMP" is the whole package parasitic inductances for the discrete device. For the half-bridge power module, the entire package parasitic inductance is the sum of "the $L_{\mathrm{P\_low}}$ of IMP" and "the $L_{\mathrm{P\_high}}$ of IMP."

B. Equivalent Lumped Inductor and Characterization Process

In the proposed method, the equivalent lumped inductor (ELI) is introduced to weigh the package parasitic inductances (see Fig. 2). It can be placed at the DC bus's high- or low-voltage side. Comparing the ELI's voltage with the IMP's voltage at the turn-ON switching process can be substituted for comparing the ELI's inductances L_{E} with the package parasitic inductances

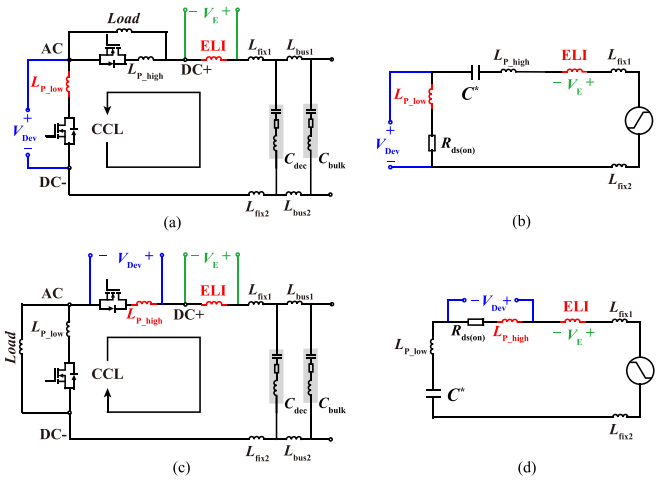

Fig. 2. Illustration for the OLFPIC method. (a) Obtain $L_{\mathrm{P\_low}}$ by measuring the low-bridge IMP at the ringing stage of low-bridge device's turn-ON transients. (b) Equivalent circuit to obtain $L_{\mathrm{P\_low}}$. (c) Obtain $L_{\mathrm{P\_high}}$ by measuring the high-bridge IMP at the ringing stage of high-bridge device's turn-ON transients. (d) Equivalent circuit to obtain $L_{\mathrm{P\_high}}$.

L_{P} of IMP. During the turn-ON process, the ringing stage is the focus [see Fig. 1(b)]. Separate each component of the waveform to obtain as

$$V_{\mathrm{Dev}} = V_{\mathrm{ds}} + k\Phi_{\mathrm{LF,MF}}\left(L_{\mathrm{bus}}, C_{\mathrm{bulk}}\right) + \Phi_{\mathrm{HF}}\left(L_{\mathrm{P}}\left|L_{\mathrm{CCL}}, C^*\right.\right) \tag{1}$$

$$V_{\mathrm{E}} = k\Phi_{\mathrm{LF,MF}}\left(L_{\mathrm{bus}}, C_{\mathrm{bulk}}\right) + \Phi_{\mathrm{HF}}\left(L_{\mathrm{E}}\left|L_{\mathrm{CCL}}, C^*\right.\right) \tag{2}$$

where V_{ds} is equal to $I_{\mathrm{d}}\mathrm{R}_{\mathrm{ds(on)}}$; $\Phi_{\mathrm{LF,MF}}(L_{\mathrm{bus}}, C_{\mathrm{bulk}})$ is the voltage component that features low- or medium-frequency oscillations mainly introduced by the large inductances or capacitances of the fixture and bus. k ($=0\sim1$) is the decoupling degree coefficient which $k=0$ represents complete decoupling and $k=1$ represents no decoupling. $\Phi_{\mathrm{HF}}(L_{\mathrm{P}}|L_{\mathrm{CCL}}, C^*)$ is the voltage component of L_{P} that features high-frequency oscillations of CCL.

The V_{Sub} is calculated as

$$\begin{aligned} V_{\mathrm{Sub}} &= V_{\mathrm{E}} - V_{\mathrm{Dev}} \\ &= \Phi_{\mathrm{HF}}\left(L_{\mathrm{E}}\left|L_{\mathrm{CCL}}, C^*\right.\right) - \Phi_{\mathrm{HF}}\left(L_{\mathrm{P}}\left|L_{\mathrm{CCL}}, C^*\right.\right) - V_{\mathrm{ds}}. \end{aligned} \tag{3}$$

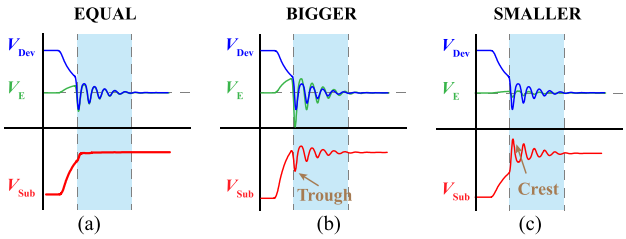

Fig. 3. Illustration for the proposed characterization method. The illustration is based on the situation when ELPHI is placed at the DC's high voltage side. The conclusions on the DC's low voltage side are similar. (a) EQUAL case. (b) BIGGER case. (c) SMALLER case.

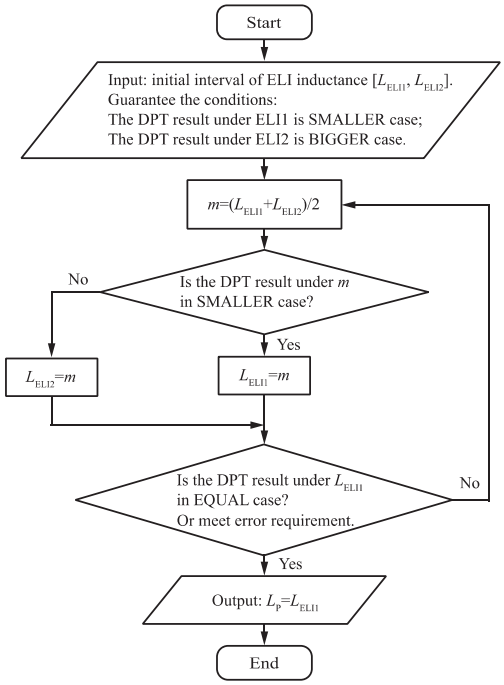

Fig. 4. Extraction flow chart of the OLFPIC method based on bisection method.

The V_{ds} is insignificant and can be discarded during the ringing stage. The differential V_{Sub} mainly depends on L_P and L_E. As for L_P and L_E, it can be divided into three cases: EQUAL is $L_P = L_E$, BIGGER is $L_P < L_E$, and SMALLER is $L_P > L_E$ (see Fig. 3). By inspecting the differential V_{Sub} in the ringing stage, we can get the relationship between L_P and L_E and the corresponding cases. As Fig. 3 shows, when the first point of arrival is the trough, it indicates the BIGGER case; when the first point of arrival is the crest, it indicates the SMALLER case; when there are no oscillations, it indicates the EQUAL case. In addition, according to the ratio of L_E and L_P, the L_P can be approximately obtained. However, the ratio method is less accurate than the mentioned method. The reason is that V_{Sub} is differential and can be immune to interference in measurement. According to the three cases, ELI will be determined as L_P. To simplify and standardize the extraction process, the bisection method can be applied to the OLFPIC. Fig. 4 shows the extraction process of package parasitic inductance by the

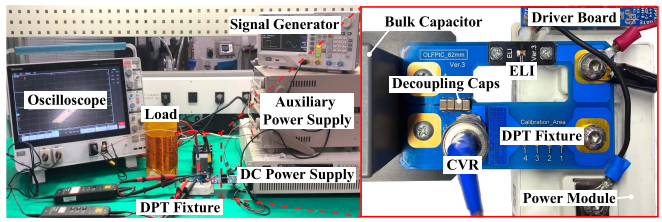

Fig. 5. Extraction fixture with the calibrated ELI board.

TABLE I
DETAILS OF MAIN EXPERIMENTAL EQUIPMENT

Objective	Details
Oscilloscope	Tektronix MDO4054C, 500 MHz, 2.5 GS/s
Voltage probe	Tektronix THDP0200 1500 V/200 MHz (OLFPIC expt.); Tektronix TPP0850 1000 V/800 MHz (trad. DPT expt.); Tektronix TPP0500B 300 V/500 MHz (both)
Current probe	T&M's CVR, SSDN-414-025, 1200 MHz
DUT	62mm power module: CREE CAS300M17BM2; TO-247 power device: CREE C3M0016120K
Extraction fixture	Simulated parasitic inductances: 52.0229 nH at 100 MHz (OLFPIC expt.); 17.2414 nH at 100 MHz (trad. DPT expt.)

OLFPIC method. After several DPTs, the ELI's inductance is very close to the DUT's package inductance. Once the result is in the "EQUAL" case or meets the error requirements, the target value can be determined.

The proposed method can directly obtain package parasitic inductances instead of the whole CCL's inductances. Therefore, the OLFPIC method is applicable for extracting the parasitic inductances in the power devices but not for the whole control loop inductances. It can be measured at low oscillation frequency (the CCL's parasitic inductances can be large, thus reducing the frequency at the ringing stage). According to the abovementioned characteristics, the proposed method is named objective-based low-frequency-range parasitic inductance characterization. The following section presents the advantages of the OLFPIC method in detail through analysis with experiments.

III. CHARACTERISTICS ANALYSIS

This section introduces the OLFPIC's characteristics and compares them with traditional DPTs via experiments and simulations. The details of the main experimental equipment are shown in Fig. 5 and Table I.

A. High Robustness and Accuracy

1) Objective-Based Characteristics: The OLFPIC method is objective-based. It can obtain the power module's L_P of the high- and low-bridge switches respectively, but the traditional DPT cannot. Fig. 6 shows the 62 mm power module extraction results by the OLFPIC using the bisection method. The fixed inductor is selected as ELI and calibrated in the extraction fixture. The final results are 9.5 nH of L_{P_high} and 5 nH of L_{P_low}. Thus, the total measured L_P is 14.5 nH. For the separate module, the datasheet's L_P is 15 nH (-3.333% error), and the simulated L_P is 14.58888 nH (-0.6092% error). In practice, the

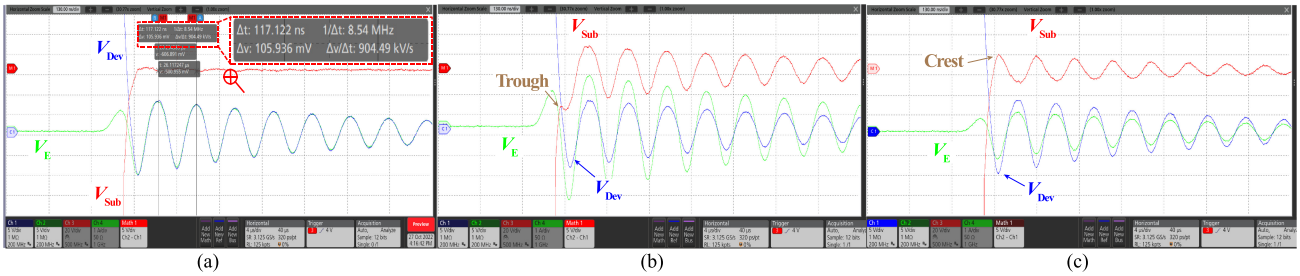

Fig. 6. Details of OLFPIC experiments about the 62 mm module's $L_{\mathrm{P\_low}}$ extraction. The test conditions: 150 V of bus voltage, about 3.3 A of load current, 10 Ω of turn-ON and turn-OFF resistors. (a) EQUAL case ($L_{\mathrm{P\_low}} = L_{\mathrm{E}} = 5$ nH). (b) BIGGER case ($L_{\mathrm{P\_low}} < L_{\mathrm{E}} = 8.5$ nH). (c) SMALLER case ($L_{\mathrm{P\_low}} > L_{\mathrm{E}} = 3.5$ nH).

module is connected to the PCB/busbar, and it is predictable that the parasitic inductance will change. The simulated L_{P} with extraction fixture is 14.04231 nH (3.259% error). Note that this 62 mm module has different $L_{\mathrm{P\_high}}$ and $L_{\mathrm{P\_low}}$ due to its internal asymmetric package structure, and the traditional DPT cannot reflect this fact. The TO-247 power device is also investigated. The L_{P} is determined as 7 nH. The L_{P} offered by CREE's LTspice model is 6.666 nH (5.011% error), and the simulated L_{P} is 6.84071 nH (2.328% error).

Furthermore, the OLFPIC method is independent of several factors, which bring sufficient errors.

a) Independence of extraneous parasitic inductances: The simulated fixture's parasitic inductances are 52.02294 nH in the OLFPIC experiments. The proposed method is objective-based. So, these extraneous parasitic inductances do not affect the characterization results. In the ringing stage, the resonant voltage amplitude of ELI and L_{P} varies according to their inductive reactance. It means that the method is independent of other parasitic inductances in CCL. Equation (3) shows that V_{Sub} does not depend on other parasitic inductances but L_{P} and L_{E}. Compared with the traditional DPT, the extraneous parasitic inductance (stemming from extraction fixture, bulk/decoupling capacitors, and others) is not the error source. It is significant for low-inductance-package power devices (SiC and GaN).

b) Independence of overshoot voltage and di/dt: There are two error sources for the traditional DPT of "$L_{\mathrm{loop}} = V_{\mathrm{overshoot}}/(di_{\mathrm{D}}/dt)$." First, because of the IMP, the experimental overshoot voltage is $V_{\mathrm{Dev\_max}}$ rather than $V_{\mathrm{overshoot}}$, which is the actual bare die's drain-source voltage. The error can be written as

$$\varepsilon_1 = \frac{|V_{\mathrm{Dev\_max}} - V_{\mathrm{Overshoot}}|}{V_{\mathrm{Overshoot}}} \times 100\%. \tag{4}$$

ε_1 would be non-negligible at the high switching speed. Fig. 7(a) shows that the ε_1 will reach about 38.21%. Second, the error stems from the approximate treatment of di_{D}/dt as

$$\varepsilon_2 = \left(\frac{V_{\mathrm{Overshoot}}}{\Delta i_{\mathrm{D}}/\Delta t} - L_{\mathrm{CCL}}\right)/L_{\mathrm{CCL}} \times 100\%. \tag{5}$$

The error will increase with the switching speed. For further explanation, the experiment of traditional DPT is conducted based on a 62 mm power module. The obtained $V_{\mathrm{Dev\_max}}$ is 55.940 V, and $\Delta i_{\mathrm{D}}/\Delta t$ is 1.21 GA/s. Thus, the experimental

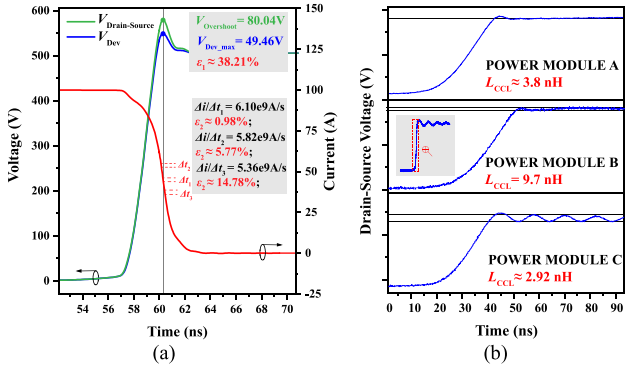

Fig. 7. Additional illustrations for the traditional DPT method. (a) Error source: the overshoot voltage $V_{\mathrm{Dev\_max}}$ due to IMP and the approximate treatment of di_{D}/dt. The simulation circuit diagram is set according to Fig. 1(a) with $L_{\mathrm{P\_high}} = L_{\mathrm{P\_low}} = 5$ nH, $L_{\mathrm{fix1}} = L_{\mathrm{fix2}} = 1$ nH, ESL of decoupling capacitor is 1 nH, gate resistance is 1 Ω. (b) Three cases in experimental DPT. Power module A (1200 V/150 A): the low-current and high-damping case. Power module B (1200 V/600 A): the case affected by the bus's parasitic inductances. The oscillations consist of medium and high components. Power module C (1200 V/600 A): the high-current and low-damping case.

L_{loop} is 46.23 nH (52.43% error, while the simulated L_{loop} is 30.32872 nH), and the experimental L_{P} is 28.99 nH (93.27% error). This result includes the wrong estimations of the fixture's inductances, which cannot be accurately determined.

c) Independence of parasitic capacitors: For the traditional DPT of "$L = 1/(4\pi^2 f^2 C^*)$," the die's output capacitors C_{oss} and the package parasitic capacitors are the error sources. As for the C_{oss}, the data provided by the manufacturer's datasheet is usually limited. Under different operation conditions (V_{gs} and V_{ds}), C_{oss} ($= C_{\mathrm{gd}} + C_{\mathrm{ds}}$) shows a drift phenomenon that is not to be ignored [10]. As for package parasitic capacitors, it is difficult to obtain via experiments. Furthermore, the oscillation may not be observed, or multiple oscillation components may be superimposed, as Fig. 7(b) shows. Thus, this method lacks accuracy and cannot be used in some cases. The traditional DPT via parasitic capacitors is also conducted to determine the 62 mm power module. The voltage oscillation is obtained as 18.31 MHz, and the C_{oss} is chosen as 2.7 nF. Thus, the experimental L_{loop} is 27.98 nH (-7.744% error), and the L_{P} is 10.80 nH (-28% error). Finally, the demand for high-bandwidth probes is also a disadvantage. See Section III-B.1 for more explanations. For the OLFPIC

method, it is independent of the uncertain parasitic capacitances, so significant errors are avoided.

d) Independence of probe's parasitic parameter and common-mode interference: The V_{Sub} is differential, as it is the result of the subtraction of V_{E} and V_{Dev}. If the errors caused by probe's parasitic parameters and common-mode interference are marked as δ, the V_{Sub} considering these errors is rewritten as

$$\begin{aligned} V_{\mathrm{Sub}} &= (V_{\mathrm{E}} + \delta_1) - (V_{\mathrm{Dev}} + \delta_2) \\ &= \Phi_{\mathrm{HF}}\left(L_{\mathrm{E}} \middle| L_{\mathrm{CCL}}, C^*\right) - \Phi_{\mathrm{HF}}\left(L_{\mathrm{P}} \middle| L_{\mathrm{CCL}}, C^*\right) \\ &\quad - V_{\mathrm{ds}} + (\delta_1 - \delta_2). \end{aligned} \tag{6}$$

When the same probe is used for measurement, the errors caused by the probe's parasitic parameters are the same. In addition, the common-mode interferences contained in V_{E} and V_{Dev} are the same (they exist the same CCL). Therefore, the mentioned errors are eliminated (i.e., $\delta_1 - \delta_2 = 0$).

2) High Sensitivity: When the package parasitic inductance L_{P} is inconsistent with the ELI, V_{Sub} will show apparent oscillations. Based on the $\mathrm{L_{P\_low}}$ extraction experiments of the 62 mm module, the voltage sensitivity of 4.161 V/nH is obtained under the test condition of 150 V bus voltage and the 3.3 A of load current. With the rise of bus voltage, the sensitivity will further increase. Under the abovementioned conditions, the sensitivity is sufficient to ensure the accuracy of package parasitic inductance characterization.

B. High Adaptability and Low Cost

1) Low Bandwidth Probe Requirements: The SiC/GaN devices feature ultrashort switching transform time, which is already close to the measurement instruments' rise time and propagation delay. According to [12], the instrument's bandwidth should be applied by "5 Times Rules" —five times of highest frequency component. As for low-inductance WBG power devices, the oscillation/ringing frequency is usually bigger than 80 MHz, which means high-bandwidth and expensive measurement instruments are needed.

As for the OLFPIC method, it does not require the high-bandwidth measurement instruments. Because of its independence from extraneous parasitic inductances, regulating the CCL's oscillation frequency is feasible by changing the inductance value. So, this method can be used in the low-frequency range. Fig. 6(a) shows that the oscillation frequency is 8.54 MHz (still in the ac area of the parasitic inductance), and only a 50 MHz probe is required to meet the accuracy requirements.

2) Low-Voltage Testing Conditions: The OLFPIC method is suitable for use under low bus voltage to ensure the safety of DUT. Fig. 6 shows that the testing voltage is only 150 V. Furthermore, the frequency at the ringing stage descends due to the high parasitic capacitances of the device under low voltage so that low-cost probes can be used.

IV. Conclusion

The OLFPIC method is based on the IMP phenomenon and works by the difference between the voltage of the package parasitic inductances and the ELI during the turn-ON ringing stage. It is object-based, low-frequency, and differential. The object-based characteristic ensures that the method is not affected by the parasitic inductances introduced by extraction fixture. The low-frequency characteristic makes the method not require high-cost and high-bandwidth voltage probes and avoid waveforms distortion and time delay at high frequency. The differential characteristic makes the method features high anti-interference performance. Thus, these characteristics ensure that the OLFPIC method features high robustness, adaptability, and accuracy, especially for WBG semiconductor package devices with higher power density and switching speed.

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