Letters

Heterogeneous Integration of Silicon-Based *RC* Snubber in SiC Power Module for Parasitic Oscillation Noise Reduction

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***Abstract*—Due to the increased switching speed and reduced device capacitance, the parasitic oscillation of the switching device has become the primary high-frequency electromagnetic interference (EMI) noise source in SiC converters. The dc-link snubber offers a potential to mitigate the noise in a cost-efficient way. However, the temperature limits and thermal de-ratings of the existing ceramic capacitor hinder the exploration of module-level integration. In this letter, a silicon-based *RC* snubber is designed to fit the working temperature of the power module. With the developed four-order damping and thermal coupling models, the iterative method is proposed to optimize the integration performance. The experiments validate the temperature stability of the integrated snubber. With the aid of the proposed *RC* snubber, the EMI noise induced by the parasitic oscillation in the prototype module is reduced by 7 to 22 dB compared with the nonsnubber module with ceramic decouplers.**

***Index Terms*—Heterogeneous substrate, parasitic oscillation noise, *RC* snubber, SiC power module, temperature stability.**

I. Introduction

Along with the improved efficiency and power density, the SiC converter suffers severer electromagnetic interference (EMI) due to the increased switching frequency, shorter transition time, and resulting in the parasitic oscillations in the power module [1]. Among these effects, the parasitic oscillation formed by junction capacitance and stray inductance generally determines the high-frequency (HF) noise spike. The high-speed switching application of SiC devices is hindered since the noises are difficult to filter out due to the limitations of magnetic materials and filter parasitics [2].

There has been literature to address this issue from several aspects. On the oscillation mechanism, the empirical methods, the segmented analytical models, and the equivalent circuits have been derived for behavior modeling [3]. The oscillations from several MHz to above 100 MHz are observed under different transistor setups, revealing an opposite trend of noise emerging with the device improvements. On mitigation methods, the passive methods are proposed for noise reduction, including the wiring/package redesign [4], [5], capacitor decoupling [6], [7], snubber suppression [8], [9], etc. Thanks to the excellent damping performance, the dc-link snubber has been recognized as an effective and cost-efficient way in discrete device-based systems. However, due to the poor temperature /voltage coefficients of the dielectric material [10], the temperature of the commercial ceramic capacitors is strictly limited below 125 °C. The thermal restriction and corresponding capacitance de-ratings hinder further exploration in module-level applications. The works in [11], [12], and [13] propose to use of the high-voltage silicon snubber with the Si_3N_4 dielectric layer for module integration. However, the integration method considering both the electrical damping and thermal behavior is still challenging.

In this letter, a silicon-based *RC* snubber is developed to fulfill the 175 °C working temperature of the power module. Furthermore, thanks to the derived four-order damping and the thermal coupling models, the iterative integration method considering the snubber temperature coefficient is proposed to optimize the snubber performance in SiC modules.

II. Snubber Structure Design

Unlike the $BaTiO_3$-based dielectric in multilayer ceramic capacitors (MLCC), the Si_3N_4 layer enables stable temperature and voltage properties with the compromise on dielectric constant. On the thermomechanical stress, owing to the similar CTE of the Si_3N_4 (3.2 ppm/°C) and the Si (2.6 ppm/°C), the stress of the silicon snubber is gentler than the MLCCs (ceramic-metal interface). The design and property highlights of the snubber are provided as follows.

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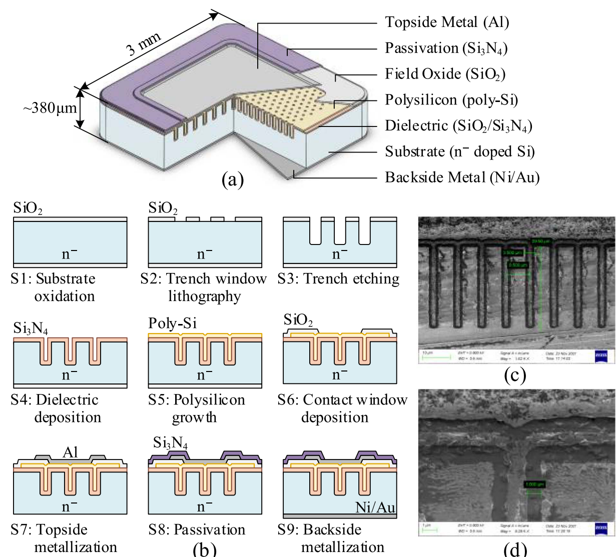

Fig. 1. Structure and fabrication process of a silicon snubber. (a) Bare die structure. (b) Fabrication process. (c) and (d) Cross-section SEM images of the dielectric area.

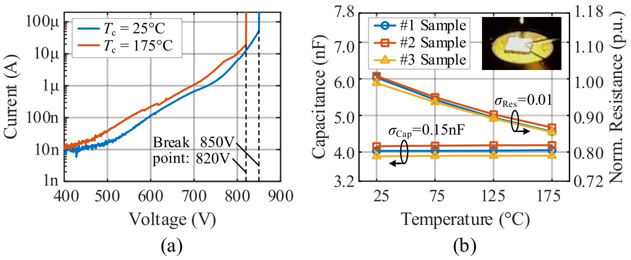

Fig. 2. Measured results of snubber characteristics. (a) Current-voltage *I–V* curves in different temperature. (b) Capacitance/resistance-temperature C/R-T curves of multiple samples.

A. RC Snubber Structure

Fig. 1 illustrates the structure and fabrication process of the silicon snubber, which is a vertical device with back-to-back electrons to fit the module mounting. The main dielectric layer employs the 1.0 μm Si_3N_4 by low-pressure chemical vapor deposition. This setup achieves the above 800 V breakdown voltage. Thanks to the hexagon hole array by deep reactive ion etching, the theoretical capacitance density is 0.45 nF/mm^2. Different snubber resistances are obtained by tuning the doping density of the n$^-$ substrate.

B. Featured Parameters

In this letter, the silicon snubbers with a 3×3 mm^2 die size are prototyped for further investigation. To validate its temperature properties, the leakage current, as well as the *RC* parameters, are measured by a probe station (FormFactor Tesla200). As shown in Fig. 2, the breakdown voltage of the bare die achieves 820 V under 175 °C. The device can withstand at least 800 V voltage from 25 °C to 175 °C with 10 μA leakage current limit. Furthermore, excellent capacitance stability is demonstrated under 150 °C

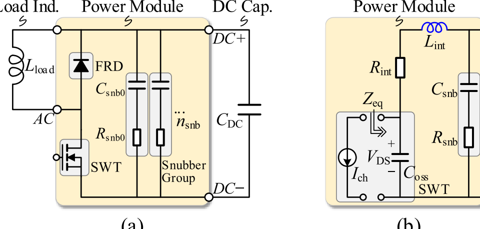

Fig. 3. Circuit model for damping analysis. (a) Equivalent circuit of a snubber integrated half-bridge module. (b) Its four-order small-signal model.

temperature rise with 500 V voltage bias. The above results validate that the snubber fits the 175 °C working temperature of SiC power modules. However, the temperature coefficient of resistance that reaches −1015 ppm/°C may influence the snubber performance, which is considered in the integration design in Section III.

III. Integration Method

Mounting of the silicon snubber employs compatible techniques with the transistors, i.e., the topside wire-bonding and backside soldering process, thus obtaining feasible manufacturability for integration. However, considering the temperature-dependent snubber resistance and the diverse module setups, the integration design method requires further study. This section first investigates the sensitivity of the snubber's damping performance under the different module and transistor setups. Then, followed by the coupled thermal model, the iterative design method is proposed to work with the temperature effects of the snubber resistance.

A. Damping Model

According to the equivalent circuit in Fig. 3(a), the small-signal model in Fig. 3(b) is employed for damping analysis. Considering the compact mounting of silicon snubbers, the parasitic inductance in that branch is ignored. The network function Z_{eq} of the drain-source port is derived as

$$Z_{\mathrm{eq}}(s) = \frac{V_{\mathrm{DS}}(s)}{I_{\mathrm{ch}}(s)} = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + 1} \quad (1)$$

where the polynomial coefficients of the denominator are

$$\begin{cases} a_1 = C_{\mathrm{oss}} R_{\mathrm{int}} + C_{\mathrm{snb}} R_{\mathrm{snb}} \\ a_2 = \left(C_{\mathrm{snb}} R_{\mathrm{int}} R_{\mathrm{snb}} + L_{\mathrm{ext}} + L_{\mathrm{int}}\right) C_{\mathrm{oss}} + L_{\mathrm{ext}} C_{\mathrm{snb}} \\ a_3 = \left(L_{\mathrm{ext}} R_{\mathrm{int}} + L_{\mathrm{ext}} R_{\mathrm{snb}} + L_{\mathrm{int}} R_{\mathrm{snb}}\right) C_{\mathrm{oss}} C_{\mathrm{snb}} \\ a_4 = L_{\mathrm{ext}} L_{\mathrm{int}} C_{\mathrm{oss}} C_{\mathrm{snb}} \end{cases} . \quad (2)$$

The four-order denominator implies two pairs of conjugate poles as

$$\begin{cases} p_{1,3} = -\alpha_1 \pm j\omega_1 \\ p_{2,4} = -\alpha_2 \pm j\omega_2 \end{cases}, \quad \omega_1 > \omega_2 \quad (3)$$

which respectively dominate the low-frequency oscillation by the external inductance L_{ext} and snubber capacitance C_{snb}, and

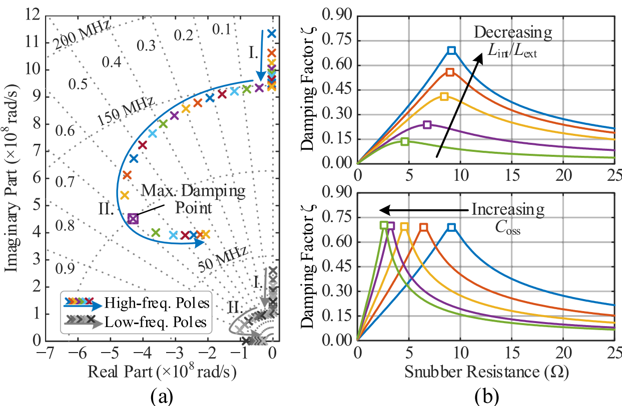

Fig. 4. Damping characteristics of the snubber. (a) Pole trajectory. (b) Sensitivity analysis for snubber position and transistor setups.

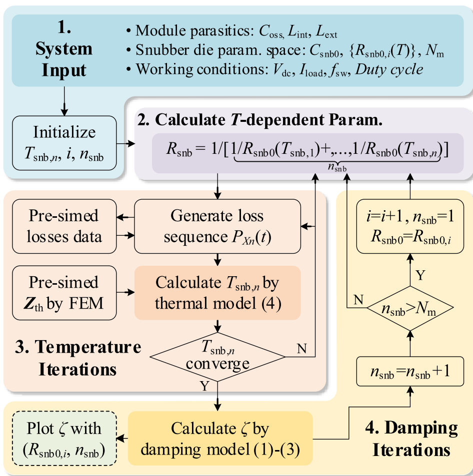

Fig. 5. Iterative algorithm for snubber optimization, where the bare die selection i and paralleling number $n_{\rm snb}$ are design variables. The temperature-dependent resistance is included in every iteration.

the HF oscillation by the internal inductance $L_{\rm int}$ and capacitance of the switching devices $C_{\rm oss}$.

To investigate the oscillation characteristics, the trajectory of the HF pole is analyzed by screening the snubber parameters in the damping-frequency ζ–ω_n coordinates, where the damping factor ζ describes how oscillations in the system decay after switching. Under the setup of an exemplary SiC module, several properties can be deduced:

1) In trajectory I of Fig. 4(a), the decoupling situation is studied when $R_{\rm snb} = 0$. With the increase of $C_{\rm snb}$, only the natural frequency of the HF pole is affected. It means that the oscillation is shifted to a lower frequency without damping, which reveals the shortage of the capacitive decoupler.
2) In trajectory II of Fig. 4(a), $R_{\rm snb}$ is increased with $C_{\rm snb}$ fixed at 10 $C_{\rm oss}$ ($\sim$10 nF). The trajectory of the HF pole shows a convex property in the ζ grid. The maximum damping point for the HF oscillation exists in the system.
3) Further study in Fig. 4(b) investigates the sensitivity of the maximum damping point with different module setups. Concerning the snubber placement, the closer the snubber is placed to the switching devices (decreasing $L_{\rm int}/L_{\rm ext}$), the better the damping effect would be obtained. This illustrates the advantage of snubber's module-level integration. Concerning the transistor setups, the maximum damping factor is irrelevant to the junction capacitance of the switching device $C_{\rm oss}$. It implies that the snubber applies to different transistor selections.

B. Thermal Model

Considering the close mounting to transistors, the coupling temperature of snubbers should be evaluated for two realistic factors. At first, due to the compatible interconnection process for snubber mounting, the working temperature of the snubber is recommended below the maximum module temperature to avoid reliability weakness at the mounting point. Moreover, considering the temperature coefficient of the snubber resistance, the damping point also requires correction according to the field thermal conditions.

The matrix thermal model [14] is built to evaluate the temperature of N sets of integrated snubbers in a module, as

$$T_{{\rm snb},n}\,(t) = \mathbb{F}^{-1}\left(\begin{bmatrix} Z_{{\rm th,S-snb},n} \\ Z_{{\rm th,D-snb},n} \\ Z_{{\rm th,snb},m-n} \end{bmatrix}^T \begin{bmatrix} P_{\rm SWT}\,(j\omega) \\ P_{\rm FRD}\,(j\omega) \\ P_{{\rm Snb},m}\,(j\omega) \end{bmatrix}\right) + T_{\rm case}\,(t) \tag{4}$$

where $T_{\rm case}$ is the case temperature, the temperature rise of the snubber n is determined by the inverse Fourier-transform of the frequency-domain thermal impedance and loss profile of the switch (S/SWT), diode (D/FRD), and snubbers ($m = 1, 2, \ldots, N$). By this method, the temperature swing and average value can be quickly obtained during the integration design.

C. Determination of Snubber Parameters

Joining the damping and thermal models, the iterative algorithm is proposed to evaluate the snubber's design space as in Fig. 5, where the working points of the snubber dies are iteratively tracked by referring to the temperature-dependent resistance and pre-simulated losses. The final output provides the field performance under different design portfolios combining the bare die resistance and paralleling quantities.

IV. Implementation and Validation

This section provides the implementation and verification results of an SiC power module to validate the integration method.

A. Module Configuration and Design Results

The prototype module employs the half-bridge topology with four paralleled SiC MOSFET chips (CREE CPM2-1200-0040 A, 1200 V/40 mΩ) in a switch position (SW1$a\ldots d$ for upper switches and SW2$a\ldots d$ for lower switches), as shown in Fig. 6(a). The external inductance $L_{\rm ext}$ and the internal inductance $L_{\rm int}$ are measured as 25 and 12 nH, respectively. Four types of snubbers with a capacitance rating of 4 nF and

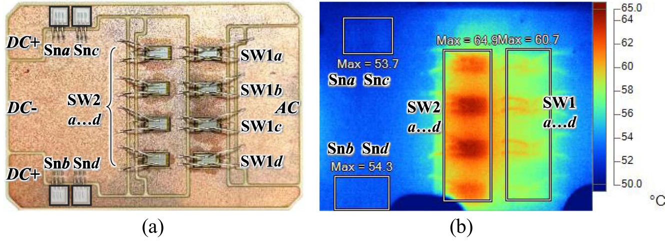

Fig. 6. Half-bridge prototype module with *RC* snubbers. (a) Substrate layout schematic. (b) Thermal image of the substrate under boost converter condition.

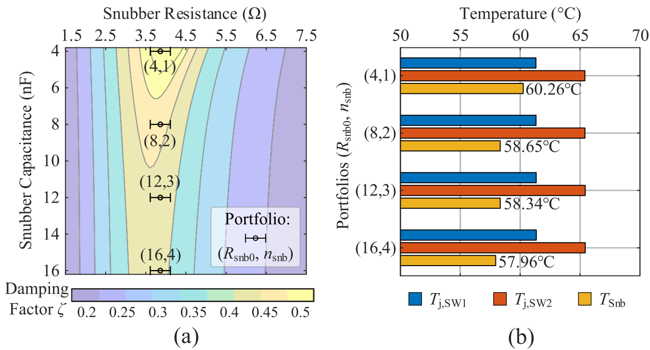

Fig. 7. Snubber design results for boost converter condition. (a) Damping effect. (b) Maximum junction temperature of switches and snubbers.

TABLE I
SWITCHING LOSSES COMPARISON OF LOWER SWITCHES

Scheme	SW2*a*		SW2*b*	
	E_{on} (μJ)	E_{off} (μJ)	E_{on} (μJ)	E_{off} (μJ)
Non-snubber	120.02	52.24	117.35	53.33
With snubber	119.15	49.7	116.15	51.05
Change rate	-0.72%	-4.86%	-1.02%	-4.28%

resistance ratings at 4, 8, 12, and 16 Ω are taken as the design candidates. To ensure the layout compactness, a maximum of four snubber chips are allowed in the module substrate, arranged at positions of Sn*a*, Sn*b*, Sn*c*, and Sn*d*. The working condition is set as a boost converter mode with $V_{\mathrm{in}} = 50$ V, $V_{\mathrm{out}} = 350$ V, $I_{\mathrm{load}} = 100$ A, $f_{\mathrm{sw}} = 10$ kHz, and $T_{\mathrm{case}} = 50$ °C.

By feeding the above setups into the iterative algorithm, the solution space is obtained as in Fig. 7. Effective damping can be achieved by adjusting the paralleled snubber number n_{sub} in the given design space $R_{\mathrm{snb0}} = \{4\ \Omega, 8\ \Omega, 12\ \Omega, 16\ \Omega\}$, since the maximum damping point of the snubber resistor R_{snb} is around 3.55 Ω. The damping factors ζ of the boost system under the four design combinations are all greater than 0.4. Table I reveals the RC snubber will not increase the switching losses.

B. Validations of Noise Reduction and Working Temperature

The oscillation turn-OFF voltage and spectral characteristics of the substrate are first evaluated using a double-pulse test with a bus voltage of 500 V, to verify the damping effect of the *RC* snubber scheme. The contrastive results of substrates without snubber, with ceramic capacitor decoupler and with

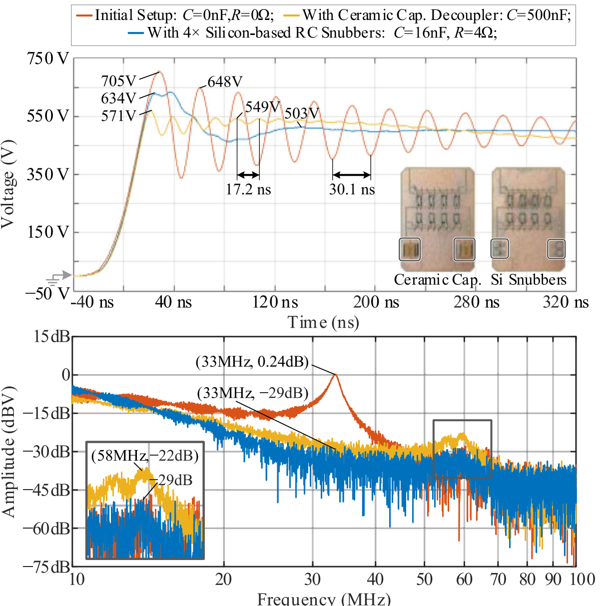

Fig. 8. Measured voltage waveform and its spectrum of power modules under double-pulse test without snubber, with ceramic capacitor decoupler and with silicon-based *RC* snubbers.

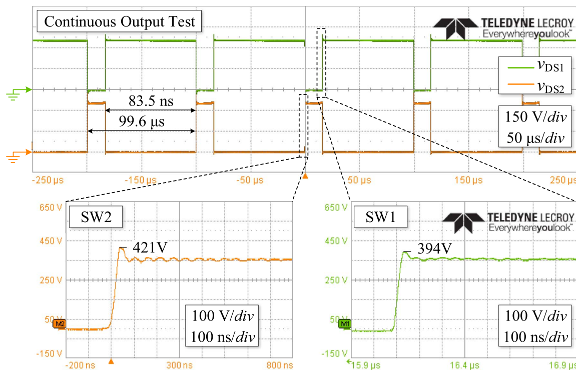

Fig. 9. Measured voltage waveforms of switches under continuous output test.

silicon-based *RC* snubbers are shown in Fig. 8. The substrate without snubber obtains a voltage overshoot of 705 V, and presents significant 33 MHz EMI noise. The ceramic capacitor scheme achieves a smaller voltage overshoot of 571 V, because the commutation loop is closed inside the substrate. However, there is still 58 MHz internal commutation loop oscillation and 1.4 MHz external commutation loop oscillation in the substrate, which increases the difficulty of the converter design. The *RC* snubber scheme realizes the best oscillation suppression effect. There is no obvious oscillation phenomenon in the turn-OFF voltage waveform and no evident HF peak in the noise spectrum. The spectral gain is reduced by 29 and 7 dB respectively compared with the nonsnubber and ceramic capacitor schemes.

Fig. 9 indicates the drain-source voltage waveform of the switches under the boost condition test. The continuous damping effect of the *RC* snubbers is verified by the turn-OFF voltage

waveforms without obvious parasitic oscillation. The steady-state temperature distribution of the substrate is measured using a thermal imager (Fluke Ti450), as shown in Fig. 6(b). The errors between the maximum temperatures in the actual chip areas and the calculation results in Section IV-A are less than 3.7 °C, which are mainly due to the loss simulation error and heat dissipation condition difference. The thermal performance of the *RC* snubber substrate and the effectiveness of the proposed design method are verified.

V. Conclusion

This letter introduced a Si-based *RC* snubber into the substrate-integrated package for SiC MOSFET modules. The substrate electrothermal coupled performance is iteratively optimized by the developed fourth-order damping and thermal coupling models. It is demonstrated that the oscillation noise can be suppressed by 29 dB and the turn-OFF overshoot voltage can be reduced by 71 V compared with the nonsnubber scheme.

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