Letters

Fully Soft-Switched DC Solid-State Circuit Breakers

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***Abstract*—This letter presents a new fully soft-switched dc solid-state circuit breaker. During dc current interruption, both main and auxiliary switches turn OFF under zero current switching (ZCS). A novel inductor–capacitor–capacitor-based active injection circuit is proposed. It eliminates transient power on switches with a fast operation, which enhances reliability. Experiments of a 350 V/90 A prototype validate the ZCS operation for both switches. The response speed reaches 4 μs, and the maximum voltage on switches is 759 V, which is within a safe range. This letter is accompanied by slides as multimedia material demonstrating major innovations and contributions.**

***Index Terms*—Active injection circuits, DC circuit breakers, solid-state circuit breakers, soft-switched circuit breakers.**

I. Introduction

THE concept of zero current switching (ZCS) is adopted in patent reference [1] for hybrid circuit breakers to realize safe turn-OFF of a main mechanical switch. The idea is to add an auxiliary active injection circuit (AIC) to generate a countercurrent pulse and cancel fault current in the main switch.

Motivated by [1], ZCS turn-OFF of the main switch is extended to solid state circuit breakers (SSCBs) with both full-controlled [2], [3], [4] and half-controlled switches [5], [6], [7], [8], [9], [10]. Compared to other SSCBs with hard-switching [11], [13], [14], [15], the major benefit of soft turn-OFF operation in SSCBs [2], [3], [4] lies in the elimination of power and energy shock in the main switch. Especially for a solid-state switch, the gate voltage oscillation during the turn OFF is significantly reduced to maintain a safe interruption. These concepts have been elaborated in [2], [3], and [4].

However, there are still limitations in existing AICs [2], [3], [4]. These AICs also contain auxiliary switches to conduct pulse currents, but the auxiliary switches do not have ZCS operation. Moreover, the auxiliary switches are usually realized by low current rating devices, which means their transient power shock could put the SSCBs under a high risk.

Manuscript received 20 September 2022; revised 6 November 2022 and 7 December 2022; accepted 14 January 2023. Date of publication 17 January 2023; date of current version 20 April 2023. This work was supported by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Grant DE-AR0001114 in the BREAKERS program monitored by Dr. Isik Kizilyalli. *(Corresponding author: Fei Lu.)*

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This article has supplementary material provided by the authors and color versions of one or more figures available at https://doi.org/10.1109/TPEL.2023.3237785.

Digital Object Identifier 10.1109/TPEL.2023.3237785

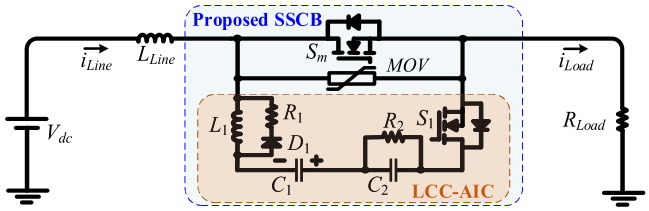

Fig. 1. Proposed LCC-AIC-based SSCB.

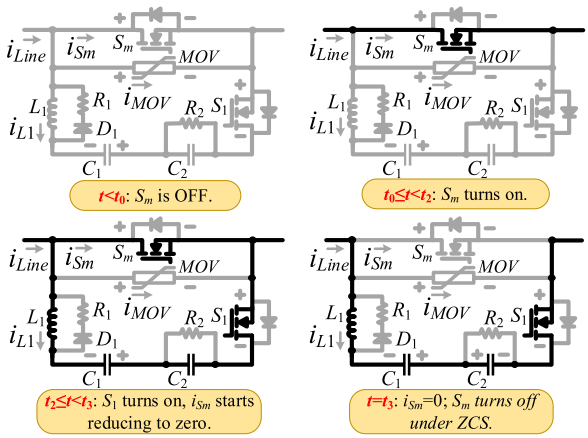

Fig. 2. Operating modes of S_m, showing ZCS is achieved.

Therefore, this letter proposes a novel inductor–capacitor–capacitor (LCC) AIC as shown in Fig. 1. It obtains a complete ZCS for both main and auxiliary switches, which significantly improves the SSCB reliability. The working principle is provided, showing ZCS for both switches, and a 350 V/90 A prototype is further implemented and tested for validation.

II. Proposed LCC-AIC-Based SSCB

A. ZCS Operation of Main Switch S_m

Figs. 2 and 3 indicate the ZCS operation of S_m during fault interruption. Before $t = t_0$, SSCB is OFF, and there is no current. The pre-voltage on C_1 is maintained as V_{aux}. As S_m is OFF, $v_{Sm} = V_{dc}$. At $t = t_0$, S_m turns ON and conducts the load current ($v_{Sm} = 0$). Regarding Fig. 3, a fault occurs at $t = t_1$, where fault current rises fast. At $t = t_2$, i_{Sm} reaches a threshold I_{th}, and then S_1 turns ON. Fault current commutates to S_1, and i_{Sm} starts decaying, where it reduces to zero at $t = t_3$. Then, S_m turns OFF under ZCS without any power shock stress. The ZCS

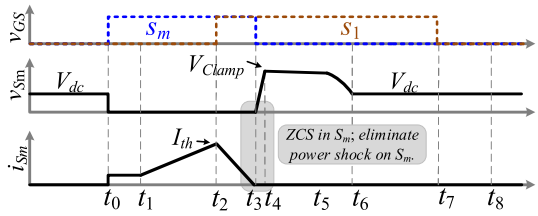

Fig. 3. Conceptual waveform showing ZCS of Sm.

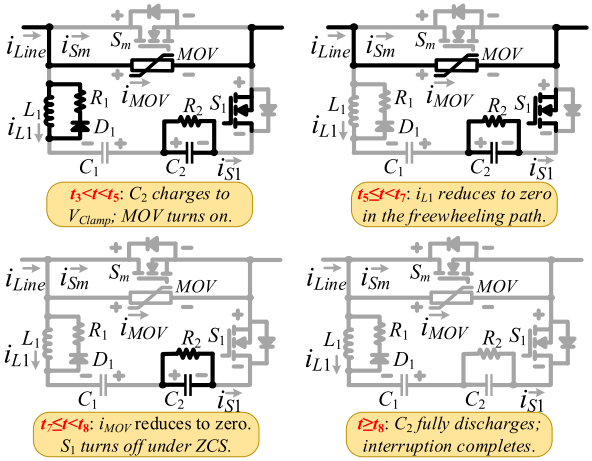

Fig. 4. Operating modes of S_1, showing ZCS is achieved.

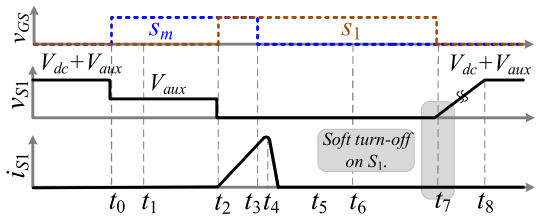

Fig. 5. Conceptual waveform showing ZCS of S_1.

operation is labeled in Fig. 3. It is noted that the SSCB still reliably interrupts the dc fault currents if i_{Sm} is not zero at the time of turning S_m OFF.

B. ZCS Operation of Auxiliary Switch S_1

Figs. 4 and 5 indicate the ZCS operation of S_1. C_2 acts as a coupling capacitor in AIC. As fault current commutates to AIC at $t = t_3$, C_1 discharges and C_2 charges. When v_{C2} reaches V_{Clamp} (the clamping voltage of MOV), MOV turns ON and forces the fault current to commutate to the MOV branch. In this case, S_1 current reduces to zero. As indicated in Figs. 4 and 5, S_1 turns OFF at $t = t_7$ under ZCS.

Compared with the existing technology [2], [3], [4], the proposed SSCB realizes ZCS in the auxiliary switch, which results in three advantages: 1) mitigate gate-source voltage oscillation on the main and auxiliary switches, 2) eliminate transient power in the auxiliary switch, and 3) reduce the voltage stress on the auxiliary switch. These factors will be clarified in Section III.

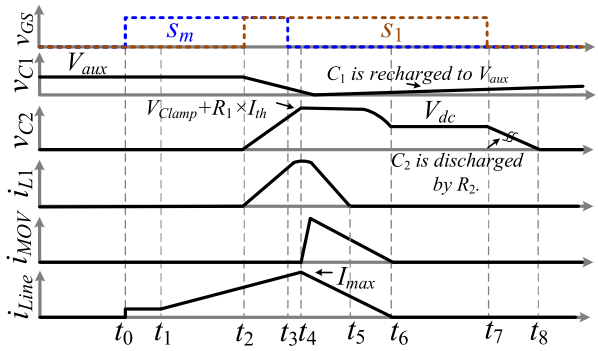

Fig. 6. Conceptual waveform showing C_1, C_2, L_1, and MOV operation.

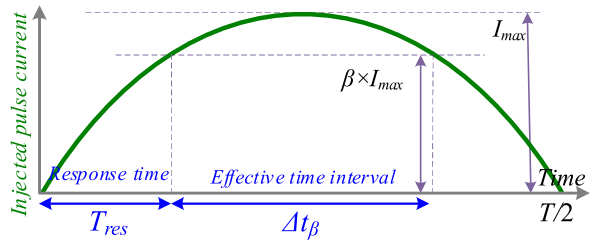

Fig. 7. Conceptual waveform of the generated pulse current by an LCC-AIC.

C. Reliable Operation in C_1, C_2, L_1, and MOV Components

Fig. 6 shows the voltage waveforms of C_1 and C_2, and the current waveforms of L_1, MOV, and the feeder (i_{Line}). v_{C2} reaches V_{Clamp} at $t = t_4$; then, fault current commutates to MOV and begins decaying. Due to the continuity of L_1 current, the freewheeling R_1-D_1 path helps to dissipate L_1 energy during $t_4<t<t_5$. MOV absorbs the inductive energy of the line current during $t_4<t<t_6$ and turns OFF at $t = t_6$, where $i_{MOV} = i_{Line} = 0$. S_1 turns OFF under ZCS at $t = t_7$. Then, voltage exchanges between C_2 and S_1, meaning v_{C2} reduces gradually, and v_{S1} increases. A $t = t_8$, $v_{S1} = V_{aux}+V_{dc}$, $v_{C2} = 0$ and interruption completes. SSCB is ready for re-closing.

D. Design Procedure

Fig. 7 shows the injected pulse current, where T_{res} is the response time of the injected pulse current shown in Fig. 7; Δt_β is the effective time interval in which S_m turns OFF under ZCS; and $0<\beta<1$ is a coefficient. Based on KVL in L_1-C_1-C_2-S_1-S_m:

$$i_{aux}(t) = (V_{aux}/L_1 \cdot \omega_d) \cdot e^{-\alpha t} \cdot \sin(\omega_d \cdot t) \tag{1}$$

where ω_d, ω_0, and α are defined as follows:

$$\begin{aligned} \omega_d &= \sqrt{\omega_0^2 - \alpha^2}, \omega_0 \\ &= 1/\sqrt{L_1 \cdot C_{eq}}, \alpha = R_e/(2 \cdot L_1). \end{aligned} \tag{2}$$

In (2), R_e and C_{eq} are given below

$$R_e \approx R_{on,Sm} + R_{on,S1}, C_{eq} = (C_1 \cdot C_2)/(C_1 + C_2) \tag{3}$$

where $R_{on,Sm}$ and $R_{on,S1}$ are the ON-state resistance of S_m and S_1, respectively. From (1) and Fig. 7, I_{max} and Δt_β can be calculated

$$\begin{aligned} I_{\max} &\approx (V_{aux}/(L_1 \cdot \omega_d)) \cdot e^{-\frac{\alpha \cdot \pi}{2 \cdot \omega_d}}, \Delta t_\beta \\ &= (\pi - 2 \cdot \arcsin(\beta))/\omega_d. \end{aligned} \tag{4}$$

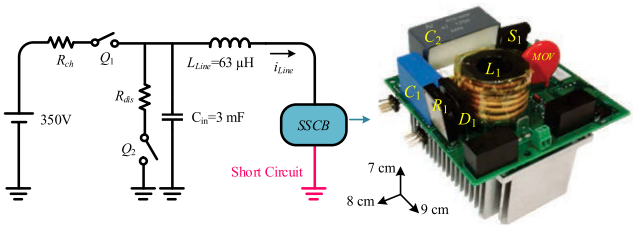

Fig. 8. DC test circuit and the implemented SSCB prototype. S_1 needs no cooling system as its handles pulse currents with duration less than 10 μs.

TABLE I
DC TEST CIRCUIT AND SSCB PROTOTYPE PARAMETERS

Component	Value	Component	Value
V_{dc}	350 V	L_{Line}	63 µH
C_1 (C_2)	1 µF (0.47 µF)	*MOV*	V320LA40BP
L_1	4 µH	D_1	C4D20120D
R_1 (R_2)	1 Ω (1 kΩ)	S_m (S_1)	C3M0016120D

1) L_1 Selection: L_1 time constant in L_1-D_1-R_1 path is designed to be less than the response time of SSCB ($t_{SSCB,res}$). Also, R_1 is minimized to reduce voltage stress on C_2 (V_{Clamp}+($R_1\times I_{th}$)). So, L_1 is found

$$L_1/R_1 < t_{SSCB,res} \Rightarrow L_1 < ((V_{F,\max} \cdot t_{SSCB,res})/I_{th}) \quad (5)$$

where $V_{F,max} = R_1\times I_{th}$, and it is limited to 100 V in this letter.

2) C_1 and C_2 Selection: Δt_β in (4) is reformulated to calculate C_{eq} in (6) below

$$C_{eq} \approx (\Delta t_\beta/(\pi - 2\cdot \arcsin(\beta)))^2 \cdot (1/L_1) \quad (6)$$

where $\omega_0 >> \alpha$ is assumed in (6). C_2 is minimized to optimize SSCB response speed. Regarding Figs. 3, 5, and 6, response time of SSCB is defined from the time SSCB reacts to fault ($t = t_2$) to the instant fault current starts decaying ($t = t_4$). During $t_2 \le t < t_4$, C_2 charges from zero to its peak value (V_{Clamp}+($R_1\times I_{th}$)). By assuming $i_{C2} \approx I_{th}$ during $t_2 \le t < t_4$, C_2 is given as follows:

$$C_2 \le (I_{th} \cdot t_{SSCB,res})/(V_{Clamp} + (R_1 \cdot I_{th})). \quad (7)$$

Then, C_1 can be calculated using (3), (6), and (7).

3) V_{aux} Selection: Given L_1, C_1, C_2, and $I_{max} = I_{th}/\beta$, (4) is rewritten to find V_{aux}

$$V_{aux} \ge ((I_{th}/\beta) \cdot L_1 \cdot \omega_d) \cdot e^{\frac{\alpha\cdot\pi}{2\cdot\omega_d}}. \quad (8)$$

In the proposed LCC-AIC, C_2 is discharged by R_2, so R_2 needs to be minimized. But R_2 generates leakage current (V_{dc}/R_2) in S_1 during $t_5 \le t < t_7$ in Fig. 4. So, a tradeoff should be made in choosing R_2. In this letter, the aim is to limit the leakage current in S_1 to 1 A and the time-constant of $R_2\times C_2$ to 500 μs.

III. EXPERIMENTAL VALIDATION

A. Experimental Results: 350 V/90 A Interruption Test

Fig. 8 shows the test circuit and SSCB prototype. Parameters are listed in Table I. Given $\beta = 0.9$, $\Delta t_{\beta,min} = 1$ μs, $V_{F,max} = 100$ V, and $I_{th} = 80$ A, R_1 is selected as 1 Ω; next, L_1 is chosen as 4 μH using (5). Then, using (3), (6), and (7), C_1 and C_2 are selected as 1 and 0.47 μF, respectively. Finally, V_{aux} is chosen as 350 V using (8). C_1 charging strategy is the same as [2], [3], [4]. Regarding the SSCB parameters (dc rating of C_2 and S_m) and dc system factors (I_{max}, L_{Line}, V_{dc}), V320LA40BP is selected for the MOV.

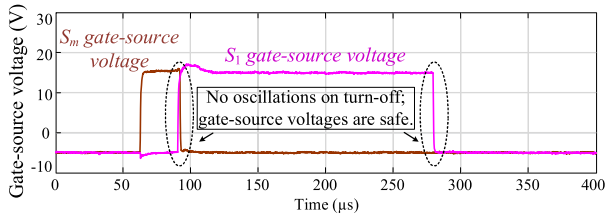

Fig. 9. Experimental results: gate-source voltage waveforms of S_m and S_1.

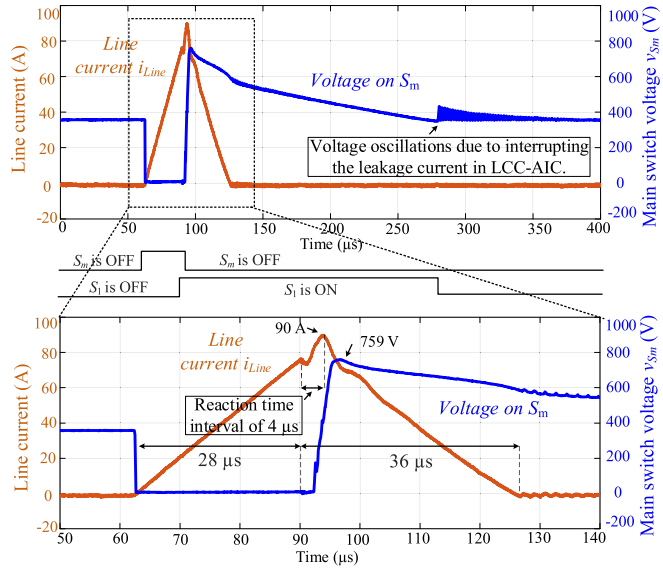

Fig. 10. Experimental results: line current and S_m voltage waveforms.

Fig. 9 shows the gate-source voltage of S_m and S_1 in conducting experiments. As shown in Fig. 9, achieving ZCS in the main and auxiliary switches minimizes the gate voltage oscillations effectively. In addition, Fig. 10 indicates the line current i_{Line}, S_m voltage v_{Sm}, and the auxiliary switch status. S_m turns ON at $t = 62$ μs, and it reaches 78 A within 28 μs. Then, SSCB reacts to fault and begins the interruption by activating LCC-AIC. The SSCB interrupts fault at $t = 126$ μs under ZCS. As shown in Fig. 10, the reaction time interval is 4 μs. The system current i_{Line} reaches the maximum value of 90 A, and it reduces to zero within 36 μs. Also, S_m experiences peak voltage of 759 V, which is safe for the selected 1.2-kV SiC MOSFET.

B. Experimental Results: ZCS Operation of S_m

Fig. 11 shows the main switch S_m current and voltage waveform, which is consistent with Section II-A and Fig. 3. S_m peak current reaches 81.6 A, and it reduces to zero within 2 μs, meaning $i_{Sm} = 0$ at $t = 92$ μs. Then, S_m turns OFF. When S_m voltage begins rising, the current in S_m is already zero, which verifies the ZCS operation. For the same fault current values, 25 kW and 1 kW power shock appears on S_m in MOV and MOV-RCD-based SSCBs, respectively [2]; while the presented SSCB obtains zero transient power. It also illustrates that the voltage rising rate across S_m is limited to $dv_{Sm}/dt = 0.25$ kV/μs.

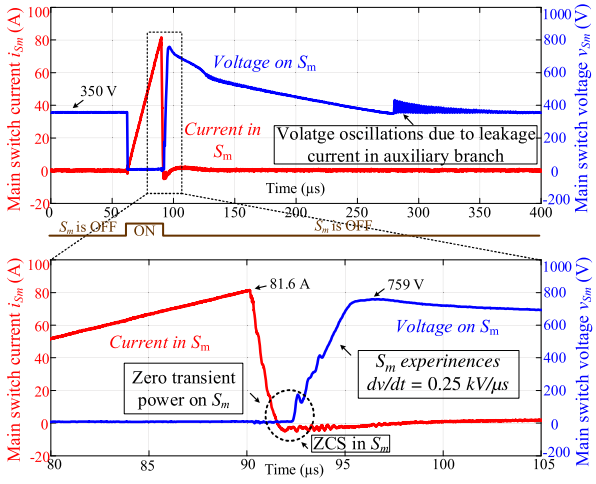

Fig. 11. Experimental results: S_m current and voltage waveforms showing ZCS.

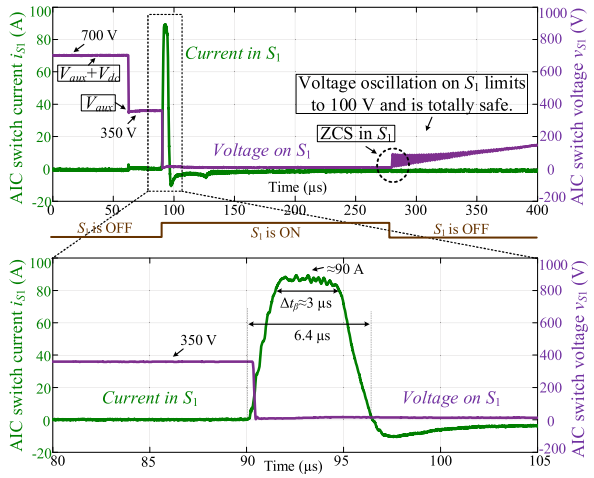

Fig. 12. Experimental results: S_1 current and voltage waveforms showing ZCS.

C. Experimental Results: ZCS Operation of S_1

Fig. 12 shows the auxiliary switch S_1 current and voltage waveform to validate the ZCS operation, following Section II-B and Fig. 5. The injected pulse current peak value reaches 90 A within 2 μs; the effective time interval is $\Delta t_\beta = 3$ μs, and S_1 current reduces to zero within 4.4 μs.

The peak voltage on S_1 is $V_{aux}+V_{dc} = 700$ V when S_m and S_1 are OFF (before $t = 62$ μs). By turning S_m ON at $t = 62$ μs, the voltage on S_1 reduces to $v_{S1} = V_{aux} = 350$ V. Finally, S_1 voltage reduces to zero as S_1 turns ON to generate the countercurrent pulse into S_m. It clearly shows that S_1 turns OFF when its current reduces to zero, verifying the expected ZCS operation.

D. Experimental Results: Transient Current Commutation

Fig. 13 shows the current commutation process among S_m, L_1, and MOV, which is critical to illustrate the ZCS operation and is summarized below.

1) By activating LCC-AIC, S_m current starts reducing, and L_1 current increases at the same time. The peak of current in S_m and L_1 reaches 81.6 A and 87 A, respectively.

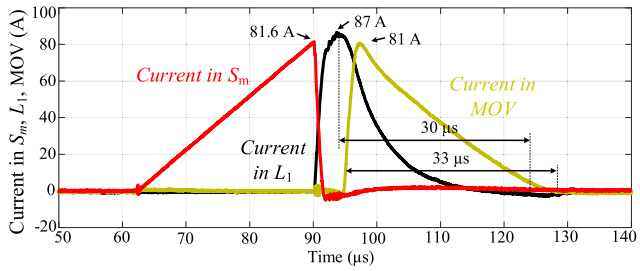

Fig. 13. Experimental results: S_m, L_1, and MOV current commutation process.

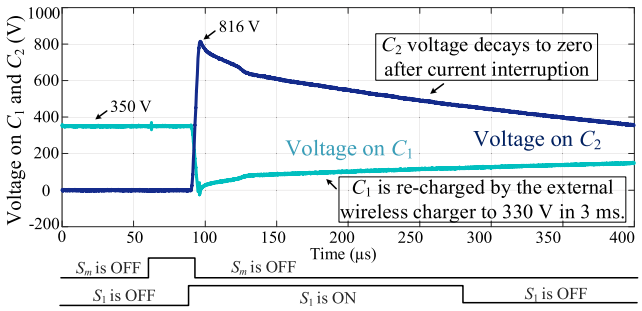

Fig. 14. Experimental results: C_1 and C_2 charge and discharge process.

2) Regarding Fig. 4, after commutating fault current from the LCC-AIC branch to MOV, L_1 current continues in a freewheeling path of D_1-R_1 and reduces to zero within 30 μs.
3) The MOV dissipates the stored inductive energy in L_{Line}; the duration process of MOV current lasts for 33 μs. This period depends on multiple parameters: V_{Clamp}, V_{dc}, L_{Line}, and the maximum fault current I_{max} aimed to be interrupted in the dc system.
4) The current commutation sequence is $S_m \rightarrow S_1 \rightarrow$MOV, which is in a good match with the line current waveform in Fig. 10, meaning that $i_{Line} = i_{Sm}+i_{S1}+i_{MOV}$ is valid.
5) The line current and S_m current waveforms need to be the same during 62 μs$<t<$90 μs. However, the maximum values have a small difference of 2 A, which is mainly caused by the measurement offset in the Rogowski current probes.

E. Experimental Results: C_1 and C_2 Charge/Discharge Process

Fig. 14 indicates the voltage waveforms of the precharge capacitor C_1 and the coupling capacitor C_2. The voltage on C_1 is the dc bus voltage 350 V before turning ON S_1. During current injection (S_1 turns ON), C_1 discharges to zero, and it can be recharged by an external charger. The external charger circuit design can follow the same procedure in [2]. With respect to the voltage on C_2, its peak value reaches 816 V. Refer to SSCB prototype in Fig. 8, the voltage ratings of the selected capacitors C_1 and C_2 are 1 kV and 1.25 kV, respectively, and their operation is safe during the dc current interruption.

F. Comparative Study

To highlight the effectiveness of the proposed SSCB, a comparison with SSCBs is presented in Table II. Compared with the 380 V/80 A LC-AIC SSCB reported in [2] and the capacitive couple-based AIC presented in [3], [4], and [16], the proposed LCC-AIC SSCB can realize

TABLE II
COMPARATIVE STUDY WITH OTHER TECHNOLOGIES IN SSCBS

SSCB	Proposed	[2]	[3],[4],[16]	[5]	[6]	[7]	[8]	[9]	[10]
Technology	Soft Turn-off	Soft Turn-off	Soft Turn-off	Complementary Commutation	Active Resonant	Load Commutation	Coupled-Inductors	Z-Source Breakers	Γ-Source Breaker
Type of Switch	SiC MOSFET	SiC MOSFET	SiC MOSFET	Thyristor	Thyristor	Thyristor	Thyristor	Thyristor	Thyristor
V_{dc}/I_{th}	350V/90A	380V/80A	4kV/100A	150V(24.5A)	380V(13A)	600V(55A)	28A(N/A)	35V(14A)	100V(70A)
Autonomous(1)	×	×	×	×	×	×	✓	✓	✓
Manual Trip(2)	✓	✓	✓	✓	✓	✓	×	×	×
Fully ZCS	✓	×	×	✓	✓	×	✓	✓	✓
Power Density(3)	7kW/L	1.2kW/L	1.3kW/L	N/A	N/A	N/A	N/A	N/A	N/A
Reaction Time(4)	4 μs	9.4 μs	77 μs	203 μs	280 μs	150 μs	50 μs	75 μs	160 μs

(1) SSCB can autonomously react to fault, and it needs no circuit detection; (2) SSCB can isolate overloads; (3) (Power Density $= \frac{DC\ Bus\ Voltage \times Current\ Rating}{Metric\ Volume}$); for the proposed SSCB and the SSCB in [2], current rating=10 A, and the current rating in [3] and [4] has been considered as 100 A; it is noted that the injection capacitor chargers are not involved in calculating the power density; dimensions of the charger used for the proposed SSCB is about 10cm×10cm×5cm; (4) it is defined from the time SSCB reacts to fault to the time instance the line current starts decaying in the system.

complete ZCS with faster response speed and a higher power density. Introducing LCC-AIC, minimizing C_1, C_2, and L_1, maximizing V_{aux}, and allowing C_1 to be completely discharged during pulse current injection stand for the faster response speed of the proposed SSCB.

Compared with the soft turn-OFF SSCBs in [2], [3], and [4], achieving ZCS for the auxiliary switch helps to reduce the voltage stress on the auxiliary switch to $V_{dc}+V_{aux}$. For example, regarding the SSCB prototype reported in [2] (with the dc bus voltage of $V_{dc} = 380$ V and the precharge voltage on the injection capacitor as $V_{aux} = 105$ V), the proposed SSCB can reduce the voltage peak on the auxiliary switch from 980 to 485 V ($V_{dc}+V_{aux} = 485$ V).

In comparison with thyristor-based SSCBs with the technology of complementary commutation, active resonant, load commutation switch, coupled-inductors, Z-source, and Γ-source, the proposed SSCB presents a fast response speed. It shows that the proposed LCC-AIC has the capability to further extend the state-of-the-art technology.

Regarding SSCBs with hard-switching operation [11], [12], [13], [14], [15], SSCBs with half-controlled switches [5], [6], [7], [8], [9], [10], mechanical breakers [17], and hybrid breakers [18], the proposed SSCB benefits from a higher reliability and an extended lifetime. However, the presented design increases the cost due to the added injection circuit, which highlights more future research work in this field.

IV. CONCLUSION

A fully soft-switched SSCB is presented with a novel LCC-AIC branch. It achieves a complete ZCS to enhance the SSCB reliability by eliminating the transient power on switches during turn-OFF. To verify the effectiveness of the SSCB, experiments of 350 V/90 A prototype have been conducted. The results show zero transient power on main and auxiliary switches during current interruption. To achieve ZCS in main switch, injected pulse current reaches 90 A within 2 μs, where it gets a safe effective time interval of 3 μs. The reaction time interval of the breaker is limited to 4 μs; where main and auxiliary switches experience the peak voltage of 759 and 700 V, respectively. The line current reduces from 90 A to zero within 36 μs under the line inductance of 63 μH. As the SSCB reacts to fault, the fault current commutates from S_m to S_1, and finally to MOV. The proposed AIC is simply controlled by a time-sequence process.

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