Communicationless Phase Cooperative Control of Inductive Power Transfer Using Asymmetrical Modulations

Julius Maximilian Placzek, Hamzeh Beiranvand, *Member, IEEE*, and Marco Liserre, *Fellow, IEEE*

***Abstract*—The dual-side control (DSC) of inductive power transfer (IPT) generally requires communication between the system sides to coordinate the local controllers. For the reduction of component count and operation in challenging environments, such as underwater, communicationless DSC is beneficial. This article investigates if and how asymmetric modulations, known for their improved performance in IPT, can be applied to phase cooperative communicationless DSC. A per side separate steady-state model is derived, and the selection criteria for modulation schemes to be suitable for phase cooperative control are determined. The crucial importance of bijective or unique phase behavior in modulations for this control scheme is identified and demonstrated. In comparison with phase modulation, it is shown that the asymmetric voltage cancelation of full-bridges is not reliably applicable to phase cooperative DSC, but the asymmetrical modulation of half-bridges is. Therefore, a phase cooperative half-bridge DSC system as a simplified low-complexity DSC scheme is further investigated, and the load step regulation boundary is derived. Analysis is verified in experiment and simulation, demonstrating zero-voltage-switching behavior, dynamic load step regulation, the impact of harmonics on magnetics losses for high coupling, and the impact of variable voltage ratio.**

***Index Terms*—Asymmetric voltage cancelation (AVC), communicationless control, dual-side control (DSC), inductive power transfer (IPT), phase cooperative control, triple phase-shift (TPS) control.**

I. Introduction

INDUCTIVE power transfer (IPT) is a solution for supplying power to consumer products, electric vehicles, etc. [1] and an enabler in demanding niches such as biomedical implants [2] and underwater applications [3].

Many control strategies for IPT systems have been proposed to deal with variable load and coupling without a hardwired feedback path. Primary-side controllers (PSCs) control power flow from the sourcing converter and require a means to close the feedback loop, typically using added communication, i.e., radio frequency (RF) [4], [5], [6], [7] or simultaneous wireless information and power transfer via modulation of the main power flow as prominently used in the ubiquitous Qi standard [8], [9]. Since this communication is time critical toward output control in a pure PSC, it has been proposed to avoid communication, i.e., by the estimation of system quantities [10], [11], [12], [13], [14] at significant complexity or by the use of resonant circuits featuring highly coupling and load-invariant transfer functions [3], [15], [16] at the cost of precision voltage regulation.

Secondary-side controllers (SSCs) avoid the feedback issue altogether by controlling the system from the receiver side with the local converter employing conventional control [17], [18], [19]. PSC and SSC IPT, however, lose efficiency due to asymmetric currents when load and coupling conditions differ from the nominal design point. This increases not only system losses but also cost for the required larger dimensioning of system components [20], [21], [22], [23], [24]. The SSC can be improved by utilizing information about the input power for efficiency optimization, which introduces wireless communication but without any requirements on latency [25]. Likewise, the conventional PSC can be optimized by using more control parameters; variable-frequency phase-shift control adds the frequency [26], but additional communication remains.

The most common solution for the issues of PSC/SSC is dual-side control (DSC), utilizing either additional dc–dc converter stages [21], [22] or dual active (DA) operation: direct modulation of dc–ac converters on both system sides, which has recently seen significant research because it avoids additional conversion stages while providing the symmetric hardware necessary for synchronous rectification and bidirectional power transfer [1], [20], [23], [24], [27], [28], [29], [30], [31], [32], [33], [34], [35]. Common DA schemes operate from the principles of two phase-shifted full-bridges and their derivatives: dual phase shift changes only two voltage magnitudes via the inner phase shifts of the converters [1], [20], [24], [33] to maximize power factor without regard for switching event placement. Triple-phase-shift (TPS) control additionally uses the angle between the converters [23], [28], [34], [35] to control soft switching at the cost of reduced power factor; Jiang et al. [34] provide a deep optimization and zero-voltage switching (ZVS) investigation for the TPS group of strategies. Asymmetric voltage cancelation (AVC) instead of phase shift modulation (PSM) can be used to implement an equivalent of the TPS technique with improved

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The authors are with the Institute of Electrical Engineering, Kiel University, 24118 Kiel, Germany (e-mail: jmpl@tf.uni-kiel.de; hab@tf.uni-kiel.de; ml@tf.uni-kiel.de).

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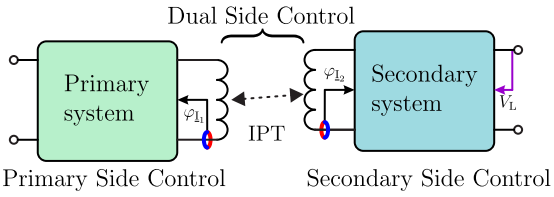

Fig. 1. Phase cooperative IPT system: DSC is achieved with each side exerting local control without additional communication.

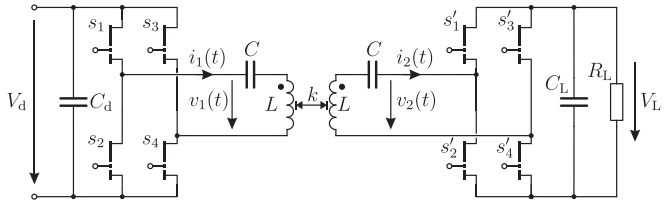

Fig. 2. Topology with two actively controlled full-bridge converters, in this example using GaN high-electron-mobility transistors (HEMTs).

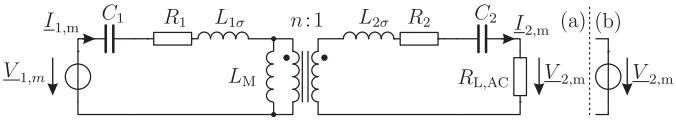

Fig. 3. AC equivalent circuit of an S/S compensated IPT system with (a) a load resistor model and (b) a load voltage source model; m denotes harmonic order.

efficiency due to improved power factor and soft switching [1]. AVC-based DSC can be further improved at very light loads under 20% by utilizing the second-order harmonics of AVC with halved switching frequency [31]. Variable-frequency TPS control adds the frequency as a fourth degree of freedom [29] to achieve the further compensation of system variations. Furthermore, DSC can be implemented using pulse density modulation [32] or a simplified converter half/full-bridge mode switching operation [30] instead of some type of quasi-periodic pulsewidth modulation (PWM), thereby reducing the number of switching events and avoiding hard-switched transitions.

Since DSC schemes reintroduce PSC, additional communication [1], [20], [21], [22], [24], [27], [28], [29], [30], [31], [34] is again widely used. In [35], sensing magnetics are used for power factor control, but communication is still required for output control because the order of DSC control loop priorities is reversed. Hence, the so-called communicationless DSC strategies have been proposed, which exploit existing system properties for DSC. Aside from a general reduction in component count, a further benefit can be identified: enabling DSC in environments such as human tissue and saltwater, which are more challenging for RF communication [2] than for IPT [3]. One common solution are perturb and observe type algorithms, also called maximum efficiency point tracking (MEPT), where the PSC probes the reaction of the SSC by attempting to reach minimum input power [9], [32], [36]. Alternatively, a phase cooperative method has been proposed, in which interaction between local control of phase and magnitude on both system sides [23], as visualized in Fig. 1, leads to the communicationless TPS control of the whole system; however, in [23], many questions about implementation, static behavior for other values of k, usage of different modulations, and dynamic behavior of the strategy remain unanswered.

This article begins with an implementation-centric analysis of phase cooperative DSC for arbitrary modulation schemes with all variables separated per system side. The analysis is used to find the selection criteria for modulation schemes that can function with phase cooperative control. These criteria are applied to the use of AVC in the version extended by half-bridge operation (AVCHB) in an effort to combine improved efficiency with communicationless control. It is shown in theory, simulation, and experiment that phase cooperative DSC is inherently incompatible with the AVC part of AVCHB modulation, the full-bridge mode, due to nonunique repeating phase behavior. Simply put, the controllers can find erroneous operating points. Conversely, the half-bridge (HB) range of AVCHB is viable and, therefore, the HB in general. From this result, a simplified HB-based system is designed and further analyzed for load step behavior. A regulation boundary condition of the two-loop control system is derived, and the regulation behavior is demonstrated in simulation and experiment. Partial ZVS operation at the most challenging borders of the operating range is demonstrated. Operation with variable output voltage equivalent to a typical battery charging process is demonstrated. This article concludes with a summary of the results on phase cooperative control and a short comparison to general DSC and MEPT schemes.

II. Cooperative DSC Theory

While other topologies, such as LCL [21], [28], have been used for DSC, the series/series (S/S) compensated topology has been the focus of direct DSC research due to its simplicity, coupling-invariant resonant frequency, and gyrator-type behavior; hence, it is retained for this work [1], [20], [22], [23], [24], [27], [29], [34], [35]. GaN is used in this article, resulting in the topology of Fig. 2. Instead of a resistive load model, it is modeled with two voltage sources as per Fig. 3(b) [29]. Considering equal transfer coils with a winding ratio of $n = 1$ with the coupling k, the model simplifies to $L_1 = L_2 = L$ with $L_{\sigma 1/2} = L_\sigma = (1-k)L$ and $L_\mathrm{M} = kL$. For power flow only, the fundamental component $m = 1$ at

$$\omega_1 = \frac{1}{\sqrt{(L_\sigma + L_\mathrm{M})C}} = \frac{1}{\sqrt{L(k+(1-k))C}} = \frac{1}{\sqrt{LC}} \quad (1)$$

corresponding to the constant current (CC) mode of S/S IPT is considered. In addition, disregarding the loss resistances, the simplified equivalent circuit can then be resolved to obtain the secondary and primary currents [1], [37]; the second suffix of $\underline{X}_{x,1}$ denotes fundamental order, the underline a complex value:

$$\underline{I}_{2,1} = j\frac{\underline{V}_{1,1}}{\omega_1 L_\mathrm{M}} = j\frac{\underline{V}_{1,1}}{\omega_1 kL} \quad (2)$$

$$\underline{I}_{1,1} = \underline{V}_{2,1}\frac{-j}{\omega_1 kL}. \quad (3)$$

The magnitudes of these quantities are dependent on coupling k, which is unknown to the controller without a dedicated estimator. The phase relationship, however, is fully decoupled from system variables and converts the voltage phase of one side to the current phase of the other side with a shift of 90°. For the utilization of this phase relationship, no further definitions have to be made for the primary, because all the primary-side phase angles are defined as referenced to zero.

With the RMS value $V_{1,1}$ and the voltage angle $\varphi_{(\underline{V}_{1,1})}$ as a function of the modulation scheme used in the primary converter, the secondary current will be

$$\underline{I}_{2,1} = j\frac{\underline{V}_{1,1}}{\omega_1 L_{\mathrm{M}}} = j\frac{\underline{V}_{1,1}}{\omega_1 kL} = V_{1,1}\frac{1}{\omega_1 kL}\angle\underline{\varphi_{(\underline{V}_{1,1})} + \frac{\pi}{2}}. \quad (4)$$

The secondary-side reference angle is, in turn, locked to the secondary current, i.e., by a phase-locked loop (PLL) to facilitate synchronous operation

$$\varphi_{\underline{I}_{2,1}} = \varphi_{PLL} = \varphi_{(\underline{V}_{1,1})} + \frac{\pi}{2}. \quad (5)$$

Hence, the phase angles of secondary quantities can be given as angle differences to the secondary current fundamental

$$\varphi_{(x,\underline{I}_{2,1})} = \varphi_{(x)} - \varphi_{(\underline{I}_{2,1})}. \quad (6)$$

The secondary fundamental voltage generated by the synchronized converter operating as a rectifier is then determined by the PLL angle (5) and the additional angular component $\varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}$ introduced by the secondary-side modulation scheme

$$\underline{V}_{2,1} = V_{2,1}\angle\underline{\varphi_{(\underline{V}_{1,1})} + \frac{\pi}{2} + \varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}}. \quad (7)$$

With the inherent phase shifts of the system canceling out this yields a primary current of:

$$\underline{I}_{1,1} = V_{2,1}\frac{1}{\omega_1 kL}\angle\underline{\varphi_{(\underline{V}_{1,1})} + \varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}}. \quad (8)$$

The primary current phase angle is the sum of the phase angles introduced by the modulation formats of both VSCs. Power transferred to the secondary-side dc link can then be calculated with the conjugate current, and it can be shown that due to the PLL action synchronizing to the primary, only the phase angle introduced by the secondary side has an impact on power flow

$$P = V_{1,1}V_{2,1}\frac{1}{\omega_1 kL}\cos(\varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}). \quad (9)$$

Power flow can, therefore, be controlled in three different ways:

1) by control of the primary RMS voltage $V_{1,1}$;
2) by control of the secondary RMS voltage $V_{2,1}$;
3) by control of the secondary phase angle $\varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}$.

To identify the impact of these options, the corresponding losses are estimated from the lossless assumption using the equivalent system resistance $R_{1,1} = R_{2,1} = R$ for the simplified symmetric system at the fundamental frequency to represent linear losses

$$P_{\mathrm{Loss},1} \approx I_{1,1}^2 R = \left(\frac{V_{2,1}}{\omega_1 kL}\right)^2 R \quad (10)$$

$$P_{\mathrm{Loss},2} \approx I_{2,1}^2 R = \left(\frac{V_{1,1}}{\omega_1 kL}\right)^2 R. \quad (11)$$

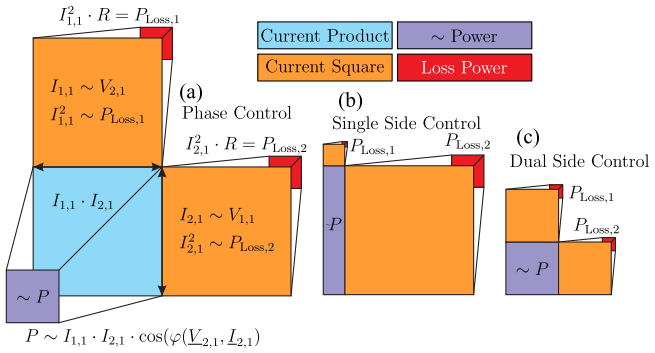

Fig. 4. Power loss and transfer diagrams for the different cases. From left to right: (a) phase control, (b) magnitude SSC, and (c) magnitude DSC for the same reduction of power.

The results of (9)–(11) are visualized in Fig. 4. The diagrams are normalized and show a typical case for low coupling coefficients k and light loads, necessitating a large reduction in output power from the nominal, which has to be designed for maximum k due to the $P \sim 1/k$ relationship per (9). DSC is basically just the common problem of minimizing the circumference while maximizing the area of a rectangle. Losses are proportional to the square currents (or voltages) scaled by resistance; useful power is proportional to the product of the two currents (or voltages) scaled by the power factor of the receiver. Only DSC of magnitudes in Fig. 4(c) yields the optimal condition; current asymmetry or nonunity power factors of the receiver reduce baseline efficiency. In practice, tradeoffs with soft switching, control, and modulation have to be considered, as discussed in the next section.

III. Modulations

In terms of modulation schemes, the TPS control based on PSM [23] is taken as a baseline, and the AVC scheme [1], [38] is compared. A modulation coefficient $0 \leq M \leq 1$ is defined to normalize the behavior of various modulations in one framework. The optimal case of the AVC strategy can be extended to zero output by driving one HB with static conduction for modulation indexes $M \leq 0.5$ [38], which makes the converter functionally and mathematically an HB. This combined scheme is here dubbed AVCHB with this distinct notation adopted because the HB range used at partial loading exhibits fundamentally different phase behavior for the purposes of cooperative IPT control.

Assuming that a maximum of switching events shall be aligned to zero current transitions, up to three for AVCHB and two for PSM in the fashion of TPS control, both these techniques can be implemented in two symmetric cases, as summarized in Fig. 5. These modulation processes shift the distribution of voltage time to a leading or lagging position in the interval, resulting in a phase shift that cannot be avoided while retaining switching event placement. The RMS magnitude and phase behavior of the fundamental components can be calculated by a Fourier series of the form $v(t) = a_0 + \sum a_{\mathrm{m}}\cos(m\omega_1 t) + b_{\mathrm{m}}\sin(m\omega_1 t)$ with

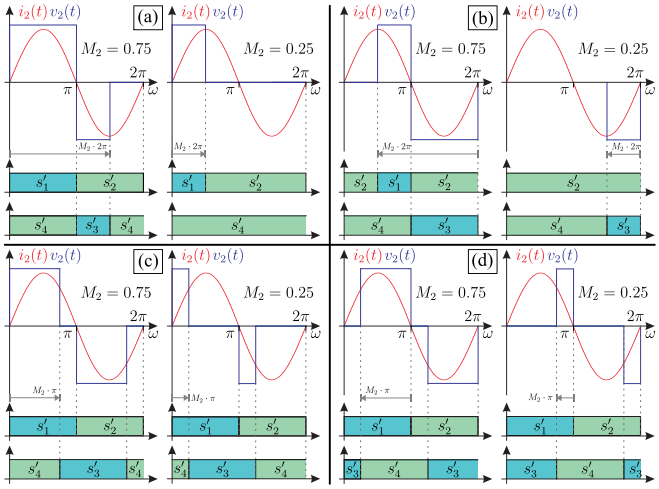

Fig. 5. Waveforms and switching patterns of (a) leading and (b) lagging AVCHB and (c) leading and (d) lagging PSM as applied to synchronous rectification in the secondary side.

the angle respective to the reference period in Fig. 5 found as

$$\varphi_m = -\arctan\left(\frac{b_m}{a_m}\right) - \pi/2 \tag{12}$$

yielding the phase angle between the fundamental voltage and the current $\varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}$ in the secondary side and the absolute phase angle $\varphi_{(\underline{V}_{1,1})}$ versus the primary PWM generation process. For leading PSM, the following relationships are obtained:

$$\frac{V_{\mathrm{PSM},1}}{V_\mathrm{L}} = \frac{4}{\pi\sqrt{2}}\cos\left(\frac{\pi - \pi\cdot M}{2}\right) \tag{13}$$

$$\varphi_{(\underline{V}_{\mathrm{PSM},1})} = \frac{\pi - \pi\cdot M}{2}. \tag{14}$$

For leading AVCHB, two cases are calculated separately, in the AVC range for $M > 0.5$:

$$\frac{V_{\mathrm{AVC},1}}{V_\mathrm{L}} = \frac{\sqrt{10 + 6\cos(\pi - \pi\cdot M)}}{\pi\sqrt{2}} \tag{15}$$

$$\varphi_{(\underline{V}_{\mathrm{AVC},1})} = \arctan\left(\frac{\sin(\pi - \pi\cdot M)}{3 + \cos(\pi - \pi\cdot M)}\right). \tag{16}$$

And for the HB range, which is equivalent to regular PWM of an HB converter for $M \le 0.5$:

$$\frac{V_{\mathrm{HB},1}}{V_\mathrm{L}} = \frac{2}{\pi\sqrt{2}}\cos\left(\frac{\pi - \pi\cdot 2\,M}{2}\right) \tag{17}$$

$$\varphi_{(\underline{V}_{\mathrm{HB},1})} = \frac{\pi - \pi\cdot 2\,M}{2}. \tag{18}$$

The HB range exhibits entirely different behavior. The phase is linear; it behaves like PSM with half-magnitude and different normalization of M. There is no qualitative difference between PSM, the HB range of AVCHB, and an HB with PWM. The lagging versions exhibit the same magnitude behavior but inverse phase shift. The behavior of the fundamental components

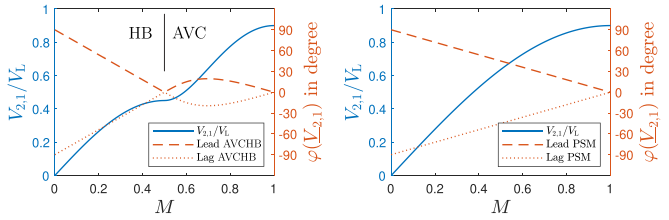

Fig. 6. Ratio of output fundamental RMS voltage to dc-link voltage and absolute phase angle of the voltage relative to the secondary current, hence PLL, for the modulations in Fig. 5.

is summarized in Fig. 6. Reconsidering the current equation (8)

$$\underline{I}_{1,1} = V_{2,1}\frac{1}{\omega_1 kL}\underline{/\varphi_{(\underline{V}_{1,1})} + \varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}} \tag{19}$$

it becomes apparent that if the modulations used by primary and secondary are of inverse phase, the primary current will also be in phase with the switching events; the modulation phases cancel out. Returning to DSC and the requirement for equal magnitudes to minimize I^2R losses, the following conditions for modulation selection can then be formulated.

1) Both the converters need to incur the same reduction in output voltage magnitude for a value of M.
2) Both the converters need to incur the same absolute phase for any given modulation index M.
3) The sign of the phase change needs to be inverse between system sides.
4) Variable input and output dc voltages can introduce current imbalance; this cannot be avoided by this scheme (fixed ratios can be covered by transformer winding ratio n, which is neglected here). The same holds true for other parameter imbalances.

Of these points, 4) is a genuine limitation, but for smaller variations, the additional losses from (10) and (11) are small.

As a side effect, some phase control and, hence, efficiency reduction are introduced, which cannot be avoided without placing the switching events away from current zero transitions as done in [20] or using dc–dc converter stages. The influence of the phase term is, however, much reduced versus SSC (i.e., $M_1 = 1$, fixed) because the covariation of $M_1 = M_2$ means that M_2 can remain significantly larger for the same P in (9); hence, the phase angle between the sides is lower. AVCHB is also better than PSM in this regard, since the absolute phase remains much smaller in the midrange $0.3 \le M \le 0.7$.

Furthermore, a closed-loop dual-side controller for the system can be designed using the phase behavior. Let the primary be operating at M_1; the secondary controller can locally alter M_2 to regulate the load, thereby altering the value of $\varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})}$, hence $\varphi_{(\underline{I}_{1,1})}$. If the primary converter now controls its modulation M_1 locally to fulfill the following steady-state equation:

$$\varphi_{(\underline{I}_{1,1})} \stackrel{!}{=} 0 = \varphi_{(\underline{V}_{1,1})} + \varphi_{(\underline{V}_{2,1},\underline{I}_{2,1})} \Leftrightarrow M_1 = M_2 \tag{20}$$

in a slowly varying way, the SSC tuned to be orders of magnitude faster will respond by tracking M_2 with only a small dynamic error in output power. This solution will then self-converge to the condition $M_1 = M_2$ because $\varphi_{(\underline{I}_{1,1})}$ is proportional to

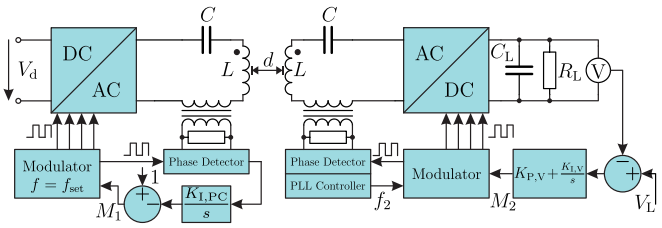

Fig. 7. Control structure for voltage control of ohmic load via DSC. The +1 offset in the primary controller visualizes the idea of fulfilling the equation by starting from maximum power transfer capability.

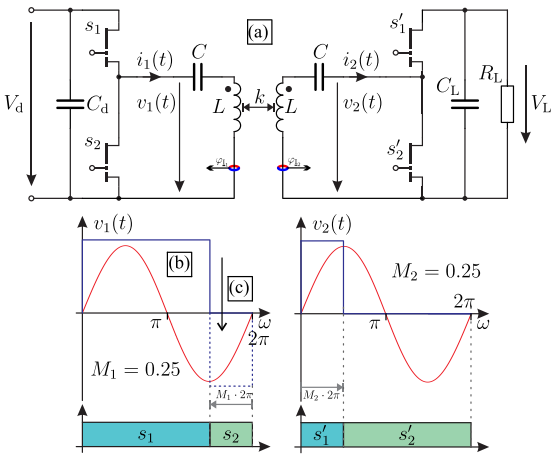

Fig. 8. HB-based communicationless DSC system proposed as result of the investigation. (a) shows how the current sensors are no longer floating, making realization potentially lower cost. Considering the waveforms for DSC, (b) and (c) show how due to the presence of a series capacitor, the DC offset of the waveform is arbitrary and the pulse (b) in fact realizes the desired pulse (c).

the required change of M_1, and the sign/direction of required adjustment need not be searched as in MEPT, which has been shown as slow, i.e., on the second scale in some literature [36]. DSC is achieved with only local control based on phase measurement, hence phase cooperative DSC. This convergence, however, requires one further condition.

5) The phase behavior of the modulations shall be bijective, i.e., unique. A specific phase angle shall be associated with only one modulation index.

While PSM offers linear phase per Fig. 6, the behavior of AVCHB is not unique and has three regions with equal phase angles at different modulation indexes; hence, the process can converge on unwanted asymmetric magnitude conditions while still fulfilling the phase condition (20). While AVCHB provides superior results in communication-based DSC [1], it is not applicable to phase cooperative DSC. Another interesting scheme is asymmetric duty-cycle modulation. It is skipped for further analysis here, as its fundamental frequency behavior is equivalent to PSM and HB modes [38].

This negative result for AVC, however, leads to a secondary positive result: the HB range by itself has simple linear phase. Since there is no mathematical difference, this control strategy is, therefore, also suitable for HB-converter-based IPT systems. The proposed system and the switching pulses used to realize DSC are shown in Fig. 8. It should be noted that unlike full-bridge-based schemes, the current sensor is not floating but on 0-V potential. Although not exploited in this article, a simple shunt sensor can then be used, offering potential reductions of system cost. Since the limitation to the HB mode effectively constitutes a reduction of power capability to $1/4$ for constant tank circuit design, larger load resistances are considered for this circuit in theory and experiment to retain comparable parameters elsewhere.

The precise lagging/leading of the secondary current around the switching event for the desired soft-switching behavior can easily be controlled in the secondary side by introducing a small offset $\varphi_{\text{offset},2}$ to the PLL set point. The primary can use an offset $\varphi_{\text{offset},1}$ to the set point of $\varphi_{(\underline{V}_{1,1})} \sim M_1$ to achieve the same at the cost of minor current imbalance. In this communicationless controller, the third phase angle of the TPS strategy designated for switching event alignment is decomposed into locally controlled phase angles, which together implement equivalent functionality. An in-depth study of ZVS ranges and determining the optimal angle set points depending on operating conditions in AVC and PSM can be found in [1] and [34]. This article concerns itself with enforcing known angles by cooperative control.

A system-level implementation for ohmic load is shown in Fig. 7; two current sensors and one voltage sensor for the output are required. The load can be controlled by a proportional–integral controller. Owing to the comparatively slow dc-link time constant, resonant tank dynamics are neglected here. For the primary symmetrizing controller, a pure integral controller tuned to not interact with the voltage controller can be used. Further information on the PLL is given in the experimental section, since its operation is closely tied to the properties of the hardware.

IV. Regulation Boundary

In summary, the phase cooperative strategy behaves similarly in time to an MEPT controller; the secondary is controlled by a fast controller and the primary by a slower controller that optimizes system efficiency. As an advantage over MEPT, no extra dc input power measurement is needed, while the resonant current sensor is already required for overcurrent protection in the case of operation outside design parameters, i.e., with no or a defective secondary. The interaction of a slow loop with a fast loop, however, has an impact on the ability to regulate step changes of the load resistance. Here, three important cases based on the steady-state load resistance R_L preceding the load step event can be distinguished.

1) Load resistance increases are always well regulated since the SSC retains full output control.
2) Load resistance decreases remaining above a certain boundary $R_{\text{Lmin}}(R_L)$ are equally well regulated since the SSC has enough resonant current available.
3) Load resistance decreases below $R_{\text{Lmin}}(R_L)$ have to wait for the slower primary controller to increase resonant current sufficiently before regulation is achieved.

The regulation boundary can be derived using the average rectified load current I_{RL}. For the HB-based solution operating

TABLE I
PARAMETERS OF EXPERIMENTS AND SIMULATIONS

Parameter	Value
$V_\mathrm{d} = V_\mathrm{L}$	48 V
P_N	500 W
R_L PSM/AVCHB	4.6–23 Ω (Factor 5 variation)
R_L HB	18–70 Ω (Factor 3.8 variation)
$D_\mathrm{Winding}/D_\mathrm{+Ferrite}$	19 cm / 21 cm
k	0.6–0.3 (Factor 2 Variation)
$L_{1/2}$	16.9–19.1 µH
f_s	52.5 kHz
$C_{1/2}$	504 nF
Power Device	GS 61008T

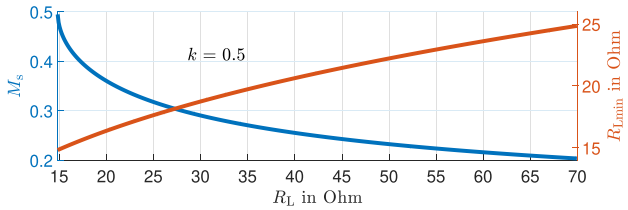

Fig. 9. Dependence of regulation boundary resistance R_Lmin on previous steady-state conditions R_L and M_s for $k = 0.5$ of the HB system in Fig. 8.

at the steady-state symmetric modulation index $0 \leq M_\mathrm{s} \leq 0.5$:

$$I_\mathrm{RL} = \frac{I_{2,1}}{\sqrt{2}\pi}(1 - \cos(2\pi M_\mathrm{s})) = \frac{V_\mathrm{L}}{R_\mathrm{L}} \tag{21}$$

which can be combined with the secondary resonant current equation (4) and HB converter RMS voltage (17) for $V_\mathrm{L} = V_\mathrm{d}$ to obtain M_s, as follows:

$$M_\mathrm{s} = \arcsin\left(\sqrt[3]{\frac{\pi^2 \omega_1 kL}{2R_\mathrm{L}}}\right). \tag{22}$$

The result can be combined with (4) and (17) again

$$R_\mathrm{Lmin} = \frac{\pi^2 \omega_1 kL}{2\cos\left(\frac{\pi - 2\pi M_\mathrm{s}}{2}\right)}. \tag{23}$$

Computing this for the system parameters of Table I leads to the results shown in Fig. 9; for light loads, there is a large regulation reserve because only a fraction of $I_{2,1}$ is utilized; this progressively decreases with larger loads toward values that can only be regulated in steady state.

Coincidentally, this type of limitation cannot be unique to the phase cooperative control scheme and must also apply to any system using the S/S topology with a slower primary controller or high latency communication, such as the communicationless MEPT search methods in [9], [32], and [36].

V. SYSTEM PARAMETERS AND SIMULATION

Simulation and experiment are parameterized for a set of transfer coils, the electrical properties of which are shown in Fig. 10. The switching frequency for practical operation is selected as the average of maximum/minimum resonant frequencies resultant from the slight variation of L with k to distribute

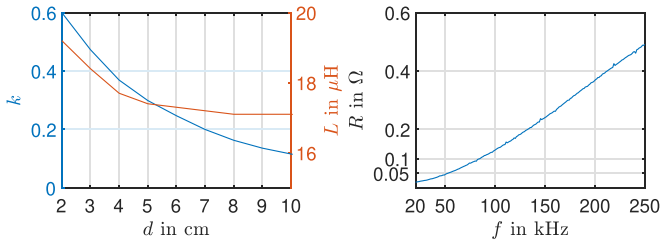

Fig. 10. Coupling k and self-inductance $L = L_1 = L_2$ as a function of distance between coils d and $R = R(f)$ of one coil in free air depending on f.

phase errors caused by minor mistuning more evenly

$$f_\mathrm{s} = \frac{f_\mathrm{max} + f_\mathrm{min}}{2} = \frac{1}{4\pi}\left(\frac{1}{\sqrt{L_\mathrm{min}C}} + \frac{1}{\sqrt{L_\mathrm{max}C}}\right). \tag{24}$$

Considering maximum power under (9) and that the constant voltage mode frequency $1/\sqrt{L_\sigma C}$ [37] should be well below $2f_\mathrm{s}$ to ensure that the second-order harmonics of asymmetric modulation have no means to generate large currents, the system parameters in Table I are chosen. A basic loss model based on manufacturer data is used for the power devices. Finally, harmonic currents are considered. With high harmonic content reaching down to the second order for asymmetric modulations and the frequency-dependent resistance of the magnetics, despite the harmonic-aware parameter choices, some harmonic currents will propagate for high k. These effects are considered in simulation by a harmonic loss model for the primary coil [38]

$$P(L_1) = \sum_{m=1}^{5} I_{1,m}^2 \cdot R\left(m \cdot \frac{\omega_1}{2\pi}\right) \tag{25}$$

the equation being evaluated on runtime with the periodic DFT of the currents and a resistance lookup table created by the impedance analysis of the magnetics as per Fig. 10.

The simulation is implemented in Simulink/PLECS. The PLL and the primary controller are designed to be faster acting than in the real experiment here, to display all events in one condensed load stepping diagram.

Since multiple cases are demonstrated in the experiment, only a limited selection of simulation results is shown. Fig. 11 shows a general survey of system behavior; voltage is regulated to precision steady state with some error during state changes, the downside of a fast primary controller. The modulations of both sides automatically track until 0.4 s and then lose track, as expected around $M \sim 0.5$ due to the nonbijective nature of the AVCHB phase. AVCHB can work or it cannot, depending on initial conditions. It is not a reliable strategy. The phase diagram in Fig. 11(c) shows how both PLL and PSC actively control ZVS and demonstrates the downside of a fast responding PLL, a significant amount of noise and minor tracking errors—hence, the PLL of the simulation is not discussed and a different system is designed for the experiment.

Because this article investigates a larger coupling up to $k = 0.6$ instead of the 0.1–0.3 range in [1], wherein harmonic losses were shown to be almost negligible, a different result regarding harmonics is obtained. For $k = 0.6$ in the range of reduced efficiency despite correct tracking between 0.2 and 0.4 s

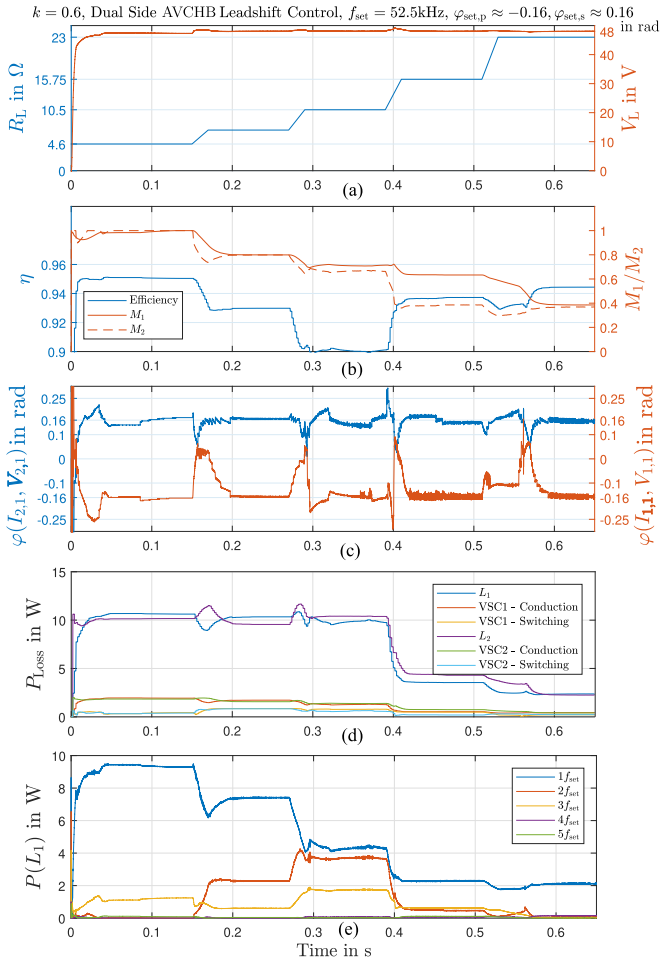

Fig. 11. Simulation of DSC AVCHB leadshift operation at design coupling. (a) Load change and output voltage regulation. (b) Efficiency and modulation index tracking. (c) Tracking of current phase angles versus local reference clocks r_1, r_2; secondary angle is positive for ZVS due to defined current direction. (d) Simulated power losses. (e) Primary coil losses per harmonic.

in Fig. 11, second- and third-order harmonic current generate more combined loss in Fig. 11(e) than the fundamental current, leading to the effect that even with AVCHB-related asymmetric tracking errors, light-load efficiency is greater than medium-load efficiency. Considering the coil properties in Fig. 10, a strong rise of resistance with frequency related to insufficiently fine subdivision of the litz wire, 55×0.4 mm, is responsible for this issue. The magnetics are retained in this study to demonstrate the effect in the experiment and underline that IPT systems with high k and high harmonic content modulations must be designed with the particular consideration of harmonic loss.

Following this general survey for the full-bridge, the dynamic behavior of the simplified HB system is investigated. The load step boundary behavior is simulated in Fig. 12. The theoretical result is confirmed. Load resistance increases in general and load resistance decreases above the boundary conditions are regulated within the time constant of the voltage control loop. Load resistance drops below the boundary achieve partial regulation and then have to wait for the primary modulation index M_1 to be increased sufficiently by the symmetrizing controller. Fig. 12

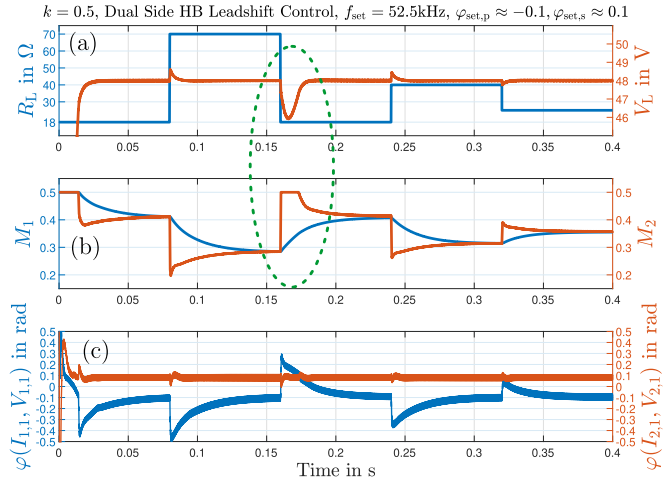

Fig. 12. Load stepping simulation of the HB system to evaluate regulation within and beyond the boundary resistance R_{Lmin} shown in Fig. 9. For a load resistance drop beyond the local R_{Lmin} within the green circle in (a), regulation is delayed. It can be seen from (b) that this is due to saturation of M_2. From (b) and (c), it can be seen in detail how the interaction of modulation and phase keeps DSC and control of ZVS conditions.

also gives a more detailed overview of the phase cooperative DSC process with a bijective modulation and a lower bandwidth PLL, hence largely free of noise and glitches.

VI. Experimental Verification

For the experimental PLL and phase detection, a variation of the strategy developed in [30], [33], [35], and [39] based on a comparator with hysteresis and a mixed-signal PLL is utilized. The strategy is simplified further based on observations about the nature of the task. A PLL can be designed with minimal bandwidth and have a very high ability to reject noise and distortion. It needs to lock on the primary system upon startup, and no frequency or rapid phase steps need to be tracked since the primary uses a slow and steady acting integral controller. Hence, the noise effects seen in simulation and also discussed in [33] are mitigated here by a simple structure using very low bandwidth. The system is controlled by one SPC5643L microcontroller unit (MCU) per side, the PWM of which is derived from an $f_{Clk} = 120\,\text{MHz}$ crystal-oscillator-derived system clock. The frequency difference between the f_s PWM signals of two MCUs is found as typically around $0.2\,\text{Hz}$. For the arbitrary selection of oscillators with common commercial tolerances of 30 ppm, this difference could be up to about 3 Hz, but the principle remains the same. A simple three-step controller is chosen, which acts only every 64 cycles of the switching frequency (PWM counter reload) with the authority to add/subtract one clock cycle to the PWM counter or do nothing, leading to a maximum average frequency reduction of

$$\overline{\Delta f_{low}} = \left[\frac{f_{Clk}}{\frac{f_{Clk}}{f_s} + 1} - f_s \right] / 64 = -0.36\,\text{Hz}. \tag{26}$$

Phase detection is implemented by a single XOR gate, a 90° shifted reference signal generated by the PWM unit, and two-stage RC low-pass filtering leaving a feedback signal with a

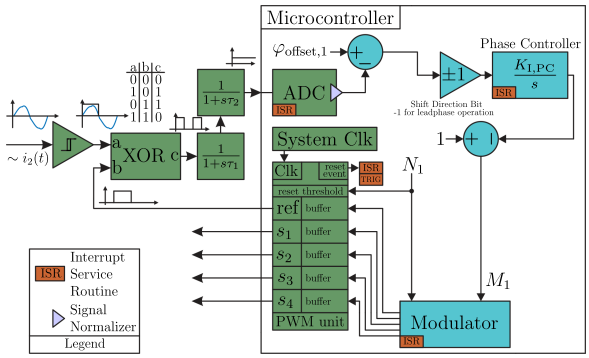

Fig. 13. Structure of the PSC. Green blocks represent hardware inside and outside the MCU; blue blocks are software routines. The interrupt service routine (ISR) for all control is executed upon periodic reset of the PWM ramp counter.

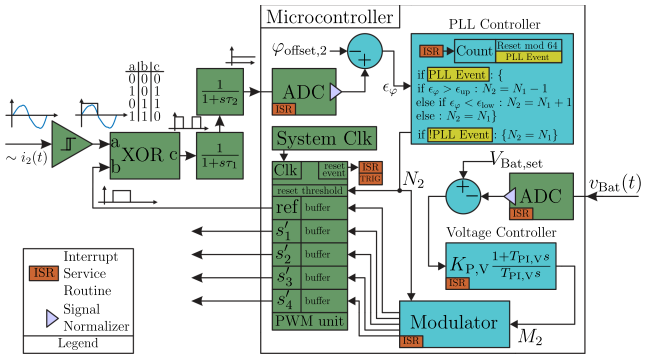

Fig. 14. Structure of the SSC. Including all power hardware and sensors per Figs. 2 and 7, the systems sides are identical except for one voltage sensing channel and the software. The PLL, only executed every 64 ISRs, is shown in pseudocode.

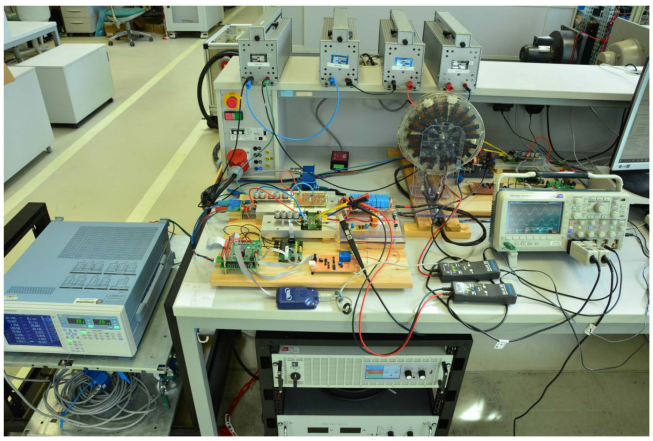

Fig. 15. Image of the laboratory setup in operation.

bandwidth of a few hertz, leading to the control structures of Figs. 13 and 14. These are used for all the experiments conducted with the setup shown in Fig. 15.

System behavior is evaluated via tests at a reduced voltage $V_\mathrm{d} = V_\mathrm{L} = 30$ V and the AVCHB scheme for nominal $V_\mathrm{d} = V_\mathrm{L} = 48$ V. For the experiment, ZVS is selected as the soft-switching condition; owing to the current reference directions defined in Fig. 2, this is achieved by a negative or lagging

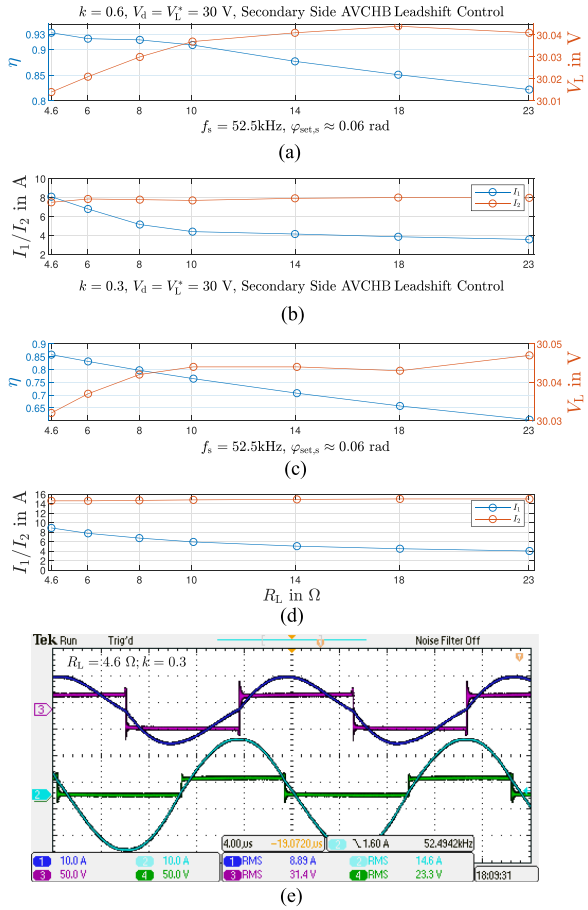

Fig. 16. AVCHB secondary-side control operation showing RMS current imbalances and the severe degradation of η for light load and low k typical of SSC on the S/S topology. System behavior (a) and (b) for $k = 0.3$ and (c) and (d) for $k = 0.6$. (e) Waveforms for 4.6 Ω load at $k = 0.3$. Trace 1/3 primary current/voltage; trace 2/4 secondary current/voltage.

angle in the primary and a positive or leading offset angle in the secondary. Only leading modulation in the secondary and lagging in the primary are considered since this arrangement offers slightly greater ability for the primary to control lagging current conditions even if the secondary is operating saturated at $M_2 = 1$, i.e., not reflecting any phase shift. This is dubbed leadshift operation because the secondary is the dominating controller. A pure SSC is tested by disabling the primary controller with $M_1 = 1$ to validate the PLL and define a baseline for efficiency. The result for leadshift AVCHB can be seen in Fig. 16. The peak efficiency 93.33% for design load and coupling ($k = 0.6$; $R_\mathrm{L} = 4.6\ \Omega$) in Fig. 16(a) is the highest observed and currents are naturally symmetrical at this point in Fig. 16(b). For all combinations of lighter load and lower coupling, the currents become increasingly asymmetrical and efficiency degrades rapidly. This is the expected behavior of an SSC on this topology. Enabling of the primary phase controller transitions the strategy to Leadshift AVCHB DSC. In practice, it is possible to obtain proper tracking by slow unidirectional variation of load, so the operating points slide only in one direction and do not enter asymmetric states. It does not constitute viable controller function. This is shown in Fig. 17 for $k = 0.6$ to validate the

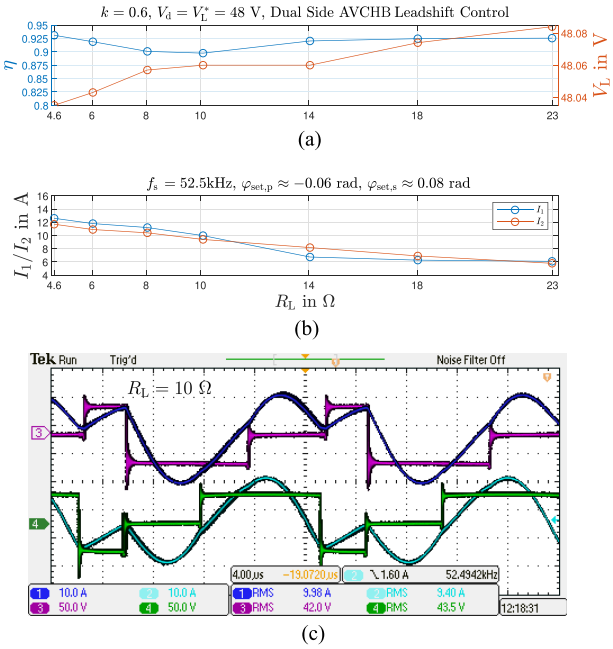

Fig. 17. DSC AVCHB operation at $k = 0.6$ for the evaluation of the harmonic model. (a) Efficiency and load regulation. (b) Current tracking. (c) Waveforms for 10-Ω load. Trace 1/3 primary current/voltage; trace 2/4 secondary current/voltage.

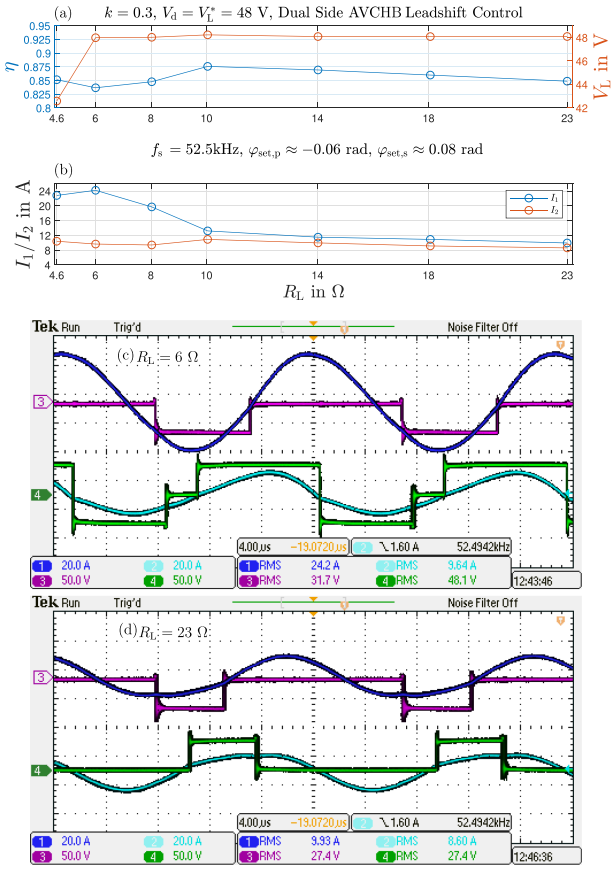

Fig. 18. DSC AVCHB operation at $k = 0.3$. (a) Efficiency and (faulty) load regulation (note much coarser scale of voltage axis versus other diagrams). (b) Current tracking. (c) Waveforms for 6-Ω load with asymmetric phase lock and failure to commence DSC. (d) Waveforms for 23-Ω load, i.e., HB operation. Trace 1/3 primary current/voltage; trace 2/4 secondary current/voltage.

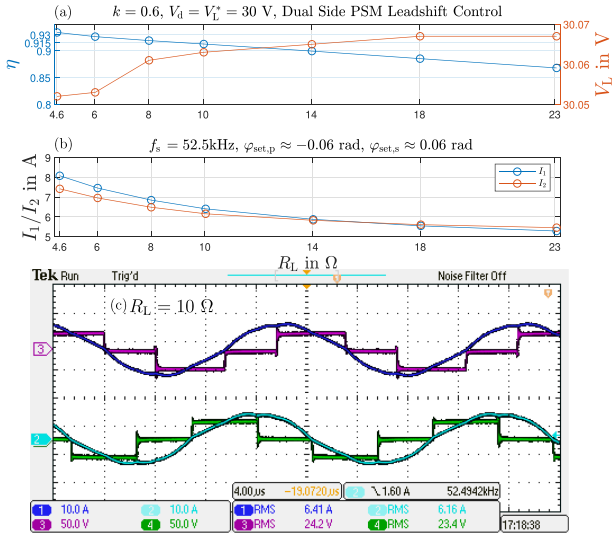

Fig. 19. DSC PSM operation at $k = 0.6$. (a) Efficiency and load regulation. (b) Current tracking. (c) Low harmonic content waveforms for 10-Ω load. Trace 1/3 primary current/voltage; trace 2/4 secondary current/voltage.

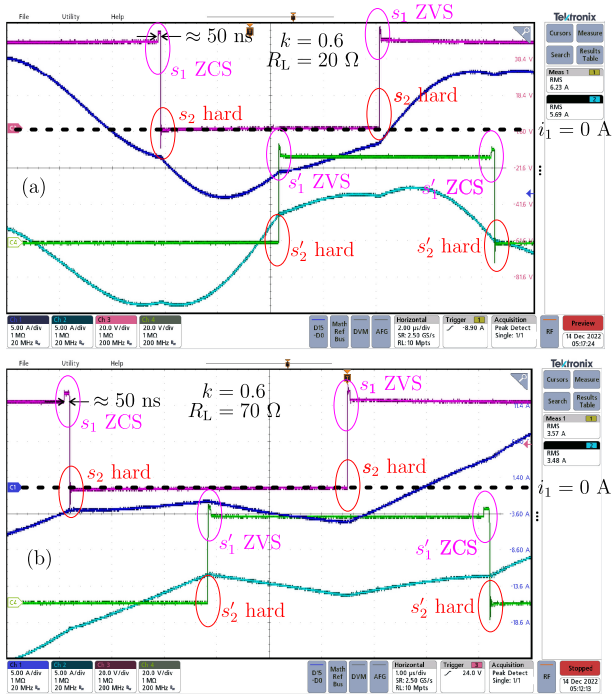

Fig. 20. Example waveforms of the system under high $k = 0.6$, hence with the maximum of harmonic currents. Both heavy (a) and light load (b) cases retain the designed phase angle and ZVS regulation. The high-side switches benefit from ZVS/ZCS; the low-side switches do not. Note that secondary current is defined in passive sign convention. Trace 1/2 primary/secondary current; trace 3/4 primary/secondary voltage.

harmonic model. Peak efficiency is marginally decreased in comparison to SSC, but the currents track symmetrically and efficiency is maintained at a high value that is no longer directly dependent on load. Instead, efficiency has a minimum at medium loads as expected from simulation due to harmonics, which is affirmed by the strongly distorted current waveform. For $k = 0.3$, mistracking due to the repeating phase behavior nature

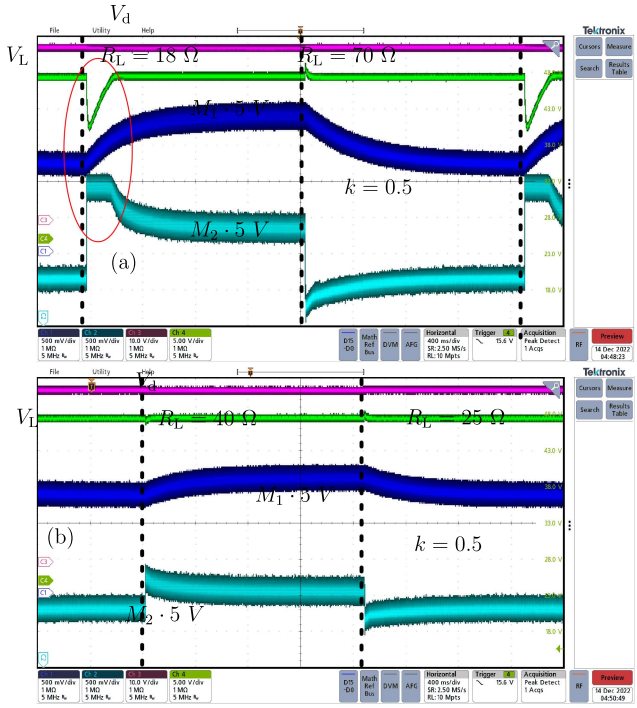

Fig. 21. Load stepping waveforms. (a) Load stepping event from light to full load, hence dropping below the boundary resistance. M_2 saturates and regulation is delayed. (b) Load step within the boundary; regulation is nominal.

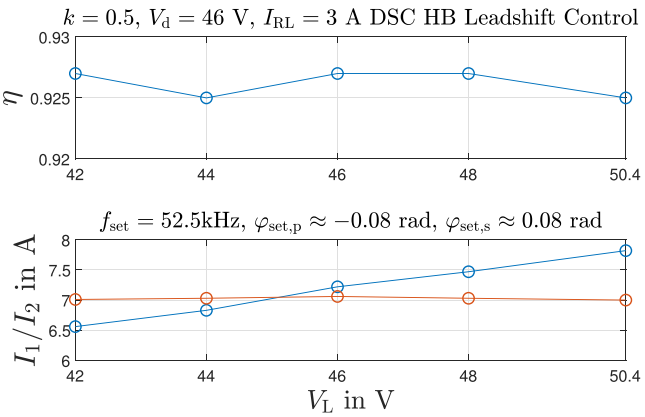

Fig. 22. Emulation of a CC charging process. Phase cooperative control cannot compensate for the voltage offset. Assuming that the system design is centered around the mid-charging voltage by setting V_d accordingly and the current is close to maximum capability, the current asymmetry is distributed evenly and in small values.

of AVCHB can be observed in Fig. 18(c); at $R_L = 4.6\,\Omega$, the output voltage is unregulated low and the system remains in this faulty state without the tracking of currents until $R_L = 10\,\Omega$. At this point, both system sides work as HBs with linear monotonic phase. Efficiency is increased and well maintained beyond. This operation is exemplified by Fig. 18(d) and demonstrates the viability for HB converters and the abrupt behavior difference between the two modes of AVCHB. Leadshift PSM DSC in Fig. 19 ($k = 0.6$; the result for $k = 0.3$ is equivalent) as the baseline for phase cooperative control shows no mistracking. Current distortion is generally reduced as seen in Fig. 19(c) and

TABLE II
COMPARISON OF DSC SCHEMES

	Standard	MEPT	Phase Cooperative
Two ac current sensors	(x)	(x)	x
DC power sensor		x	
Communication	x		
Modulation	Any	Any	Unique Phase
Variable parameters.	+	+	–
Step regulation	?	o	+

efficiency is superior to AVCHB down to $R_L = 10\,\Omega$ but not maintained as well toward light load because no shutdown of HBs occurs.

VII. EXPERIMENTS FOR THE HB SYSTEM

Further experimentation is undertaken on the simplified HB-based topology of Fig. 8. The ZVS behavior is shown in Fig. 20 for heavy and light load at maximum coupling, hence with the most harmonic content. In both cases, the set phase regulation is maintained on both sides since no additional current zero transition happens even for these extreme values. The upper devices s_1 and s_1' always benefit from ZVS/ZCS; the lower devices s_2 and s_2' are subject to hard switching. For smaller values of k, the waveforms are generally less distorted and angular regulation is only improved. Load step regulation is investigated in Fig. 21. Since the currents at lighter loads are significantly distorted, as seen in Fig. 20, it is not helpful to evaluate the step response from a current envelope. Instead, the converter control signals for s_2 and s_1' are low-pass filtered and used as proportionals of M_1 and M_2. The signals are noisy due to the vicinity of an operating power converter but give a real-time indication of system state closely replicating simulation in Fig. 12. In Fig. 21(a), only the load rejection is regulated within the settling time of the voltage controller; full regulation of the load increase must wait for the primary symmetrizing controller since the load is below the boundary. In Fig. 21(b), no such issue occurs.

While mainly suitable for fixed-voltage systems, the impact of variable voltage, e.g., battery charging, on the strategy is investigated as a final experiment. Considering cycling, the lifetime of a Li-ion battery is extended greatly by the prevention of deep cycling. Hence, most of the charging time should be located in a 3.5–4.2-V CC window [40]. Multiplied by 12 cells, output voltages of 42–50.4 V are considered for an input voltage of $V_d = 46$ V, simulating a system design centered on that range. The results are shown in Fig. 22. The current asymmetry in this use case, and a direct function of voltage offset, is distributed around the mean and has a low impact on system efficiency.

VIII. CONCLUSION

In this article, the usage of asymmetrical modulations for phase cooperative communicationless DSC of IPT is investigated. While AVC provides superior efficiency retention ($> 90\%$) to PSM at light load, even at high $k = 0.6$ and considering harmonic losses, it is not applicable due to the lack of bijective phase behavior. Inspired by AVCHB, an HB-based

system using simple PWM is designed. For this system, the boundary between fast and delayed regulation of load steps is derived. Owing to the symmetric nature of DSC, significant regulation reserve is maintained by the secondary side especially at light load, allowing almost a triple increase in power to be regulated from light load. Load increases within the boundary, and all load rejections are regulated in the experiment within milliseconds and with less than 2 V of maximum error. The design of a low-complexity mixed-signal PLL is shown, which uses only ± 0.36 Hz of maximum frequency deviation to keep phase lock. The controlled switching behavior for the most distorted currents at $k = 0.6$ is shown to ensure the soft switching of one switch, while the other switch operates fully hard due to asymmetric switching. Finally, a static test of the HB system design is undertaken for the additional consideration of the voltage imbalances to be expected in a typical battery charging cycle covering 42–50.4 V. Because the normalized voltage deviation from the design median is small, the impact on efficiency is marginal, and the system maintains 92.5% efficiency.

Table II gives a short comparison of this DSC scheme with MEPT and standard (communication based) DSC. Assuming that ac current sensors are always required in practice for self-protection in the case of fault, cooperative DSC has the lowest system requirements, even more so when implemented as an HB, but is limited in the selection of modulations and blind toward parameter variation. In terms of regulation, all the DSC schemes should exhibit the quasi-instantaneous regulation reserve shown here, with the symmetrizing loop being tendentially slower for MEPT and entirely dependent on the communication system for the standard strategy.

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Julius Maximilian Placzek received the M.Sc. degree in electrical engineering in 2019 from the Institute of Electrical Engineering and Information Technology, Kiel University, Kiel, Germany, where he is currently working toward the Dr.-Ing. (Ph.D.) degree in electrical engineering with the Chair of Power Electronics.

In his bachelor and master theses, he developed and investigated systems for simultaneous wireless information and power transfer with a focus on harsh environments such as water. His research interests include control of inductive power transfer, battery charging, and talkative power—systems using power flow to communicate information.

Hamzeh Beiranvand (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering and the Ph.D. degree in control and efficiency optimization of solid-state transformers from Lorestan University, Khorramabad, Iran, in 2011, 2014, and 2020, respectively.

He received a scholarship from the Ministry of Education of Iran during his bachelor for the period of four years. Since October 2020, he has been a Postdoctoral Researcher with the Chair of Power Electronics, Kiel University, Kiel, Germany, and leading the battery group. In 2021, he was Elected Member of Kiel Nano, Surface and Interface Science, Kiel University. He has authored or coauthored more than 40 conference and journal papers during his research profession. His research interests include batteries and interaction between batteries and power electronic converters.

Marco Liserre (Fellow, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from Bari Technical University, Bari, Italy, in 1998 and 2002, respectively.

He was an Associate Professor with Bari Technical University. In 2012, he was a Professor of Reliable Power Electronics with Aalborg University, Aalborg, Denmark. Since 2013, he has been a Full Professor with the Chair of Power Electronics, Kiel University, Kiel, Germany. He got offered and declined professorships at the Ilmenau University of Technology; the Technical University of Munich, Munich, Germany; and the Hamburg University of Technology, Hamburg, Germany. He has authored or coauthored more than 600 technical papers (one-third of them in international peer-reviewed journals), a book, and two granted patents, with more under evaluation, some of them involving companies. These works have received more than 45 000 citations. He was listed in ISI Thomson report "The world's most influential scientific minds" in 2014. In 2022, he joined Fraunhofer Institute for Silicon Technology, Itzehoe, Germany, as a Deputy Director and Director of a new Center for "Electronic Energy Systems" funded for 5 Million Euro.

Dr. Liserre is a Member of the IEEE Industry Applications Society, the IEEE Power Electronics Society (PELS), the IEEE Power and Energy Society, and the IEEE Industrial Electronics Society. He serves all these societies in different capacities. In the PELS, he is an AdCom Member (second mandate). He is a Co-Editor for IEEE OPEN JOURNAL OF POWER ELECTRONICS. He is an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS (JESTPE). He is a Guest Editor for Several Special Issues of JESTPE. He is a Technical Committee Chairman of the new Committee on Electronic Power Grid Systems. He is a Member of the IEEE Digital Committee. He is an IES-Liaison responsible, eGrid 2021 Workshop Co-Chairman, the Co-Chairman of 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems, and Organizer in Kiel. He has received the IES 2009 Early Career Award, the IES 2011 Anthony J. Hornfeck Service Award, the 2014 Dr. Bimal Bose Energy Systems Award, the 2017 IEEE PELS Sustainable Energy Systems Technical Achievement Award, the 2018 IEEE-IES Mittelmann Achievement Award, and six IEEE Journal Awards.