Common-Mode Circuit Analysis of Current-Source Photovoltaic Inverter for Leakage Current and EMI

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***Abstract*—Leakage current and electromagnetic interference (EMI) are closely related to the common-mode (CM) circuit in transformerless photovoltaic inverter systems. However, the correlation between them is elusive, as they are always studied independently because of the different frequency bands involved. This article establishes the CM circuit models of the current-source inverter, and the inherent relationship and the affecting factors between leakage current and CM EMI are revealed. Based on the established models, the leakage current and conducted EMI are accurately predicted with a reduced computational burden. In addition, some suppression measures for leakage current and CM EMI are derived, including the effectiveness of connecting a neutral wire. Finally, through simulations and experiments, the correctness of the theoretical analysis is verified.**

***Index Terms*—Current-source inverters (CSIs), electromagnetic interference (EMI), leakage current, photovoltaic (PV) system.**

I. Introduction

ALTHOUGH residential photovoltaic (PV) power generation systems have gained extensive development in the past few years [1], there are still longstanding challenges with PV inverters in terms of reliability, safety, and electromagnetic compatibility (EMC) [2], [3]. PV inverters are mainly classified into voltage-source inverters (VSIs) and current-source inverters (CSIs) [4]. To date, VSIs are the most common interface between PV panels and the grid, considering the economics [5]. However, individual VSI is hard to cope with the household applications powered by low-voltage PV panels, which requires an additional boost converter to improve the adaptability of the inverter [6]. Alternatively, CSI can provide an interface to the residential grid and low-voltage PV panels due to its inherent boost capability [7]. Therefore, CSIs have also received extensive attention in recent years [8], [9].

Due to the high-frequency switching behavior, the common-mode (CM) voltage of CSI is inevitably generated [10], [11]. The CM voltage propagates through the circuits and parasitic components of the CSI system and causes CM currents. In different frequency bands, the CM current presents diverse types of hazards. At a lower frequency range, the CM current flows through the parasitic capacitance of the PV panels to the ground, which is called leakage current. Excessive leakage current can lead to a potential personal safety hazard, so the leakage current must be suppressed to a low level [12]. At higher frequencies, the CM current flows through the power interface to the utility grid and generates CM electromagnetic interference (EMI) [4]. And the EMI will interfere with other functioning equipment, so the EMI should also be attenuated to comply with the standards [13].

The solutions to the suppression of leakage current in CSI can be classified into two categories: software and hardware methods. The software ones mainly refer to the methods of modifying modulation strategies to suppress the leakage currents. A near state modulation method is proposed to optimize the space vector pulsewidth modulation strategy, which reduces the CM voltage and leakage current to a certain extent by eliminating the zero vectors [14]. In addition, a nearest three-state modulation of CSI is proposed in [15], which reduces the peak value of the CM voltage and the leakage current. However, the bipolar current pulses degrade the quality of differential-mode (DM) current. The hardware methods refer to the methods of modifying circuit topologies to suppress the leakage currents. A modified topology with two X2-type capacitors and a neutral wire is proposed to reduce the CM voltages for PV CSI [16]. Similarly, a new three-phase buck rectifier is presented to suppress the high-frequency distortion of three input currents [17]. However, an obvious low-frequency neutral wire current exists in the neutral wire of the CSI, which may result in EMI issues for the converter's gate driver circuits and control signals [18]. Moreover, a four-leg CSI and a current source H7 concept are proposed in [19] and [20], respectively. Combining these two concepts, a CSI7 topology with an integrated CM return path is presented in [21] to address the leakage current issue and reduce the neutral wire current. In fact, the neutral wire circulating current problem in the split-capacitor four-wire CSI can be addressed by designing proper controllers and modulation schemes. In [22], a modulation strategy with zero average CM voltage is proposed for the

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split-capacitor four-wire CSI, which ensures approximate zero neutral wire current and reduces the leakage current obviously. However, compared to the conventional CSI, the duty cycles in the split-capacitor four-wire CSI are limited to no more than two-thirds, which reduces the dc current utilization.

The research work on the EMI issue in CSI mainly covers CM EMI analysis and EMI attenuation. The conducted EMI of CSIs is evaluated in [23] using the equivalent circuits, and the transfer function-based CM EMI analysis has been achieved. In addition, the CM EMI generation mechanism of H7 CSI is also analyzed in [24], and combined with the proposed modulation scheme, the conducted CM EMI is reduced. However, the extra switch means an increase in cost, which is not conducive to industrial implementation. To suppress EMI, a common approach for the already operating prototypes is to design EMI filters by first measuring the original CM voltage source and then determining the required insertion loss based on the standard limits that need to be met [25], [26]. However, this approach is time-consuming. To approach this dearth of efficiency, it is necessary to establish a CM EMI equivalent circuit model to guarantee the EMI prediction. A CM EMI equivalent circuit model is proposed in [18] for a current-source converter system, which contains a CSI. And a CM EMI filter design is conducted based on the proposed equivalent circuit model, which suppresses the CM EMI significantly. In addition, a new CM EMI equivalent circuit for CSI is proposed in [27], which reduces the computation time of CM EMI prediction.

Although both leakage current and CM-conducted EMI issues are closely related to CM current, they have always been studied independently in the past. To avoid attending to one thing and losing another to address the leakage current and EMI issues, in this article, the leakage current and CM-conducted EMI of the split-capacitor four-wire CSI are studied at the same time. The CM equivalent circuit models for leakage current and CM-conducted EMI are developed. Based on those models, the leakage current and the CM-conducted EMI can be predicted accurately with a reduced computational burden, and the improvement solutions for reducing leakage current and CM-conducted EMI are deduced.

The rest of this article is organized as follows. In Section II, leakage current analysis for PV CSI is introduced. In Section III, the CM EMI equivalent circuit model of PV CSI considering parasitic parameters is established, and the attenuation of CM EMI is derived. In Section IV, the parasitic parameters of the critical components in CSI are investigated. In Section V, simulations and experiments are implemented to validate the proposed CM EMI equivalent circuit models for leakage current and conducted CM EMI. Finally, Section VI concludes this article.

II. PV CSI With Reduced Leakage Current

A. Topology of PV CSI With Reduced Leakage Current

The topology of the grid-tied split-capacitor four-wire CSI investigated in this article is shown in Fig. 1. The CSI is implemented using developed reverse-blocking insulated gate bipolar transistors (RB-IGBTs). On the dc side, the PV panels fed a stable current to the inverter through a dc filter composed of split capacitors ($C_{\rm dc1}$ and $C_{\rm dc2}$) and inductors ($L_{\rm dc1}$ and $L_{\rm dc2}$). On the ac side, the inverter is connected to the grid through a filter composed of ac capacitors (C_f) and inductors (L_f). Different from the conventional CSI, a neutral wire is added to connect the midpoint of the dc link (O') and the neutral point of the ac filter capacitors (O). $C_{\rm pv1}$ and $C_{\rm pv2}$ represent the parasitic capacitors between the PV panels and ground, which are 50–150 nF/kWp for glass-faced modules and 1 μF/kWp for thin-film modules [3].

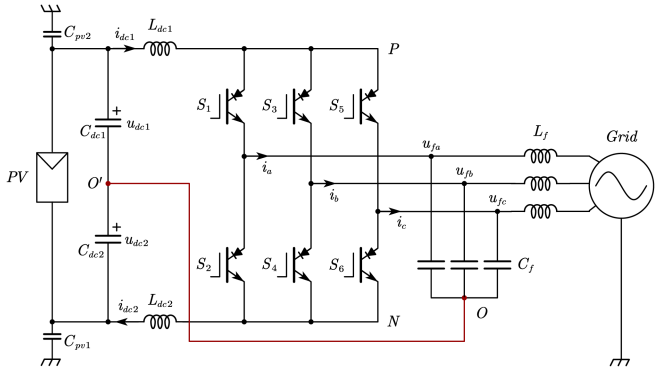

Fig. 1. Topology of the grid-tied split-capacitor four-wire CSI.

B. Equivalent Circuit Model for Leakage Current Analysis

The equivalent circuit of the PV CSI is shown in Fig. 2(a). Z_N represents the parasitic impendence of the added neutral wire connecting the points O and O'. The voltages v_{PO} and v_{NO} are expressed as follows:

$$v_{PO} = \begin{bmatrix} S_1 & S_3 & S_5 \end{bmatrix} \begin{bmatrix} u_{fa} & u_{fb} & u_{fc} \end{bmatrix}^T \tag{1}$$

$$v_{NO} = \begin{bmatrix} S_2 & S_4 & S_6 \end{bmatrix} \begin{bmatrix} u_{fa} & u_{fb} & u_{fc} \end{bmatrix}^T. \tag{2}$$

According to the requirements in IEC 60755 for the bandwidth of B-type leakage current detectors for PV inverters [28], the frequency concerned by leakage current analysis is less than 1 kHz [29]. Therefore, only the influence of $C_{\rm pv1}$ and $C_{\rm pv2}$ on leakage current is taken into account, and the small parasitic capacitances, such as the parasitic capacitance of cables and device leads, are ignored.

As only the common equivalent circuit is concerned, the equivalent circuit shown in Fig. 2(a) is reduced to that shown in Fig. 2(b). Furthermore, since the impedance of bulk capacitors ($C_{\rm dc1}$, $C_{\rm dc2}$, and C_f) decreases rapidly as the frequency increases compared to $C_{\rm pv1}$ and $C_{\rm pv2}$, they are considered short-circuited at frequencies above tens of hertz, as illustrated in Fig. 2(c). According to Thevenin's theorem, the circuit between nodes O and O' can be simplified to an equivalent voltage source $v_{\rm eq}$ in series with equivalent internal impedance Z_1, as shown in Fig. 2(d). Based on the superposition theorem, the equivalent voltage $v_{\rm eq}$ between nodes O and O' can be derived as follows:

$$v_{\rm eq} = \frac{Z_N \left[Z\left(L_{\rm dc2}\right) v_{PO} + Z\left(L_{\rm dc1}\right) v_{NO} \right]}{Z\left(L_{\rm dc1}\right) Z\left(L_{\rm dc2}\right) + Z_N \left[Z\left(L_{\rm dc1}\right) + Z\left(L_{\rm dc2}\right) \right]} \tag{3}$$

and the impedance $Z_1 = Z(L_{\rm dc1})//Z(L_{\rm dc2})//Z_N$. Thus, the leakage current $i_{\rm leakage}$ can be expressed as follows:

$$i_{\rm leakage} = \frac{v_{\rm eq}}{Z_1 + Z_2 + Z\left(C_{\rm pv}\right)} \tag{4}$$

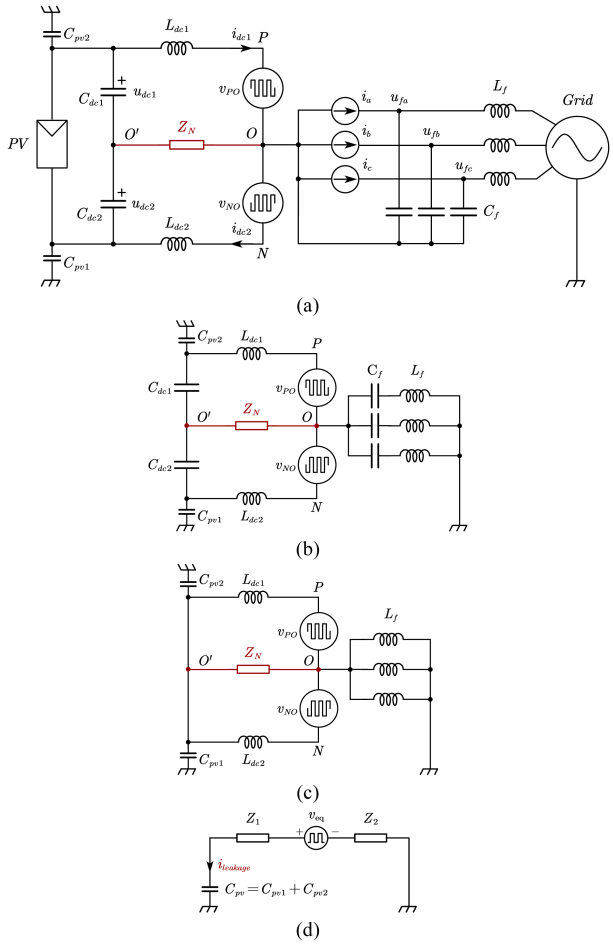

Fig. 2. CSI equivalent circuit model for leakage current analysis. (a) Equivalent model. (b) Reduced CM equivalent circuit. (c) CM equivalent circuit at high frequency. (d) Simplified CM equivalent circuit.

where $Z_2 = Z(L_f)/3$, and $Z(L_{\rm dc1})$, $Z(L_{\rm dc2})$, $Z(L_f)$, and $Z(C_{\rm pv})$ represent the impedances of $L_{\rm dc1}, L_{\rm dc2}, L_f$ and $C_{\rm pv}$, respectively. By rewriting (3), we have

$$v_{\rm eq} = \frac{Z_N\{[Z(L_{\rm dc1})+Z(L_{\rm dc2})]\,v_{\rm cm}+[Z(L_{\rm dc2})-Z(L_{\rm dc1})]\,v_{\rm dm}\}}{Z(L_{\rm dc1})\,Z(L_{\rm dc2})+Z_N[Z(L_{\rm dc1})+Z(L_{\rm dc2})]} \tag{5}$$

where $v_{\rm cm} = (v_{PO} + v_{NO})/2$, which is often referred to as CM voltage, and $v_{\rm dm} = (v_{PO} - v_{NO})/2$, which is the DM voltage. Combining (4) and (5), it can be deduced that besides the CM voltage, the DM voltage also contributes to the leakage current when $Z(L_{\rm dc1}) \neq Z(L_{\rm dc1})$. Therefore, in order to reduce the leakage current, the circuit parameters in Fig. 2(c) should be designed to be symmetrical, that is, $L_{\rm dc1} = L_{\rm dc2}$. When $Z(L_{\rm dc1}) = Z(L_{\rm dc2}) = Z(L_{\rm dc})$, (5) can be simplified to

$$v_{\rm eq} = \frac{Z_N}{Z(L_{\rm dc})/2 + Z_N} v_{\rm cm}. \tag{6}$$

C. Comparison With the Conventional CSI

When $Z_N \to \infty$, it corresponds to the case of the conventional CSI without the neutral wire. Thus, (6) can be simplified to

$$v_{\rm eq} = v_{\rm cm}. \tag{7}$$

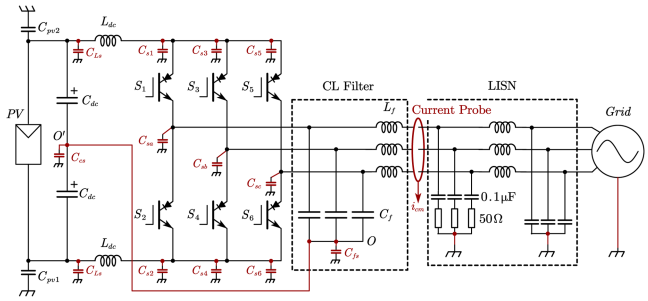

Fig. 3. Topology of the grid-tied split-capacitor four-wire CSI considering parasitic capacitors.

Clearly, the equivalent voltage $v_{\rm eq}$ is larger than that in (6), which means that the neutral wire is an effective solution to suppress leakage current. In addition, (7) also reveals that the leakage current in conventional CSI is significantly affected by the switching frequency. In contrast, the equivalent voltage $v_{\rm eq}$ of four-wire CSI is always small at different switching frequencies due to the low neutral wire impedance. Thus, the leakage current of the four-wire CSI is small at different switching frequencies.

According to (4)–(6), it can be known that the CM leakage current can be reduced from the following two aspects.

1) To minimize leakage current, $Z(L_{\rm dc})$ should be as large as possible, and Z_N should be as small as possible. However, increasing $Z(L_{\rm dc})$ will increase cost and volume inevitably. Thus, a cost-effective solution is to make the connection between points O and O' as short as possible during the design to minimize Z_N.
2) Besides, minimizing the high-frequency components of $v_{\rm cm}$ may be an effective solution to reduce leakage current, which could be realized by designing modulation schemes.

III. CM Equivalent Circuit Model for EMI of PV CSI

A. PV CSI Considering Parasitic Capacitance

For EMI analysis, researchers are interested in a higher and wider frequency range than that in leakage current analysis. For example, the conducted disturbance frequency range specified by the CISPR 11 standard is 150 kHz to 30 MHz (CISPR Band B), while the leakage-current-related frequency range is below 1 kHz. Therefore, the role of parasitic capacitances in circuits at such high frequencies cannot be ignored in CM EMI studies. The parasitic capacitance of CSI with symmetrical parameters is mainly derived from two sources: a component leads to ground capacitance and a printed circuit board (PCB) traces to ground capacitance, as demonstrated in Fig. 3. As shown in Fig. 3, C_{cs} is the parasitic capacitance between the midpoint of the dc-link and ground. Two C_{Ls}s are the parasitic capacitances of the dc inductors $L_{\rm dc}$s. The parasitic capacitances of the phase-legs to the ground are denoted as C_{s1}–C_{s6}, whereas the parasitic capacitance of the bridge-leg midpoints to the ground is denoted as C_{sa}, C_{sb}, and C_{sc}. C_{fs} denotes the parasitic capacitance between the neutral point of the ac filter capacitor and the ground.

Furthermore, a line impedance stabilization network (LISN) is introduced at the ac power port for the repeatability of the test,

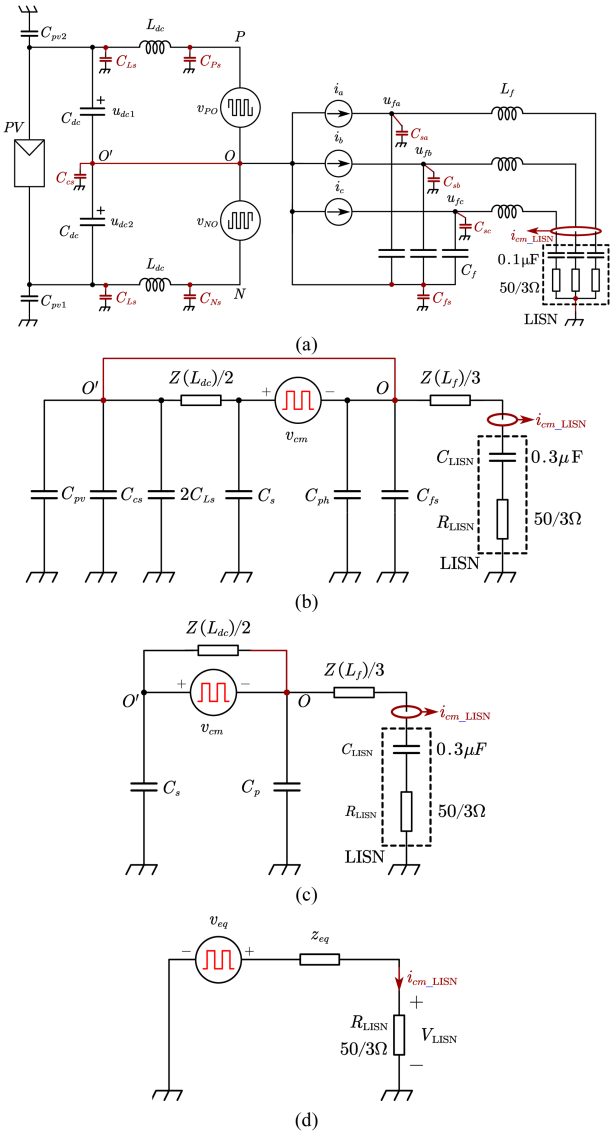

Fig. 4. CM EMI equivalent circuit for the grid-tied split-capacitor four-wire CSI. (a) Equivalent circuit with parasitic capacitors. (b) CM EMI circuit model. (c) CM EMI circuit model with merged parasitic capacitors. (d) Simplified equivalent circuit model for CM EMI.

which provides a precise impedance with high EMI isolation and couples EMI noise to the LISN's measurement port for the test. However, the existing commercial LISN cannot separate the DM and CM noise. To this end, a high-frequency current probe is introduced in Fig. 3 to measure the CM current $i_{\rm cm}$ flowing into the LISN to reflect the CM disturbance emission level of PV CSI.

B. Equivalent Circuit Model for CM EMI Analysis

When taking into account the effect of parasitic capacitance within CISPR Band B, the equivalent CM circuit will be quite different from the leakage current equivalent model shown in Fig. 2. By replacing the switches in Fig. 3 with controlled voltage sources and current sources, the equivalent circuit shown in Fig. 4(a) is derived, where $C_{Ps} = C_{s1} + C_{s3} + C_{s5}$ and $C_{Ns} = C_{s2} + C_{s4} + C_{s6}$. Because of the high EMI isolation of LISN, CM noise can be effectively blocked from propagating to the grid. Thus, only the branches of 0.1 μF capacitor $C_{\rm LISN}$ and 50 Ω resistor $R_{\rm LISN}$ need to be considered.

Extracting the CM noise propagation path in Fig. 4(a), the CM EMI circuit model shown in Fig. 4(b) is obtained. It should be noted that the bulk capacitors ($C_{\rm dc}$ and C_f) are regarded as short circuits at high frequency, as discussed in the previous section. Thus, the parasitic capacitors $C_{\rm pv1}$ and $C_{\rm pv2}$ can be merged into one capacitor $C_{\rm pv}$ because of their parallel connections. And the same can be done for C_{Ls}s, as well as C_{sa}, C_{sb}, and C_{sc}, so we have $C_{\rm pv} = C_{\rm pv1} + C_{\rm pv2}$, $C_s = C_{Ps} + C_{Ns}$, and $C_{ph} = C_{sa} + C_{sb} + C_{sc}$. On the dc side, the nodes P and N are connected in parallel in the CM EMI model; assuming that the circuit parameters are symmetrical, the CM impedance of dc inductors is $Z(L_{\rm dc})/2$. Similarly, the CM impedance of ac inductors is $Z(L_f)/3$. In addition, in order to suppress the leakage current, according to the analysis presented in Section II, the neutral wire is designed to be as short as possible, so that the impedance of the neutral wire can be considered to be zero.

Further, by merging the parasitic capacitors in Fig. 4(b), the CM EMI circuit can be simplified as shown in Fig. 4(c), where $C_p = C_{\rm pv} + C_{cs} + 2C_{Ls} + C_{ph} + C_{fs}$. By using the Thevenin theorem, the CM EMI circuit can be equivalently reduced to the circuit in Fig. 4(d), where

$$v_{\rm eq} = \frac{C_s}{C_s + C_p} v_{\rm cm} \tag{8}$$

$$z_{\rm eq} = Z\left(C_s + C_p\right) + Z\left(L_f\right)/3 + Z\left(C_{\rm LISN}\right) \tag{9}$$

and the CM noise current is given as follows:

$$i_{\rm cm\_LISN} = \frac{v_{\rm eq}}{z_{\rm eq} + R_{\rm LISN}}. \tag{10}$$

The CM noise attenuation can be defined as a transfer function from CM voltage to CM noise current, as identified in (11). A similar definition has been documented previously for a VSI presented in [30]

$$\mathrm{TF}\left(\mathrm{Att}_{\rm cm}\right) = i_{\rm cm\_LISN}/v_{\rm cm}. \tag{11}$$

To facilitate the calculation, the logarithm is taken for both sides of (11). And substituting it into (8)–(10), the CM noise attenuation of the PV CSI can be expressed as follows:

$$\begin{aligned}\mathrm{Att}_{\rm cm} &= v_{\rm cm}\,[\mathrm{dB}\mu\mathrm{V}] - i_{\rm cm\_LISN}\,[\mathrm{dB}\mu\mathrm{A}] \\ &= 20\lg\left(z_{\rm eq} + R_{\rm LISN}\right) - 20\lg\left(\frac{C_s}{C_s + C_p}\right) \\ &= 20\lg\left\{\begin{array}{c} Z\left(C_s\right) + \\ \frac{C_s + C_p}{C_s}\left[Z\left(L_f\right)/3 + Z\left(C_{\rm LISN}\right) + R_{\rm LISN}\right] \end{array}\right\}.\end{aligned} \tag{12}$$

C. Comparison With the Conventional CSI

By letting the wire highlighted in red in Fig. 4(b) be open, the CM equivalent circuit of the conventional CSI without the neutral wire is obtained, as shown in Fig. 5(a), where $C_{s(\rm dc)} = C_{\rm pv} + C_{cs} + 2C_{Ls}$, and $C_{s(\rm ac)} = C_{ph} + C_{fs}$. Further simplifying

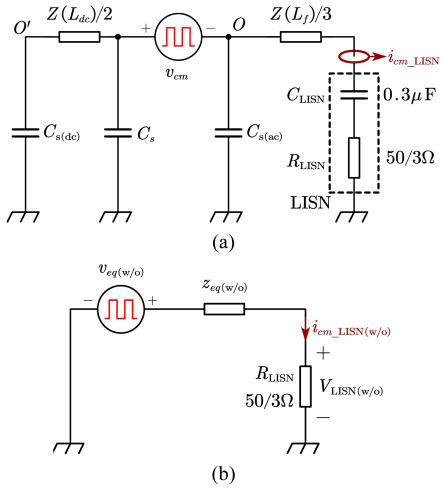

Fig. 5. CM EMI equivalent circuit for the conventional CSI without the neutral wire. (a) Equivalent circuit with parasitic capacitors. (b) Simplified equivalent circuit model for CM EMI.

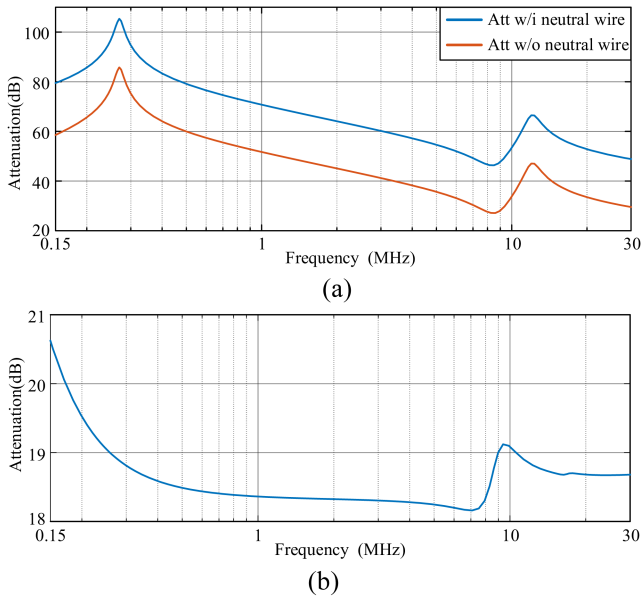

Fig. 6. CM EMI attenuation introduced by the neutral wire. (a) CM noise attenuation of the CSI with and without the neutral wire. (b) Increased CM noise attenuation by the added neutral wire.

the CM equivalent circuit yields a more compact equivalent circuit, as shown in Fig. 5(b), where equivalent CM voltage and equivalent CM impedance are expressed as follows:

$$v_{\mathrm{eq(w/o)}} = \frac{Z\left(C_{s(\mathrm{ac})}\right)}{Z_{O'} + Z\left(C_{s(\mathrm{ac})}\right)} v_{\mathrm{cm}} \tag{13}$$

$$z_{\mathrm{eq(w/o)}} = Z_{O'} \parallel Z\left(C_{s(\mathrm{ac})}\right) + Z\left(L_f\right)/3 + Z\left(C_{\mathrm{LISN}}\right) \tag{14}$$

where $Z_{o'} = [Z(C_{s(\mathrm{dc})}) + Z(L_{\mathrm{dc}})/2]//Z(C_s)$.

The CM noise attenuation for conventional CSI without the neutral wire can be derived as follows:

$$\begin{aligned}\mathrm{Att}_{\mathrm{cm(w/o)}} &= v_{\mathrm{cm}}\left[\mathrm{dB}\mu\mathrm{V}\right] - i_{\mathrm{cm\_LISN}}\left[\mathrm{dB}\mu\mathrm{A}\right] \\ &= 20\lg\left(z_{\mathrm{eq(w/o)}} + R_{\mathrm{LISN}}\right) - 20\lg\left[\frac{Z\left(C_{s(\mathrm{ac})}\right)}{Z_{O\prime} + Z\left(C_{s(\mathrm{ac})}\right)}\right] \\ &= 20\lg\left\{\frac{Z_{O\prime}+}{\frac{1}{\frac{Z_{O\prime}}{Z\left(C_{s(\mathrm{ac})}\right)}+1}\left[Z\left(L_f\right)/3 + Z\left(C_{\mathrm{LISN}}\right) + R_{\mathrm{LISN}}\right]}\right\}.\end{aligned} \tag{15}$$

According to (12) and (15), the calculated CM noise attenuation of the CSI with and without the neutral wire is illustrated in Fig. 6(a). Subtracting (15) from (12), the CM EMI attenuation of the neutral wire under the same system parameters is shown in Fig. 6(b), which shows that the added neutral wire increases about 19 dB CM attenuation within CISPR Band B.

In addition, it can be deduced that increasing the dc inductance could slightly attenuate the CM EMI of the conventional CSI from (13). In the split-capacitor four-wire CSI, however, the dc inductance does not contribute to CM EMI attenuation due to a shorted neutral wire. Furthermore, because C_{cs} and C_{fs} could be intendedly changed, according to (12), increasing C_{cs} and C_{fs} could reduce the CM EMI of the split-capacitor four-wire CSI. On the other hand, in conventional CSI, increasing C_{fs} could reduce CM EMI, but increasing C_{cs} will increase CM EMI instead.

As demonstrated in (12) and (15), the following conclusions can be drawn.

1) Increasing the dc inductance has no contribution to the CM attenuation of the split-capacitor four-wire CSI and only a limited contribution to CM attenuation for conventional CSI, although it has an effect on leakage current suppression as analyzed in Section II.
2) Connecting the neutral wire can effectively attenuate both CM EMI and leakage current.
3) Adding capacitors between the dc capacitors' middle point and/or the ac capacitor neutral point and ground can increase C_{cs} and C_{fs}, respectively. Thus, the CM EMI of the split-capacitor four-wire CSI can be attenuated. However, in conventional CSI, only increasing C_{fs} has little effect on the CM attenuation.

Although leakage current and CM EMI are all closely related to the CM circuit of PV inverter systems, their equivalent circuits are different. The main reason for this is that the concerned frequency bands of the two issues are different. In different frequency bands, the principal circuit components in a circuit need to be considered are different. The reason for taking into account the two issues at the same time is that such a way could avoid attending to one thing and losing another. Moreover, the statement "reducing leakage current is beneficial to EMI attenuation" in the published literature can be verified.

IV. Parasitic Extraction of Critical Components

A. Parasitic Parameters of Inductors

From Fig. 4(c), the CM impedance of the ac inductors $Z(L_f)/3$ has a significant effect on the attenuation of the CM EMI. Because CM parasitics are critical to the CM impedance of the ac inductors, the accurate CM impedances of inductors

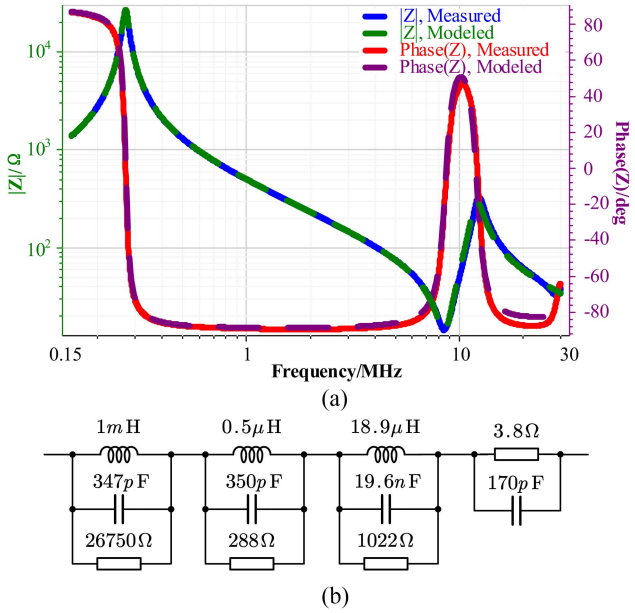

Fig. 7. Measured and modeled CM impedance of L_f. (a) Measured and fitted results of impedance and phase. (b) CM equivalent circuit of $Z(L_f)/3$.

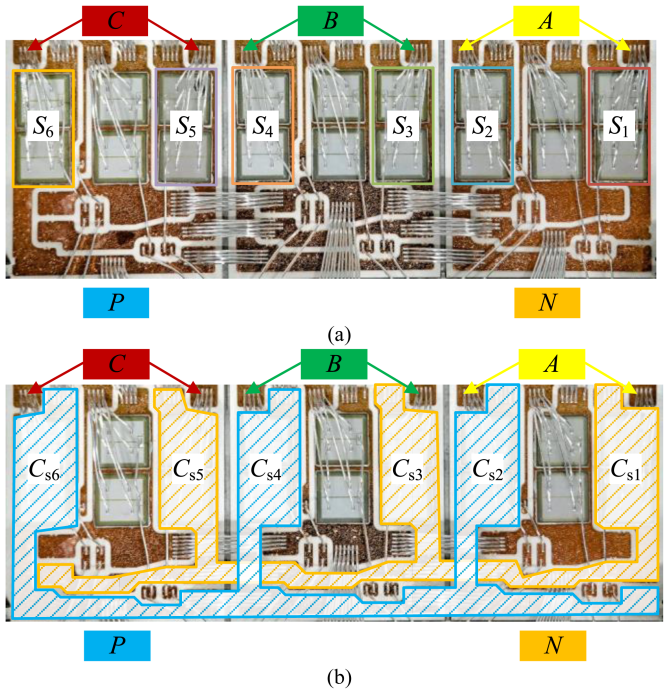

Fig. 8. Top view of an RB-IGBT power module. (a) Package internal layout. (b) Parasitic capacitance distribution areas.

in this study are measured by a precision impedance analyzer (Wayne Kerr 6500B) within CISPR Band B. And the parasitic parameters of inductors are estimated by the fitting method [31], [32] using the electrochemical impedance analysis tool EC-Lab Zfit. Fig. 7(a) presents the measured and fitted CM impedances of L_f in Fig. 4. Clearly, the fitting results are basically consistent with the measured ones. The fitted CM equivalent circuit with parameters of $Z(L_f)/3$ is shown in Fig. 7(b). The CM equivalent circuit of $Z(L_{\rm dc})/2$ can also be obtained by the same method, which is not shown here due to limited space.

B. CM Parasitic Capacitance in the PV CSI

According to (10), the parasitic capacitances have a significant impact on the attenuation of CM EMI. There are two categories of parasitic capacitance in Fig. 4(b): CM parasitic capacitance of the power module (C_s and C_{ph}), and CM parasitic capacitance of passive devices (C_{cs}, C_{Ls}, and C_{fs}).

In this study, the CSI circuit is implemented by a Fuji 18MBI100W power module that integrates multiple RB-IGBTs. Fig. 8(a) shows the internal layout of the power module package. The CSI switches S_1–S_6 are implemented using a subset of the devices in the power module, and each switch of the bridge arms is realized by two RB-IGBT bare dies in parallel. The parasitic capacitance C_{Ps} equals the parasitic capacitance to ground from the orange-shaded area in Fig. 8(b). Similarly, C_{Ns} is indicated by the blue-shaded area in Fig. 8(b). The power module was mounted on the grounded heat sink, and the CM parasitic capacitances are measured by 6500B. Due to the symmetry of the circuit topology and layout, the CM parasitic capacitance of the power module C_s is measured to be 14.52 nF, and the differences within CISPR Band B are less than 0.01 nF. In addition, since the power module is installed on the PCB during parasitic capacitance measurement, the measured C_{ph} includes C_{fs} according to Fig. 4(b).

On the other hand, the CM parasitic capacitances of passive devices are introduced by the distributed capacitance of the device leads and PCB traces to the ground. These capacitances can be measured directly. All the measured CM parasitic capacitances shown in Fig. 4(b) are listed in Table I.

TABLE I
SYSTEM PARASITIC PARAMETERS FOR CSI

Symbol	Descriptions	Value
C_s	Parasitic capacitance of the power module	14.52 nF
C_{cs}	Parasitic capacitance at the midpoint of C_{dc}	272 pF
C_{Ls}	Parasitic capacitance of L_{dc}	273 pF
$C_{ph}+C_{fs}$	Parasitic capacitance at the neutral point of C_f	254.5 pF

V. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Prototype and Experiment Setup

A 500-W prototype of CSI is built in the EMC laboratory with the parameters listed in Table II, which is shown in Fig. 9(a). And the test setup is shown in Fig. 9(b). The PV simulator (ITECH IT6018C) is adopted to provide dc power for the CSI, the maximum power point (MPP) voltage is 100 V, and the MPP current is 5 A.

For the purpose of the EMI test, a three-phase LISN (SCHWARZBECK NNLK 8121) is adopted to stabilize the line impedance of the ac power supply port. In addition, a high-frequency current probe (R&S EZ-17) is used to measure

TABLE II
SYSTEM PARAMETERS FOR CSI

Symbol	Descriptions	Value
C_{dc}	DC-link capacitance, C_{dc1}=C_{dc2}=C_{dc}	160 μF
L_{dc}	DC inductance, L_{dc1}=L_{dc2}=L_{dc}	5 mH
C_f	AC filter capacitance	20 μF
C_{pv}	PV panels parasitic capacitance, C_{pv} = C_{pv1} + C_{pv2}	44 nF
L_f	AC filter inductance	3 mH
u_{dc}	PV panels MPP voltage, u_{dc} =u_{dc1}+u_{dc2}	100 V
u_g	Gird voltage, RMS	380 V

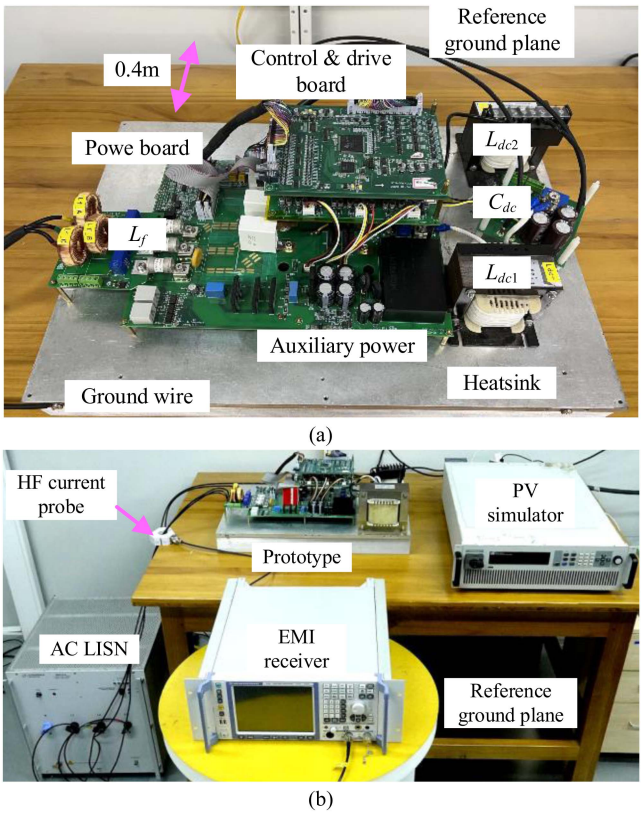

Fig. 9. Prototype and experiment setup photograph for three-phase PV CSI. (a) PV CSI prototype. (b) Test setup.

the CM current of the PV CSI, and an EMI test receiver (R&S ESR7) with a 9-kHz resolution bandwidth and a peak detector is used to obtain the EMI spectrum in the experiment.

The parasitic capacitance increases with the increase in the PV panel area [33], [34]. Compared with the real PV systems, the parasitic capacitance of the PV simulator is negligibly small. Thus, to match reality, extra capacitors are connected between the earth and the dc buses of CSI intentionally. In the following setup, two 22-nF film capacitors are used.

B. Leakage Current Equivalent Model Validation

Fig. 10 shows the simulation and experimental results of the leakage current. Fig. 10(a) shows the simulation result with (w/) and without (w/o) the neutral wire, and Fig. 10(b) shows the experimental ones. As seen, both the simulated and experimental waveforms show that the neutral wire has a significant

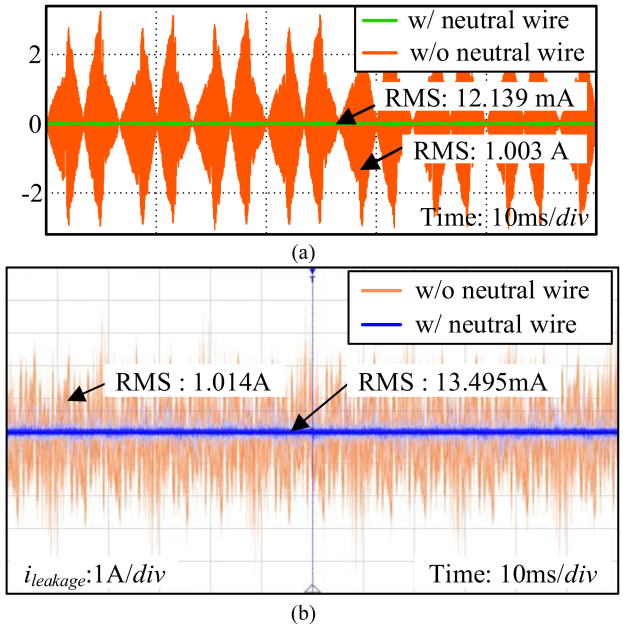

Fig. 10. Leakage current equivalent model validation. Leakage current i_{leakage} obtained from (a) equivalent model and (b) experimental rig.

suppression effect on the leakage current, which demonstrates the validity of the leakage current equivalent model. In addition, Fig. 10 also compares the leakage currents with and without the neutral wire (the CSI without the neutral wire means the conventional CSI). It is clear that the neutral wire is effective in suppressing the leakage current.

Fig. 11 shows the measured leakage currents at different switching frequencies. As illustrated in Fig. 11(a)–(c), the RMS values of the leakage current of the conventional CSI are 589.74, 671.75, and 786.15 mA when the switching frequencies are 10, 16, and 20 kHz, respectively. The results of the split-capacitor four-wire CSI are illustrated in Fig. 11(d)–(f), and the RMS values of the leakage current are 56.498, 71.547, and 79.237 mA, respectively, at corresponding switching frequencies. For clarity, the experimental results are summarized in Fig. 12. It can be found that the leakage current of the conventional CSI is significantly larger than that of the split-capacitor four-wire CSI. And the leakage current of the conventional CSI varies considerably with the switching frequency, whereas the leakage current of the four-wire CSI is almost unchanged.

C. CM EMI Equivalent Model Validation

In order to validate the CM EMI equivalent model, simulations and experiments have been conducted. First, a conventional EMI full circuit simulation is performed in the ANSYS Twin Builder environment, and the CM current spectrum at the grid port is obtained. Second, the predicted spectrum of the CM current is obtained by capturing the CM voltage source v_{cm} from the experimental rig with an oscilloscope and feeding it into the equivalent circuit model shown in Fig. 4(d). Finally, the spectrum of the CM current flowing through the LISN is directly measured with a high-frequency current probe and an

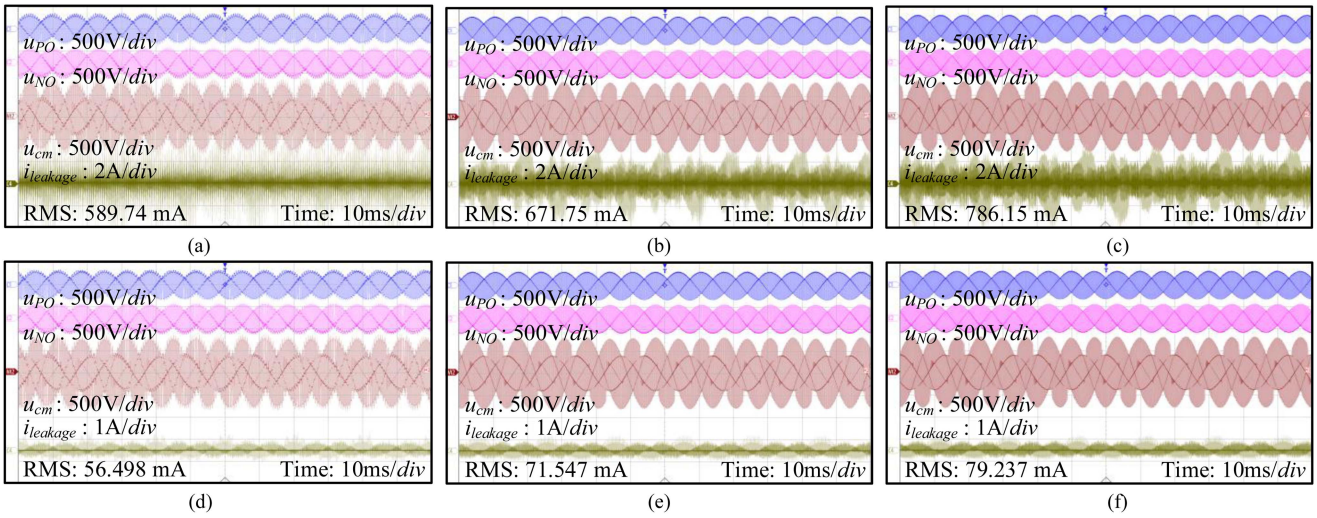

Fig. 11. Measured leakage currents at different switching frequencies. Conventional CSI at (a) 10, (b) 16, (c) 20 kHz. Split-capacitor four-wire CSI at (d) 10, (e) 16, and (f) 20 kHz.

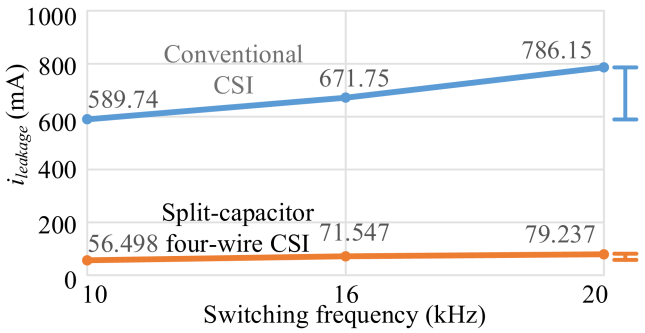

Fig. 12. RMS values of measured leakage currents at different switching frequencies.

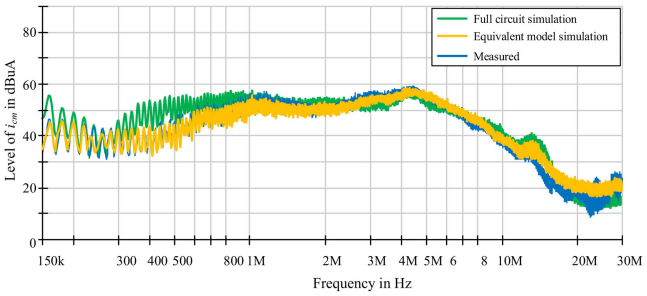

Fig. 13. CM EMI model validation. CM current spectra obtained from full circuit simulation, proposed equivalent model, and experimental rig.

EMI test receiver. The spectra of the CM current through the above-mentioned three methods are shown in Fig. 13. As can be seen, the CM current spectrum of the equivalent model fits well with those of the full circuit simulation and experimental measurements. Because the $v_{\rm cm}$ captured by the oscilloscope reflects the nonideal effects of the CSI, and the rise and fall times of the switches are considered in the full circuit simulation, the difference between the spectra of the three CM currents is small. Especially, the difference between the simulated and measured

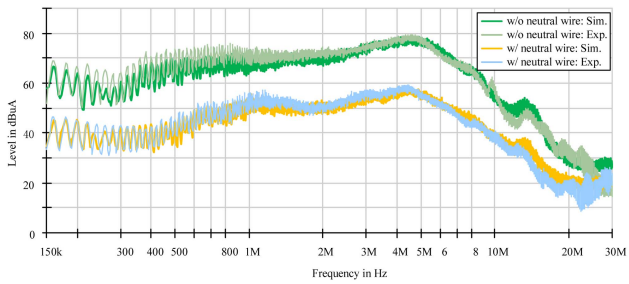

Fig. 14. CM EMI spectrum for conventional CSI and split-capacitor four-wire CSI.

spectrum is within 3.6 dB, which is within the uncertainty limits specified in [35]. Thus, it is safe to say that the simulation results are consistent with the experiments, and the differences can be attributed to the measurement uncertainties.

Fig. 14 shows the simulated and measured CM EMI spectra of the conventional CSI and the split-capacitor four-wire CSI. It is clear that the neutral wire is effective to reduce CM EMI, and about 20 dB attenuation over the frequency range (150 kHz, 25 MHz) is obtained.

Fig. 15 shows the measured CM EMI spectra before and after increasing the 1-mH dc inductance. Fig. 15(a) shows the results of the conventional CSI. As can be seen, increasing the dc inductance can slightly attenuate CM EMI. Fig. 15(b) shows the results of the split-capacitor four-wire CSI. It is found that increasing dc inductance, in this case, has little contribution to CM EMI attenuation. Clearly, the experimental results agree well with the theoretical analysis.

Fig. 16 shows the CM EMI measurement results with and without improvement approaches by changing parameters C_{cs} and C_{fs} (in this study, a 68-nF capacitor is connected in parallel with C_{cs} or C_{fs}). Fig. 16(a) illustrates the CM EMI measurement results of the conventional CSI. As can be seen, increasing C_{cs} deteriorates the CM EMI spectrum of the conventional CSI, but increasing C_{fs} is an effective way to reduce the level of CM

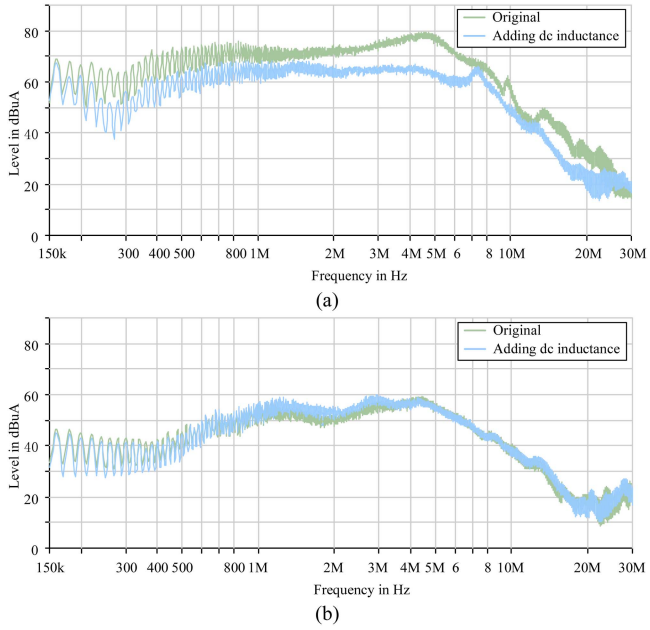

Fig. 15. CM EMI spectrum with increasing DC inductance. (a) Conventional CSI. (b) Split-capacitor four-wire CSI.

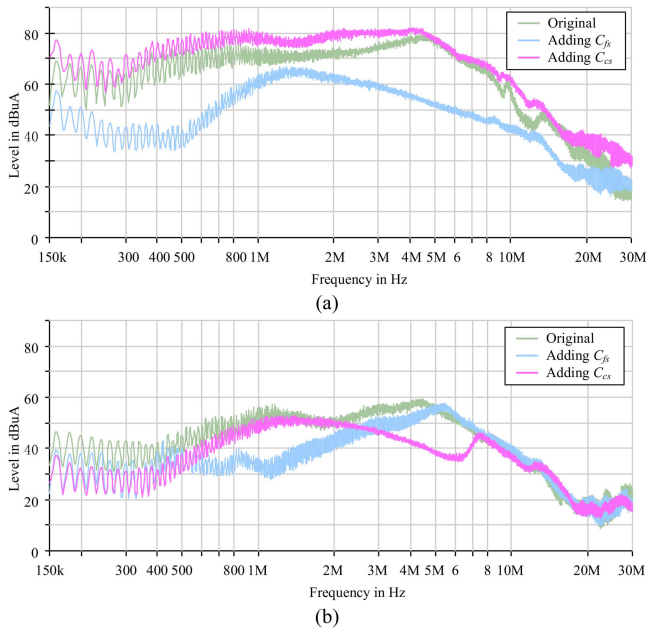

Fig. 16. CM EMI model validation with increasing parasitic capacitance (C_{cs} and C_{fs}). (a) Conventional CSI. (b) Split-capacitor four-wire CSI.

EMI. Fig. 16(b) illustrates the CM EMI measurement results of the split-capacitor four-wire CSI. It is found that the CM EMI could be attenuated by increasing C_{fs} or C_{cs} in split-capacitor four-wire CSI. Clearly, the experimental results in Fig. 16 are also consistent with the analysis presented before.

VI. Conclusion

In this article, the CM equivalent models of the PV CSI with or without neutral wire for analysis of the leakage current and conducted CM EMI are developed. It is verified that leakage current and CM EMI are closely related to the CM circuit. Due to the fact that the frequency bands involved are far apart, the differences in the factors affecting them are also revealed. Moreover, some suppression measures for leakage current and CM EMI are derived spontaneously. Based on the established models, the leakage current and CM EMI can be predicted with satisfactory accuracy and less computational consumption. By comparison, it is also verified that connecting a neutral wire is effective to reduce both leakage current and CM EMI.

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