Letters

Analysis and Design of a Cost-Effective Single-Input and Regulatable Multioutput WPT System

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***Abstract*—In this letter, a single-input and regulatable multioutput wireless power transfer system is presented. In particular, the system uses positive and negative half-wave rectifiers and a synchronous rectifier to realize multiple output channels. Each output channel is controllable, providing a flexible wireless charger to meet various charging requirements. Moreover, this system utilizes the inherent half-wave-rectifier channels (#B and #C) to detect synchronous signals for the rectifiers rather than using additional synchronous detection circuits, thereby leading to a cost-effective system. Finally, a 300 W laboratory prototype is contrasted with three voltage levels, i.e., 48, 30, and 24 V. With the help of the control logic, this system shows excellent robustness against different occasions, such as load variations, input disturbance, and misalignment. The overall efficiency ranges from 86.7% to 90.6%.**

***Index Terms*—Single-input and regulatable multioutput (SIRMO), synchronous rectifier, wireless power transfer (WPT).**

I. INTRODUCTION

WIRELESS power transfer (WPT) is a practical technology that contributes to a wide range of applications, such as smartphones and electric vehicles [1]. Single-input-and-single-output (SISO) WPT system has been widely investigated because of its simplicity [2]. In this digital age, electric appliances have become more and more complicated. It is quite challenging for traditional SISO WPT to meet the multiple output charging target requirements. Therefore, the industry is calling for emerging wireless chargers equipped with multiple outputs.

To achieve multiple outputs, one way is to increase the number of transmission paths by using multi-input-and-multioutput (MIMO) systems [3]. This means that a large number of transmitting and receiving equipment are involved in achieving multiple charging paths.

To save cost, simplify the structure, and reduce the cross-coupling phenomenon caused by MIMO systems [4], it is more popular to adopt the single-input-and-multioutput (SIMO) WPT systems nowadays. One way to realize it is by single-T [5] or double-T [6] resonant circuits, which can achieve voltage or current conversion by configuring the passive components, such as inductors and capacitors. However, such passive topologies are difficult to adjust output voltages or currents during the charging process. Therefore, some scholars have adopted dc–dc converters [7]. Although dc–dc converters meet different charging requirements with varying outputs, they are still bulky as well as requiring much additional installation space. That is why recent investigations gradually integrate dc–dc converters into rectifiers, i.e., active bridge rectifiers, to further save space and improve compactness. One promising application based on the active rectifiers should be single-input and dual-output (SIDO) WPT system [8]. Such a SIDO system can simultaneously realize dual regulatable outputs, which can charge the driving system and control system of automatic-guided vehicles.

To further improve the performance of the SIMO WPT system, this letter presents a SIMO WPT system based on the different types of rectifiers, including one synchronous rectifier and two half-wave rectifiers. Three regulatable output channels are successfully built. The potential application scenarios can be hybrid energy storage system and other systems, which usually require three controllable voltages [7]. In summary, the contributions and advantages of this letter can be summarized as follows.

1) Single-input and regulatable multioutput (SIRMO): Different from the article presented in [7], the presented work considers both half-wave and full-wave rectifiers to ensure the SIRMO. Three output channels (#A, #B, and #C) are holistically considered. Specifically, channel #A is installed with a synchronous rectifier, while channels #B and #C are equipped with half-wave rectifiers utilizing the positive and negative half periods of the ac voltage source, respectively.

Manuscript received 29 January 2023; revised 3 March 2023; accepted 21 March 2023. Date of publication 27 March 2023; date of current version 20 April 2023. This work was supported by the National Natural Science Foundation of China under Grant 52007012. *(Corresponding authors: Xiaofei Li; Heshou Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3262027.

Digital Object Identifier 10.1109/TPEL.2023.3262027

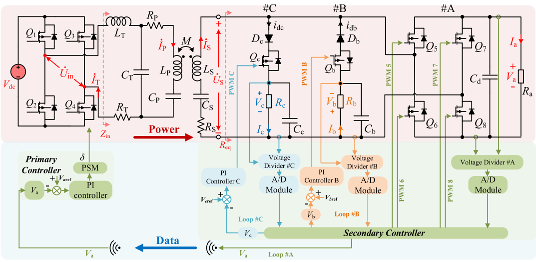
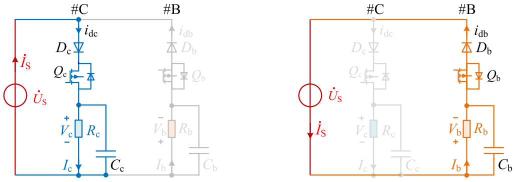


Fig. 1. Entire circuit diagram of the presented WPT system.



(a) (b)

Fig. 2. Equivalent circuit of the presented WPT system. (a) Positive half period. (b) Negative half period.

2) Synchronous signal detection: In this letter, the benefits of the half-wave rectifiers (Rectifier #B and #C) go far beyond the multiple outputs. They also serve as synchronous signal detection [i.e., finding the zero-cross points (ZCPs)] to provide synchronous signals for the synchronous rectifier. Compared with the article presented in [8], the presented structure saves valuable space on the secondary side since there are no additional detecting circuits or sensors for synchronous rectification, thereby leading to a compact and cost-saving system.

II. Circuit Topology and System Control

A. Circuit Topology

Fig. 1 illustrates the circuit scheme of the presented WPT system, which utilizes the inductor–capacitor–capacitor-series (*LCC*-S) compensation topology. L_T, L_P, and L_S are the compensation coil, transmitter coil, and receiver coil, respectively. R_T, R_P, and R_S are the parasitic resistances of L_T, L_P, and L_S, respectively. Q_5, Q_6, Q_7, and Q_8 constitute the synchronous rectifiers. And for the synchronous rectifier, usually, the switching sequence shall be synchronized with the current direction, i.e., Q_5 (Q_6) and Q_8 (Q_7) should be ON (OFF) state when i_S is positive; Q_6 (Q_5) and Q_7 (Q_8) should be ON (OFF) state when i_S is negative [9]. For the positive half-wave rectifier (i.e., #C), the output voltage can be controlled when i_S is positive, while for the negative half-wave rectifier (i.e., #B), the output voltage can be controlled when i_S is negative.

C_T, C_P, and C_S are the compensation capacitors that satisfy the following equations:

$$C_T=\left(\omega^2 L_T\right)^{-1}, C_P=\left[\omega^2\left(L_P-L_T\right)\right]^{-1}, C_S=\left(\omega^2 L_S\right)^{-1} \tag{1}$$

where ω is the operating angular frequency of the inverter, which satisfies $\omega = 2\pi f$. Besides, C_b, C_c, and C_d are the output capacitors in three output channels, which are all selected as large enough as 220 μF. Thus, the dc outputs are relatively constant [8].

Since most of the higher order harmonics are trapped in the resonant circuit [5], to simplify the analysis, only the fundamental component is considered in this letter. Phase-shifted modulation (PSM) is used to control the inverter, and the fundamental inverter output voltage in phasor form can be written as follows [6]:

$$\dot{U}_{\text{in}} = \frac{2\sqrt{2}V_{\text{dc}}}{\pi}\sin\frac{\delta}{2}\angle 0^\circ \tag{2}$$

where δ is the conduction angle.

By using Kirchhoff voltage law, the following equations can be derived:

$$\begin{cases}\dot{U}_{\text{in}} = \left(jX_{LT}+R_T-jX_{CT}\right)\dot{I}_T + jX_{CT}\dot{I}_P\\ 0=\left(jX_{LP}+R_P-jX_{CP}-jX_{CT}\right)\dot{I}_P+jX_{CT}\dot{I}_T-jX_M\dot{I}_S\\ 0=-jX_M\dot{I}_P+\left(jX_{LS}+R_S-jX_{CS}\right)\dot{I}_S+\dot{U}_S\\ \dot{U}_S = R_{\text{eq}}\dot{I}_S\end{cases} \tag{3}$$

where

$$\begin{cases}X_{LT}=\omega L_T \quad X_{CT}=1/\omega C_T \;\; X_{LP}=\omega L_P \quad X_{CP}=1/\omega C_P\\ X_{LS}=\omega L_S \;\; X_{CS}=1/\omega C_S \;\; X_M=\omega M \;\; R_{\text{eq}}=R_{\text{eqa}}||R_{\text{eqb}}||R_{\text{eqc}}\end{cases} \tag{4}$$

and $R_{\text{eq }a}$, $R_{\text{eq }b}$, and $R_{\text{eq }c}$ are the equivalent input resistance of the three rectifiers (i.e., rectifiers #A, #B, and #C, respectively), which can be obtained as follows [8]:

$$R_{\text{eqa}} = \tfrac{8}{\pi^2}R_a, \quad R_{\text{eqb}} = \tfrac{U_S^2}{V_b^2}R_b, \quad R_{\text{eqc}} = \tfrac{U_S^2}{V_c^2}R_c \tag{5}$$

where V_b and V_c are the output voltages of half-wave-rectifier channels #B and #C, respectively. R_a, R_b, and R_c are the output resistances of the three output channels (#A, #B, and #C). U_S is the root-mean-square value of $\dot{U}_S$.

Substituting (1), (2), and (4) into (3), one can obtain the following:

$$\begin{cases}\dot{U}_S = \frac{X_M X_{CT}\dot{U}_{\text{in}}R_{\text{eq}}}{\left(R_{\text{eq}}+R_S\right)\left(2R_P R_T+X_{CT}^2\right)+R_T X_M^2}\\ \dot{I}_T = \frac{\dot{U}_{\text{in}}\left(2R_{\text{eq}}R_P+2R_P R_S+X_M^2\right)}{\left(R_{\text{eq}}+R_S\right)\left(2R_P R_T+X_{CT}^2\right)+R_T X_M^2}.\end{cases} \tag{6}$$

In terms of output channel #A, according to the relationship between the input and output voltage of the synchronous rectifier [6], V_a can be expressed as follows:

$$V_a = \sqrt{2}\pi U_s/4. \tag{7}$$

Fig. 2 indicates the equivalent circuit of output channels #B and #C, where $\dot{U}_S$ is the bus voltage. The output voltage of channel #C can be expressed as follows:

$$V_c=\frac{1}{2\pi}\int_0^{2\pi D_{Qc}}\sqrt{2}U_s\sin(\omega t)d\omega t=\frac{\sqrt{2}U_s}{2\pi}\left(1-\cos\left(2\pi D_{Qc}\right)\right) \tag{8}$$

where D_{Qc} is the duty cycle of pulsewidth modulation (PWM) C (i.e., the drive signal of Q_c) in the positive half period. Similarly,

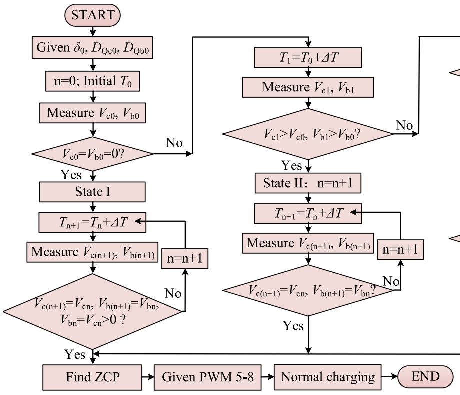


Fig. 3. Flowchart for synchronous signal detection and system charging.

the output voltage of channel #B can be expressed as follows:

$$V_b = -\frac{1}{2\pi}\int_{\pi}^{\pi+2\pi\cdot D_{Qb}} \sqrt{2}U_s \sin(\omega t)d\omega t$$
$$= \frac{\sqrt{2}U_s}{2\pi}\left(1-\cos\left(2\pi D_{Qb}\right)\right) \qquad (9)$$

where D_{Qb} is the duty cycle of PWM B (i.e., the drive signal of Q_b) in the negative half period.

As can be seen from (7)–(9), V_a, V_c, and V_b are all affected by bus voltage (i.e., $\dot{U}_S$). When the bus voltage is determined, V_c and V_b can be controlled independently.

The output impedance of the inverter can be calculated as follows:

$$Z_{\text{in}} = \frac{\dot{U}_{\text{in}}}{\dot{I}_T} = \frac{(R_{\text{eq}}+R_S)(2R_PR_T+X_{CT}^2)+R_TX_M^2}{(2R_{\text{eq}}R_P+2R_PR_S+X_M^2)}. \qquad (10)$$

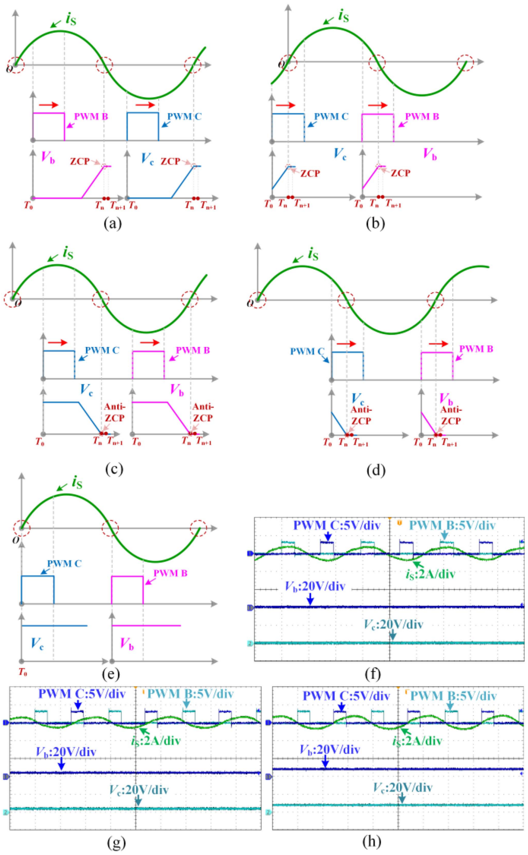
By calculating (4), (5), (8), and (9), R_{eq} can be obtained as follows:

$$R_{\text{eq}} = \frac{8\pi^2R_aR_bR_c}{\pi^4R_bR_c+(2\cos(2\pi D_{Qb})-2)^2R_aR_c+(2\cos(2\pi D_{Qc})-2)^2R_aR_b}. \qquad (11)$$

As can be seen from (10) and (11), since R_{eq} is purely resistive, Z_{in} is also purely resistive, indicating that the whole system can achieve input zero phase angle (ZPA) [6].

B. Synchronous Signal Detection

The flowchart for synchronous signal detection and system charging is shown in Fig. 3. Before the normal charging, it is necessary for the system to find the ZCPs first. After that, the synchronous drive signals PWM 5, PWM 6, PWM 7, and PWM 8 can be given. The system enters into the normal charging stage. And V_a, V_b, and V_c can be regulated by controlling δ, D_{Qb}, and D_{Qc}. As shown in Fig. 3, the conduction angle δ and duty ratios D_{Qc} and D_{Qb} are set as δ_0, D_{Qc0}, and D_{Qb0} to initialize the system by transferring a small amount of energy to the receiver for synchronous signal detection.



(a) (b) (c) (d) (e) (f) (g) (h)

Fig. 4. Diagram of i_S, driving signals (PWM C and PWM B), and the variation of V_c and V_b for synchronous signal detection. (a) State I. (b) State II. (c) State III. (d) State IV. (e) End state of synchronous signal detection. (f) Starting waveform of state I in the experiment. (g) Intermediate waveform of state I in the experiment. (h) End waveform of state I in the experiment.

Because the primary controller and secondary controller are not synchronized, the initial time reference T_0 of PWM C and PWM B is random, which can be given in Fig. 4(a)–(d). This letter moves the time reference of PWM C and PWM B to search out ZCPs for the synchronous rectifier. The ultimate state is shown in Fig. 4(e), where PWM C and B find out the positive and negative half-wave ZCPs, respectively. ΔT is the step change of time references, which is selected as 20 ns in this letter. By accumulating the count number n, the next-step voltages

($V_{c(n+1)}$ and $V_{b(n+1)}$) are measured and compared with the previous ones (V_{cn} and V_{bn}).

ZCPs for Fig. 4(a)–(d) can be found as follows.

1) As shown in Fig. 4(a), if $V_{c0} = V_{b0} = 0$, the state is confirmed as state I. Then, the time reference would not keep adjusting until $V_{c(n+1)} = V_{cn} = V_{b(n+1)} = V_{bn} > 0$. As a result, the correct ZCPs can be found at the time T_n.
2) As shown in Fig. 4(b), if $V_{c1} > V_{c0}$ and $V_{b1} > V_{b0}$, the state is confirmed as state II. Then, the time reference would not keep adjusting until $V_{c(n+1)} = V_{cn}$ and $V_{b(n+1)} = V_{bn}$. As a result, the correct ZCPs can be found at the time T_n.
3) As shown in Fig. 4(c), if $V_{c1} = V_{c0} > 0$ and $V_{b1} = V_{b0} > 0$, the state is confirmed as state III. Then, the time reference would not keep adjusting until $V_{c(n+1)} = V_{cn} = V_{b(n+1)} = V_{bn} = 0$. As a result, the anti-ZCPs can be found at the time T_n. It should be noted that the phase difference between ZCP and anti-ZCP is 180°. Thus, the corresponding ZCPs can be found by shifting 180° phase angle.
4) As shown in Fig. 4(d), if $V_{c1} < V_{c0}$ and $V_{b1} < V_{b0}$, the state is confirmed as state IV. Similar to Fig. 4(c), the time reference would not keep adjusting until $V_{c(n+1)} = V_{cn} = V_{b(n+1)} = V_{bn} = 0$. The correct anti-ZCPs can be found at the time T_n. Similarly, the corresponding ZCPs can be found by shifting 180° phase angle.

Fig. 4(f)–(h) show the experimental starting waveform, intermediate waveform, and end waveform of state I to find the ZCPs. By comparing Fig. 4(f)–(h) with Fig. 4(a), it can be seen that the change characteristics of V_c and V_b can well correspond, and two PWM signals (PWM B and PWM C) can capture ZCP almost without deviation, which verifies that the proposed system can achieve synchronous signal detection.

C. System Control

The control logic of the proposed system is shown in Fig. 1. There are two controllers, i.e., the primary controller and the secondary controller. Furthermore, there are three closed control loops in the presented system, including one outer loop (Loop #A) to regulate V_a and two inner loops (Loop #B and Loop #C) to regulate V_b and V_c.

In terms of outer control loop #A, the secondary controller samples the output voltage V_a by using the A/D module after the voltage divider and then transfers it to the primary side. The primary controller picks up the information of V_a. The error between V_a and the reference V_{aref} is sent to the proportion–integral (PI) controller, and then, the processed result is delivered to the PSM controller for conduction angle δ calculation for regulating $\dot{U}_S$ and thus V_a. As for inner control loops #B and #C, the secondary controller samples the output voltage V_b and V_c by adopting the A/D module after the voltage divider. Error information (V_b and V_{bref}, and V_c and V_{cref}) are sent to their PI controller, respectively, and then voltages V_b and V_c can be regulated by controlling D_{Qb} and D_{Qc}, respectively. It can be seen the loop #A can affect the output bus voltage ($\dot{U}_S$); therefore, adjusting V_a will also cause changes in V_b and V_c. As for loops #B and #C, they can only regulate V_b and V_c, respectively.

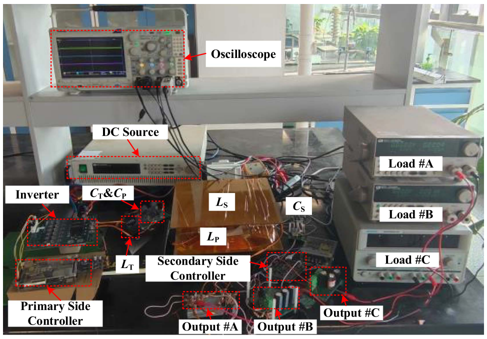


Fig. 5. Photograph of the experimental prototype.

TABLE I
SYSTEM PARAMETERS

V_{dc}	L_T	L_P	L_S	R_T
80 V	43.3 μH	104 μH	103 μH	0.12 Ω
R_S	C_T	C_P	C_S	R_P
0.26 Ω	81 nF	58 nF	34 nF	0.26 Ω
V_a	V_b	V_c	f	M
48 V	30 V	24 V	85 kHz	32.4 μH

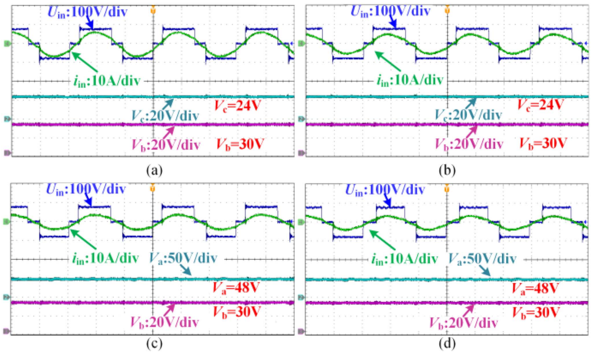


Fig. 6. Diagram of the ZPA validation. (a) $R_a = 10\ \Omega$ and $R_b = R_c = 20\ \Omega$. (b) $R_a = 10\ \Omega$ and $R_b = R_c = 30\ \Omega$. (c) $R_a = 20\ \Omega$ and $R_b = R_c = 20\ \Omega$. (d) $R_a = 20\ \Omega$ and $R_b = R_c = 30\ \Omega$.

III. EXPERIMENTAL VALIDATION

A. Experimental Prototype

In order to verify the feasibility of the proposed SIRMO WPT system, an experimental prototype is fabricated, as demonstrated in Fig. 5. The parameters of the system are listed in Table I.

B. ZPA Validation

Fig. 6 illustrates the output voltage and current of the inverter (u_{in} and i_{in}) and the dc voltage outputs when (a) $R_a = 10\ \Omega$ and $R_b = R_c = 20\ \Omega$, (b) $R_a = 10\ \Omega$ and $R_b = R_c = 30\ \Omega$, (c) $R_a = 20\ \Omega$ and $R_b = R_c = 20\ \Omega$, and (d) $R_a = 20\ \Omega$ and $R_b = R_c = 30\ \Omega$. As can be seen from Fig. 6, u_{in} and i_{in} are in the

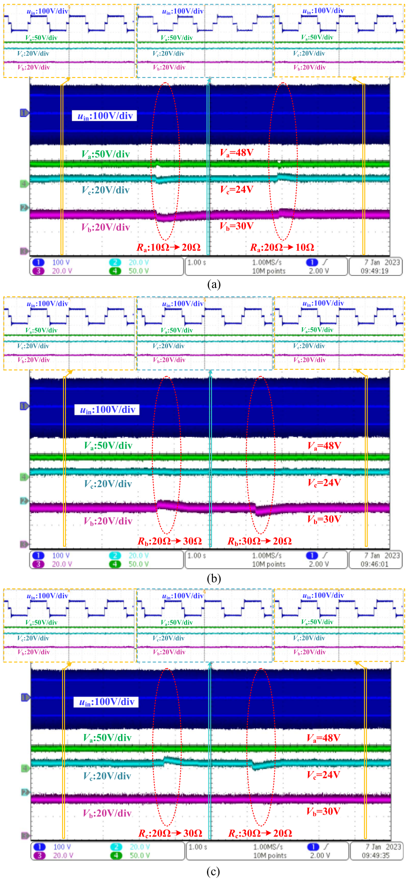


Fig. 7. Dynamic response. (a) When R_a changes from 10 to 20 Ω and back to 10 Ω. (b) When R_b changes from 20 to 30 Ω and back to 20 Ω. (c) When R_c changes from 20 to 30 Ω and back to 20 Ω.

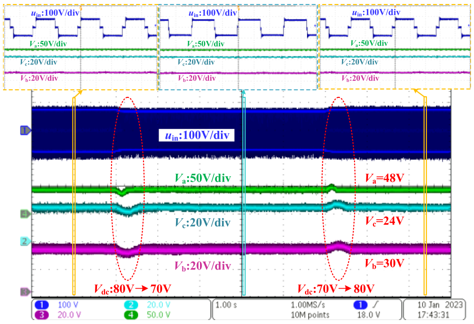


Fig. 8. Dynamic response to the input disturbance.

same phase regardless of the change of R_a, R_b, and R_c, which indicates that the inverter can achieve ZPA and the circulation of the reactive power is not significant [6].

C. Dynamic Response Under Load Variation Conditions

Fig. 7(a)–(c) illustrate the dynamic response when the load changes in the outer loop (Loop #A) and two inner loops (Loop #B and Loop #C), i.e., R_a, R_b, and R_c, respectively. Fig. 7(a) depicts that the change of outer loop #A's load (R_a) affects not only itself but also two inner loops (Loop #B and Loop #C). It shows that R_a is changed from 10 to 20 Ω and back to 10 Ω again.

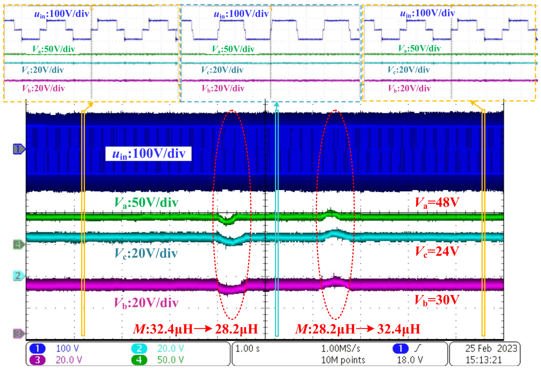


Fig. 9. Dynamic response when *M* changes.

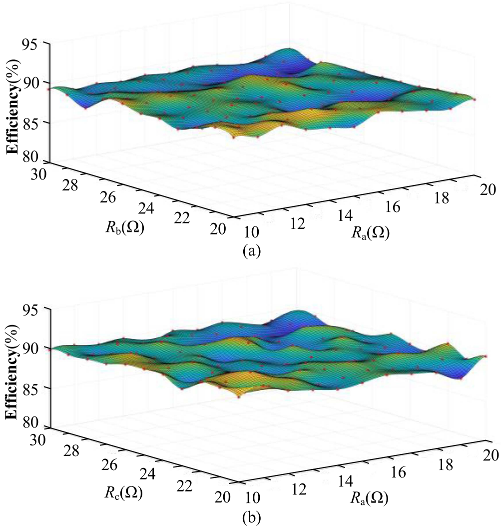


Fig. 10. Measured efficiency results correspond to changes in (a) R_a and R_b and (b) R_a and R_c.

And all the voltages can be controlled to their reference values, i.e., 48, 30, and 24 V. Fig. 7(b) depicts that the change of inner loop #B's load (R_b) only affects itself. It shows that R_b is changed from 20 to 30 Ω and back to 20 Ω again. Itself voltage V_b can be maintained at 30 V with a small over/undershoot. And there is almost no change for V_a and V_c. Similarly, Fig. 7(c) depicts that the change of inner loop #C's load (R_c) only affects itself. It shows that R_c is changed from 20 to 30 Ω and back to 20 Ω again. Itself voltage V_c can be maintained at 24 V with a small over/undershoot. And there is almost no change for V_a and V_b.

D. Disturbance Rejection

Fig. 8 depicts the input disturbance rejection response of the system. The input voltage varies from 80 to 70 V and then back to 80 V again. Due to the control strategy, the presented system can maintain the three voltages at 48, 30, and 24 V, respectively.

Fig. 9 shows the dynamic response of the system when misalignment occurs, i.e., mutual coupling (*M*) varies. *M* varies from 32.4 to 28.2 μH and then back to 32.4 μH again. As can be seen from Fig. 9, the three voltages can be controlled at the target values of 48, 30, and 24 V, respectively.

TABLE II
COMPARISONS BETWEEN THIS LETTER AND THE ARTICLES PRESENTED IN [3], [4], [5], [6], [7], AND [8]

Ref	Method	Output Channels	Volume and Cost	Efficiency	Characteristic
[3]	MIMO	6	High	45.1%	Multiple transmitting and receiving coils
[4]	SIMO with multiple receivers	2	High	84.5%	Multiple receiver coils
[5]	SIMO with multiple single-T resonant circuits	2	High	89.3%	Multiple high-order single T-compensation networks
[6]	SIMO with multiple double-T resonant circuits	2	High	91.1%	Multiple high-order double T compensation networks
[7]	SIMO with multiple DC/DC converters	3	High	85%	Regulable multiple outputs (RMOs) with DC/DC converters
[8]	SIMO with multiple active rectifiers	2	Med	90.9%	RMO; Using hall current sensor
This letter	SIMO with multiple active rectifiers	3	Low	90.6%	SIRMO; Two type rectifiers without additional sensors

The measured efficiency results that correspond to load variations are shown in Fig. 10, where Fig. 10(a) shows the results correspond to changes in R_a and R_b while $R_c = 20\ \Omega$; Fig. 10(b) shows the results correspond to changes in R_a and R_c while $R_b = 20\ \Omega$. As can be seen from Fig. 10, the overall efficiency ranges from 86.7% to 90.6%.

IV. DISCUSSION

A comparison between this letter and the articles presented in [3], [4], [5], [6], [7], and [8] is summarized in Table II. Compared with the articles presented in [3] and [4], the proposed method can realize multiple outputs with only one receiver coil, saving space and cost, and avoiding cross coupling between multiple receivers. Compared with the articles presented in [5] and [6], the proposed method can achieve multiple outputs without using a large number of high-order compensation networks on the receiver side, such as single-T or double-T topology, so its volume and cost are considerable. Besides, unlike the passive topologies in [5] and [6], the proposed method can achieve multiple controllable outputs. Compared with the article presented in [7], the proposed method realizes multiple regulable outputs through active rectifiers instead of dc/dc converters. Therefore, the volume and cost of the proposed method are more advantageous. Compared with the article presented in [8], the proposed method utilizes the inherent half-wave-rectifier channels (#B and #C) to detect synchronous signals for the rectifiers rather than using additional synchronous detection circuits, thereby leading to a volume-saving and cost-effective system. As for the efficiency, the efficiency of this letter is close to that of the articles presented in [6] and [8] but higher than that of the articles presented in [3], [4], [5], and [7].

V. CONCLUSION

This letter presents a SIRMO (WPT) system. Three regulatable output channels are successfully built. Different types of rectifiers are thoroughly considered, including one synchronous rectifier and two half-wave rectifiers. Moreover, this system utilizes the inherent half-wave-rectifier channels (#B and #C) to detect synchronous signals. A 300 W laboratory prototype is contrasted with three voltage levels, i.e., 48, 30, and 24 V. The experimental results show that adjusting V_a will also cause changes in V_b and V_c. As for the closed loops #B and #C, they can only regulate V_b and V_c, respectively. With the help of the control logic, this system shows excellent robustness against different occasions, such as load variations, input disturbance, and misalignment. The overall efficiency ranges from 86.7% to 90.6%.

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