An Intuitive and Noniterative Design Methodology for CLLC Chargers Employing Simplified Operation Modes Model

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***Abstract*—This article mainly focuses on the simplified operation modes (SOM) model and resonant parameter design for the CLLC charger. Based on the mathematical and detailed operation waveform assumptions, the voltage gain model expressions and the operation mode boundaries are calculated directly, providing the high efficiency and high reliability of the CLLC converter. The proposed SOM model is more accurate in depicting the voltage gain compared with the conventional fundamental harmonic approximation model. Moreover, the SOM model is more intuitive and has less computational complexity than the complicated and unsolvable time-domain model. As for the parameter design process, the inductance ratio k and characteristic impedance Z_0 are selected instead of specific inductances and capacitances. Relying on the SOM model, a step-by-step parameter design methodology is studied, which avoids repetitive iterations and streamlines the procedure. The voltage gain range, efficiency, soft-switching operation, mode boundaries, and system stability are considered comprehensively and realized in this process. The simulations and experiments validate that the proposed SOM model is accurate, and the design methodology is straightforward through a 1-kW CLLC charger prototype with 97% peak efficiency.**

***Index Terms*—Characteristic impedance, CLLC converter, inductance ratio, simplified operation modes (SOM) model.**

I. Introduction

THE isolated bidirectional dc–dc converters (IBDCs) play essential roles in electric vehicles charging, dc microgrids, data center power supplies, and energy storage systems (ESSs), etc [1], [2], [3], [4], [5]. One of the promising IBDC candidates is the CLLC converter due to its high conversion efficiency, excellent full range of soft-switching characteristics, high flexibility, and low electromagnetic interference [6], [7], [8]. Besides, compared with the conventional LLC resonant converters, the CLLC converter can realize bidirectional boost and buck mode operation.

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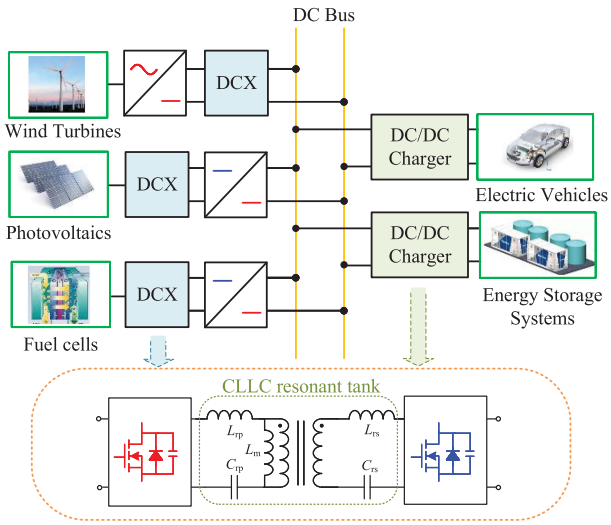


Fig. 1. Applications of the CLLC converter.

The applications of the CLLC converter can be classified into the CLLC dc transformers (DCXs) and the CLLC dc chargers, as shown in Fig. 1. For the CLLC-DCX, the switching frequency is close to or equal to the resonant frequency. As a result, the major functions such as galvanic isolation and constant voltage gain can be achieved [9]. To widen the output voltage range, two-stage structures like CLLC-DCX+dc/dc [10] or ac/dc+CLLC-DCX [11] are commonly used. For the CLLC dc chargers, the pulse frequency modulation (PFM) method is always employed to widen the output voltage range. In this application, high system efficiency and excellent reliability are required. However, it is challenging to find the appropriate resonant parameters (two inductors, one transformer, and two capacitors involved in the resonant tank) that give CLLC converters good performance.

The existing research regarding the parameter optimization of the CLLC converter can be cataloged into two the following main methods: 1) first harmonic approximation (FHA)-based; 2) time-domain model (TDM)-based parameter design methods. The FHA-based method is simple and straightforward, where the relationship between the voltage gain and the switching frequency is easy to obtain [12], [13], [14]. The idea of the FHA-based method is to decompose the square wave voltage using Fourier decomposition. In this process, the high-order component is

ignored, and only the effect of the fundamental harmonic is considered. The accuracy of the FHA model is acceptable when the CLLC converter works near the resonant frequency. This is because the current and voltage waveforms in the resonant tank are close to the sine wave, so the higher-order harmonics can be neglected. Therefore, the FHA model is adopted in the CLLC-DCX application, where narrow frequency and output voltage regulation ranges are needed. Huang et al. [15] proposed a robust circuit parameters design scheme considering the real inductances and capacitances variation. [16] focused on the resonant frequency, considering the power loss optimization based on the artificial intelligence algorithm. In contrast to the conventional symmetrical parameters design method, [17] proposed a detailed asymmetric parameter methodology, narrowing the switching frequency range and reducing power loss. Similarly, [18] illustrated a semiAI-based asymmetric parameters design approach that can achieve against the parameter variations and ensure good power transfer ability. However, one of the FHA model's disadvantages is that the approximation results are not accurate enough when the operation frequency is far from the resonant frequency. The approximation will cause significant obstacles in optimizing the parameters of the dc charger. To improve the accuracy of the FHA model, considering the influence of higher odd-order harmonics, [19] proposed an extended harmonics approximation-based parameters method. Nevertheless, the accuracy is still unsatisfactory.

To improve the gain model's accuracy, a more precise TDM-based analytical method known as operation mode analysis (OMA) is proposed. The resonant voltage and current expressions for a specific resonant model can be adequately obtained, and then the operating characteristic can be determined. The operating modes under various frequency and load conditions can be obtained by combining the operation stages at different times in the time-domain [20]. Then, the time domain solutions can be derived by combining the boundary conditions. However, although OMA improves analytical accuracy, the implied nonlinear relationship with trigonometric items makes the visualized gain model solution problematic. Although examining the parameters individually across the satisfactory parameter range may be a viable strategy, the high calculation cost makes this method difficult to implement. Hence, some modified TDM-based methods are proposed for the LLC and CLLC converters to simplify the computation. Fang et al. [21] provided an approximation method for peak gain estimation. Liu et al. [22] proposed a modified gain model obtained by combining frequency domain and time-domain analysis. However, this model is inadequate since only switching frequencies below the resonant frequency are examined. Cao et al. [23] introduced a simplified TDM-based gain model based on the superposition principle and the energy conservation law. Zhao et al. [24] proposed a design methodology of CLLC based on parameter equivalent principle and time-domain model. To summarize, the prior research's computation amount employing TDM-based approaches is still huge, and iteration is mandatory and unavoidable, which makes it challenging to implement the design process in practice. Another modeling method could also be employed to analyze the resonant converter that is the Laplace-related methods [25], [26]. In [26], a generalized Laplace-based steady-state modeling (LBSM) method is proposed to determine accurate closed-form steady-state solutions for a broad class of power converters. Nevertheless, the method per se is still complex To summarize, the comparison results among the previously discussed modeling methods are listed in Table I.

TABLE I
COMPARISON AMONG THE MODELING METHODS

	FHA	OMA	LBSM	**SOM**
Domain	Frequency	Time	Laplace	**Time**
Accuracy	⋆	⋆⋆⋆⋆	⋆⋆⋆⋆	⋆⋆⋆
Simplicity	⋆⋆⋆⋆	⋆	⋆	⋆⋆⋆
Applicable to DCM	No	Yes	Yes	**Yes**
Symbolic solution	Yes	No	Yes	**Yes**

DCM: discontinuous conduction mode
The bold entities are the method proposed by this research.

In conclusion, with the tradeoff between model accuracy and calculation difficulty in mind, a novel simplified gain model with operation boundaries is proposed in this research. In this process, some necessary approximations are considered to solve the time-domain expressions. The main contributions of this article can be summarized as follows.

1) An accurate and low-computation SOM model for the CLLC converter is proposed. Compared with the inaccurate FHA model and the complicated TDM, this presented SOM model is more accurate and straightforward due to the mathematical and detailed operation waveform assumptions. Moreover, the operation boundaries are also investigated, which is vital to ensure reliability and efficiency in the operation of CLLC converters.
2) An intuitive and comprehensive parameter design procedure for the CLLC converter is proposed. Based on the previously introduced SOM model, a step-by-step illustration of the parameter design methodology without iteration using the inductance ratio k and characteristic impedance Z_0 is demonstrated. Besides the essential voltage gain requirement, in this procedure, soft switching, system stability, efficiency, current/voltage stress, and reliability are also taken into consideration to attain excellent system performance.

The rest of this article is organized as follows. Section II presents the SOM model. Section III introduces the parameter design consideration and methodology. Section IV validates the system using simulations and experiments. Finally, Section V concludes this article.

II. SOM MODEL

The system configuration is shown in Fig. 2. Eight MOSFETs $Q_1 \sim Q_4$ and $S_1 \sim S_4$ constitute the CLLC converter. The resonant frequency f_r of the converter based on the CLLC resonant tank can be expressed as

$$f_r = \frac{1}{2\pi\sqrt{L_{rp}C_{rp}}} = \frac{1}{2\pi\sqrt{L_{rs}C_{rs}}} \tag{1}$$

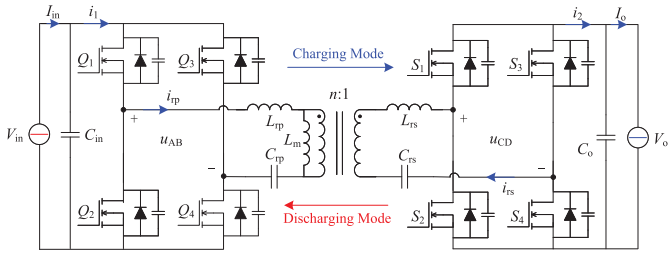


Fig. 2. Circuit diagram of CLLC charger.

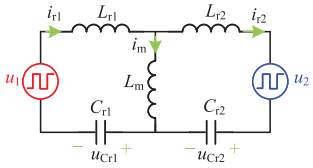


Fig. 3. Equivalent circuit of the CLLC converter.

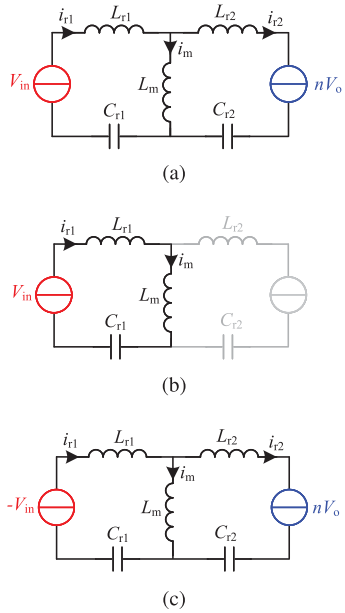


Fig. 4. Three equivalent circuits in different stages. (a) P stage. (b) O stage. (c) N stage.

where L_{rp}, L_{rs}, C_{rp}, and C_{rs} are the series inductor and capacitor of the primary and secondary sides, respectively.

This CLLC converter regulates the output voltage using the PFM method. In the charging mode, the primary-side switches Q_i ($i = 1, 2, 3, 4$) work at the switching frequency f_s, where Q_1 and Q_4 are driven with 50% duty-cycle, and Q_2 and Q_3 are complementary to Q_1 and Q_4. The secondary-side switches S_i are not driven, and the body diodes are used for rectification. In the discharging mode, the principle remains similar, but S_i are controlled by the same 50% duty-cycle signals, and Q_i operate as the rectifier. The switching and resonant angular frequency are defined as ω_s and ω_r, respectively. The ratio ω_s/ω_r is defined as the normalized frequency ω_n. C_{in} is the dc-link capacitors, and C_o is used as the capacitive filter. The turn ratio of the transformer is n. The system input dc voltage and the output voltage are V_{in} and V_o, respectively. The resonant currents of the primary and secondary sides are i_{rp} and i_{rs}. The current i_m is the magnetizing current.

The equivalent circuit of the CLLC converter is shown in Fig. 3. To unify the characteristics in charging and discharging mode, secondary-side resonant parameters are designed to match the value of primary-side parameters after reflection [17]. Thus, the CLLC resonant converter acquired symmetrical resonant parameters that can be expressed as

$$\begin{cases} L_{r1} = L_{r2} = L_{rp} = n^2 L_{rs} \\ C_{r1} = C_{r2} = C_{rp} = C_{rs}/n^2. \end{cases} \tag{2}$$

Basically, the magnetizing inductance L_m is designed to be k times that of L_{rp}, i.e.,

$$k = \frac{L_m}{L_{rp}} = \frac{L_m}{n^2 L_{rs}}. \tag{3}$$

All the operation modes of CLLC converters can be classified into three stages as P, N, and O [27], as shown in Fig. 4. The input and output voltage in the P stage have the same polarity. On the contrary, the input and output voltage in the N stage have the opposite polarity. The converter works in the O stage if the secondary side current remains zero. The detailed expressions and working waveforms are analyzed as follows.

A. Three Operation Stages

The P stage equivalent circuit is shown in Fig. 4(a). According to Kirchhoff's law, the circuit can be expressed by

$$\begin{cases} L_m \frac{di_{m,P}}{dt} + L_{r1} \frac{di_{r1,P}}{dt} + u_{Cr1,P} = V_{in} \\ L_{r2} \frac{di_{r2,P}}{dt} + u_{Cr2,P} + nV_o = L_m \frac{di_{m,P}}{dt} \\ i_{r1,P} = C_{r1} \frac{du_{Cr1,P}}{dt} \\ i_{r2,P} = C_{r2} \frac{du_{Cr2,P}}{dt} \\ i_{r1,P} = i_{r2,P} + i_{m,P} \end{cases} \tag{4}$$

where $i_{r1,P}$ and $i_{r2,P}$ are the reflection resonant currents of the primary and secondary sides at the P stage, respectively. $u_{Cr1,P}$ and $u_{Cr2,P}$ are the capacitor voltage.

Using the Laplace and inverse Laplace transforms for (4), the resonant current time-domain is given as

$$i_{r1,P} = P_1 \cos\phi - P_2 \sin\phi + k_1 P_4 \sin(k_1\phi) + P_3 \cos(k_1\phi) \tag{5}$$

where $\phi = \omega_r t$, P_1, P_2, P_3, and P_4 are the variables to be determined. The intermediate parameter k_1 is defined as

$$k_1 = \sqrt{\frac{1}{2k+1}}. \tag{6}$$

Similar to the primary-side resonant current, the secondary-side resonant current can be stated as

$$i_{r2,P} = P_1 \cos\phi - P_2 \sin\phi - k_1 P_4 \sin(k_1\phi) - P_3 \cos(k_1\phi). \tag{7}$$

TABLE II
CLLC CONVERTER CHARACTERISTICS IN DIFFERENT OPERATION MODES

Switch frequency	$\omega_n < 1$					$\omega_n = 1$	$\omega_n > 1$				
Operation Mode	PN	PON	PO	OPO	O	P	O	OP	OPO	NOP	NP
Conduction Continuity	CCM	DCM	DCM	DCM	OFF	CCM	OFF	DCM	DCM	DCM	CCM
Voltage Gain	Buck and boost mode		Boost mode		Cutoff mode	Unity mode	Cutoff mode	Buck mode			
Load Condition	Heavy→light					Independent	Light→heavy				

CCM: continuous conduction mode; DCM: discontinuous conduction mode

Based on the current and voltage relationship between capacitors and inductors, the voltages of the capacitors are

$$\begin{cases} v_{\mathrm{Cr1},P} = -Z_0(P_1\sin\phi + P_2\cos\phi - P_4\cos(k_1\phi)) \\ \qquad -Z_0\frac{P_3}{k_1}\sin(k_1\phi) + V_{\mathrm{in}} \\ v_{\mathrm{Cr2},P} = -Z_0(P_1\sin\phi + P_2\cos\phi + P_4\cos(k_1\phi)) \\ \qquad Z_0\frac{P_3}{k_1}\sin(k_1\phi) - nV_{\mathrm{o}} \end{cases} \tag{8}$$

where Z_0 is characteristic impedance, which can be given as

$$Z_0 = \sqrt{\frac{L_{\mathrm{rp}}}{C_{\mathrm{rp}}}} = n^2\sqrt{\frac{L_{\mathrm{rs}}}{C_{\mathrm{rs}}}}. \tag{9}$$

Similarly, the O stage [Fig. 4(b)] expressions can be described as

$$\begin{cases} i_{\mathrm{r1},O} = O_1\cos(k_2\phi) - O_2k_2\sin(k_2\phi) \\ v_{\mathrm{Cr1},O} = -Z_0(O_2\cos(k_2\phi) + \frac{O_1}{k_2}\sin(k_2\phi)) + V_{\mathrm{in}} \end{cases} \tag{10}$$

where O_1 and O_2 are the variables to be determined. The intermediate parameter is defined as

$$k_2 = \sqrt{\frac{1}{k+1}}. \tag{11}$$

Likewise, the N stage [Fig. 4(c)] is expressed as

$$\begin{cases} i_{\mathrm{r1},N} = N_1\cos\phi - N_2\sin\phi + k_1N_4\sin(k_1\phi) \\ \qquad +N_3\cos(k_1\phi) \\ i_{\mathrm{r2},N} = N_1\cos\phi - N_2\sin\phi - k_1N_4\sin(k_1\phi) \\ \qquad -N_3\cos(k_1\phi) \\ v_{\mathrm{Cr1},N} = -Z_0(N_1\sin\phi + N_2\cos\phi - N_4\cos(k_1\phi)) \\ \qquad -Z_0\frac{N_3}{k_1}\sin(k_1\phi) + V_{\mathrm{in}} \\ v_{\mathrm{Cr2},N} = -Z_0(N_1\sin\phi + N_2\cos\phi + N_4\cos(k_1\phi)) \\ \qquad +Z_0\frac{N_3}{k_1}\sin(k_1\phi) + nV_{\mathrm{o}} \end{cases} \tag{12}$$

where N_1, N_2, N_3, and N_4 are the variables to be determined.

With various combinations of the three operation stages, the CLLC converter can acquire different operation modes, which is shown in Table II [28]. In practice, the boost ($f_s < f_r$) and buck ($f_s > f_r$) modes are essential to regulate the chargers in a wide voltage range. When $f_s < f_r$, the PO mode is preferred. In this mode, the primary-side switches can realize zero voltage switching (ZVS), and the secondary-side switches can realize zero current switching (ZCS). In addition, the voltage gain is monotonic, which increases as the frequency decreases. The PN/PON modes should be prevented because the soft switching may be lost. Also, in these modes, the voltage gain curve is nonmonotonic, which may lead to the dysfunction of the feedback controller. When $f_s > f_r$, the NP mode is recommended. This is because the output power is too low, and high efficiency cannot be guaranteed when the CLLC converter works in other modes. Furthermore, as shown in Table II, the converter works in the OPO mode when a light load is applied. When $f_s > f_r$, a very high switching frequency is required to obtain a small voltage gain in the OPO mode. Thus, the phase-shift control or circuit reconfiguration methods can be used to improve the poor voltage regulation ability [29]. The OPO mode when $f_s < f_r$ will be discussed in Section II-C. The following are the main recommended CLLC converter operation modes.

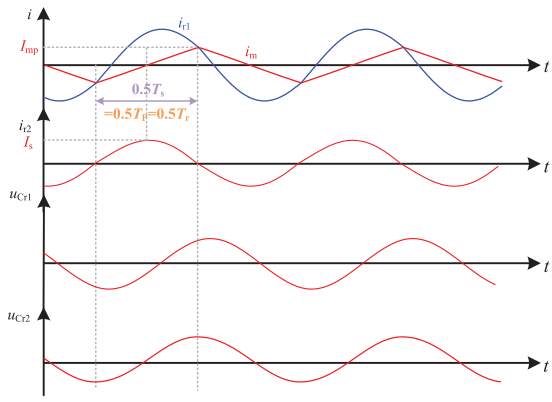


Fig. 5. Waveforms in P mode.

B. Operation Model in P Mode

When f_s equals to f_r, the CLLC converter works in the P modes. In this mode, all the passive components on the primary and secondary sides work at resonant conditions, and the system efficiency is at its highest. The waveforms in P mode are shown in Fig. 5. Therefore, the duration of the P stage is the same as the resonant period T_r and switching period T_s, i.e.,

$$\frac{T_{\mathrm{P}}}{2} = \frac{T_{\mathrm{r}}}{2} = \frac{T_{\mathrm{s}}}{2} = \frac{\pi}{\omega_{\mathrm{r}}}. \tag{13}$$

The current satisfies the half-wave symmetry and continuity principles, which can be expressed as

$$\begin{cases} i_{\mathrm{r1},P}(0) + i_{\mathrm{r1},P}\left(\frac{T_{\mathrm{P}}}{2}\right) = 0 \\ i_{\mathrm{r2},P}(0) = i_{\mathrm{r2},P}\left(\frac{T_{\mathrm{P}}}{2}\right) = 0. \end{cases} \tag{14}$$

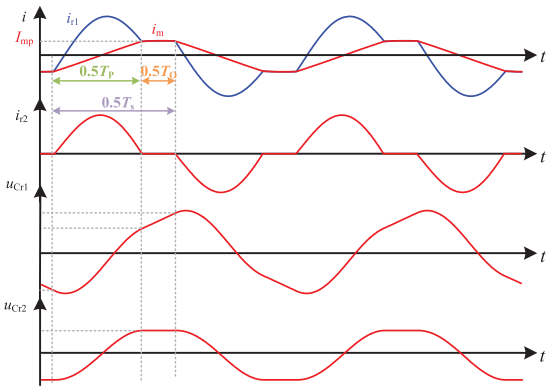


Fig. 6. Waveforms in PO mode.

Similarly, the capacitor voltages satisfy

$$\begin{cases} u_{\mathrm{Cr1},P}(0) + u_{\mathrm{Cr1},P}\left(\frac{T_\mathrm{s}}{2}\right) = 0 \\ u_{\mathrm{Cr2},P}(0) + u_{\mathrm{Cr2},P}\left(\frac{T_\mathrm{s}}{2}\right) = 0. \end{cases} \tag{15}$$

Assume there is no loss when the power is transferred from the primary side to the secondary side. Hence, the energy conservation law can be utilized, which is given by

$$V_\mathrm{in} I_\mathrm{in} = V_\mathrm{o} I_\mathrm{o}. \tag{16}$$

The input ac currents i_1 and i_2 in Fig. 2 are equal to i_{r1} and ni_{r2} in half a positive switching period, respectively. Thus, the input current and output current I_in and I_o can be derived as

$$\begin{cases} I_\mathrm{in} = \frac{2}{T_\mathrm{s}} \int_0^{\frac{T_\mathrm{r}}{2}} i_{\mathrm{r1},P}(t)\mathrm{d}t \\ I_\mathrm{o} = \frac{2n}{T_\mathrm{s}} \int_0^{\frac{T_\mathrm{r}}{2}} i_{\mathrm{r2},P}(t)\mathrm{d}t. \end{cases} \tag{17}$$

Then, the voltage gain can be derived as

$$\frac{V_\mathrm{o}}{V_\mathrm{in}} = \frac{I_\mathrm{in}}{I_\mathrm{o}} = 1. \tag{18}$$

Therefore, the voltage gain when $f_\mathrm{s} = f_\mathrm{r}$ is equal to one, which can also be called the unity mode. This feature, along with the load-independent operation characteristic, makes the CLLC converter an ideal DCX in the P mode. In this mode, the simplified open-loop control ($f_\mathrm{s} = f_\mathrm{r}$ and duty cycle $D = 0.5$) is suitable to implement, achieving high efficiency for the CLLC converter.

C. Operation Model in PO Mode

When f_s is smaller than f_r, the CLLC converter works in the OPO/PO/PON/PN modes. As analyzed previously, the PO operation mode is expected because of its soft-switching characteristics. Besides, the gain curves in the PN/PON modes are nonmonotonic, which makes the output voltage hard to regulate using the feedback controller.

The waveforms are shown in Fig. 6 in PO mode. The duration of the P stage can be derived as

$$\frac{T_\mathrm{P}}{2} \approx \frac{T_\mathrm{r}}{2} = \frac{\pi}{\omega_\mathrm{r}}. \tag{19}$$

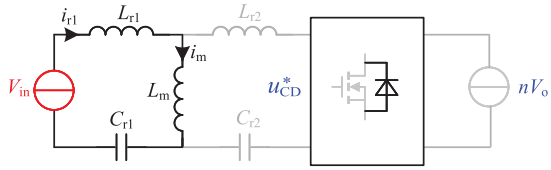


Fig. 7. Equivalent circuit at $\frac{1}{2}T_\mathrm{P}$ and $\frac{1}{2}T_\mathrm{s}$.

According to the inductance current and capacitance voltage continuity and symmetry principles, the following conditions should be satisfied:

$$\begin{cases} i_{\mathrm{r1},P}(0) + i_{\mathrm{r1},O}\left(\frac{T_\mathrm{s}}{2}\right) = 0 \\ i_{\mathrm{r2},P}(0) = 0 \\ u_{\mathrm{Cr1},P}(0) + u_{\mathrm{Cr1},O}\left(\frac{T_\mathrm{s}}{2}\right) = 0 \\ u_{\mathrm{Cr2},P}(0) + u_{\mathrm{Cr2},P}\left(\frac{T_\mathrm{P}}{2}\right) = 0 \\ i_{\mathrm{r1},P}\left(\frac{T_\mathrm{P}}{2}\right) - i_{\mathrm{r1},O}(0) = 0 \\ i_{\mathrm{r2},P}\left(\frac{T_\mathrm{P}}{2}\right) = 0 \\ u_{\mathrm{Cr1},P}\left(\frac{T_\mathrm{P}}{2}\right) - u_{\mathrm{Cr1},O}(0) = 0. \end{cases} \tag{20}$$

By taking (19), (20) into (5), (7), (8), and (10), the variables could be obtained using the same number of equations. Thus, the gain in PO mode can be expressed as

$$G_\mathrm{PO}(k,\omega_\mathrm{n}) = \frac{nV_\mathrm{o}}{V_\mathrm{in}} = \frac{2k_2 \cos\left(\frac{\pi k_1}{2}\right) G_1}{(k_2 - 2k_1)\, G_2 + (2k_1 + k_2)\, G_3} \tag{21}$$

where

$$\begin{cases} G_1 = \cos\left(\frac{\pi(\omega_\mathrm{n}-1)k_2}{2\omega_\mathrm{n}}\right) \\ G_2 = \cos\left(\frac{\pi(\omega_\mathrm{n}k_1+(\omega_\mathrm{n}-1)k_2)}{2\omega_\mathrm{n}}\right) \\ G_3 = \cos\left(\frac{\pi(\omega_\mathrm{n}k_1-(\omega_\mathrm{n}-1)k_2)}{2\omega_\mathrm{n}}\right). \end{cases} \tag{22}$$

Fig. 7 illustrates the equivalent circuit when the CLLC converter works in the O stage, where u^*_CD represents the voltage u_CD across two switching nodes of the secondary-side bridge after reflection. Normally, the current i_{r1} is equal to i_m in this stage. However, as shown in Fig. 7, when the output current becomes too large, the capacitors may be overcharged. Thus, a jump in voltage u^*_CD will occur when the overcharged capacitors cause the secondary-side diodes to turn ON in advance. Assuming the CLLC converter enters O stage, if $u^*_\mathrm{CD}(t)$ drops from $+nV_\mathrm{o}$ to $-nV_\mathrm{o}$, the charger will enter the N stage at $t = \frac{1}{2}T_\mathrm{r}$ [23]. Therefore, the boundaries of PO, PON, and PN modes can be expressed by

$$\begin{cases} \left|u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{P}\right)\right| < nV_\mathrm{o} \;\;\&\;\; \left|u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{s}\right)\right| \le nV_\mathrm{o} & \text{PO mode} \\ \left|u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{P}\right)\right| < nV_\mathrm{o} \;\;\&\;\; \left|u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{s}\right)\right| > nV_\mathrm{o} & \text{PON mode} \\ \left|u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{P}\right)\right| \ge nV_\mathrm{o} & \text{PN mode} \end{cases} \tag{23}$$

where

$$\begin{cases} u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{P}\right) = V_\mathrm{in} - u_{\mathrm{Cr1},P}\left(\frac{T_\mathrm{P}}{2}\right) - u_{\mathrm{Cr2},P}\left(\frac{T_\mathrm{P}}{2}\right) \\ u^*_\mathrm{CD}\left(\frac{1}{2}T_\mathrm{s}\right) = V_\mathrm{in} - u_{\mathrm{Cr1},O}\left(\frac{T_\mathrm{s}}{2}\right) - u_{\mathrm{Cr2},O}\left(\frac{T_\mathrm{s}}{2}\right). \end{cases} \tag{24}$$

TABLE III
SIMULATION PARAMETERS IN VERIFYING MODE BOUNDARIES

Symbol	Value	Symbol	Value
V_{in}	500 V	f_{r}	100 kHz
L_{rp}, L_{rs}	16 μH	L_{m}	200 μH
C_{rp}, C_{rs}	158.3 nF	n	1

Then, (23) can be rewritten as

$$\begin{cases} u_{\text{Cr1},P}(\frac{T_{\text{P}}}{2}) + u_{\text{Cr2},P}(\frac{T_{\text{P}}}{2}) < V_{\text{in}} + nV_{\text{o}} \\ u_{\text{Cr1},O}(\frac{T_{\text{s}}}{2}) + u_{\text{Cr2},O}(\frac{T_{\text{s}}}{2}) < V_{\text{in}} + nV_{\text{o}}. \end{cases} \tag{25}$$

To simplify the analysis, the magnetizing current i_{m} remains constant after i_{m} touches i_{r1} until half a switching period. In other words, $i_{\text{m}}(t) = I_{\text{m}}$ during the O mode. Thus, causing the primary-side capacitor voltage to increase linearly. According to the capacitor voltage symmetry principles in a half period, the voltage increment of the primary-side capacitor can be obtained.

Consequently, the condition of the CLLC converter working in PO mode can be expressed as

$$Z_0 < \frac{2n^2\omega_{\text{n}}R_{\text{o}}}{\pi G_{\text{PO}}} \tag{26}$$

where R_{o} is the output resistance. The output resistance can be expressed as

$$R_{\text{o}} = \frac{V_{\text{o}}}{I_{\text{o}}} = \frac{P_{\text{out}}}{V_{\text{o}}} \tag{27}$$

where P_{out} is the output power.

This boundary condition is simulated in PLECS software. The simulation parameters are listed in Table III. Fig. 8 shows the simulation results when the load changes from 40 to 35 Ω. It shows that the operation mode of the CLLC converter changes from PO mode to PON mode. The calculated boundaries when the switching frequency is 50 kHz according to (26) is $R_{\text{o}} < 39.8\,\Omega$, which can verify the effectiveness of (26).

The CLLC converter is possible to work in the OPO mode when $f_{\text{s}} < f_{\text{r}}$ under light loading. Using the parameters in Table III, the gain versus switching frequency with increasing R_{o} can be depicted in Fig. 9. When the $R_{\text{o}} = 50\,\Omega$, the CLLC converter works in PO mode. When the $R_{\text{o}} = 300$ or $500\,\Omega$, the CLLC converter works in OPO mode. It is apparent that under the same switching frequency, the gain increases as the resistance increases. For specific CLLC parameters, the gain in OPO mode is larger than it is in the PO mode. In other words, the worst condition occurs at the heavy load rather than the light load. In the OPO mode, the closed-loop controller can increase the switching frequency to maintain the output voltage constant. Therefore, the light-load condition when $f_{\text{s}} < f_{\text{r}}$ need not be considered in designing a CLLC converter.

D. Operation Model in NP Mode

When f_{s} is larger than f_{r}, the CLLC converter is expected to work in NP mode and the operating waveforms

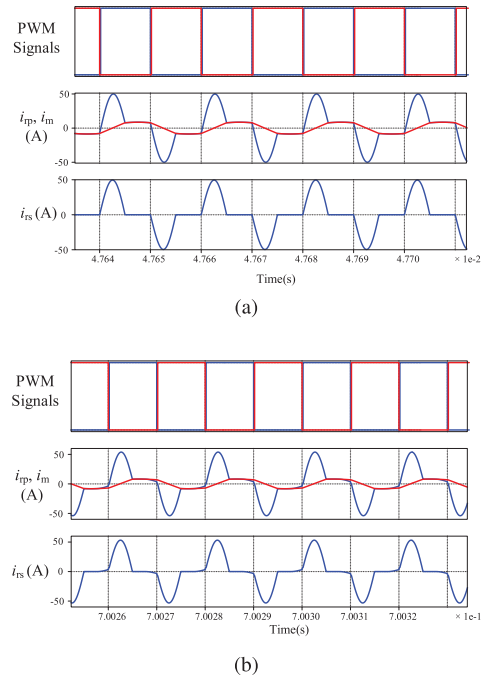


Fig. 8. PO/PON boundary simulation results when output power increases. (a) $R_{\text{o}} = 40\,\Omega$. (b) $R_{\text{o}} = 35\,\Omega$.

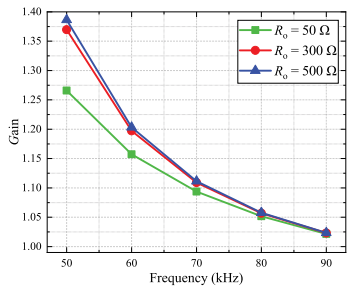


Fig. 9. Gain curves when R_{o} increases.

are shown in Fig. 10. According to the inductance current and capacitance voltage continuity and symmetry principles, we have

$$\begin{cases} i_{\text{r1},P}(0) + i_{\text{r1},N}\left(\frac{T_{\text{s}}}{2}\right) = 0 \\ i_{\text{r2},P}(0) = i_{\text{r2},N}\left(\frac{T_{\text{s}}}{2}\right) = 0 \\ i_{\text{m},P}(0) + i_{\text{m},N}\left(\frac{T_{\text{s}}}{2}\right) = 0 \\ u_{\text{Cr1},P}(0) + u_{\text{Cr1},N}\left(\frac{T_{\text{s}}}{2}\right) = 0 \\ u_{\text{Cr2},P}(0) + u_{\text{Cr2},N}\left(\frac{T_{\text{s}}}{2}\right) = 0. \end{cases} \tag{28}$$

It is challenging to get voltage gain using (28) due to the existence of the highly nonlinear trigonometric items. Therefore, the transient N mode is ignored to simplify the analysis. Accordingly, the resonant current drops to zero at $t = \frac{1}{2}T_{\text{s}}$ and the capacitors voltages increment is slight. Therefore, the P stage equations can be used when the circuit at $t = \frac{1}{2}T_{\text{s}}$ to obtain the

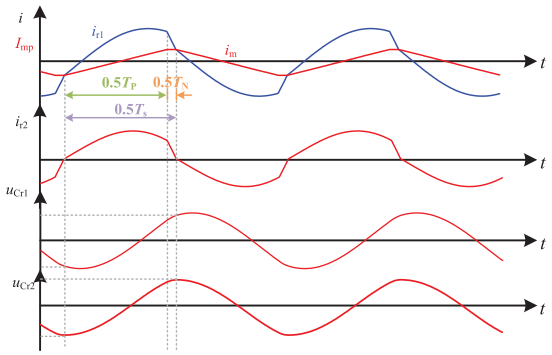


Fig. 10. Waveforms in NP mode.

time-domain expressions. Thus

$$\begin{cases} i_{r2,P}(0) = 0 \\ i_{m,P}(0) + i_{m,P}\left(\frac{T_s}{2}\right) = 0 \\ u_{Cr1,P}(0) + u_{Cr1,P}\left(\frac{T_s}{2}\right) = 0 \\ u_{Cr2,P}(0) + u_{Cr2,P}\left(\frac{T_s}{2}\right) = 0 \\ I_o = \frac{2n}{T_s}\int_0^{\frac{T_s}{2}} i_{r2,P}(t)\mathrm{d}t = \frac{V_o}{R_o}. \end{cases} \tag{29}$$

By taking (29) into (5), (7), and (8), the voltage gain in NP mode can be obtained as

$$G_{NP}(k, Z_0, R_o, \omega_n) = \frac{nV_o}{V_{in}} = \frac{G_4 + k_1 G_6}{G_4 - \frac{\pi Z_0}{n^2 \omega_n R_o} G_5 - k_1 G_6} \tag{30}$$

where

$$\begin{cases} G_4 = \cos\frac{\pi}{\omega_n} - 1 \\ G_5 = \cos\frac{\pi}{\omega_n} + 1 \\ G_6 = \sin\left(\frac{\pi}{\omega_n}\right)\tan\left(\frac{\pi k_1}{2\omega_n}\right). \end{cases} \tag{31}$$

The quality factor can be defined to relate the characteristic impedance Z_0 and load R_o, i.e.,

$$Q = \frac{Z_0}{n^2 R_o}. \tag{32}$$

Then, (30) can be rewitten as

$$G_{NP}(k, Z_0, R_o, \omega_n) = \frac{nV_o}{V_{in}} = \frac{G_4 + k_1 G_6}{G_4 - \frac{\pi Q}{\omega_n} G_5 - k_1 G_6}. \tag{33}$$

E. Comparisons Among SOM, FHA, and TDM

In this section, the conventional FHA model, SOM model, and TDM are compared. The principle of the FHA model is straightforward. When the converter works near the resonant frequency, the current and voltage waveforms in the resonant tank will be close to the sine wave. Thus, the higher-order harmonics can be neglected, and only the fundamental component needs to be considered. The equivalent circuit of the FHA model is shown in Fig. 11 [13]. In the FHA model, the input source on the primary side can be replaced by a sinusoidal voltage source with a frequency that is the same as the switching frequency of the converter. The secondary-side rectifier, filter capacitor,

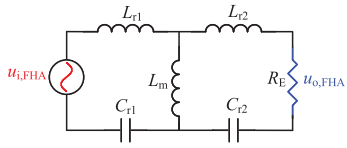
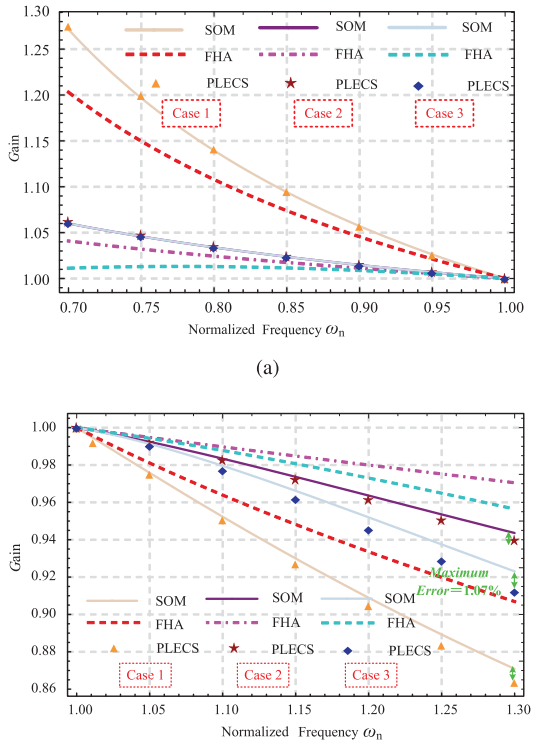


Fig. 11. Equivalent circuit of the FHA model.



(a)

(b)

Fig. 12. Gain curves versus ω_n with different cases. (a) $\omega_n \le 1$. (b) $\omega_n \ge 1$.

and load can be replaced by the equivalent resistance R_E. The equivalent resistance R_E can be expressed as

$$R_E = \frac{8n^2}{\pi^2} R_o. \tag{34}$$

Thus, the output voltage gain of the CLLC converter using the FHA model can be deduced as

$$G_F = \frac{1}{\sqrt{\frac{\pi^4 Q^2}{64 k^2}\left[a\omega_n - \frac{b}{\omega_n} + \frac{1}{\omega_n^3}\right]^2 + \left(1 + \frac{1}{k} - \frac{1}{k\omega_n^2}\right)^2}} \tag{35}$$

where $a = 2k + 1$, $b = 2k + 2$.

According to (35), it is evident that the main merit of the FHA model is that the gain model of all modes can be given using one expression. However, the accuracy of the FHA model is not enough to properly design a CLLC converter.

The gain comparison among the FHA method, the proposed SOM model, and PLECS simulation results are shown in Fig. 12. The system specifications of different cases are listed in Table IV. According to Fig. 12(a), there is a large gap between the gain curves of the FHA method and of the simulation results. Also, the voltage step-up characteristic cannot be reflected in Case 3. As a result, the FHA model is unsuitable for the design

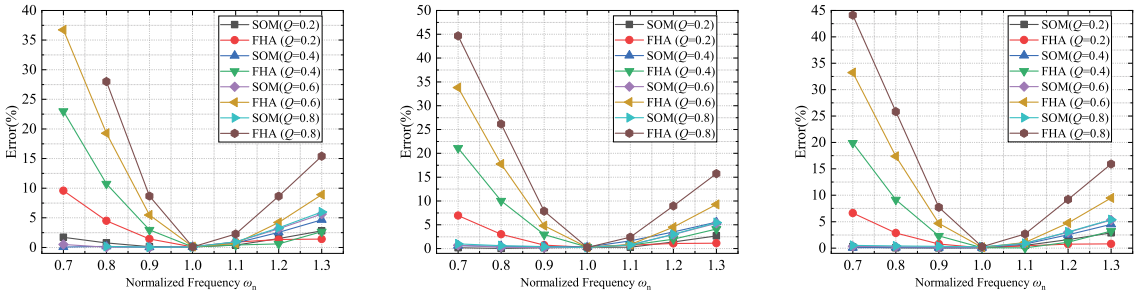


Fig. 13. Gain errors versus ω_n with different k. (a) $k = 5$. (b) $k = 10$. (c) $k = 15$.

TABLE IV
SIMULATION SPECIFICATIONS

Parameters	Case 1	Case 2	Case 3
k	5	18.75	18.75
Z_0	25	10	10
n	2	1	1
R_o	25 Ω	100 Ω	60 Ω
f_r	200 kHz	100 kHz	100 kHz
Mode	Charging	Charging	Discharging

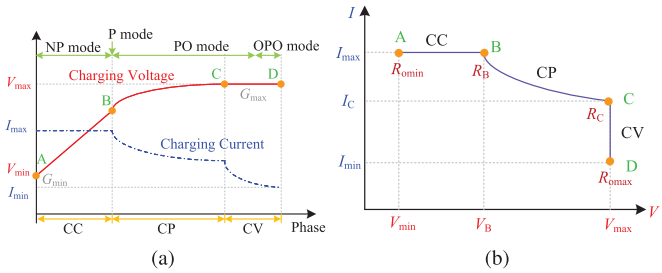


Fig. 14. Battery charging profile. (a) Typical charging profile of lithium-ion batteries. (b) V-I curve of the battery charging profile.

process. Oppositely, the SOM model is nearly identical to the simulation, no matter how diverse the values of k and Z_0 are. From Fig. 12(b), both the SOM model and the FHA method have errors compared with the simulation results. However, the SOM gain model curve is closer to the simulation results than the FHA model. The maximum error is 1.07%, which is negligible. The relative errors of the SOM model are due to the approximations assumed in dealing with the TDM. This approximation is a tradeoff between calculation complexity and accuracy.

To analyze the proper scope of application of the SOM and FHA model, the voltage gain error is calculated. The definition of error is defined as

$$\text{Error} = \frac{|V_o - V_{o,cal}|}{V_o} \times 100\% \tag{36}$$

where V_o is the simulated output voltage and $V_{o,cal}$ is the calculated output voltage according to the FHA or SOM model.

Fig. 13 shows the voltage gain accuracy as percentage error with different k and Q. It is obvious that the proposed model is more accurate in most cases. For all points of the SOM model, the errors are negligible. Especially when $f_s < f_r$, the errors are lower than 2%. Also, the maximum error, which is just under 6%, occurs when both switching frequency and quality factor are high. However, for the FHA model, the errors are acceptable when $Q \leq 0.4$ and $\omega_n > 1$, which means that the FHA model is only suitable for the low load quality factors application with upper resonant frequency. This conclusion is consistent with [25]. The SOM makes up the deficiency of FHA, making the gain expression valid in a large frequency range and in DCM mode.

The TDM, without any simplification, is as accurate as the PLECS simulation results. The voltage gain can be obtained by solving (5), (7), (8), (10), (20), and (28). However, although TDM improves analytical accuracy, the implied nonlinear relationship with trigonometric items makes it challenging to acquire the visualized gain solution. Therefore, combining the benefits of the accurate TDM and the simple FHA model, the SOM model is proposed in this article.

III. PARAMETER DESIGN METHODOLOGY

A. Design Consideration

As indicated in Fig. 14(a), the charging process for lithium-ion batteries typically involves the following three main phases [30]: 1) constant current (CC) phase; 2) constant power (CP) phase; 3) constant voltage (CV) phase. Several conditions should be addressed in order to meet the charge requirements.

1) At the beginning (Point A) of the CC charging process, the output voltage is minimum. The CLLC converter should work in NP mode, and the minimum voltage gain should be smaller than the minimum requirement G_{min}.
2) When the output voltage reaches the nominal value (Point B), the chargers enter the CP phase, and the CLLC enters P mode.
3) Then, the required voltage increases until the output voltage reaches the maximum (Point C). The possibility of CLLC jumping the PO boundary occurred in this period. A suitable characteristic impedance Z_0 is needed to ensure the CLLC converter works in PO mode. The maximum voltage gain should be larger than the requirement G_{max}.
4) After the output voltage reaches its maximum, the chargers will enter the CV phase until the current reaches the minimum (Point D). In this phase, the CLLC converter might work in PO/OPO mode. The closed-loop controller increases frequency to maintain the voltage constant when the lower output power is required.

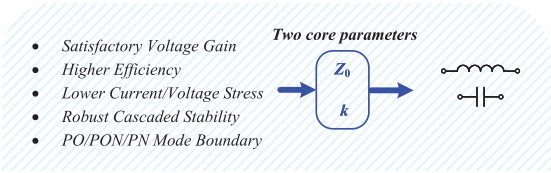


Fig. 15. Design consideration for CLLC converter.

Based on Fig. 14(a), the V-I curve of the battery charging profile could be obtained, which is shown in Fig. 14(b). For point A, the output voltage is minimum, and the current is maximum. Thus, at this point, the output resistance is minimum ($R_{\mathrm{o\,min}}$). Likewise, at point D, the output resistance is maximum ($R_{\mathrm{o\,max}}$). Therefore, in the charging process, the output resistance is between these two boundaries, which can be expressed as $R_{\mathrm{o}} \in [R_{\mathrm{o\,min}}, R_{\mathrm{o\,max}}]$. Besides, the resonant parameters are mainly constrained by (26) and (30). Hence, the battery load could be simplified as the resistive load in the design procedure.

To fulfill the system performance requirements, two core parameters inductance ratio k and characteristic impedance Z_0 are selected. To obtain the optimal parameters for the CLLC converters, the voltage gain, efficiency, stability, and operation mode boundary are considered, as shown in Fig. 15.

The effect of different parameters on the efficiency is evaluated first. For the CLLC resonant converter, the primary-side switches can realize ZVS turn-ON. Thus, the overall system loss can be deduced as

$$P_{\mathrm{loss}} = P_{\mathrm{swcon}} + P_{\mathrm{swoff}} + P_T + P_{\mathrm{other}}. \tag{37}$$

Each of them is analyzed in [16] and [31].

1) Switches conduction loss P_{swcon}

$$P_{\mathrm{swcon}} = 2I_{\mathrm{rp(rs)}}^2 R_{\mathrm{dson}} \tag{38}$$

where $I_{\mathrm{rp(rs)}}$ is the primary (secondary) rms resonant current. R_{dson} is the MOSFET ON-resistor and can be found in the MOSFET datasheet.

2) Switches turn-OFF loss P_{swoff}

$$P_{\mathrm{swoff}} = \frac{I_{\mathrm{mp}}^2 t_d^2 f_{\mathrm{s}}}{12 C_{\mathrm{oss}}} \tag{39}$$

where t_d is the dead time and C_{oss} is the junction capacitors for MOSFETs.

3) Transformer loss P_T

$$P_T = P_{\mathrm{Fe}} + P_{\mathrm{Copper}} \tag{40}$$

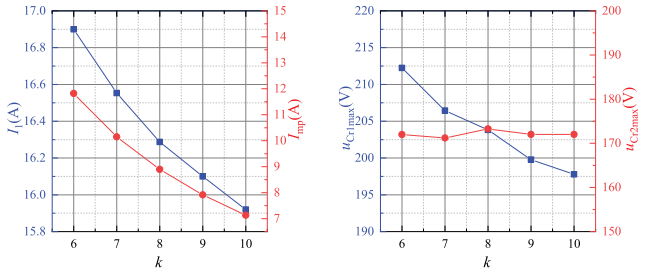
$$P_{\mathrm{Fe}} = P_{\mathrm{v}} V_{\mathrm{e}} \tag{40a}$$

where P_{v} is the relative core losses and V_{e} is the effective magnetic volume. Both of them can be obtained in the magnetic core datasheet

$$P_{\mathrm{Copper}} = I_{\mathrm{rp}}^2 R_T \tag{40b}$$

where R_T is the equivalent ac resistance of the transformer.

4) Other loss P_{other}, including but not limited to resonant inductor and capacitor loss, driving circuit loss, and MOSFETs turn-ON loss in NP mode.



(a) (b)

Fig. 16. Current stress and voltage stress with different k. (a) Current versus k. (b) Maximum capacitors voltage versus k.

The theoretical efficiency can be expressed as

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}}. \tag{41}$$

It is evident that the system efficiency is highly dependent on the rms value of the resonant current I_{rp} and the transient value of the magnetizing inductance current I_{mp}. The resonant current simulation results when the output voltage gain is constant are shown in Fig. 16(a). It shows that the current decreases when k increases, which demonstrates that an increasing k leads to higher system efficiency and lower current stress for the power semiconductors [13]. In addition, the capacitor's voltage stresses are important to ensure the system works safely. The simulation results shows that the larger k selection is beneficial for a safe operation. To summarize, an increasing k selection can reduce the current and voltage stress and benefit the system efficiency performance of CLLC converters. Besides, when k becomes small, the slight change in switching frequency will cause a large gain change, which is difficult to stabilize and is unsuitable for closed-loop control.

However, the increase of k is limited by other factors. The larger k may lead to lower voltage gain and may not even fulfill the output requirements. Therefore, the objective of this design process is to find the maximum inductance ratio k_{max} under some restrictions. For instance, the limitation of output voltage gain, ZVS conditions, and resonant current.

The characteristic impedance Z_0 is another key parameter that has a great impact on the PO/PON/PN boundary. Besides, the resonant current also has a relationship with Z_0. Thus, a suitable Z_0 should be considered. To improve the system stability, it is better to have a lower maximum output impedance Z_{out} for the CLLC converter. Fig. 17 shows that the lower Z_{out} can be obtained by increasing Z_0. In conclusion, a larger Z_0 is beneficial for the cascaded system stability and efficiency. However, a satisfactory gain range and the PO working restrictions may not be accomplished if a large Z_0 is employed.

B. Step-By-Step Design Procedure

In this section, a step-by-step design procedure for a CLLC resonant converter is presented, which is shown in Fig. 18. The specifications of the designed CLLC converter are listed in Table V.

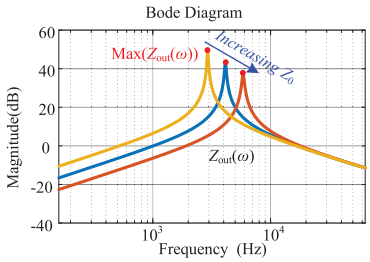


Fig. 17. Bode plot of the output impedance of CLLC converter with different Z_0.

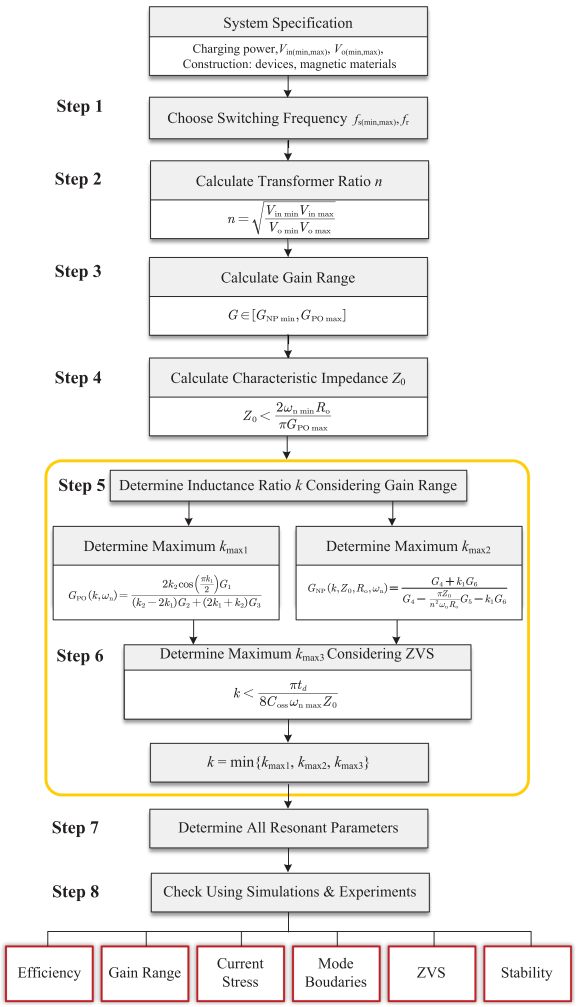


Fig. 18. Parameter design procedure of the CLLC converter.

1) *Step 1. Choose switching frequency f_s Range:* In this step, the main objective is to determine the optimal minimum switching frequency $f_{s\,min}$ that ensures the energy contained in the resonant tank achieves the minimum [32]. The energy can be expressed as

$$E(f_{s\,min}) = E_0 \frac{1+\left(\frac{f_{s\,min}}{f_r}\right)^2}{\frac{f_{s\,min}}{f_r}\left(1-\left(\frac{f_{s\,min}}{f_r}\right)^2\right)} \tag{42}$$

TABLE V
DESIGN SPECIFICATIONS

Parameters	Symbol	Value
Input voltage	V_{in}	200 V
Output voltage range	V_o	170 V $\sim$ 230 V
Rated output voltage range	$V_{o,rated}$	200 V
Resonant frequency	f_r	100 kHz
Switching frequency	f_s	55 kHz $\sim$ 150 kHz
Rated output power	$P_{o,rated}$	1000 W

where E_0 is the energy expression component that has nothing to do with frequency. Through the derivation of (42), the optimal switching frequency $f_{s\,min}$ can be calculated approximately. Considering the power density, the resonant and switching frequencies are set, as shown in Table V.

2) *Step 2. Choose transformer ratio n:* To narrow the CLLC converter switching frequency range, it is preferred to design the converter with a symmetrical operation range in both charging and discharging modes [33]. Therefore, the transformer ratio of n should be reasonably designed to make the voltage gain range almost the same in these two operation modes, which can be illustrated by

$$n = \sqrt{\frac{V_{in\,min}V_{in\,max}}{V_{o\,min}V_{o\,max}}} \tag{43}$$

where $V_{in\,min}$, $V_{in\,max}$, $V_{o\,min}$, and $V_{o\,max}$ are the minimum and maximum values of input and output voltages, respectively.

3) *Step 3. Calculate voltage-gain requirements:* Obtaining the required voltage gain is the main objective in the design process, and the gains in charging/discharging modes are expressed as

$$\begin{aligned} G_{C\,min(max)} &= nV_{o\,min(max)}/V_{in} \\ G_{D\,min(max)} &= V_{in}/(nV_{o\,max(min)}). \end{aligned} \tag{44}$$

Then, the gain requirement G is

$$G \in [G_{NP\,min}, G_{PO\,max}] \tag{45}$$

$$G_{PO\,max} = \max\{G_{C\,max}, G_{D\,max}\} \tag{45a}$$

$$G_{NP\,min} = \min\{G_{C\,min}, G_{D\,min}\}. \tag{45b}$$

4) *Step 4. Determine characteristic impedance Z_0 using PO/PON/PN boundaries:* In this application, the input voltage and output power can be seen as constants. Hence, the minimum value of $(G_{PO}\omega_n)_{min}$ should be obtained to get the PO/PON/PN boundaries according to (26). However, (26) indicates that the core parameters, k and Z_0, are coupled in the design process. A common approach to obtain the $(G_{PO}\omega_n)_{min}$ is to adopt the iterative process; however, this process is less intuitive and not expected. Fig. 19(a) shows Z_0 values with different k. In this figure, Z_0 decreases as k increases. When k is larger than 7, the minimum values of Z_0 are close. The higher the k, the closer the Z_0 values. Therefore, to simplify the design

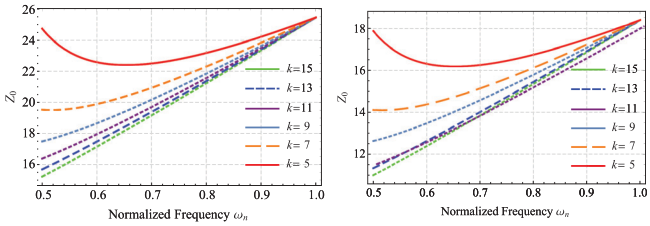


Fig. 19. Z_0 versus $\omega_{\rm n}$ with different k. (a) Charging mode. (b) Discharging mode.

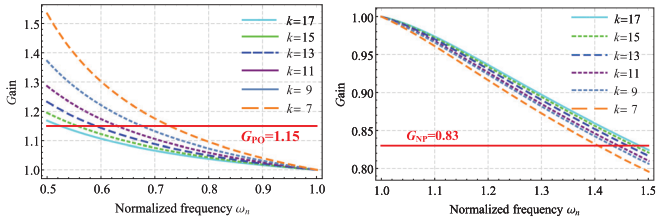


Fig. 20. Gain curves with different inductance ratios. (a) PO mode. (b) NP mode.

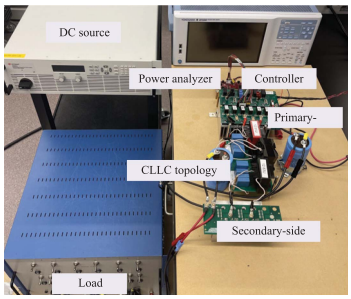


Fig. 21. Experiment prototype.

process and avoid solving by iteration, $Z_0 = 10$ is set with a safety margin because a higher appropriate Z_0 is preferred.

5) *Step 5. Determine inductance ratio k using voltage gain restriction:* Fig. 20 shows the gain curve with different k. To fulfill the basic voltage gain requirement, the gain in PO mode should be higher than 1.15 when 55 kHz $\leq f_{\rm s} <$ 100 kHz. Identically, the gain in NP mode should be lower than 0.83 when 150 kHz $\geq f_{\rm s} >$ 100 kHz. Combining these conditions, the k should be lower than 15. Therefore, to ensure good efficiency performance, $k = 14$ is preset in this step.

6) *Step 6. Determine inductance ratio k considering ZVS condition:* This step is to verify that the k and Z_0 can ensure the ZVS realization. To achieve ZVS, the primary-side current should discharge the output capacitance of four primary switches during the dead time t_d [13]. Therefore, to satisfy the ZVS criteria, the k should meet

$$k \leq \frac{\pi t_d}{8 C_{\rm oss} \omega_{\rm n\,max} Z_0}. \tag{46}$$

7) *Step 7. Determine all resonant parameters:* In the previous steps, the proper parameters k and Z_0 are selected. Thus, the resonant inductors and capacitors can be

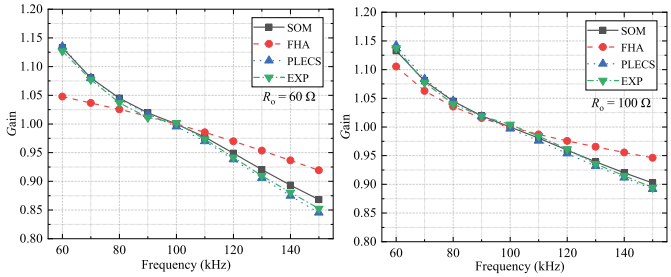


Fig. 22. Voltage gain comparison. (a) Charging mode. (b) Discharging mode.

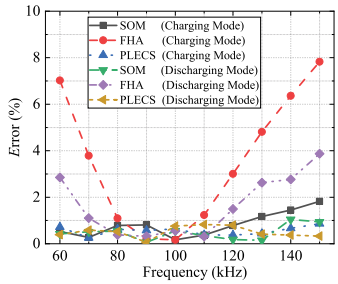


Fig. 23. Voltage gain errors.

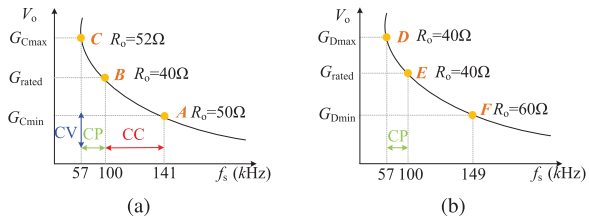


Fig. 24. Test results. (a) Charging mode. (b) Discharging mode.

TABLE VI
DESIGN RESULTS

Parameters	Symbol	Design
Inductance ratio	k	14
Characteristic impedance	Z_0	9.42
Transformer turns ratio	n	1
Primary-side series inductance	$L_{\rm rp}$	15 μH
Secondary-side series inductance	$L_{\rm rs}$	15 μH
Magnitizing inductance	$L_{\rm m}$	210 μH
Primary-side series capacitance	$C_{\rm rp}$	168.9 nF
Secondary-side series capacitance	$C_{\rm rs}$	168.9 nF

determined by

$$L_{\rm rp} = n^2 L_{\rm rs} = \frac{Z_0}{\omega_{\rm r}} = \frac{L_{\rm m}}{k}$$
$$C_{\rm rp} = \frac{C_{\rm rs}}{n^2} = \frac{1}{\omega_{\rm r} Z_0} = \frac{k}{4\pi^2 f_{\rm r}^2 L_{\rm m}}. \tag{47}$$

8) *Step 8. Verification using simulations and experiments:* All the designed resonant parameters are listed in Table VI. The detailed simulation and experiment results are analyzed in Section IV. Typically, the proposed parameter design methodology is intuitive and noniterative. This is because of the high accuracy of the proposed

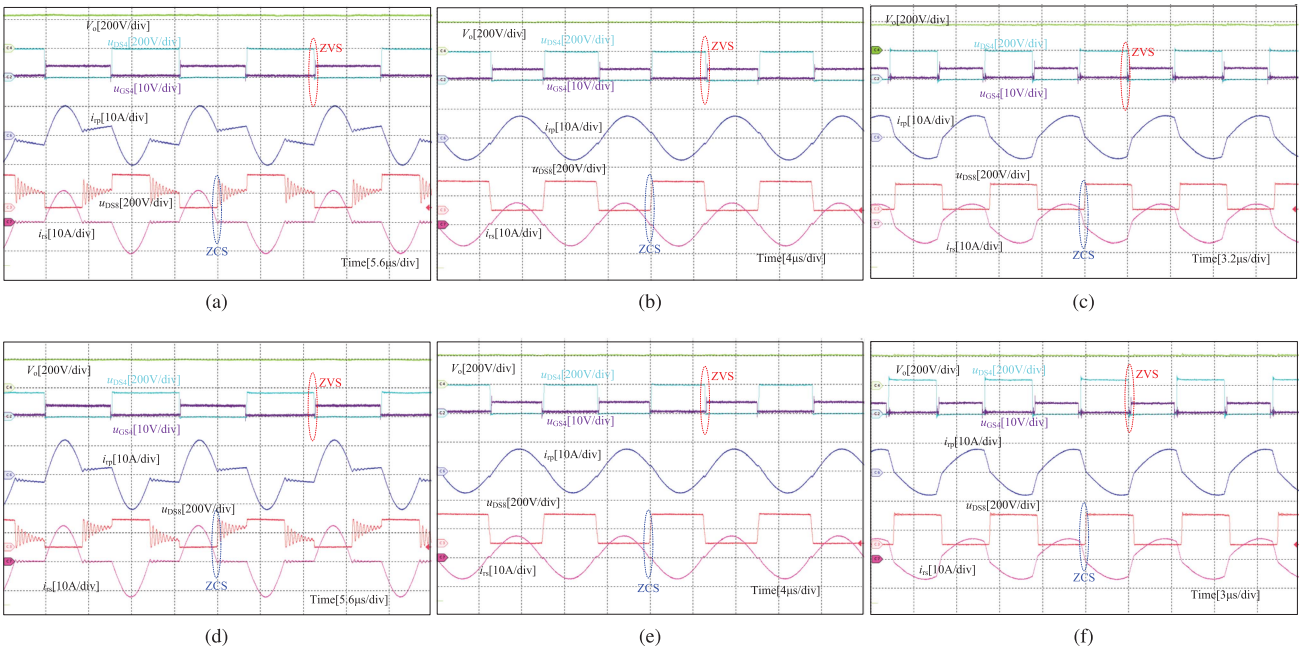


Fig. 25. Detailed waveforms. (a) Point A. (b) Point B. (c) Point C. (d) Point D. (e) Point E. (f) Point F.

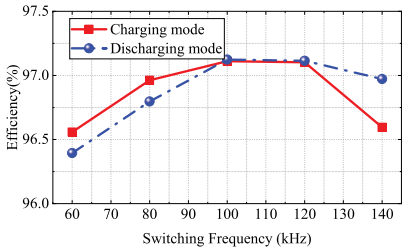


Fig. 26. Efficiency curves when output power is 1 kW.

SOM model and intuitive parameter design methodology. In some extreme situations, if the simulation result does not satisfy the system specification, the designer could change the value of characteristic impedance Z_0 first. If the updated Z_0 is still not effective, the user can decrease the inductance ratio k to fulfill the system specifications.

IV. Experiments

A. Experiment Setup

A 1-kW CLLC converter prototype is designed and implemented to verify the correctness and effectiveness of the proposed simplified model and parameter design process. The experimental platform is shown in Fig. 21. The transformer uses PQ5050 cores, and the resonant inductors use EE cores. Metalized polypropylene film capacitors are utilized as the resonant capacitors. TI Launchpad-F28379D is used to control the CLLC charger.

B. Experiment Results

First of all, the voltage gain expressions are verified. The gain comparison among SOM model, FHA model, PLECS simulation and experiment results (EXP) is shown in Fig. 22. Fig. 23 shows the voltage gain accuracy as percentage error. Figs. 22 and 23 together illustrate that the SOM model results are closer to the experimental results. Oppositely, the FHA model is not satisfactory. Its error increases rapidly when the switching frequency becomes far from the resonant frequency. Therefore, the proposed model is better for parameter design.

Then, the conditions when the CLLC charger works in different modes are studied. Fig. 24(a) shows that the frequency modulation range is 57 kHz–141 kHz with different output power in charging mode, which can satisfy the output voltage requirement from 170 V to 230 V. According to the battery charging profile, six key points A–F with different voltage gains are tested, as shown in Fig. 25. The corresponding loads are also listed in Fig. 24. This frequency modulation range matches the theoretical analysis well. In detail, for point A [Fig. 25(a)], the converter works in the NP mode. The output voltage is 170 V (the minimum gain requirement), and the operation frequency is 141 kHz. For point B [Fig. 25(b)], the converter works in the P mode, and the output voltage is rated. For point C [Fig. 25(c)], the converter works in the PO mode, and the output voltage is 230 V (the maximum gain requirement). In addition, the primary-side MOSFETs' ZVS turn-OFF and secondary-side diodes' ZCS turn-ON can be realized for all points. Similarly, Fig. 24(b) and Fig. 25(d)–(f) show that the designed parameters could also satisfy the performance requirements in discharging mode. In conclusion, the experimental results demonstrate strong agreement to the SOM model.

The system efficiency when the output power is 1 kW is tested using the power analyzer YOKOGAMA WT5000, and the efficiency curve is illustrated in Fig. 26. In the entire voltage regulation process, the system efficiency is larger than 96%, and the peak efficiency is 97.1% when the switching frequency is 100 kHz, which verifies the acquisition of high efficiency.

TABLE VII
COMPARISON WITH PREVIOUS PARAMETER DESIGN METHODS

References	[15]	[13]	[17]	[27]	[28]	[23]	[24]	This paper
Topology	CLLC	CLLC	CLLC	CLLC	LLC	CLLC	CLLC	CLLC
Model	FHA	FHA	FHA	Time-domain	Time-domain	Time-domain	Time-domain	Time-domain
Operation mode	P mode	N/A	N/A	P/PO modes	PO mode	P/PO/NP modes	N/A	P/PO/NP modes
Accuracy	⋆⋆⋆	⋆	⋆	⋆⋆⋆⋆	⋆⋆⋆⋆	⋆⋆⋆	⋆⋆⋆⋆	⋆⋆⋆
Iteration required	No	Yes	Yes	Yes	Yes	N/A	Yes	No
Voltage gain expression visualization	Yes	Yes	Yes	No	No	No	No	Yes
Complexity	⋆	⋆	⋆⋆⋆	⋆⋆⋆	⋆⋆⋆	N/A	⋆⋆⋆⋆	⋆

C. Comparison With Previous Parameter Design Methods

The comparison with other parameter design methods are listed in Table VII. Compared with the FHA-based methods, the accuracy of the proposed SOM model is significantly improved Simultaneously, the SOM model contains more information regarding the soft-switching characteristics and the reliability zone. Therefore, this design method is more comprehensive. Likewise, by simplifying the time-domain model, the calculation amount is significantly reduced. The visualized voltage gain expressions can be obtained with the tradeoff between calculation simplicity and accuracy, which benefits the engineers' parameter design. In this procedure, repeated iterations are avoided, and the complexity of obtaining the best parameters is decreased dramatically. In conclusion, the proposed model matches the real converter very well. The presented parameter design method is intuitive and straightforward, providing high efficiency and reliability for the CLLC converter.

V. CONCLUSION

A SOM model for the CLLC converter by simplifying the operation mode expressions and waveforms is illustrated in this article. The proposed model is much more accurate and intuitive than the traditional FHA method and the complicated TDM. Moreover, the conditions that ensure the system operates in high efficiency and reliability zone (PO/PON/PN boundaries) are studied. In consideration of the system efficiency, soft-switching conditions, gain range, current/voltage stress, a simple and direct parameter design methodology without iteration using k and Z_0 is proposed. The simulation and experimental results show great consistency with the proposed SOM model and the parameter design methodology.

REFERENCES

[1] N. Chen et al., "Synchronous rectification based on resonant inductor voltage for CLLC bidirectional converter," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 547–561, Jan. 2022.

[2] H. Chen, K. Sun, L. Lu, S. Wang, and M. Ouyang, "A constant current control method with improved dynamic performance for CLLC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1509–1523, Feb. 2022.

[3] Z. Zhang, C. Liu, M. Wang, Y. Si, Y. Liu, and Q. Lei, "High-efficiency high-power-density CLLC resonant converter with low-stray-capacitance and well-heat-dissipated planar transformer for EV on-board charger," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10831–10851, Oct. 2020.

[4] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A novel three-level CLLC resonant DC–DC converter for bidirectional EV charger in DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2334–2344, Mar. 2021.

[5] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018.

[6] H. Chen, K. Sun, H. Shi, J.-I. Ha, and S. Lee, "A battery charging method with natural synchronous rectification features for full-bridge CLLC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2139–2151, Feb. 2022.

[7] W. L. Malan, D. M. Vilathgamuwa, and G. R. Walker, "Modeling and control of a resonant dual active bridge with a tuned CLLC network," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7297–7310, Oct. 2016.

[8] S. Zou, A. Mallik, J. Lu, and A. Khaligh, "Sliding mode control scheme for a CLLC resonant converter," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12274–12284, Dec. 2019.

[9] Y. Cao, M. Ngo, R. Burgos, A. Ismail, and D. Dong, "Switching transition analysis and optimization for bidirectional CLLC resonant DC transformer," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3786–3800, Apr. 2022.

[10] Y. Cao, M. Ngo, N. Yan, Y. Bai, R. Burgos, and D. Dong, "DC distribution converter with partial power processing for LVDC/MVDC systems," in *Proc. IEEE 4th Int. Conf. DC Microgrids*, 2021, pp. 1–8.

[11] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kV SiC-Based 7 kV/400 V DC transformer for future data centers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 753–767, Jun. 2019.

[12] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.

[13] J.-H. Jung, H.-S. Kim, M.-H. Ryu, and J.-W. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013.

[14] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J.-S. Lai, "Design of bidirectional DC–DC resonant converter for vehicle-to-grid (V2G) applications," *IEEE Trans. Transport. Electrific.*, vol. 1, no. 3, pp. 232–244, Oct. 2015.

[15] J. Huang et al., "Robust circuit parameters design for the CLLC-Type DC transformer in the hybrid AC–DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1906–1918, Mar. 2019.

[16] B. Zhao, X. Zhang, and J. Huang, "AI algorithm-based two-stage optimal design methodology of high-efficiency CLLC resonant converters for the hybrid AC–DC microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9756–9767, Dec. 2019.

[17] J. Min and M. Ordonez, "Bidirectional resonant CLLC charger for wide battery voltage range: Asymmetric parameters methodology," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6662–6673, Jun. 2021.

[18] J. Huang, X. Zhang, and B. Zhao, "Simplified resonant parameter design of the asymmetrical CLLC-Type DC transformer in the renewable energy system via semi-artificial intelligent optimal scheme," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1548–1562, Feb. 2020.

[19] A. Sankar, A. Mallik, and A. Khaligh, "Extended harmonics based phase tracking for synchronous rectification in CLLC converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6592–6603, Aug. 2019.

[20] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "3.3 kW CLLC converter with synchronous rectification for plug-in electric vehicles," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2017, pp. 1–6.
[21] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.
[22] J. Liu, J. Zhang, T. Q. Zheng, and J. Yang, "A modified gain model and the corresponding design method for an LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6716–6727, Sep. 2017.
[23] Y. Cao, M. Ngo, D. Dong, and R. Burgos, "A simplified time-domain gain model for CLLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 3079–3086.
[24] L. Zhao, Y. Pei, L. Wang, L. Pei, W. Cao, and Y. Gan, "Design methodology of bidirectional resonant CLLC charger for wide voltage range based on parameter equivalent and time domain model," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12041–12064, Oct. 2022.
[25] M. Daryaei, M. Ebrahimi, and S. A. Khajehoddin, "Alternative approach to analysis and design of series resonant converter at steady state," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4424–4435, Jun. 2019.
[26] M. Daryaei, S. A. Khajehoddin, J. Mashreghi, and K. K. Afridi, "A new approach to steady-state modeling, analysis, and design of power converters," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12746–12768, Nov. 2021.
[27] Z. Lv, X. Yan, Y. Fang, and L. Sun, "Mode analysis and optimum design of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1513–1520.
[28] J. Deng, C. C. Mi, R. Ma, and S. Li, "Design of LLC resonant converters based on operation-mode analysis for level two PHEV battery chargers," *IEEE/ASME Trans. Mechatronics*, vol. 20, no. 4, pp. 1595–1606, Aug. 2015.
[29] D. Shu and H. Wang, "Light-load performance enhancement technique for LLC-Based PEV charger through circuit reconfiguration," *IEEE Trans. Transport. Electrific.*, vol. 7, no. 4, pp. 2104–2113, Dec. 2021.
[30] H. J. Chae, W. Y. Kim, S. Y. Yun, Y. S. Jeong, J. Y. Lee, and H. T. Moon, "3.3 kW on board charger for electric vehicle," in *Proc. 8th Int. Conf. Power Electron. - ECCE Asia*, 2011, pp. 2717–2719.
[31] F. Lin, X. Zhang, and X. Li, "Design methodology for symmetric CLLC resonant DC transformer considering voltage conversion ratio, system stability, and efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10157–10170, Sep. 2021.
[32] M. Ivankovic and J. M. Hancock, "Part I: LLC calculator, FHA analysis based on a vector algorithm." 2018. [Online]. Available: https://www.infineon.com/dgdl/Infineon-Part-I_LLC_calculator-AN-v01_00-EN.pdf?fileId=5546d46265487f7b0165670ca6287978
[33] L. Wang, Q. Luo, and T. Luo, "A time-domain optimization design methodology for CLLC resonant converter," in *Proc. IEEE 1st Int. Power Electron. Appl. Symp.*, 2021, pp. 1–5.

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