# An Integrated Three-Phase AC–DC Wireless-Power-Transfer Converter With Active Power Factor Correction Using Three Transmitter Coils

Junwei Liu, *Member, IEEE*, Chi Shing Wong, *Member, IEEE*, Zilin Li, *Member, IEEE*, Xingyue Jiang, and K. H. Loo, *Member, IEEE*

***Abstract*—Three-phase ac–dc converters are more commonly used for high-power applications compared with single-phase converters. For high-power wireless power transfer (WPT) applications, such as wireless electric vehicle chargers, usually a two-stage topology is applied, which consists of a three-phase ac–dc rectifier with power factor correction and a dc–dc converter for WPT. Recently, there are several studies on three-phase single-stage WPT solutions being proposed to reduce power conversion stages and, furtherly, increase the overall efficiency and reduce system cost. In this article, an integrated three-phase ac–dc WPT converter topology with active power factor correction is proposed. The count of power semiconductor devices is significantly reduced compared with the state-of-the-art three-phase single-stage topologies. Moreover, three transmitter coils are used to enhance the system power capacity. Topology description, operation analysis, control method, power loss analysis, and reference design guideline of the proposed topology are presented in detail. Finally, a laboratory prototype is built and evaluated. The functionalities, performances, and advantages are demonstrated by the corresponding experimental results.**

***Index Terms*—Integrated, power factor correction (PFC), single-stage, three-phase, wireless power transfer (WPT).**

## I. Introduction

WIRELESS power transfer (WPT) technology has been applied to industrial, consumer, and medical products with power levels ranging from several milliwatts to tens of kilowatts, including mobile phone wireless chargers [1], light-emitting diode (LED) drivers [2], [3], biomedical implants contactless power supply [4], [5], [6], and electric vehicle (EV) charger [7], [8], [9], [10], [11]. It is getting increasing popularity because of the advantages of convenience, safety, and reliability as compared with the traditional wired power transmission. There have been a variety of studies on WPT, as most of those are focused on dc–dc topologies [12], [13], [14], [15], energy efficiency optimization [16], [17], [18], [19], load and coupling identification [20], [21], and multicoil systems [9], [22], [23], [24]. Recently, ac–dc WPT systems [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35] are drawing more attention because of the increasing demands for grid-connected applications, such as EV chargers.

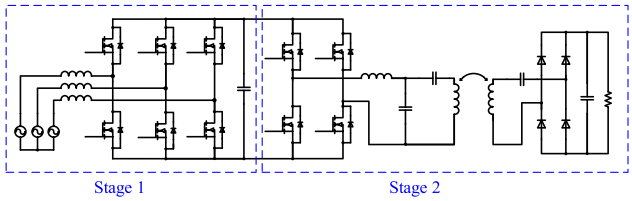


Fig. 1. Example of traditional two-stage three-phase AC–DC WPT converter with PFC.

For high-power grid-connected applications, three-phase topologies are preferred than single-phase solutions. Atypical three-phase ac–dc WPT converter is required to provide good power quality to the power grid. It usually consists of two power conversion stages: a front-end three-phase ac–dc power-factor-correction (PFC) rectifier as the first stage, and a dc–dc WPT converter as the second stage, as shown in Fig. 1. Usually three-phase six-switch PFC rectifier [36], [37], Vienna rectifier [38], [39], Swiss rectifier [40], TAIPEI rectifier [39], or other types of three-phase PFC rectifier [42], [43], [44] are used as the first stage, while the second stage can be dc–dc WPT converters with different compensation networks. Generally, a three-phase two-stage topology needs two control strategies for both stages, which obviously increases the system control complexity. Besides, the highest efficiency cannot be achieved due to more power losses in two power conversion stages. Moreover, it cannot achieve the lowest cost because more power semiconductor devices are required.

Manuscript received 8 August 2022; revised 12 November 2022 and 25 December 2022; accepted 18 January 2023. Date of publication 23 January 2023; date of current version 20 April 2023. This work was supported in part by Hong Kong Polytechnic University Postdoctoral Fellowships Scheme under Project G-YW4X and in part by Hong Kong RGC Postdoctoral Fellowship Scheme 2019/2020 under Project PDFS 2021-5S10. Recommended for publication by Associate Editor A. Kuperman. *(Corresponding author: Zilin Li.)*

Junwei Liu, Chi Shing Wong, Xingyue Jiang, and K. H. Loo are with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong (e-mail: liujunwei_hust@hotmail.com; chi.shing.wong@connect.polyu.hk; xingyue.jiang@connect.polyu.hk; kh.loo@polyu.edu.hk).

Zilin Li is with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong (e-mail: zi-lin.li@connect.polyu.hk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3238877.

Digital Object Identifier 10.1109/TPEL.2023.3238877

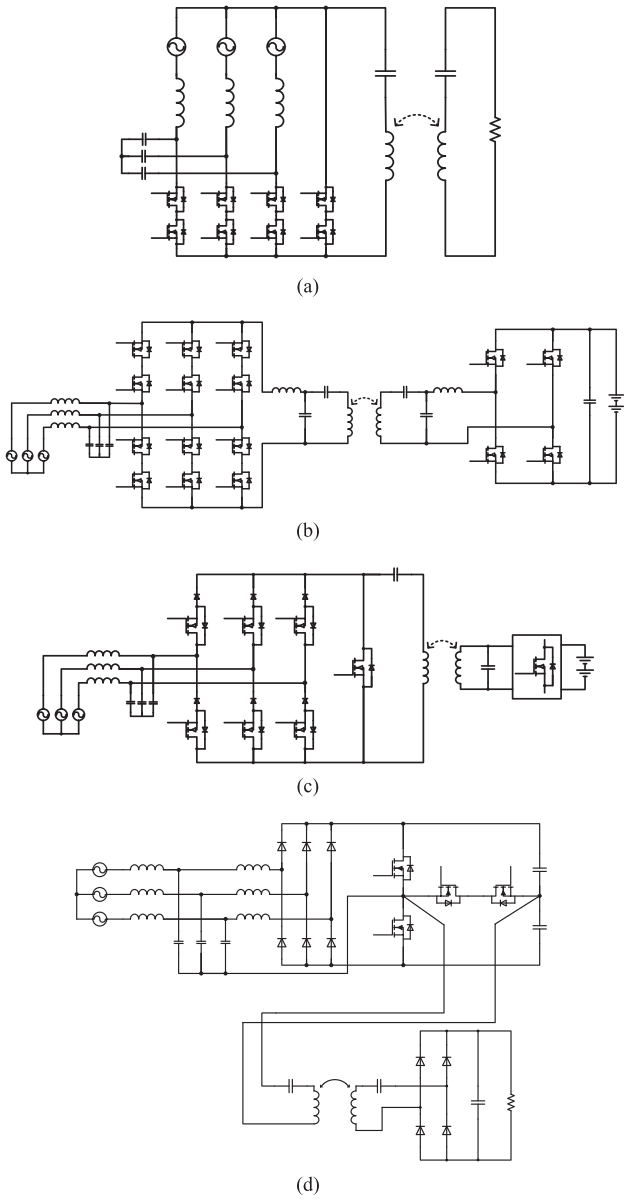


Fig. 2. State-of-the-art three-phase single-stage and integrated AC–DC WPT topologies. (a) Matrix topology I [26]. (b) Matrix topology II [27]. (c) Matrix topology III [28]. (d) T-type-based topology [29].

Recently, there have been several studies [26], [27], [28], [29] on integrating both three-phase ac–dc PFC rectifier and dc–dc WPT converter into only one power conversion stage. They are proposed to overcome the drawbacks of two-stage topologies. Most of them apply direct ac–ac or matrix topologies [26], [27], [28], as shown in Fig. 2(a)–(c). There is no dc bus capacitor in these topologies, and all the low-frequency ripples are filtered by the secondary-side output capacitor. Although these topologies apply only one power conversion stage, their counts of power semiconductor are still very high. At the system primary side, the matrix topologies proposed in [26] and [27] utilize 8 and 12 active switches, respectively. The matrix converter proposed in [28] utilize seven active switches and six diodes in total at the primary side. A three-phase single-stage topology with a dc bus link is proposed to further reduce the count of active switches [29]. It uses a common T-type inverter to realize PFC and isolated dc–dc conversion functionalities simultaneously, as shown in Fig. 2(d). Although only four active switches are used, six more diodes are still required. Moreover, the input power quality is not sufficiently high because the PFC function is naturally achieved by input inductor current working in discontinuous current mode (DCM), which also causes higher losses of input inductors and active switches, and electromagnetic interference (EMI) problems.

In general, more switches not only increase the cost of power semiconductor devices but also increase the cost of corresponding gate drivers and isolated dc–dc power supplies. With the design target of further reducing system cost, this article proposes a novel integrated three-phase ac–dc WPT converter topology with three transmitter coils. The count of power semiconductor devices is significantly reduced compared with the state-of-the-art three-phase single-stage topologies. Besides, the input currents are actively shaped to achieve a sufficiently high power quality for the three-phase power source. Moreover, the proposed topology utilizes three transmitter coils at the primary side to enhance the system power capacity, which has not been explored in the existing studies on three-phase single-stage solutions.

In this article, topology description, operation analysis, control method, and power loss analysis of the proposed converter are introduced and illustrated in Section II. Then, the design procedure and considerations for the laboratory prototype are given in Section III. Finally, the experimental results are presented to verify the analysis, design, and performances in Section IV. Finally, Section V concludes this article.

## II. Proposed Topology

### A. Inspiration and Design Philosophy

For high-power grid-connected ac–dc WPT applications, a three-phase ac input interface is preferred than a single-phase ac input interface. The traditional grid-connected ac–dc WPT converters aiming for three-phase ac input interface require two power conversion stages, including the three-phase ac–dc PFC rectifier as the first stage and the dc–dc WPT converter as the second stage, as shown in Fig. 1. The traditional two-stage topology utilizes one three-phase six-switch bridge structure and one full-bridge structure in the primary side to achieve three-phase line-frequency ac–dc PFC operation and high-frequency dc–ac conversion for primary WPT coil, respectively. Since the outputs of the three-phase six-switch bridge structure with sinusoidal pulsewidth modulation (SPWM) not only include line-frequency components but also include switching-frequency (carrier frequency) components, the idea of using only one three-phase six-switch bridge structure in the primary side to achieve two functions is inspired. In other words, the switching-frequency components of the three-phase six-switch bridge structure's outputs can be used to excite the WPT resonant tank.

In general, more power switches not only increase the cost of power semiconductor devices but also increase the cost of the corresponding gate drivers and isolated dc–dc power supplies.

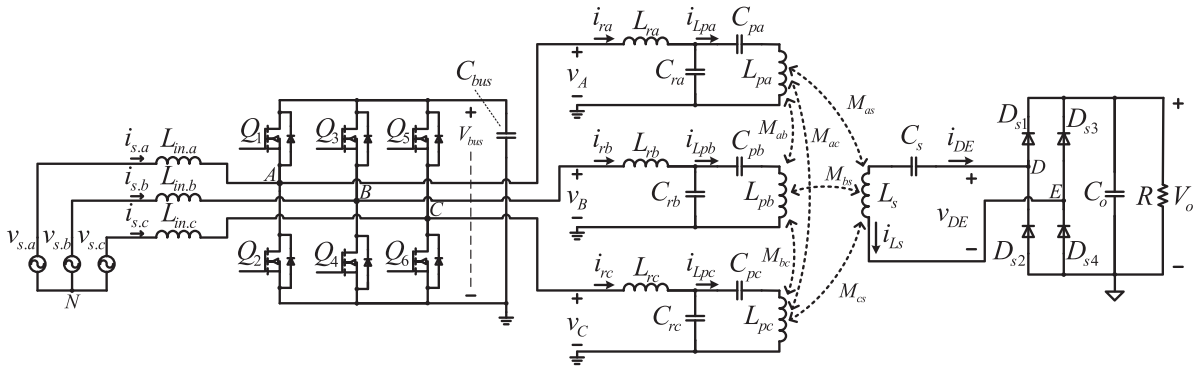


Fig. 3. Proposed integrated three-phase AC–DC WPT converter.

The inspiration of this idea is to minimize the count of power semiconductor devices of the three-phase ac–dc WPT system and, further, to reduce the system cost, while providing high performances of system efficiency and PFC. In the meantime, the problems of unbalanced switch current stress and severe output double-line-frequency ripple should be avoided.

There are three output ports (A, B, C in Fig. 3) of the three-phase six-switch bridge structure. Considering the requirements of switch current stress balancing and output double-line-frequency ripple suppression, three output ports should be connected to three identical transmitter coils. While considering the minimization of the power semiconductor device count, only one receiver coil as well as one full-bridge rectifier (with only four diodes) would be preferred. Therefore, according to the above analysis, the structure of three transmitter coils and one receiver coil is selected and the proposed topology is finally inspired.

### B. Topology Description

Fig. 3 shows the proposed integrated three-phase ac–dc WPT converter with reduced power devices count and active PFC. There are three transmitter coils with *LCC* compensations at the primary side, while there is one receiver coil with series compensation at the secondary side. The self-inductances of the transmitter coils are noted as $L_{pa}$, $L_{pb}$, and $L_{pc}$, respectively. The *LCC* compensation parameters of $L_{pa}$ are noted as $L_{ra}$, $C_{ra}$, and $C_{pa}$. The *LCC* compensation parameters of $L_{pb}$ are noted as $L_{rb}$, $C_{rb}$, and $C_{pb}$. The *LCC* compensation parameters of $L_{pc}$ are noted as $L_{rc}$, $C_{rc}$, and $C_{pc}$. The self-inductance of the receiver coil is noted as $L_s$, and $C_s$ is defined as its compensation capacitor. $M_{ab}$, $M_{bc}$, and $M_{ac}$ are defined as the mutual inductances between the transmitter coils. $M_{as}$, $M_{bs}$, and $M_{cs}$ are defined as the mutual inductances of the transmitter coils and the receiver coil, respectively. A three-phase six-switch bridge structure is used to perform PFC and WPT coils excitation functions simultaneously. $Q_1$–$Q_6$ are defined as the power switches of the three-phase bridge structure. $v_{s.a}$, $v_{s.b}$, and $v_{s.c}$ are defined as the phase voltages of the three-phase voltage source. $L_{\text{in}.a}$, $L_{\text{in}.b}$, and $L_{\text{in}.c}$ are defined as the input PFC inductors. $C_{\text{bus}}$ is defined as the dc bus capacitor. $D_{s1}$–$D_{s4}$ are defined as the secondary-side rectifier diodes. $C_o$ is the output capacitor. The load resistance is noted as $R$.

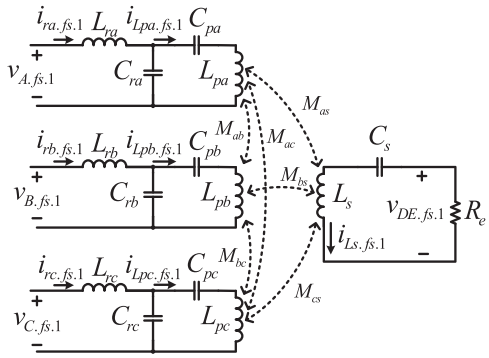


Fig. 4. FHA (at switching frequency $f_s$) equivalent circuit of the WPT conversion part.

As shown in Fig. 3, the three-phase input currents are noted as $i_{s.a}$, $i_{s.b}$, and $i_{s.c}$. The voltages at nodes A, B, and C of the three-phase bridge are noted as $v_A$, $v_B$, and $v_C$, respectively. The currents flowing through $L_{ra}$, $L_{rb}$, and $L_{rc}$ are noted as $i_{ra}$, $i_{rb}$, and $i_{rc}$, respectively. The currents flowing through $L_{pa}$, $L_{pb}$, and $L_{pc}$ are noted as $i_{Lpa}$, $i_{Lpb}$, and $i_{Lpc}$, respectively. $V_{\text{bus}}$ is defined as the dc bus voltage across $C_{\text{bus}}$. The current flowing through $L_s$ is noted as $i_{Ls}$. The voltage and current of the secondary-side full-bridge rectifier is noted as $v_{DE}$ and $i_{DE}$, respectively. $V_o$ is the output voltage.

### C. WPT Conversion Part

The WPT conversion part receives the excitations from the three-phase bridge structure and transfers the power wirelessly to the dc load. Applying fundamental harmonic approximation (FHA) method at switching frequency ($f_s$), the equivalent circuit is shown in Fig. 4, where $v_{A.fs.1}$, $v_{B.fs.1}$, $v_{C.fs.1}$, $i_{ra.fs.1}$, $i_{rb.fs.1}$, $i_{rc.fs.1}$, $i_{Lpa.fs.1}$, $i_{Lpb.fs.1}$, $i_{Lpc.fs.1}$, $i_{Ls.fs.1}$, and $v_{DE.fs.1}$ are the switching-frequency ($f_s$) fundamental (first order) components of $v_A$, $v_B$, $v_C$, $i_{ra}$, $i_{rb}$, $i_{rc}$, $i_{Lpa}$, $i_{Lpb}$, $i_{Lpc}$, $i_{Ls}$, and $v_{DE}$, respectively. Applying Kirchhoff's voltage law to the equivalent circuit, the following equations are obtained:

$$\begin{aligned} v_{A.fs.1} &= j\omega_s L_{ra}\cdot i_{ra.fs.1} + \tfrac{1}{j\omega_s C_{ra}}\cdot(i_{ra.fs.1} - i_{Lpa.fs.1}) \\ \tfrac{1}{j\omega_s C_{ra}}\cdot(i_{ra.fs.1} - i_{Lpa.fs.1}) &= \left(j\omega_s L_{pa} + \tfrac{1}{j\omega_s C_{pa}}\right)\cdot i_{Lpa.fs.1} \\ &+ j\omega_s M_{ab}\cdot i_{Lpb.fs.1} + j\omega_s M_{ac}\cdot i_{Lpc.fs.1} + j\omega_s M_{as}\cdot i_{Ls.fs.1} \end{aligned} \quad (1)$$

$$\begin{aligned} &v_{B.fs.1} = j\omega_s L_{rb}\cdot i_{rb.fs.1} + \tfrac{1}{j\omega_s C_{rb}}\cdot(i_{rb.fs.1} - i_{Lpb.fs.1}) \\ &\tfrac{1}{j\omega_s C_{rb}}\cdot(i_{rb.fs.1} - i_{Lpb.fs.1}) = \left(j\omega_s L_{pb} + \tfrac{1}{j\omega_s C_{pb}}\right)\cdot i_{Lpb.fs.1} \\ &+j\omega_s M_{ab}\cdot i_{Lpa.fs.1} + j\omega_s M_{bc}\cdot i_{Lpc.fs.1} + j\omega_s M_{bs}\cdot i_{Ls.fs.1} \end{aligned} \tag{2}$$

$$\begin{aligned} &v_{C.fs.1} = j\omega_s L_{rc}\cdot i_{rc.fs.1} + \tfrac{1}{j\omega_s C_{rc}}\cdot(i_{rc.fs.1} - i_{Lpc.fs.1}) \\ &\tfrac{1}{j\omega_s C_{rc}}\cdot(i_{rc.fs.1} - i_{Lpc.fs.1}) = \left(j\omega_s L_{pc} + \tfrac{1}{j\omega_s C_{pc}}\right)\cdot i_{Lpc.fs.1} \\ &+j\omega_s M_{ac}\cdot i_{Lpa.fs.1} + j\omega_s M_{bc}\cdot i_{Lpb.fs.1} + j\omega_s M_{cs}\cdot i_{Ls.fs.1} \end{aligned} \tag{3}$$

$$\begin{aligned} &v_{DE.fs.1} = \left(j\omega_s L_s + \tfrac{1}{j\omega_s C_s}\right)\cdot i_{Ls.fs.1} \\ &+ j\omega_s M_{as}\cdot i_{Lpa.fs.1} + j\omega_s M_{bs}\cdot i_{Lpb.fs.1} \\ &+j\omega_s M_{cs}\cdot i_{Lpc.fs.1} \\ &v_{DE.fs.1} = -R_e\cdot i_{Ls.fs.1} \end{aligned} \tag{4}$$

where $R_e$ is the equivalent resistance, calculated as follows:

$$R_e = \frac{8}{\pi^2}R. \tag{5}$$

From (4), if $L_s$ and $C_s$ are designed at resonant condition, $v_{DE.fs.1}$ is determined by $i_{Lpa.fs.1}$, $i_{Lpb.fs.1}$, and $i_{Lpc.fs.1}$, as well as $M_{as}$, $M_{bs}$, and $M_{cs}$. Hence, if $i_{Lpa.fs.1}$, $i_{Lpb.fs.1}$, and $i_{Lpc.fs.1}$ can be independently controlled by $v_{A.fs.1}$, $v_{B.fs.1}$, and $v_{C.fs.1}$, respectively, the output voltage $v_{DE.fs.1}$ can be regulated correspondingly. To achieve this target, the design requirements of the compensation parameters are expressed as follows:

$$\omega_s L_s - 1/(\omega_s C_s) = 0 \tag{6}$$

$$\omega_s L_{ra} - \frac{1}{\omega_s C_{ra}} = \omega_s L_{rb} - \frac{1}{\omega_s C_{rb}} = \omega_s L_{rc} - \frac{1}{\omega_s C_{rc}} = 0. \tag{7}$$

By substituting (6) and (7) into (1)–(4), the voltage relation from $v_{A.fs.1}$, $v_{B.fs.1}$, and $v_{C.fs.1}$ to $v_{DE.fs.1}$ is obtained as follows:

$$v_{DE.fs.1} = v_{A.fs.1}\frac{M_{as}}{L_{ra}} + v_{B.fs.1}\frac{M_{bs}}{L_{rb}} + v_{C.fs.1}\frac{M_{cs}}{L_{rc}}. \tag{8}$$

From (8), the load voltage is load independent and can be directly regulated by $v_{A.fs.1}$, $v_{B.fs.1}$, and $v_{C.fs.1}$ together.

For the input ports of the equivalent circuit, as shown in Fig. 4, the input impedances should be designed resistive or close to resistive. From (1)–(7), the input impedances are obtained as follows: Eqs. (9)–(11) shown at the bottom of this page.

The modulation and control targets are focused on providing constant output voltage and minimizing reactive power resulting from the transmitter coils. In the following sections, the specific modulation and control methods will be introduced in detail.

### D. Three-Phase PFC Rectifier Part

The three-phase PFC rectifier part consists of a three-phase voltage source, three input PFC inductors, a three-phase active bridge structure, and a bus capacitor. SPWM method is applied to achieve the PFC rectifying function because of its fixed frequency characteristic. Neglecting the parasitic resistances of the switches and inductors, the mathematical model is obtained as follows:

$$\begin{aligned} L_{\text{in}.a}\frac{di_{s.a}}{dt} &= v_{s.a} + \frac{v_{A.lo} + v_{B.lo} + v_{C.lo}}{3} - v_{A.lo} \\ L_{\text{in}.b}\frac{di_{s.b}}{dt} &= v_{s.b} + \frac{v_{A.lo} + v_{B.lo} + v_{C.lo}}{3} - v_{B.lo} \\ L_{\text{in}.c}\frac{di_{s.c}}{dt} &= v_{s.c} + \frac{v_{A.lo} + v_{B.lo} + v_{C.lo}}{3} - v_{C.lo} \end{aligned} \tag{12}$$

where $v_{A.lo}$, $v_{B.lo}$, and $v_{C.lo}$ are the low-frequency components of $v_A$, $v_B$, and $v_C$, including dc and ac line-frequency fundamental (first order) components. The inductances of $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$ are designed with the same value, noted as $L_{in}$. The phase voltages are expressed as follows:

$$\begin{aligned} v_{s.a} = V_{sp}\sin(\omega_l t),\ v_{s.b} = V_{sp}\sin\left(\omega_l t + \frac{2\pi}{3}\right), \\ v_{s.c} = V_{sp}\sin\left(\omega_l t + \frac{4\pi}{3}\right) \end{aligned} \tag{13}$$

where $V_{sp}$ is the peak value of the ac input phase voltage, and $\omega_l$ is the line frequency in radian. For ideal PFC requirement, the input phase currents are expressed as follows:

$$\begin{aligned} i_{s.a} = I_{sp}\sin(\omega_l t),\ i_{s.b} = I_{sp}\sin\left(\omega_l t + \frac{2\pi}{3}\right), \\ i_{s.c} = I_{sp}\sin\left(\omega_l t + \frac{4\pi}{3}\right) \end{aligned} \tag{14}$$

$$Z_{A.fs.1} = \frac{L_{ra}}{\left\{\begin{array}{l}\left[\frac{M_{as}^2}{L_{ra}} + \frac{v_{B.fs.1}M_{as}M_{bs}}{v_{A.fs.1}L_{rb}} + \frac{v_{C.fs.1}M_{as}M_{cs}}{v_{A.fs.1}L_{rc}}\right]\frac{1}{R_e} \\ +\frac{1}{j\omega_s}\left[1 - \left(\frac{L_{pa}}{L_{ra}} - \frac{1}{\omega_s^2 L_{ra}C_{pa}}\right) - \frac{v_{B.fs.1}M_{ab}}{v_{A.fs.1}L_{rb}} - \frac{v_{C.fs.1}M_{ac}}{v_{A.fs.1}L_{rc}}\right]\end{array}\right\}} \tag{9}$$

$$Z_{B.fs.1} = \frac{L_{rb}}{\left\{\begin{array}{l}\left[\frac{M_{bs}^2}{L_{rb}} + \frac{v_{A.fs.1}M_{as}M_{bs}}{v_{B.fs.1}L_{ra}} + \frac{v_{C.fs.1}M_{bs}M_{cs}}{v_{B.fs.1}L_{rc}}\right]\frac{1}{R_e} \\ +\frac{1}{j\omega_s}\left[1 - \left(\frac{L_{pb}}{L_{rb}} - \frac{1}{\omega_s^2 L_{rb}C_{pb}}\right) - \frac{v_{A.fs.1}M_{ab}}{v_{B.fs.1}L_{ra}} - \frac{v_{C.fs.1}M_{bc}}{v_{B.fs.1}L_{rc}}\right]\end{array}\right\}} \tag{10}$$

$$Z_{C.fs.1} = \frac{L_{rc}}{\left\{\begin{array}{l}\left[\frac{M_{cs}^2}{L_{rc}} + \frac{v_{B.fs.1}M_{cs}M_{bs}}{v_{C.fs.1}L_{rb}} + \frac{v_{A.fs.1}M_{cs}M_{as}}{v_{C.fs.1}L_{ra}}\right]\frac{1}{R_e} \\ +\frac{1}{j\omega_s}\left[1 - \left(\frac{L_{pc}}{L_{rc}} - \frac{1}{\omega_s^2 L_{rc}C_{pc}}\right) - \frac{v_{B.fs.1}M_{bc}}{v_{C.fs.1}L_{rb}} - \frac{v_{A.fs.1}M_{ac}}{v_{C.fs.1}L_{ra}}\right]\end{array}\right\}}. \tag{11}$$

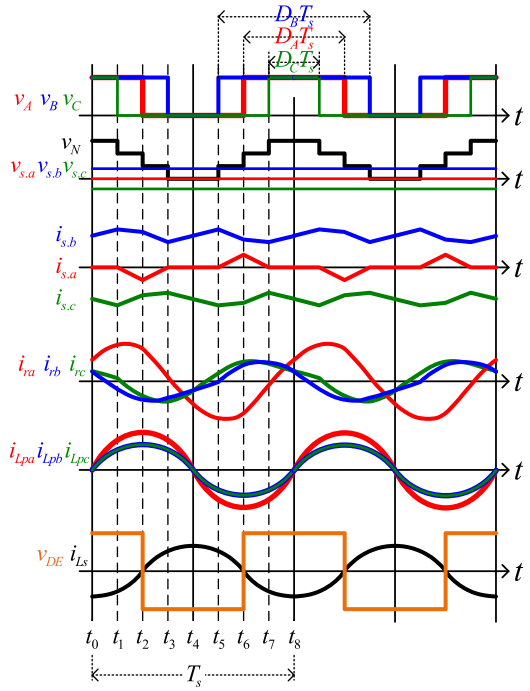


Fig. 5. Key operational waveforms.

where $I_{sp}$ is the peak value of the phase currents. $v_{A.lo}$, $v_{B.lo}$, and $v_{C.lo}$ can be solved as follows:

$$\begin{aligned} v_{A.lo} &= V_{sp}\sin(\omega_l t) - \omega_l L_{\text{in}} I_{sp}\cos(\omega_l t) + V_{\text{bus}}/2 \\ v_{B.lo} &= V_{sp}\sin(\omega_l t + 2\pi/3) - \omega_l L_{\text{in}} I_{sp}\cos(\omega_l t + 2\pi/3) \\ &\quad + V_{\text{bus}}/2 \\ v_{C.lo} &= V_{sp}\sin(\omega_l t + 4\pi/3) - \omega_l L_{\text{in}} I_{sp}\cos(\omega_l t + 4\pi/3) \\ &\quad + V_{\text{bus}}/2. \end{aligned} \tag{15}$$

Therefore, the duty cycles of $v_A$, $v_B$, and $v_C$ are obtained as follows:

$$\begin{aligned} D_A(\theta) &= \frac{V_{sp}}{V_{\text{bus}}}\sin(\theta) - \frac{\omega_l L_{\text{in}} I_{sp}}{V_{\text{bus}}}\cos(\theta) + 0.5 \\ D_B(\theta) &= \frac{V_{sp}}{V_{\text{bus}}}\sin\left(\theta + \frac{2\pi}{3}\right) - \frac{\omega_l L_{\text{in}} I_{sp}}{V_{\text{bus}}}\cos\left(\theta + \frac{2\pi}{3}\right) + 0.5 \\ D_C(\theta) &= \frac{V_{sp}}{V_{\text{bus}}}\sin\left(\theta + \frac{4\pi}{3}\right) - \frac{\omega_l L_{\text{in}} I_{sp}}{V_{\text{bus}}}\cos\left(\theta + \frac{4\pi}{3}\right) + 0.5 \end{aligned} \tag{16}$$

where $\theta$ is defined as the ac line angle, equal to $\omega_l t$.

### *E. Integrated-Power-Stage Analysis*

Fig. 5 shows the key waveforms of the proposed topology within a switching period $T_s$. $v_A$, $v_B$, and $v_C$ are the two-level pulsewidth modulation (PWM) voltages with duty cycles varying with ac line angle. Their switching-frequency fundamental components are obtained as follows:

$$\begin{aligned} v_{A.fs.1} &= (2V_{\text{bus}}/\pi)\sin(D_A\pi)\cos(\omega_s t) \\ v_{B.fs.1} &= (2V_{\text{bus}}/\pi)\sin(D_B\pi)\cos(\omega_s t) \\ v_{C.fs.1} &= (2V_{\text{bus}}/\pi)\sin(D_C\pi)\cos(\omega_s t). \end{aligned} \tag{17}$$

$V_{DE}$'s switching-frequency fundamental component is expressed as follows:

$$v_{DE.fs.1} = (4V_o/\pi)\cos(\omega_s t). \tag{18}$$

From (8), (17), and (18), the voltage transfer gain from $V_{\text{bus}}$ to $V_o$ is obtained as follows:

$$\frac{V_o}{V_{\text{bus}}} = \frac{\sin(D_A\pi)}{2}\frac{M_{as}}{L_{ra}} + \frac{\sin(D_B\pi)}{2}\frac{M_{bs}}{L_{rb}} + \frac{\sin(D_C\pi)}{2}\frac{M_{cs}}{L_{rc}}. \tag{19}$$

To simplify the control, $M_{as}$, $M_{bs}$, and $M_{cs}$ are designed with the same value $M_{ps}$. The compensation parameters and self-inductances of the transmitter coils, as well as their mutual inductances, are also designed identically:

$$\begin{aligned} &L_{ra} = L_{rb} = L_{rc} = L_r \\ &C_{ra} = C_{rb} = C_{rc} = C_r \\ &C_{pa} = C_{pb} = C_{pc} = C_p \\ &L_{pa} = L_{pb} = L_{pc} = L_p \\ &M_{ab} = M_{bc} = M_{ca} = M_{pp}. \end{aligned} \tag{20}$$

Hence, the voltage transfer gain from $V_{\text{bus}}$ to $V_o$ is updated as follows:

$$V_o/V_{\text{bus}} = (M_{ps}/(2L_r)) \cdot h_{ABC} \tag{21}$$

where $h_{ABC}$ is defined as follows:

$$h_{ABC} = \sin(D_A\pi) + \sin(D_B\pi) + \sin(D_C\pi). \tag{22}$$

From (16), since the term of $\omega_l L_{\text{in}} I_{sp}$ is much smaller than $V_{sp}$ in practical condition, $D_A$, $D_B$, and $D_C$ are approximated as follows:

$$\begin{aligned} D_A(\theta) &\approx r_m\sin(\theta) + 0.5 \\ D_B(\theta) &\approx r_m\sin\left(\theta + \frac{2\pi}{3}\right) + 0.5 \\ D_C(\theta) &\approx r_m\sin\left(\theta + \frac{4\pi}{3}\right) + 0.5 \end{aligned} \tag{23}$$

where $r_m$ is defined as the ratio of $V_{sp}$ and $V_{\text{bus}}$

$$r_m = \frac{V_{sp}}{V_{\text{bus}}} = \frac{\sqrt{2}V_{s.\text{rms}}}{V_{\text{bus}}} \tag{24}$$

where $V_{sp}$ and $V_{s.\text{rms}}$ are defined as the peak and root-mean-square (RMS) values of the ac input phase voltage, respectively. The range of $r_m$ is limited as follows:

$$0 < r_m \le 0.5. \tag{25}$$

Fig. 6 shows the relations of $h_{ABC}$ and line angle $\theta$ with different $r_m$ values. It can be observed that $h_{ABC}$ hardly varies with line angle $\theta$. $h_{ABC}$ can be considered constant if $r_m$ is fixed. It can also be indicated that $h_{ABC}$ can be regulated by $r_m$, and $h_{ABC}$ can be approximately expressed as follows:

$$h_{ABC} \approx 1 + 2\cos\left(\frac{\sqrt{3}}{2}r_m\pi\right). \tag{26}$$

From (20) and Fig. 6, the output voltage $V_o$ monotonously increases with $V_{\text{bus}}$. Therefore, if $V_o$ varies with the positions of

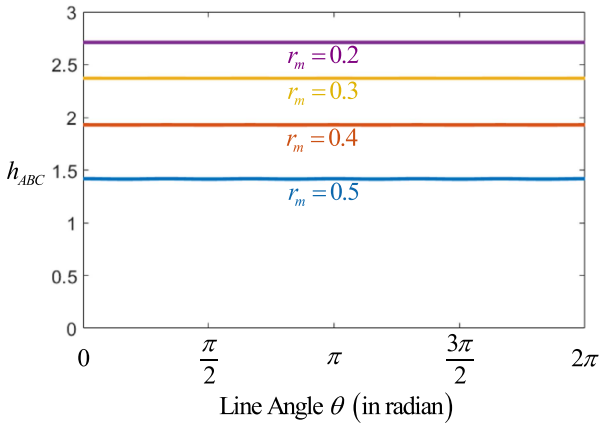


Fig. 6. Relations of $h_{ABC}$ and line angle $\theta$ (in radian) with different $r_m$ values.

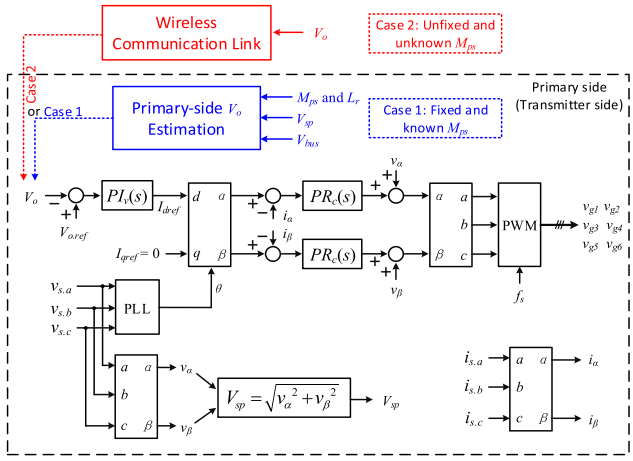


Fig. 7. Control block diagram.

primary- and secondary-side coils, $V_{\text{bus}}$ can be adjusted accordingly to maintain constant $V_o$ under different mutual inductance conditions.

For $i_{ra}$, $i_{rb}$, and $i_{rc}$, their reactive currents should be minimized to reduce the conduction losses on $L_{ra}$, $L_{rb}$, and $L_{rc}$, and the switches. The RMS value of $i_{ra}$'s, $i_{rb}$'s, and $i_{rc}$'s switching-frequency fundamental reactive components within a line period can be derived as follows:

$$I_{rx.\text{reactive}} = \frac{\sqrt{2}V_{\text{bus}}}{\pi\omega_s L_r} \sqrt{\begin{array}{l} \frac{\left(1+2\cos\left(\sqrt{3}r_m\pi/2\right)\right)^2 M_{pp}^2}{L_r^2} \\ +\left(1-\frac{L_p-M_{pp}}{L_r}+\frac{1}{\omega_s^2 L_r C_p}\right)^2 \cdot \left(\begin{array}{l} 7.56r_m^3-6.68r_m^2 \\ +0.15r_m+1.0 \end{array}\right) \\ -\left[\begin{array}{l} 2\left(1-\frac{L_p-M_{pp}}{L_r}+\frac{1}{\omega_s^2 L_r C_p}\right) \\ \times \frac{\left(1+2\cos\left(\sqrt{3}r_m\pi/2\right)\right)M_{pp}}{L_r} \\ \times \left(\begin{array}{l} 1.38r_m^3-2.89r_m^2 \\ +0.05r_m+1.0 \end{array}\right) \end{array}\right] \end{array}}. \tag{27}$$

The design criterion is selecting the optimal $C_p$ that can minimize $I_{rx.\text{reactive}}$, and the optimal $C_p$ is calculated as follows:

$$C_p = \frac{1}{\omega_s^2 L_r} \cdot \frac{1}{\left[\begin{array}{l} \frac{\left(1+2\cos\left(\sqrt{3}r_m\pi/2\right)\right)M_{pp}}{L_r} \cdot \frac{\left(\begin{array}{l} 1.38r_m^3-2.89r_m^2 \\ +0.05r_m+1.0 \end{array}\right)}{\left(\begin{array}{l} 7.56r_m^3-6.68r_m^2 \\ +0.15r_m+1.0 \end{array}\right)} \\ +\frac{L_p-M_{pp}}{L_r}-1 \end{array}\right]} \tag{28}$$

where $r_m$ is defined and limited as (24) and (25).

### F. Control Method

The proposed converter is designed with constant output voltage. Fig. 7 shows the proposed control method, which is based on the control scheme of the traditional three-phase PFC SPWM rectifier. In the proposed control method, there are one voltage control loop and one current control loop. PI$_v$ is the proportional–integral (PI) compensation module for the outer voltage loop to regulate $V_o$. PR$_c$ is the proportional–resonant (PR) compensation module for the inner current loop to control the three-phase input current and achieve PFC. $V_{o.\text{ref}}$ is defined as the reference values of $V_o$. $v_{g1}$–$v_{g6}$ are the gate driving signals of switches $Q_1$–$Q_6$.

For the constant output voltage realization, there are two cases to be discussed. Case 1 refers to the condition of fixed and known mutual inductance between the transmitter and receiver coils. From (21), (24), and Fig. 6, ideally, $V_o$ is independent of load conditions and can be estimated only with primary-side information. Hence, in this case, primary-side control without secondary-side output voltage information feedback can be achieved; hence, no wireless communication link is necessary. Case 2 refers to the condition of unfixed and unknown mutual inductance between the transmitter and receiver coils. In this case, since $V_o$ cannot be estimated only with the primary-side information, a wireless communication link is required to transfer secondary-side $V_o$ information to the primary-side controller.

### G. Power Loss Analysis

The system power loss mainly consists of input inductors ($L_{\text{in}.a}$, $L_{\text{in}.b}$, and $L_{\text{in}.c}$), switches ($Q_1$–$Q_6$), primary-side compensation inductors ($L_{ra}$, $L_{rb}$, and $L_{rc}$), primary-side coils ($L_{pa}$, $L_{pb}$, and $L_{pc}$), secondary-side coil ($L_s$), and secondary-side diodes ($D_{s1}$–$D_{s4}$), which are analyzed and calculated in detail as follows. The ac line angle $\theta$ ($= \omega_l t$) is introduced for clearer illustration.

1) *Input inductors ($L_{\text{in}.a}$, $L_{\text{in}.b}$, and $L_{\text{in}.c}$):* The total copper loss is given by the following equation:

$$P_{L\text{in}.cu} = 3 \cdot I_{s.\text{rms}}^2 \cdot R_{L\text{in}} \tag{29}$$

where $I_{s.\text{rms}}$ is defined as the RMS value of ac input currents $i_{s.a}$, $i_{s.b}$, and $i_{s.c}$. $R_{L\text{in}}$ is the equivalent series resistance (ESR) of the input inductors. The total core loss is omitted because the input current ripple is designed small enough to fulfill the PFC requirement.

2) *Switches ($Q_1$–$Q_6$):* The total conduction loss is given by the following equation:

$$P_{Q.\text{con}} = 3 \cdot R_{\text{ds.on}} \cdot \frac{1}{2\pi T_s} \int_0^{2\pi} \left[ \int_0^{T_s} \left( i_{ra}(\theta, t) - i_{s.a}(\theta) \right)^2 dt \right] d\theta \tag{30}$$

where $R_{\text{ds.on}}$ is the turn-ON drain–source (DS) resistance. $i_{s.a}$ is obtained from (14). $i_{ra}$ contains fundamental and nonignorable higher order harmonics, calculated as follows:

$$i_{ra}(\theta, t) = \frac{2V_{\text{bus}}}{\pi} \frac{\sin(D_A \pi)}{|Z_{A.fs.1}|} \cos\left(\omega_s t - \angle Z_{A.fs.1}\right) + \sum_{n=2}^{\infty} \frac{2V_{\text{bus}}}{n\pi} \frac{\sin(nD_A \pi)}{|Z_{A.fs.n}|} \cos\left(n\omega_s t - \angle Z_{A.fs.n}\right) \tag{31}$$

where $Z_{A.fs.1}$ can be calculated from (9), (17), and (20), and is expressed as follows:

$$Z_{A.fs.1}(\theta) = \frac{L_r}{\left\{ \begin{array}{l} \left( \frac{M_{ps}^2}{L_r R_e} - \frac{M_{pp}}{j\omega_s L_r} \right) \cdot \frac{\sin(D_B(\theta)\pi) + \sin(D_C(\theta)\pi)}{\sin(D_A(\theta)\cdot\pi)} \\ + \frac{1}{j\omega_s} \left[ 1 - \left( \frac{L_p}{L_r} - \frac{1}{\omega_s^2 L_r C_p} \right) \right] + \frac{M_{ps}^2}{L_r R_e} \end{array} \right\}}. \tag{32}$$

And $Z_{A.fs.n}$ ($n = 2, 3, 4, 5, \ldots$) can be calculated as follows:

$$Z_{A.fs.n} = j \cdot \left( n\omega_s L_r - \frac{1}{n\omega_s C_r} \right), \quad n = 2, 3, 4, 5, \ldots . \tag{33}$$

$D_A$, $D_B$, and $D_C$ are obtained from (23).

The proposed integrated topology cannot guarantee soft-switching operations for full load range since the ac input currents ($i_{s.a}$, $i_{s.b}$, and $i_{s.c}$) are working in continuous current mode with a small ripple. The total switching loss is given by the following equation:

$$P_{Q.\text{sw}} = 3 \cdot \frac{1}{2\pi T_s} \left( \frac{E_{\text{on.test}} + E_{\text{off.test}}}{V_{\text{ds.test}} I_{d.\text{test}}} \right) \int_0^{2\pi} V_{\text{bus}} \left( i_{\text{sw2}} + i_{\text{sw6}} \right) d\theta \tag{34}$$

where $E_{\text{on.test}}$ and $E_{\text{off.test}}$ are the reference switching-ON and switching-OFF energies under the testing DS voltage and current ($V_{\text{ds.test}}$ and $I_{d.\text{test}}$) condition, which can be obtained from the datasheet. $i_{\text{sw2}}$ and $i_{\text{sw6}}$ are the critical switching currents at $t_2$ and $t_6$, respectively, calculated as follows:

$$i_{\text{sw2}} = \begin{cases} 0 & i_{ra}(\theta, t_2) - i_{s.a}(\theta) \geq I_{\text{zvs. min}} \\ \left| i_{ra}(\theta, t_2) - i_{s.a}(\theta) \right| & i_{ra}(\theta, t_2) - i_{s.a}(\theta) < I_{\text{zvs.min}} \end{cases}$$
$$i_{\text{sw6}} = \begin{cases} 0 & i_{ra}(\theta, t_6) - i_{s.a}(\theta) \leq -I_{\text{zvs.min}} \\ \left| i_{ra}(\theta, t_6) - i_{s.a}(\theta) \right| & i_{ra}(\theta, t_6) - i_{s.a}(\theta) > -I_{\text{zvs.min}} \end{cases} \tag{35}$$

where $i_{s.a}$ and $i_{ra}$ are calculated from (14) and (31), respectively. $I_{\text{zvs.min}}$ is the minimum current to achieve zero voltage switching (ZVS) operation, determined by the switch's parasitic DS capacitance and the switching deadtime. $t_2$ and $t_6$ are defined in Fig. 5, calculated as follows:

$$t_2 = 0.5 D_A(\theta) T_s, \quad t_6 = \left[ 1 - 0.5 D_A(\theta) \right] T_s \tag{36}$$

where $D_A$ is obtained from (23).

3) *Primary-side compensation inductors ($L_{ra}$, $L_{rb}$, and $L_{rc}$):* The total copper loss is calculated as follows:

$$P_{Lr.cu} = 3 \cdot R_{Lr} \cdot \frac{1}{2\pi T_s} \int_0^{2\pi} \left[ \int_0^{T_s} \left( i_{ra}(\theta, t) \right)^2 dt \right] d\theta. \tag{37}$$

$R_{Lr}$ is the ESR of $L_{ra}$, $L_{rb}$, and $L_{rc}$, which should be measured under the condition of removing the magnetic core. Hence, $R_{Lr}$ only includes the winding copper loss factor. $i_{ra}$ can be obtained by (31). The total core loss can be derived from Steinmetz equation [45], [46]

$$P_{Lr.\text{core}} = \frac{3 \cdot V_e \cdot \lambda \cdot f_s^{\alpha}}{2\pi} \cdot \int_0^{2\pi} \left( \frac{\mu_0 N}{l_g} \cdot \frac{2V_{\text{bus}}}{\pi} \frac{\sin\left(D_A(\theta) \cdot \pi\right)}{Z_{A.fs.1}(\theta)} \right)^{\beta} d\theta \tag{38}$$

where $D_A$ and $Z_{A.fs.1}$ can be calculated from (23) and (32), respectively. $V_e$ is the volume of the magnetic core. $N$ is the number of turns. $l_g$ is the air gap distance. The constants $\lambda$, $\alpha$, and $\beta$ can be found from the datasheet.

4) *Primary-side coils ($L_{pa}$, $L_{pb}$, and $L_{pc}$):* The total loss can be calculated as follows:

$$P_{Lp} = 3 \cdot R_{Lp} \cdot \frac{1}{2\pi} \cdot \int_0^{2\pi} \left( \frac{\sqrt{2} V_{\text{bus}}}{\pi} \frac{\sin\left(D_A(\theta) \cdot \pi\right)}{\omega_s L_r} \right)^2 d\theta. \tag{39}$$

$R_{Lp}$ is the ESR of $L_{pa}$, $L_{pb}$, and $L_{pc}$, which should be measured under the condition with the ferrite shielding plates placed. Hence, $R_{Lp}$ includes both copper loss factor of the coils and the core loss factor of the ferrite shielding plates. $D_A$ can be calculated from (23).

5) *Secondary-side coil ($L_s$):* The loss of $L_s$ is given by the following equation:

$$P_{Ls} = R_{Ls} \cdot \left( \frac{\pi P_o}{2\sqrt{2} V_o} \right)^2. \tag{40}$$

$R_{Ls}$ is the ESR of $L_s$, which should also be measured under the condition with the ferrite shielding plates placed. Hence, $R_{Ls}$ includes both copper loss factor of the coils and the core loss factor of the ferrite shielding plates.

6) *Secondary-side diodes ($D_{s1}$–$D_{s4}$):* The total loss is resulting from the diode forward voltage drop, given by the following equation:

$$P_{Ds} = 2 \cdot (P_o / V_o) \cdot V_{Ds} \tag{41}$$

where $V_{Ds}$ is the forward voltage drop of the diodes.

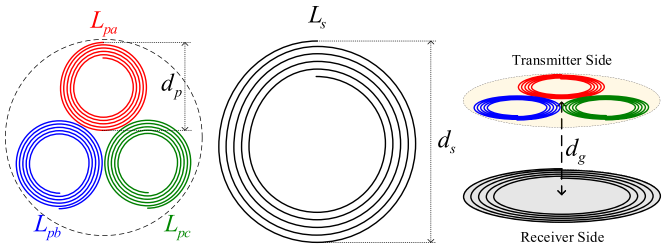


Fig. 8. Schematic diagram of the WPT coils.

## III. Design Procedure and Considerations

### A. Design Procedure

To verify the design and control of the proposed topology, a 1600-W scaled-down laboratory prototype with constant $V_o$ is designed and implemented. The design procedures are given as follows.

*1) Requirements of Input and Output:* Phase voltage of the three-phase voltage source is designed to be 110 $V_{\rm rms}$, 50 Hz at rated condition. The allowable voltage fluctuation range is 10%. Maximum output power $P_{o.\max}$ is 1600 W, with constant output voltage $V_o$ to be 200 V, and hence, maximum output current $I_{o.\max}$ is 8 A.

*2) Design of Bus Voltage and WPT Resonant Tank:* From (24) and (25), the minimum $V_{\rm bus}$ (noted as $V_{\rm bus.min}$) is limited as follows:

$$V_{\rm bus.\,min} \geq 2V_{sp.\max} = 342.2\,{\rm V}. \tag{42}$$

Here, to transfer a sufficient switching-frequency fundamental component to the WPT resonant tank, $V_{\rm bus.min}$ is designed as 380 V. Considering the voltage stress of the switches and bus capacitor, the maximum allowable $V_{\rm bus}$ (noted as $V_{\rm bus.max}$) is limited as 500 V.

For the proposed topology, to simplify the control and evenly distribute the power switches' electrical stresses, the three transmitter coils are required to be designed identically in shape and number of turns so that their self-inductances are the same, as shown in Fig. 8. Moreover, three transmitter coils' center points are required to be positioned with a 120° angular interval in the same horizontal plane. The transmitter coils' horizontal plane's center point is required to be aligned to the receiver coil's center point, as shown in Fig. 8. With such design regulations, the mutual inductances between the transmitter coils and the receiver coil ($M_{as}$, $M_{bs}$, and $M_{cs}$) are guaranteed the same. In addition, the transmitter and receiver coils should be deigned in circle shape. It is suggested to add magnetic shielding plates (ferrite plates) above and below the magnetic coupler coils to concentrate the coupler inner magnetic field and shield the outward magnetic field. The magnetic shielding plates are required to be designed in circle shape and aligned with the magnetic coupler coils. Fig. 9 shows the design of the magnetic shielding plates of WPT coils. There are two identical designed shielding plates placed to cover the transmitter coils and the receiver coil, respectively. The detailed design, structure, and dimension of the magnetic shielding plates are presented in Fig. 9(c). Each

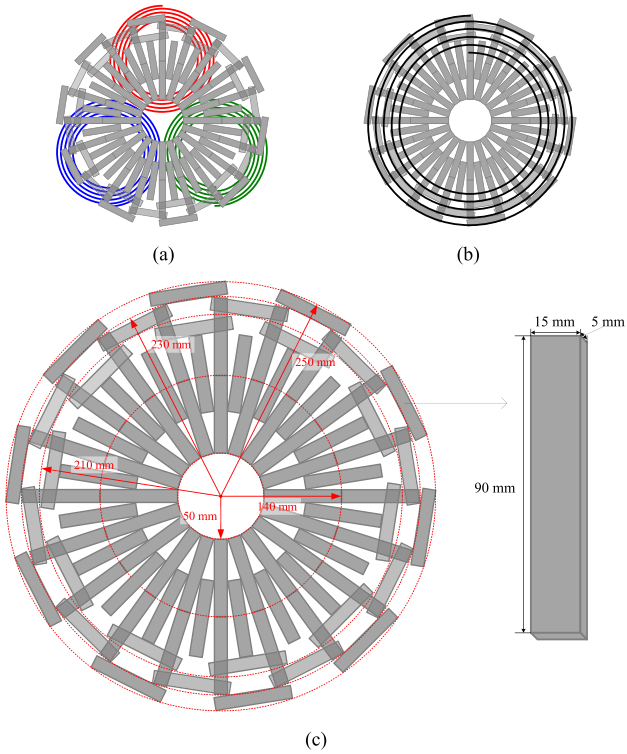


Fig. 9. Design of magnetic shielding plates of WPT coils. (a) Magnetic shielding plate covering the transmitter coils. (b) Magnetic shielding plate covering the receiver coil. (c) Design, structure, and dimension of the magnetic shielding plate.

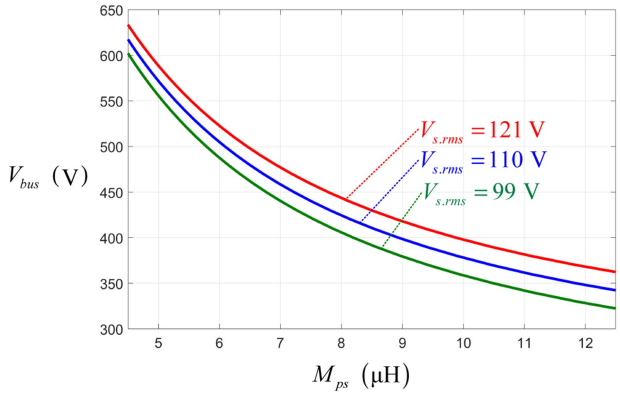


Fig. 10. Relations of $M_{ps}$ and $V_{\rm bus}$ for different ac input phase voltage conditions.

plate consists of 90 discrete ferrite bars. Each ferrite bar is made of PC95 Mn–Zn ferrite material with the dimension of 90 mm height, 15 mm width, and 5 mm thickness. The magnetic ferrite plates are designed in circle shape with 50 mm inner radius and 250 mm outer radius. There are 60 ferrite bars evenly distributed in radial direction outer the circle with 50 mm radius. There are 30 ferrite bars evenly distributed in tangential direction close to the circles with 210, 230, and 250 mm radius. The magnetic shielding plate design is proposed by balancing the shielding performance and weight/volume.

Considering the characteristics of the proposed topology, wireless charging for automated guided vehicle (AGV) would be

a potential application. The three transmitter coils can be placed underground, and the single receiver coil is placed at the bottom plain (chassis) of the AGV. Since the AGV can be navigated and positioned accurately, the horizontal alignment requirement can be realized. In addition, since vertical distance variance range is allowable for the proposed topology, wireless charging for AGVs with different chassis heights can be achieved.

In this laboratory prototype design, according to the chassis height requirement of some specific AGVs, the minimum vertical distance $d_{g.\min}$ is designed as 70 mm [47]. Then, according to the common designed coupling coefficient (between the transmitter coil and receiver coil) range, the coupling coefficient between the transmitter coil and receiver coil is initially designed within the range from 0.1 to 0.15. There is no other specific limitation on the sizes of the coils. Hence, the outer diameter ($d_p$) and number of turns ($n_p$) of the transmitter coils are designed as 250 mm and 10, respectively. The outer diameter ($d_s$) and number of turns ($n_s$) of the receiver coil are designed as 480 mm and 9, respectively. To reduce ac resistance of resonant coils, the litz wire with 1000 strands (each strand's diameter is 0.1 mm) and 7.85 mm$^2$ cross-sectional area is used. Finally, the measured values of transmitter coil's self-inductance, receiver coil's self-inductance, mutual inductance between transmitter coils, and the maximum mutual inductance between transmitter and receiver coils are 37.5 $\mu$H, 96.2 $\mu$H, 2.2 $\mu$H, and 9.0 $\mu$H, respectively. The coupling coefficient between the transmitter coils is denoted by $k_{pp}$. The coupling coefficient between the transmitter coil and receiver coil is denoted by $k_{ps}$. In the prototype, the maximum $k_{ps}$ (denoted by $k_{ps.\max}$) is 0.15, when the transmitter coil and receiver coil are within the minimum vertical distance $d_{g.\min}$ (70 mm), which fulfil the initial requirements.

From (21)–(24), it can be analyzed that the primary-side compensation inductance $L_r$ is determined by $M_{ps.\max}$, $V_o$, $V_{\text{bus.min}}$, and $V_{sp.\min}$

$$L_r = \frac{M_{ps.\max} \cdot h_{ABC}\big|_{r_m=\frac{V_{sp.\min}}{V_{\text{bus.min}}}} \cdot V_{\text{bus.min}}}{2V_o} \tag{43}$$

where $V_{sp.\min}$ is defined as the minimum peak value of the input phase voltage. From (43), $L_r$ is calculated as 17.7 $\mu$H. When $L_r$ is confirmed, with the predetermined $V_{sp.\max}$ and $V_{\text{bus.max}}$, the minimum allowable $M_{ps}$ ($M_{ps.\min}$) is calculated as follows:

$$M_{ps.\min} = \frac{2V_oL_r}{h_{ABC}\big|_{r_m=\frac{V_{sp.\max}}{V_{\text{bus.max}}}} \cdot V_{\text{bus.max}}} \tag{44}$$

where $V_{sp.\max}$ is defined as the maximum peak value of the input phase voltage. Hence, from (44), $M_{ps.\min}$ is designed as 6.5 $\mu$H and the corresponding maximum allowable vertical distance $d_{g.\max}$ is 105 mm.

The magnetic core of the compensation inductors is TDK E 55/28/21 (B66335 series) with N87 ferrite material. Practically, $L_r$ is measured as 17.1 $\mu$H. From (6), (7), and (20), with known $L_r$ and $L_s$ values, $C_r$ and $C_s$ can be obtained as 205.0 and 36.3 nF, respectively. From (27) and (28), $C_p$ is designed to make minimize $I_{rx.\text{reactive}}$ so that the conduction losses on $L_{ra}$, $L_{rb}$, $L_{rc}$, and switches $Q_1$–$Q_6$ can be reduced. By calculation, $C_p$ is designed as 146.0 nF.

From (21)–(26), with confirmed $L_r$ and $V_o$, for $M_{ps.\max}$ condition, when input phase voltage is at minimum value (99 $V_{\text{rms}}$), the bus voltage is 380 V; when input phase voltage is at nominal value (110 $V_{\text{rms}}$), the bus voltage is 399 V; when input phase voltage is at maximum value (121 $V_{\text{rms}}$), the bus voltage is 418 V. For $M_{ps.\min}$ condition, when input phase voltage is at minimum value (99 $V_{\text{rms}}$), the bus voltage is 462 V; when input phase voltage is at nominal value (110 $V_{\text{rms}}$), the bus voltage is 480 V; when input phase voltage is at maximum value (121 $V_{\text{rms}}$), the bus voltage is 500 V.

*3) Bus Capacitor $C_{bus}$ and Output Capacitor* $C_o$ *Selection:* To reduce the bus voltage ripple, $C_{\text{bus}}$ is selected to be with 500 $\mu$F capacitance and 500 V voltage rating. $C_o$ is selected to be with 220 $\mu$F capacitance and 450 V voltage rating to filter the switching-frequency ripple.

*4) Design of Input Inductors (*$L_{in.a}$, $L_{in.b}$, *and* $L_{in.c}$*):* From the article presented in [48] and [49], the input inductors' value should fulfill the maximum and minimum limitation as follows:

$$\frac{V_{s.\text{rms}}}{2\sqrt{6}f_sI_{\text{rpl. max}}} \le L_{\text{in}} \le \frac{\sqrt{V_{\text{bus}}^2/8 - V_{s.\text{rms}}^2}}{\omega_l I_{s.\text{rms}}} \tag{45}$$

where $V_{s.\text{rms}}$ and $I_{s.\text{rms}}$ are defined as the RMS values of the input ac phase voltages and phase currents. $I_{\text{rpl.max}}$ is defined as the maximum ripple current of input ac phase currents. Hence, the input inductors are designed with 5.0 mH inductance identically. The magnetic core of the input inductors is made of Si–Fe material and in toroid shape with 25.6 mm inner diameter, 58 mm outer diameter, and 48.3 mm height.

### *B. Considerations on Vertical Distance Variation of the WPT Coils*

For vertical distance (between the transmitter plain and receiver coil) variation condition, $M_{as}$, $M_{bs}$, and $M_{cs}$ are still kept the same with each other ($M_{as} = M_{bs} = M_{cs} = M_{ps}$). Therefore, the vertical distance is allowed to vary in a range, meaning that $M_{ps}$ is allowed to vary in a proper range.

When $M_{ps}$ varies, the three-phase ac input PFC and input current total harmonic distortion (THD) are not affected and still maintain high performance since the three-phase ac currents are independently controlled by the inner current loop, as shown in Fig. 7. In other words, the shaping and control of the three-phase ac currents are independent from the WPT coils and their misalignment since the SPWM voltage outputs of the three-phase six-switch bridge structure are still 120° angular symmetric, which is determined by the inner current loop and SPWM control. When $M_{ps}$ varies, the output voltage $V_o$ can also maintain constantly equal to the output voltage reference $V_{o.\text{ref}}$ because of the outer voltage control loop, as shown in Fig. 7. In the outer voltage control loop, the difference of $V_o$ and $V_{o.\text{ref}}$ is fed to the corresponding PI compensation block to generate an active input current control command $I_{d.\text{ref}}$ and furtherly regulate the ac input power.

However, when $M_{ps}$ varies and $V_o$ is maintained constant by the outer voltage control loop, the bus voltage $V_{\text{bus}}$ would change to fulfil the voltage transfer gain from $V_{\text{bus}}$ to $V_o$. From (21), (24), and (26), when $V_{s.\text{rms}}$ and $V_o$ are fixed, the relation

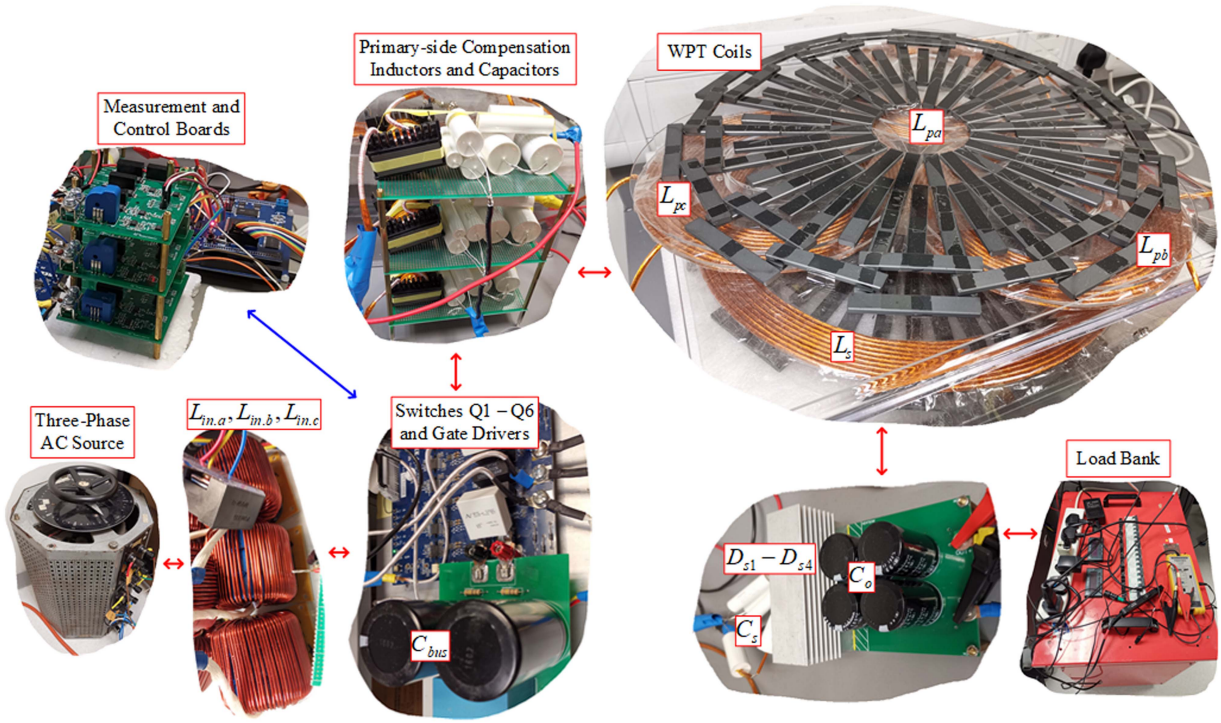


Fig. 11. Setup of the laboratory prototype.

between $M_{ps}$ and $V_{\text{bus}}$ can be obtained as follows:

$$\frac{V_o}{V_{\text{bus}}} = \frac{M_{ps}}{2L_r} \cdot \left[1 + 2\cos\left(\frac{\sqrt{3}}{2} \cdot \frac{\sqrt{2}V_{s.\text{rms}}}{V_{\text{bus}}} \cdot \pi\right)\right]. \quad (46)$$

With the confirmed $V_o$ and $L_r$ of the laboratory prototype, the relation curves between $V_{\text{bus}}$ and $M_{ps}$ for different ac input phase voltage ($V_{s.\text{rms}}$) conditions are obtained, as shown in Fig. 10. In the laboratory prototype, because of this characteristic, when $V_{\text{bus}}$ is limited from 380 to 500 V, $M_{ps}$ is limited ranging from 6.5 to 9.0 $\mu$H.

### C. Considerations on Horizontal Misalignment of the WPT Coils

The horizontal misalignment is not suggested because it would cause two negative impacts on system operation because of different $M_{as}$, $M_{bs}$, and $M_{cs}$. The first negative impact is the severe output double-line-frequency ripple. The second negative impact is the unbalanced current stresses of the switches.

However, for practical implementation and operation, a small range of horizontal misalignment may be inevitable. For this practical condition, if a lager output capacitor is applied to absorb the additional double-line-frequency ripple, and switches with a larger current rating are used to stand the unbalanced and possibly additional current stresses, then the two mentioned negative impacts can be alleviated and would not affect the converter's normal operation when the horizontal misalignment occurs.

The general procedure to solve the problem of misalignment is summarized as follows:

1) measure the values of $M_{as}$, $M_{bs}$, and $M_{cs}$ for all critical misalignment conditions;
2) calculate and select the maximum double-line-frequency ripple (with (47) in the Appendix) over all the critical misalignment conditions;
3) calculate the required additional output capacitance (with (48) in the Appendix) according to the maximum ripple and acceptable ripple;
4) calculate and select the maximum switch current stress (with (49)–(51) in the Appendix) over all the critical misalignment conditions;
5) select the switches with the current rating larger than the maximum current stress.

### D. Design Summary and Laboratory Prototype

Setup of the laboratory prototype is shown in Fig. 11 and Table I gives the detailed design parameters of the laboratory prototype. Wolfspeed SiC power module CCS050M12CM2 is used as the power switches $Q_1$–$Q_6$ to reduce switching and conduction losses. Wolfspeed C4D40120D is used as the secondary-side full-bridge rectifier diodes $D_{s1}$–$D_{s4}$. The coupling coefficient ($k_{pp}$) between the transmitter coils is 0.06. The coupling coefficient ($k_{ps}$) between the transmitter coils and the receiver coil ranges from 0.11 to 0.15.

## IV. Experimental Results

According to the proposed design procedure, the laboratory prototype is implemented with rated 1600 W output power. In the experiments, due to the limitation of load bank, operations

TABLE I
DESIGN SUMMARY OF THE LABORATORY PROTOTYPE

| Parameter | Values | Parameter | Values |
|---|---|---|---|
| $P_{o.max}$ | 1600 W | $k_{pp}$ | 0.06 |
| $V_o$ | 200 V | $M_{ps}$ | 6.5–9.0 μH |
| $v_s$ | 99–121 $V_{rms}$, 50 Hz | $k_{ps}$ | 0.11–0.15 |
| $V_{bus}$ | 380–500 V | $L_s$, $C_s$ | 96.2 μH, 36.3 nF |
| $f_s$ | 85 kHz | $R_{Ls}$ | 135 mΩ |
| $L_{in}$ | 5.0 mH | $C_{bus}$ | 500 μF, 500 V |
| $R_{Lin}$ | 200 mΩ | $C_o$ | 220 μF, 450 V |
| $L_r$, $C_r$ | 17.1 μH, 205.0 nF | $D_{s1}$–$D_{s4}$ | Wolfspeed C4D40120D |
| $R_{Lr}$ | 45 mΩ | | |
| $L_p$, $C_p$ | 37.5 μH, 146.0 nF | $Q_1$–$Q_6$ | Wolfspeed CCS050M12CM2 |
| $R_{Lp}$ | 65 mΩ | | |
| $M_{pp}$ | 2.2 μH | Control Unit | TI DSP F28335 |

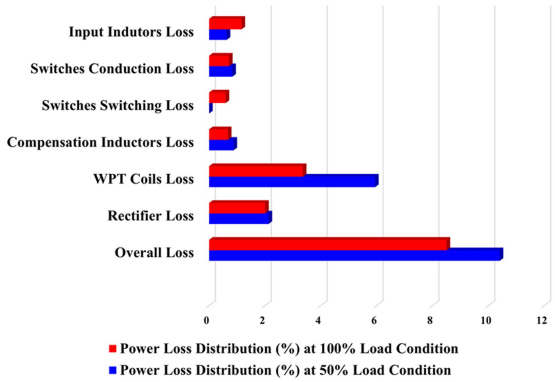


Fig. 13. Power loss distribution (proportion to input power) for maximum $M_{ps}$ condition at 100% and 50% load conditions.

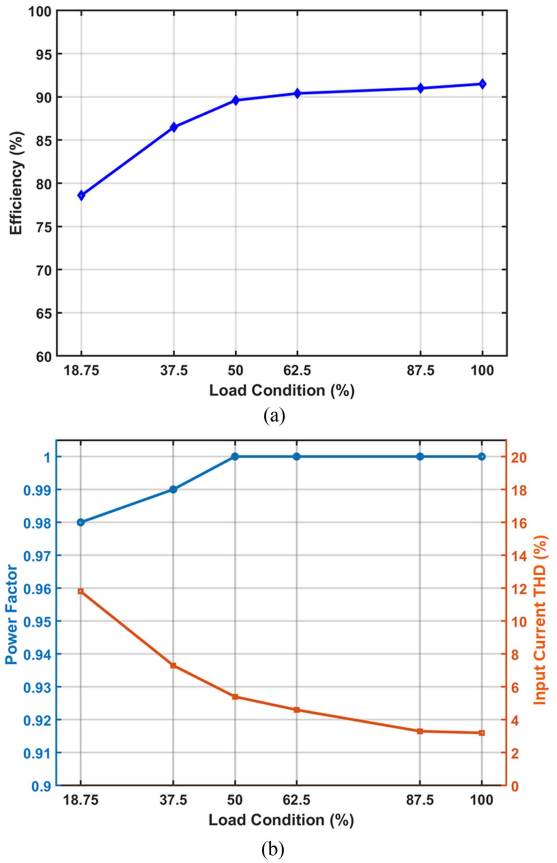


Fig. 12. Performances for maximum $M_{ps}$ condition at different load conditions. (a) Efficiency. (b) PF and input current THD.

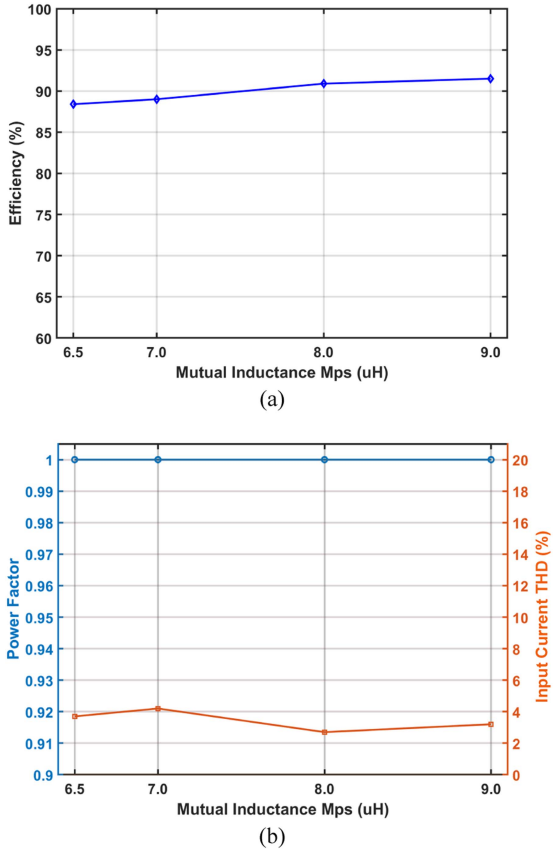


Fig. 14. Performances for different $M_{ps}$ conditions at 100% load condition. (a) Efficiency. (b) PF and input current THD.

at 18.75%, 37.5%, 50%, 62.5%, 87.5%, and 100% load conditions (300–1600 W) are tested to verify the functionalities and advantages of the proposed topology.

Fig. 12(a) shows the overall efficiency for maximum $M_{ps}$ condition at different load conditions and Fig. 12(b) shows the PF and input current THD for maximum $M_{ps}$ condition at different load conditions. At 100% load condition, the efficiency, PF, and input current THD achieve 91.5%, 1.0, and 3.2%, respectively. Fig. 13 presents the power loss distribution for maximum $M_{ps}$ condition at 100% and 50% load conditions. It can be observed that the total losses of the switches $Q_1$–$Q_6$ are not dominant. Fig. 14 shows the efficiency, PF, and input current THD for different $M_{ps}$ conditions at 100% load condition. Fig. 15 shows the three-phase input current for maximum $M_{ps}$ condition at 100% and 50% load conditions. Figs. 16 and 17 present the primary-side key operation waveforms for different ac line angles $\theta$ $(= \omega_l t)$ for maximum $M_{ps}$ condition at 100% and 50% load conditions, respectively. Fig. 18 shows the secondary-side

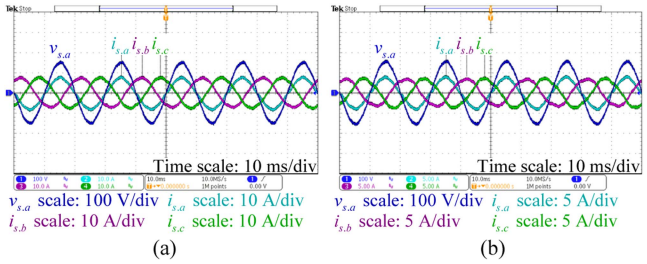


Fig. 15. Three-phase input currents for maximum $M_{ps}$ condition at different load conditions. (a) 100% load. (b) 50% load.

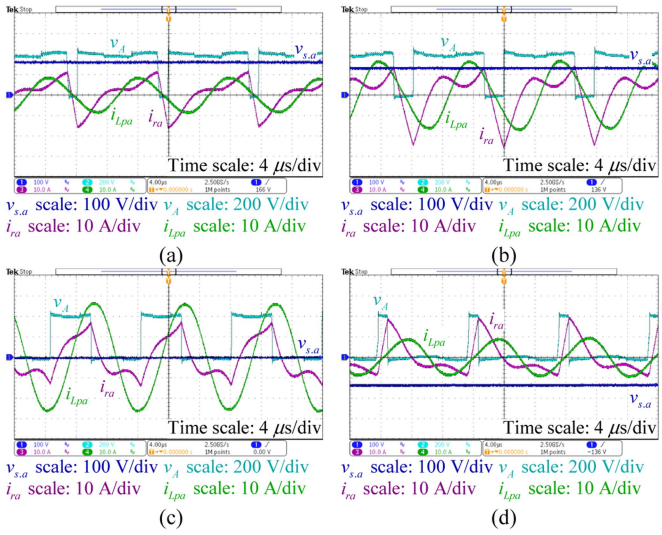


Fig. 16. Primary-side waveforms ($v_{s.a}$, $v_A$, $i_{ra}$, and $i_{Lpa}$) for maximum $M_{ps}$ condition at 100% load condition. (a) $\omega_l t = \pi/2$. (b) $\omega_l t = \pi/3$. (c) $\omega_l t = 0$. (d) $\omega_l t = -\pi/3$.

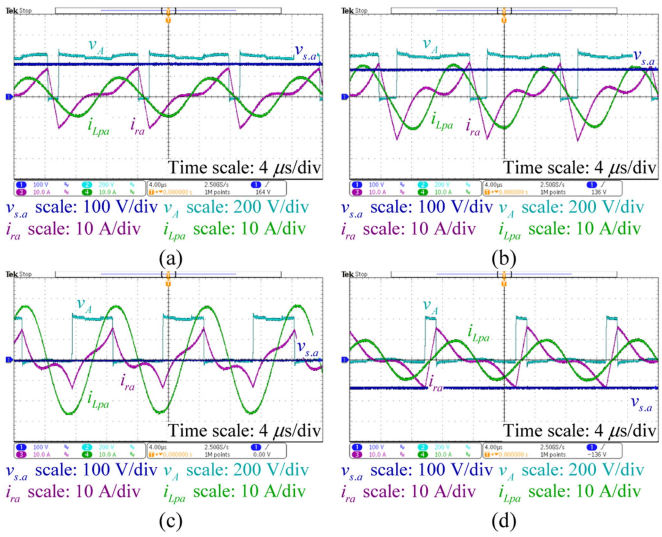


Fig. 17. Primary-side waveforms ($v_{s.a}$, $v_A$, $i_{ra}$, and $i_{Lpa}$) for maximum $M_{ps}$ condition at 50% load condition. (a) $\omega_l t = \pi/2$. (b) $\omega_l t = \pi/3$. (c) $\omega_l t = 0$. (d) $\omega_l t = -\pi/3$.

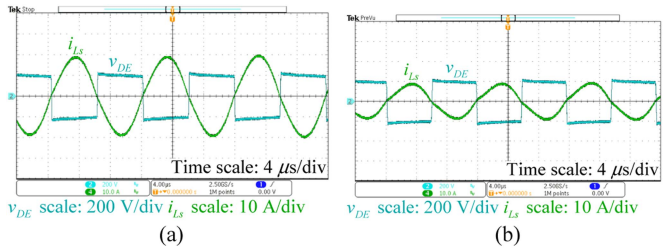


Fig. 18. Secondary-side waveforms of $v_{DE}$ and $i_{Ls}$ for maximum $M_{ps}$ condition at different load conditions. (a) 100% load. (b) 50% load.

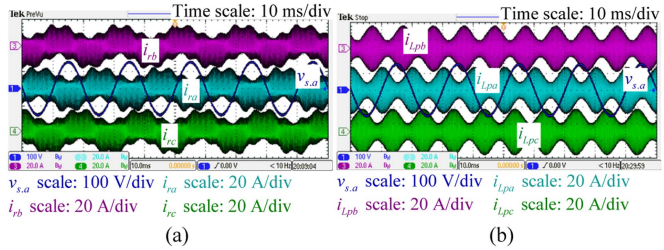


Fig. 19. AC line-frequency profile waveforms for 100% load and maximum $M_{ps}$ condition. (a) $i_{ra}$, $i_{rb}$, and $i_{rc}$. (b) $i_{Lpa}$, $i_{Lpb}$, and $i_{Lpc}$.

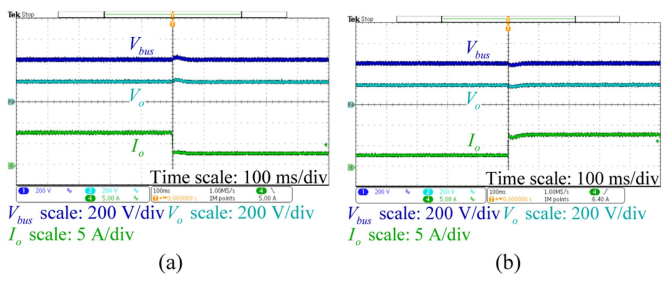


Fig. 20. Load step responses for maximum $M_{ps}$ condition ($V_{\rm bus}$, $V_o$, and $I_o$). (a) 100% to 37.5% load. (b) 37.5% to 100% load.

operation waveforms for maximum $M_{ps}$ condition at 100% and 50% load conditions The ac line-frequency profile waveforms of the primary-side compensation inductors' and coils' currents for 100% load and maximum $M_{ps}$ condition are presented in Fig. 19. The step responses of load changing from 100% to 37.5% and reverse are presented in Fig. 20.

Table II compares the proposed topology with other state-of-the-art single-stage three-phase ac–dc WPT topologies. The efficiency and input power quality are better than others. Compared with the matrix topologies [26], [27], [28], the primary-side power semiconductor device amount of the proposed topology is significantly reduced. Although only four switches are used in the primary side of the T-type-based topology [29], six more diodes are still required. Moreover, its input current is not actively shaped, and its DCM input current will cause higher losses of input inductors and active switches, and EMI problems. The experiments of the traditional two-stage topology, as shown in Fig. 1, are also implemented for comparison. The peak efficiency of the traditional two-stage topology is lower than that of the proposed topology. In addition, the traditional two-stage

TABLE II
COMPARISONS OF THREE-PHASE AC–DC WPT SYSTEM TOPOLOGIES

| Topologies | Peak efficiency (%) | PF | Input current THD (%) | Primary-side power semiconductor device count |
|---|---|---|---|---|
| Proposed topology | 91.5 | 1.0 | 3.2 | 6 switches |
| Matrix topology I [26] | 85 | <0.95 | >20.0 | 8 switches |
| Matrix topology II [27] | 75.1 | 0.95 | N/A | 12 switches |
| Matrix topology III [28] | 89.4 | 0.67 | 110.8 | 6 diodes + 7 switches |
| T-type-based topology [29] | 89.2 | 1.0 | 3.5 | 6 diodes + 4 switches |
| Two-stage topology (Fig. 1) | 89.1 | 1.0 | 3.0 | 10 switches |
| Two-stage topology [50] | <85 | <0.98 | >5.0 | 7 diodes + 5 switches |
| Two-stage topology [51] | 91.0 | not reported | not reported | 12 switches |

topology requires four more active power switches. Compared with other two existing traditional two-stage topologies [50], [51], the proposed integrated topology also exhibits significant advantages in terms of the overall performance.

## V. CONCLUSION

A novel integrated three-phase ac–dc WPT converter with active PFC is proposed to reduce the power semiconductor device count and improve the system overall efficiency. It uses three transmitter coils to enhance the system primary-side power capacity. The topology description, theoretical analysis, control method, and power loss analysis are presented with details. Besides, the design procedure for a design example is given and the corresponding laboratory prototype is built to verify the performances and advantages of the proposed topology. Compared with the existing single-stage three-phase ac–dc WPT topologies, the proposed topology exhibits significant advantages when efficiency, ac input power quality, and power semiconductor device count are comprehensively considered.

## APPENDIX

When there occurs a horizontal misalignment condition, $M_{as}$, $M_{bs}$, and $M_{cs}$ may not be identical, and the output voltage can be calculated as follows:

$$v_o = \left[M_{as}\sin\left(D_A\pi\right) + M_{bs}\sin\left(D_B\pi\right) + M_{cs}\sin\left(D_C\pi\right)\right]\frac{V_{\text{bus}}}{2L_r} \tag{47}$$

where $D_A$, $D_B$, and $D_C$ can be calculated from (23). $\theta$ refers to the ac line angle, equal to $\omega_l t$. The curve of $v_o$ in relation to $\theta$ is thereby calculated, and the corresponding double-line-frequency ripple $\Delta V_{o.\text{org}}$ can be obtained. An additional dc output capacitor can be added to reduce the unwanted double-line-frequency ripple to an acceptable level. The additional output capacitance $C_{o.\text{add}}$ is calculated as follows:

$$C_{o.\text{add}} = \frac{P_o}{\omega_l V_{o.\text{avg}}^2}\sqrt{\frac{1-\left(1-\frac{\Delta V_{o.\text{org}}^2}{2V_{o.\text{avg}}^2}\right)^2}{1-\left(1-\frac{\Delta V_{o.\text{new}}^2}{2V_{o.\text{avg}}^2}\right)^2}-1} \tag{48}$$

where $\Delta V_{o.\text{new}}$ is the acceptable double-line-frequency ripple after adding $C_{o.\text{add}}$. $V_{o.\text{avg}}$ is the average dc output voltage.

For the horizontal misalignment condition, to prevent the switches from being broken by the overcurrent problem due to the unbalanced switch currents, the switch current rating should be designed and selected according to the maximum current stress. The RMS currents of $Q_1$ and $Q_2$ are denoted by $I_{Q.12.\text{rms}}$. The RMS currents of $Q_3$ and $Q_4$ are denoted by $I_{Q.34.\text{rms}}$. The RMS currents of $Q_5$ and $Q_6$ are denoted by $I_{Q.56.\text{rms}}$. They can be calculated as follows:

$$I_{Q.12.\text{rms}} = \sqrt{\frac{1}{2}\cdot\frac{1}{2\pi T_s}\int_0^{2\pi}\left[\int_0^{T_s}\left(i_{ra}\left(\theta,t\right)-i_{s.a}\left(\theta\right)\right)^2 dt\right]d\theta} \tag{49}$$

$$I_{Q.34.\text{rms}} = \sqrt{\frac{1}{2}\cdot\frac{1}{2\pi T_s}\int_0^{2\pi}\left[\int_0^{T_s}\left(i_{rb}\left(\theta,t\right)-i_{s.b}\left(\theta\right)\right)^2 dt\right]d\theta} \tag{50}$$

$$I_{Q.56.\text{rms}} = \sqrt{\frac{1}{2}\cdot\frac{1}{2\pi T_s}\int_0^{2\pi}\left[\int_0^{T_s}\left(i_{rc}\left(\theta,t\right)-i_{s.c}\left(\theta\right)\right)^2 dt\right]d\theta} \tag{51}$$

where $i_{s.a}$, $i_{s.b}$, and $i_{s.c}$ are obtained from (14). And $i_{ra}$, $i_{rb}$, and $i_{rc}$ are calculated as follows:

$$i_{ra}\left(\theta,t\right) = \frac{2V_{\text{bus}}}{\pi}\frac{\sin\left(D_A\pi\right)}{\left|Z_{A.fs.1}\right|}\cos\left(\omega_s t-\angle Z_{A.fs.1}\right) + \sum_{n=2}^{\infty}\frac{2V_{\text{bus}}}{n\pi}\frac{\sin\left(nD_A\pi\right)}{\left|Z_{A.fs.n}\right|}\cos\left(n\omega_s t-\angle Z_{A.fs.n}\right) \tag{52}$$

$$i_{rb}\left(\theta,t\right) = \frac{2V_{\text{bus}}}{\pi}\frac{\sin\left(D_B\pi\right)}{\left|Z_{B.fs.1}\right|}\cos\left(\omega_s t-\angle Z_{B.fs.1}\right) + \sum_{n=2}^{\infty}\frac{2V_{\text{bus}}}{n\pi}\frac{\sin\left(nD_B\pi\right)}{\left|Z_{B.fs.n}\right|}\cos\left(n\omega_s t-\angle Z_{B.fs.n}\right) \tag{53}$$

$$i_{rc}\left(\theta,t\right) = \frac{2V_{\text{bus}}}{\pi}\frac{\sin\left(D_C\pi\right)}{\left|Z_{C.fs.1}\right|}\cos\left(\omega_s t-\angle Z_{C.fs.1}\right) + \sum_{n=2}^{\infty}\frac{2V_{\text{bus}}}{n\pi}\frac{\sin\left(nD_C\pi\right)}{\left|Z_{C.fs.n}\right|}\cos\left(n\omega_s t-\angle Z_{C.fs.n}\right). \tag{54}$$

$Z_{A.fs.1}$, $Z_{B.fs.1}$, and $Z_{C.fs.1}$ can be calculated from (9)–(11). The compensation parameters and self-inductances of the transmitter coils, as well as their mutual inductances, are also designed identically as (20). $Z_{A.fs.n}$, $Z_{B.fs.n}$, and $Z_{C.fs.n}$ can be calculated as follows:

$$Z_{A.fs.n} = Z_{B.fs.n} = Z_{C.fs.n} = j \cdot \left( n\omega_s L_r - \frac{1}{n\omega_s C_r} \right), \quad n = 2, 3, 4, 5, \ldots . \tag{55}$$

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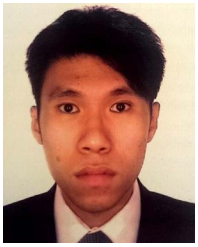
**Junwei Liu** (Member, IEEE) received the B.Eng. degree in water conservancy and hydropower engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2012, and the Ph.D. degree in power electronics from the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong, in 2018.

He is currently a Research Fellow with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong. His research interests include wireless power transfer, power factor correction, and ac–dc single-stage topologies.



**Chi Shing Wong** (Member, IEEE) received the B.Eng.(Hons.) degree in electronic and information engineering and the Ph.D. degree in power electronics from The Hong Kong Polytechnic University, Hong Kong, in 2013 and 2018, respectively.

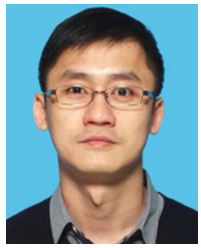
He was a Visiting Scholar with the School of Electrical, Electronic and Computer Engineering, University of Western Australia, from January 2017 to May 2017. From 2019 to 2020, he was a Postdoctoral Fellow with The State Key Laboratory of Internet of Things for Smart City, University of Macau, under the UM Macao Talent Program. He is currently with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong, under the Hong Kong RGC Postdoctoral Fellowship Scheme. He serves as a reviewer for various international journals and conferences. His research interests include solid-state transformer, inductive power transfer, vehicle-to-grid, LED driver circuit design, power-factor-correction regulators, and resonant power conversion.

**Zilin Li** (Member, IEEE) received the B.S. degree from China Agricultural University, Beijing, China, in 2011, the M.S. degree from the South China University of Technology, Guangzhou, China, in 2017, and the Ph.D. degree from The Hong Kong Polytechnic University, Hong Kong, in 2022, all in electrical engineering.

He is currently a Postdoctoral Fellow with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong. His research interests include power electronics, microgrids, and power electronic-based power systems.

**Xingyue Jiang** is currently working toward the Ph.D. degree in electronic and information engineering with The Hong Kong Polytechnic University, Hong Kong.

His current research interests include peer-to-peer energy trading, energy path planning, and energy Internet.



**K. H. Loo** (Member, IEEE) received the B.Eng. (Hons.) and Ph.D. degrees in electronic engineering from the University of Sheffield, Sheffield, U.K., in 1999 and 2002, respectively.

From 2002 to 2004, he was in the Japan Society for the promotion of Science Postdoctoral Fellow with Ehime University, Matsuyama, Japan. Since 2006, he has been with The Hong Kong Polytechnic University, Hong Kong, where he is currently an Associate Professor with the Department of Electronic and Information Engineering. His research interests include power electronics for renewable energy systems.

Dr. Loo has been an Associate Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION since 2013 and IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS since 2019, and a reviewer for various international journals and conferences. He is currently the Chair of the Power Electronics and Control Sub-Committee of the IEEE Technical Committee on Transportation Electrification.