Advanced Power Cycling Test Integrated With Voltage, Current, Temperature, and Humidity Stress

Yanhao Wang, Erping Deng, *Member, IEEE*, Lixin Wu, Haiyang Cao, Yuxing Yan, Pin Zeng, Yiming Zhang, Yushan Zhao, and Yongzhang Huang, *Member, IEEE*

***Abstract*—In this article, an advanced power cycling test (PCT) with high voltage, large current, high temperature, and high humidity stress is proposed to get closer to the actual working conditions of power electronics in the accelerated aging test. The proposed test, integrated with high-voltage high-humidity high-temperature reverse bias test and standard dc PCT, achieves precise measurement at the microsecond, millivolt, and microampere accuracy. A 6-kV/750-A prototype is built to verify the feasibility and effectiveness, and the noise mitigation method for measurement under high voltage is analyzed. The proposed test was carried out on the full-bridge power modules for electric vehicles, and the lifetime exhibits lower than the standard PCT. The root cause is the increment of thermal resistance at an early stage due to moisture invasion, which results in a failure mode change. Finally, the electrochemical corrosion signs induced by sulfur/carbon under voltage, temperature, and humidity stress are also revealed by optical inspection and scanning electron microscope.**

***Index Terms*—Actual working conditions, corrosion signs, failure mode change, high-voltage high-humidity high-temperature reverse bias test (HV-H3TRB), power cycling test (PCT), precise measurement.**

I. Introduction

POWER modules, such as insulated gate bipolar transistors (IGBTs) or silicon carbide metal–oxide–semiconductor field-effect transistors (SiC MOSFETs), are widely used in the power conversion system, e.g., electric vehicles, industrial motors, et cetera [1]. Standard reliability tests for power modules usually include high-temperature gate bias for gate reliability, high-temperature reverse bias and high-voltage high-humidity high-temperature reverse bias test (HV-H3TRB) for chip edge termination blocking capability, and power cycling test (PCT) for packaging reliability [1], [2]. HV-H3TRB and PCT are the two critical tests for power semiconductor devices operated in humid environments for long-term reliability [3]. However, the standard tests aim at only one stress, for example, the voltage or temperature stress, without considering the actual application with high voltage, large current, high temperature, and high humidity existing simultaneously.

For HV-H3TRB, the leakage current increasing or blocking voltage decreasing are the two most common failure phenomena for power modules, which indicates the blocking capability degradation of devices under test (DUTs) [4]. The root causes are electrochemical migration (metal corrosion, migration, and formation of a dendrite), aluminum corrosion, and the change of charge distribution [4], [6]. Only constant high voltage, high temperature, and high humidity are applied during the aging process.

For PCT, bond wire fatigue and solder layer degradation are the two most common failure modes for power modules [7]. The root cause is the mismatch of the coefficient of temperature expansion between two layers [8], resulting in the thermal stress at the interface under cyclic temperature variations. However, high voltage is not applied, and the humidity environment is also not considered.

Over the past decades, both tests are mainly investigated separately, the stresses are not coupled, and failure is not related, which is not close to the actual application. A big step was made over the past two years. Hoffmann has conducted consecutive tests of HV-H3TRB and PCT to investigate the coupling physics and relationship between the two tests in which DUTs are operated 50% cycles to failure in PCT first and followed by HV-H3TRB till the end of life (EoL) with HV-H3TRB failure criterion [3] or performed 85 °C/85%RH, 80% nominal blocking voltage V_{CES} for 2139 to 2429 h in HV-H3TRB first and followed by PCT till EoL with the PCT failure criterion [9].

The results show that there are interaction failure mechanisms of thermal resistance increment between HV-H3TRB and PCT. However, this is powerful to prove that the standard separated reliability tests have many drawbacks. Meanwhile, this consecutive method cannot apply the electrochemical and thermomechanical stress at the same time, and in HV-H3TRB, the temperature, humidity, and voltage are set constant. While in actual working conditions, such as electric vehicles in a humid environment, the voltage, current, temperature, and humidity exist simultaneously, and the temperature and humidity also vary, which cannot be represented by the consecutive test. In

Manuscript received 24 September 2022; revised 4 January 2023; accepted 10 February 2023. Date of publication 20 February 2023; date of current version 20 April 2023. This work was supported by the National Natural Science Foundation of China under Grant 52007061. Recommended for publication by Associate Editor D. G. Lamar. *(Corresponding author: Erping Deng.)*

Yanhao Wang, Lixin Wu, Yuxing Yan, Yiming Zhang, Yushan Zhao, and Yongzhang Huang are with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources, North China Electric Power University, Beijing 102206, China (e-mail: wyh18800107889@163.com; wulixin19981218@163.com; yuxingyan2021@163.com; yiming_zhang_ncepu@163.com; 15958164074@163.com; huang_y_z@ncepu.edu.cn).

Erping Deng is with the Hefei University of Technology, Hefei 230009, China (e-mail: erping.deng@hfut.edu.cn).

Haiyang Cao and Pin Zeng are with the NIO Company, Ltd., Shanghai 201800, China (e-mail: haiyang.cao@nio.com; mike.zeng@nio.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3246498.

Digital Object Identifier 10.1109/TPEL.2023.3246498

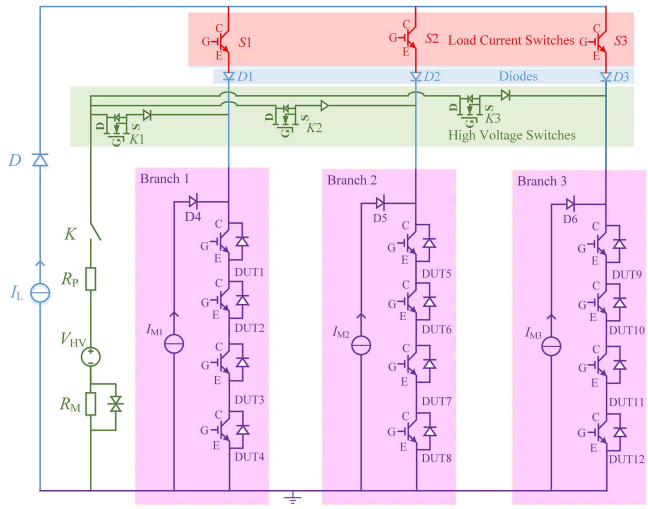


Fig. 1. Test circuit of the proposed PC+HV-H3TRB.

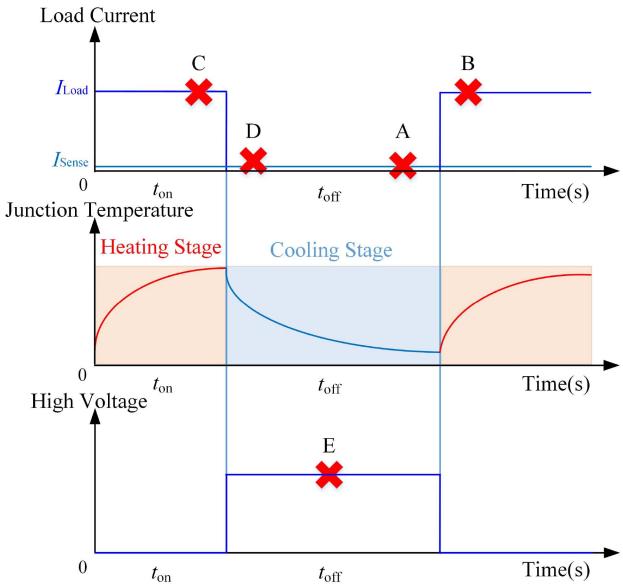


Fig. 2. Schematic diagram of the measurement points.

conclusion, there is no such reliability test to apply the electrochemical and thermomechanical stress simultaneously up to now.

In this article, an advanced integrated HV-H3TRB with PCT (named PC+HV-H3TRB for short) test is proposed to apply electrochemical and thermomechanical stress simultaneously for power modules. This test can reflect the actual working condition (existing voltage, current, temperature, temperature gradient, and humidity at the same time). The temperature and humidity vary with junction temperature in the HV-H3TRB stage. The rest of this article is organized as follows. In Section II, the test circuit and principle of the proposed PC+HV-H3TRB are introduced first, then the test implementation and precise measurement method for the parameters are analyzed. Section III illustrates a 6-kV/750-A prototype of PC+HV-H3TRB and the noise mitigation method for measurement. In Section IV, the standard PCT is introduced first, then parameters development, lifetime distribution, and optical inspection of DUTs performed by standard PCT and PC+HV-H3TRB are compared and discussed, and scanning electron microscope (SEM) is utilized to explore the failure mechanism further. Finally, Section V concludes this article.

II. Proposed PC+HV-H3TRB Test

A. Principle of the Proposed PC+HV-H3TRB

Fig. 1 shows the test circuit of the proposed PC+HV-H3TRB based on the standard PCT presented in our previous articles [10], [11]. The working principle is that load current I_L flows DUTs and is switched to different branches through load current switches $S1$–$S3$. High voltage is applied to DUTs through high-voltage switches $K1$–$K3$ at one order behind load current to use the cooling stage of power cycling to conduct HV-H3TRB with varying temperature and humidity, which is closer to actual working conditions. For example, when the load current flows in the first branch, the blocking voltage is applied to the third branch. After t_{on}, $S2$ closes, and the load current is transferred to the second branch. Then, the $S1$ and gate signals of DUT1–DUT4 are turned OFF, $K3$ is turned OFF, $K1$ is turned ON, and the blocking voltage is transferred to the first branch during the PCT cooling stage.

It is worth noting that diodes are widely used in the circuit for blocking voltage. Diodes D and $D1$–$D6$ block high voltage to protect the load current source I_L, load current switches $S1$–$S3$, and measurement current sources I_{M1}–I_{M3}. The reason is that when the first branch is conducting load current, the third branch is blocking high voltage. This high voltage will be applied to the load current switch, load current source, and measurement current source. Since the load current switch is IGBT and its emitter–collector resistance is not enough to block such high voltage, diodes $D1$–$D3$ are used, similar to D, and $D4$–$D6$. V_{HV}, K, R_P, and R_M means the high voltage source, high voltage relay, protection resistor, and leakage current measurement resistor, respectively.

As is presented in Fig. 2, load current flows, and junction temperature T_j rises during t_{on}, load current removes and junction temperature T_j falls during t_{off}, and high voltage is applied during t_{off}. The parameters of ON-state voltage drop V_{CEsat} (at millivolt accuracy), power loss P_{loss}, thermal resistance between junction and heatsink R_{thjhs}, junction temperature T_j, and heatsink temperature T_{hs}, are monitored or calculated at four points (A, B, C, and D) near the rising edge and falling edge of load current at the microsecond accuracy. Points A, B, C, and D correspond to the cold V_{CEsat} under I_M [V_{CEsat}_cold(I_M)], the cold V_{CEsat} under I_L [V_{CEsat}_cold(I_L)], the hot V_{CEsat} under I_L [V_{CEsat}_hot(I_L)], and the hot V_{CEsat} under I_M [V_{CEsat}_hot(I_M)], respectively. Cold means DUTs have not been heated yet, while hot represents that DUTs have been heated by load current I_L. Points A and D are used to monitor T_j, Point D also calculates junction-case thermal resistance R_{thjhs} by the formula $R_{thjhs} = (T_j - T_{hs})/P$, where T_{hs} is the heatsink temperature and P is the power loss.

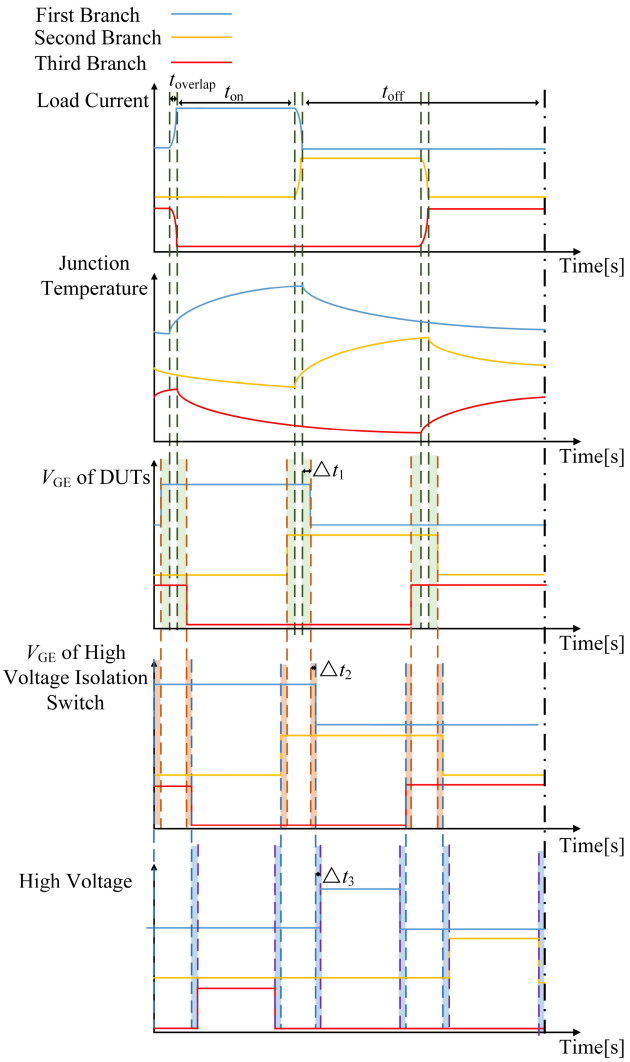


Fig. 3. Sequence of control signals in PC+HV-H3TRB.

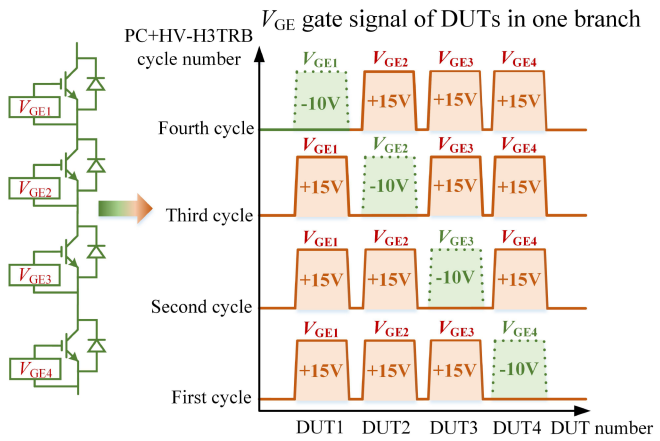


Fig. 4. Sequential method for the leakage current measurement.

Point D indicates the solder layer status. Points B and C are used to monitor V_{CEsat} at load current cold and hot, respectively, indicating the status of bond wires. B is used for failure assessment of bond wires because it is not affected by the increasing junction temperature T_j with the aging process. Leakage current I_{CES} (measured at microampere accuracy) is monitored through R_M during the cooling stage (Point E) at the second accuracy.

B. Test Implementation

The test implementation of the proposed PC+HV-H3TRB is given in Fig. 3. The purpose of the control sequence design is to monitor parameters at A–E points at the microsecond, millivolt, and microampere accuracy.

When load current flows, all gate signals of DUTs are controlled and turned ON, leading to an increment of junction temperature, V_{GE} of the high-voltage isolation switch sets to ON-state, and at this moment, no high voltage is applied. When load current draws, gate signals of DUTs are controlled and turned OFF, performing HV-H3TRB at the decreasing junction temperature, V_{GE} of high-voltage isolation switch sets to OFF-state to protect data acquisition (DAQ) system of power cycling, high voltage applies. Leakage current is then measured through leakage current measurement resistor R_M at microampere accuracy. In Fig. 3, the t_{on} is the power-ON time, t_{off} is the power-OFF time, t_{overlap} is the deadtime during branch change, Δt_1 means the delay time between load current switches and gate signals of DUTs, Δt_2 means the delay time between gate signals of DUTs and high-voltage isolation switches, and Δt_3 means the delay time between high-voltage isolation switches and applied high voltage.

Since the DAQ power cycling system is under high voltage, rational selection of Δt_1, Δt_2, and Δt_3 strongly influences the measurement accuracy. Increase Δt_1 results in a more extended turned-ON gate signal of DUTs, which allows sufficient time for the measurement current I_M to flow and monitor junction temperature T_j. An increase in Δt_2 causes adequate time for high-voltage isolation switch operation after DUTs turn OFF. An increment of Δt_3 means sufficient time for high-voltage isolation switch operation before high voltage is applied. To summarize, Δt_1 influences the measurement accuracy of T_j, where a sufficiently large Δt_1 avoids measurement errors caused by I_M during load current switching between different branches. Δt_2 and Δt_3 are essential to leakage current measurement and protect for DAQ system under high voltage, where sufficiently large Δt_2 and Δt_3 enable $K1$–$K3$ and relative switches block the high voltage applied to DUT and DAQ system. However, the parameter of Δt_1, Δt_2, and Δt_3 cannot be too large because of resulting in a shorter testing time of power cycling and HV-H3TRB. In Sections III and IV, Δt_1, Δt_2, and Δt_3 are set at 8, 4, and 50 ms, respectively. Since t_{on} and t_{off} are usually determined at several seconds, which is almost 100 times as much as Δt_1, Δt_2, and Δt_3, thus the influence on test time is negligible.

In each branch, DUTs are connected in serial and share the applied high voltage, which is unsuitable for the HV-H3TRB test. Therefore, the sequential method for the leakage current measurement is proposed. As displayed in Fig. 4, gate signals are given to DUTs in the cooling stage of power cycling in turn. Only

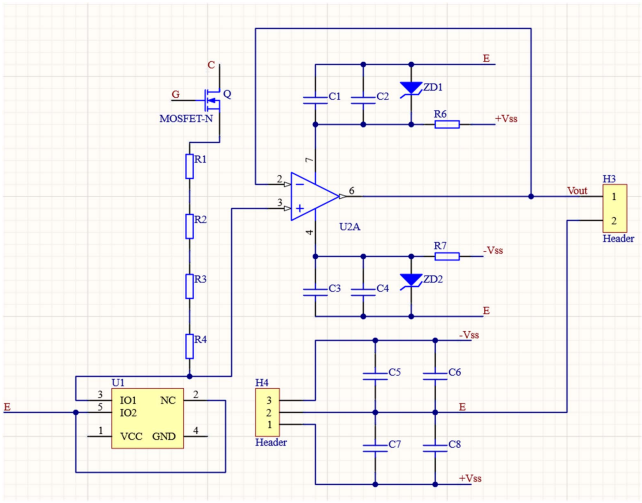


Fig. 5. High-voltage isolation circuit to protect DAQ.

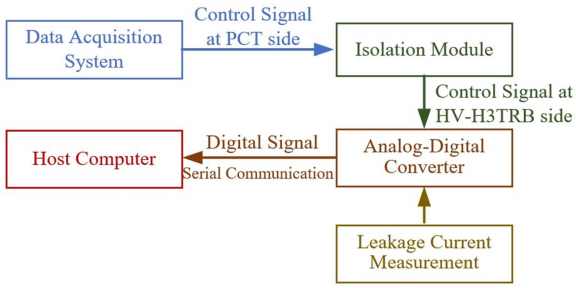


Fig. 6. Flowchart of distributing leakage current to the right DUT.

one device in the same branch is turned OFF in each cycle, and the blocking voltage is applied to that DUT, and R_M measures the leakage current at microampere accuracy. This method was also reported in [12] and will sacrifice some test time of HV-H3TRB on DUTs. However, compared with other methods, such as series–parallel conversion (convert to the parallel relationship between DUTs when applied high voltage), whether the cost of the whole test bench or the feasibility, the sequential method is better and more accessible.

C. Precise Measurement Method for Parameters in PC+HV-H3TRB

Two central problems need to be figured out, and one is the precise measurement of V_{CEsat} and T_j at the microsecond and millivolt accuracy under high voltage. The other one is that the power cycling sequence should be consistent with HV-H3TRB. That is to say, the information of the control sequence in power cycling should tell the HV-H3TRB side, and the leakage current measured in the polling method can be distributed to the right DUT.

The high-voltage isolation circuit is designed to solve the first problem. It uses SiC MOSFET Q as a high-voltage isolation switch (its V_{GE} is controlled, corresponding to Fig. 3) for its high frequency in switching and blocking high voltage. The circuit diagram is shown in Fig. 5 . It is worth noting that the measuring wire should be capable of blocking high voltage and maintaining low measurement noise simultaneously.

The isolation modules are used to solve the second problem, which can transport information from the PCT side to the HV-H3TRB side as shown in Fig. 6. The main idea bifurcates into two parts: one is the measurement of leakage current I_{CES} at microampere at second accuracy, and the DAQ system of HV-H3TRB can achieve this process and transmit it to the analog–digital converter. The other is the control signal transferred from the PCT DAQ system. After the isolation process, it is converted to the analog–digital converter. This digital signal will be utilized to distribute the I_{CES} data to the corresponding DUTs, and the time scale in this process is at second accuracy.

III. Measurements of the PC+HV-H3TRB

A. Prototype of the Proposed PC+HV-H3TRB

To verify the feasibility and effectiveness of the proposed topology, a 6-kV/750-A PC+HV-H3TRB prototype is developed (shown in Fig. 7) with a 6-kV/0.1-A voltage source and 20-V/750-A current source. DUTs are placed in a constant temperature humidity chamber, providing high temperature and humidity environmental stress. Power cycling and HV-H3TRB test bench are placed separately to reduce electrical disturbance between elements. The PCT side includes a load current source, measurement current source, cooling system, DAQ for PCT, switches, and diodes. The HV-H3TRB side involves a voltage source, DAQ for HV-H3TRB, printed circuit board (PCB) of high-voltage relay, and gate signals for DUTs, isolation modules, and so on.

B. Noise Mitigation for Measurement

Since V_{CEsat} is measured at millivolt, microsecond accuracy, this article evaluates the measurement noise of the PC+HV-H3TRB test first. The V_{CEsat} of DUTs under measurement current I_M is displayed in Fig. 8, and the oscillation is about ± 1.5 mV, corresponding to ± 0.75 °C in measuring virtual junction temperature T_{vj} via the K-factor method [12].

The relationship between T_{vj} and V_{CEsat} for the DUT used in Section IV is plotted in Fig. 9. Generally, the slope is around -2 mV/°C for the silicon p-n junction.

For the precise measurement of the leakage current in the PC+HV-H3TRB test, leakage current paths are necessary to analyze first [see Fig. 10(a)]. The assumption high voltage is applied to branch 1, and the gate signal of DUT1 is turned OFF according to Fig. 4. Four leakage currents are flowing through R_M in total, one is the leakage current I_{CES1} of DUT1, the second is the reverse leakage current I_{CES2} of the diode $D1$, and the others are leakage currents I_{CES3} and I_{CES4} through $K2$ and $K3$.

For I_{CES3} and I_{CES4}, the $K1$–$K3$ are discrete SiC MOSFETs with 1200 V nominal voltage, its drain–source leakage current I_{DSS} is far below 0.3 μA when blocking 500 V at room temperature (where I_{DSS} equals 0.3 μA at 85 °C/85%RH, 960 V in our previous study [13]), which is less than one-tenth of the total

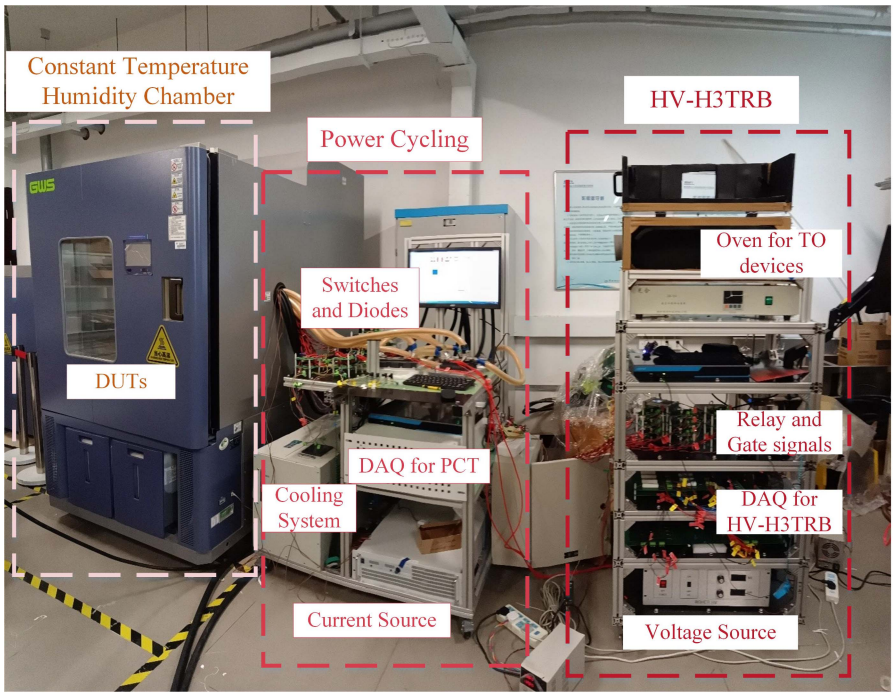


Fig. 7. 6-kV/750-A prototype of PC+HV-H3TRB.

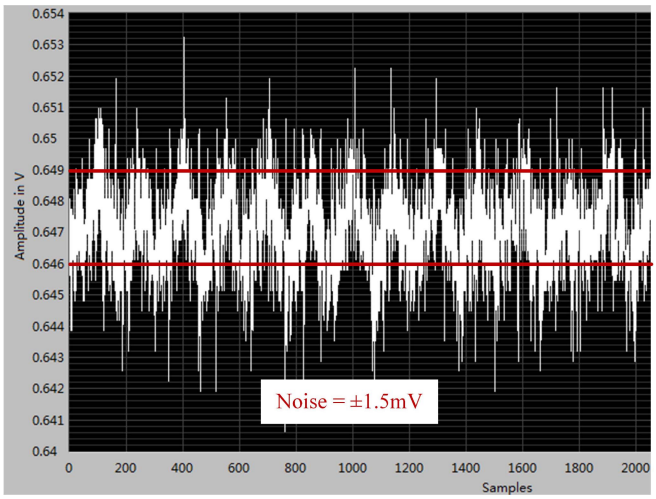


Fig. 8. Measured V_{CEsat} for DUT1.

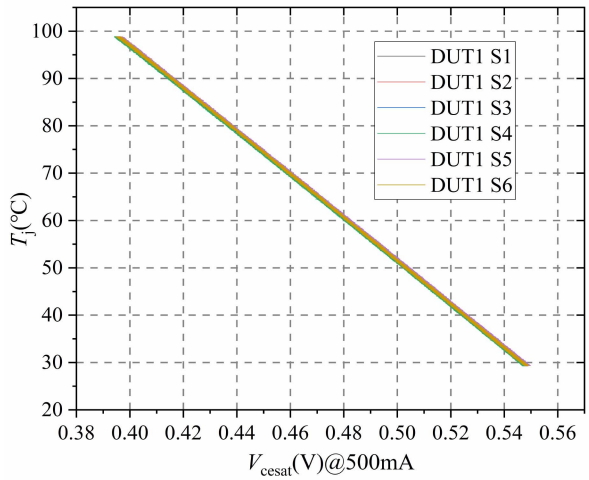
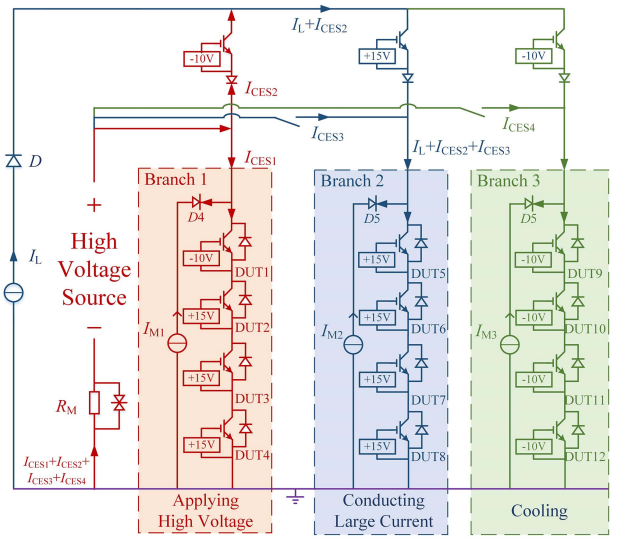


Fig. 9. Schematic and physical map for the connection of DUTs.

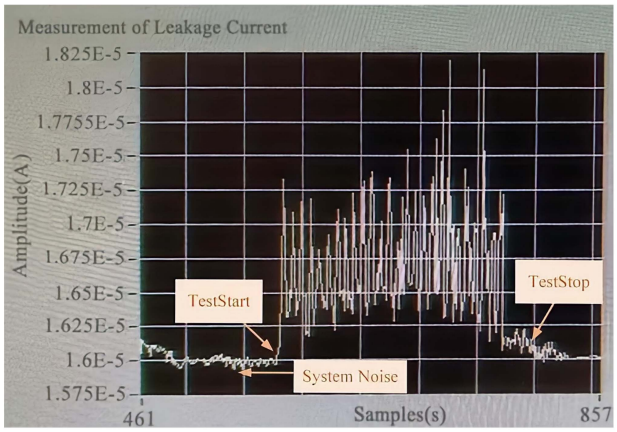
leakage current I_{CES} of 3 μA measured in Section IV. Second, the leakage currents of $K2$ and $K3$ remain constant during the PC+HV-H3TRB test because their aging at room temperature is negligible; thus, the variation of total leakage current ΔI_{CES} is determined by DUTs' degradation and irrelevant to $K2$ and $K3$, and the leakage currents I_{CES3} and I_{CES4} of $K2$ and $K3$ can be ignored.

For I_{CES1} and I_{CES2}, $D1$ is very important because it conducts load current and blocks high voltage; here, we use a diode of 3300 V/1200 A to block 500 V to make I_{CES2} constant. Since the total leakage current $I_{\mathrm{CES}} \approx I_{\mathrm{CES1}} + I_{\mathrm{CES2}}$, when the aging of $D1$ is negligible and I_{CES2} is constant, I_{CES} can reflect the variation of I_{CES1}, and the relative variation amount ΔI_{CES} equals the DUT1s leakage current development ΔI_{CES1}, which indicates the blocking capability degradation of DUT1. The assessment of leakage current I_{CES} is shown in Fig. 10(b) in which I_{CES} is measured at the microampere accuracy.

Furthermore, the V_{CEsat} waveform of DUT1 at four points (A–D) for one cycle in the PC+HV-H3TRB is measured in Fig. 11. The sample rate of V_{CEsat} is controlled at 15 kHz. The V_{CEsat} starts at V_{CEsat}_cold(I_M) of point A, which is about 0.484 V. When load current I_L flows, V_{CEsat} increases, and after an oscillation process (induced by load current source) of fewer than 200 samples (13 ms), the V_{CEsat}_cold(I_L) reaches stable at around 1.55 V. After heating by load current I_L for $t_{\mathrm{on}} =$ 2 s, the V_{CEsat}_hot(I_L) increases by 0.07 V compared with



(a)



(b)

Fig. 10. Leakage current measurement method. (a) Leakage current path analysis. (b) Waveform of measured I_{CES} for DUT1.

V_{CEsat}_cold(I_L). Finally, when the load current is removed, the V_{CEsat} drops quickly and increases slowly after several samples, representing the spot of V_{CEsat}_hot(I_M) and $T_{j\max}$. Since the slope of the *K*-factor is negative, the V_{CEsat}_hot(I_M) declining indicates a $T_{j\max}$ increase, and we should avoid selecting the spots of V_{CEsat}_hot(I_M) declining. This phenomenon is caused by measurement error when DUT is turned OFF, and after measurement delay time t_{MD}, the spot of V_{CEsat}_hot(I_M) increasing should be selected. This article selects a t_{MD} at 330 μs (corresponding to sample number at around 5) to monitor $T_{j\max}$, and the sample rate of 15 kHz is enough to capture $T_{j\max}$ accurately in the PC+HV-H3TRB test.

IV. Comparison of Standard PCT and Proposed PC+HV-H3TRB

A. Test Setup

To verify the feasibility and effectiveness of the proposed PC+HV-H3TRB, hybridPACK drive modules FS820R08A6P2B for electric vehicles are tested separately in standard PCT and the proposed PC+HV-H3TRB test at the same test condition. The test condition is set that the maximum junction temperature $T_{j\max} \approx 150$ °C, junction temperature swing $\Delta T_j \approx 90$ K, power-ON-time $t_{\mathrm{on}} = 1$ s, power-OFF-time $t_{\mathrm{off}} = 2$ s, load current $I_L = 608$ A, cooling temperature $T_{\mathrm{inlet}} = 57$ °C, flow rate $v_{\mathrm{coolant}} = 12$ L/min, and measurement delay time $t_{\mathrm{MD}} = 330$ μs.

The failure criteria for PCT are the 5%V_{CEsat} increment for bond wire fatigue and 20%R_{thjhs} increment for solder layer degradation [1]. Ten times leakage current I_{CES} increase is also counted as a failure criterion [14]. The V_{CEsat} and R_{thjhs} development and lifetime of DUTs in the standard PCT are compared with those in PC+HV-H3TRB. Since PC+HV-H3TRB applies more stresses, three additional test conditions of HV-H3TRB are added: applied high voltage $V_{\mathrm{CES}} = 500$ V, ambient temperature $T_{\mathrm{Ambient}} = 50$ °C, and ambient humidity $H_{\mathrm{Ambient}} = 85\%$RH. The selecting principle for these test conditions is that accelerating moisture invasion as much as possible while not triggering impractical failure mechanisms. For ambient humidity H_{Ambient}, a high value, such as 95%RH, may cause condensation easily with varying junction temperature and leads to DUTs' breakdown; thus, 85%RH is selected as a compromise. For ambient temperature T_{Ambient}, when it is high, such as 85 °C/85%RH, the moisture around the heatsink will condense and cause breakdown as well (heatsink temperature is at 57 °C and determined by standard PCT condition). A temperature of 50 °C is also selected as a compromise. For voltage, 80% nominal blocking voltage V_{nom} is the limit to prevent impractical failure mechanisms [4], considering the margin; here, 500 V is selected.

Two DUTs (each DUT has six single switches) are used in each test to avoid random events and to avoid confusion, DUT′*i*′-S′*j*′ designates the *j*th switch of test device *i* (e.g., DUT3-S1 means the first switch of DUT3) in the later discussion. DUT3 and DUT6 conduct standard PCT, while DUT5 and DUT7 conduct PC+HV-H3TRB. The standard PCT is performed at the test bench, as shown in Fig. 12, which includes the load current source, DAQ system, PCBs, measurement current sources, thermocouples, DUTs, and so on. V_{GE} signal and V_{CEsat} measurement are connected to the PCBs and DAQ system separately. Thermocouples measure the inlet and outlet temperature. DUTs are fixed on the heatsink, heated by load current, and cooled by the cooling system.

In Fig. 13, the current flowing path for both standard PCT and PC+HV-H3TRB is straight through. In PC+HV-H3TRB, the cooper and cable for loading current should be designed thicker and larger for poor dissipation inside the chamber.

B. Results Discussion

The development of V_{CEsat} and R_{thjhs} for DUT3 and DUT6 in standard PCT is displayed in Fig. 14 in the following text.

For HybridPACK drive modules, six single switches are packaged to form the entire full-bridge module, and thus, the failure of only one switch means the failure of the whole device. The DUTs conducted by the standard PCT all failed by bond wire fatigue at a 5% increment, and none of them reached the failure criterion

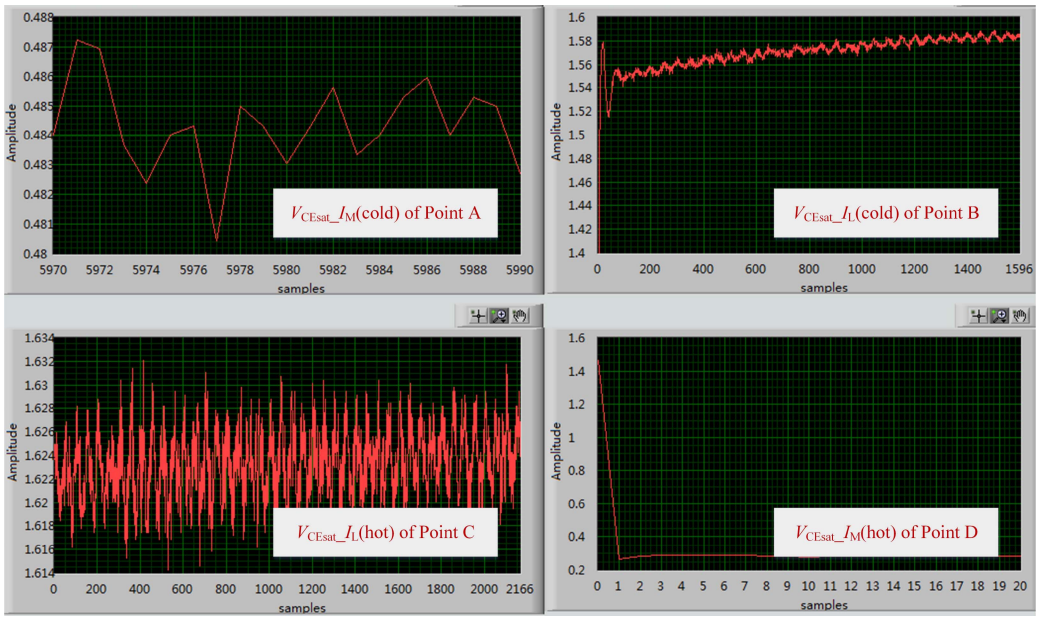


Fig. 11. V_{CEsat} waveform of DUT1 at A–D during PC+HV-H3TRB test.

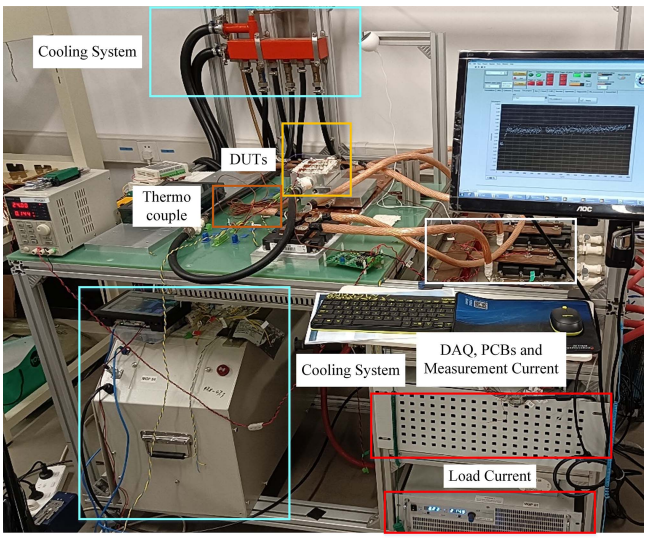


Fig. 12. Photograph of the standard PCT test bench.

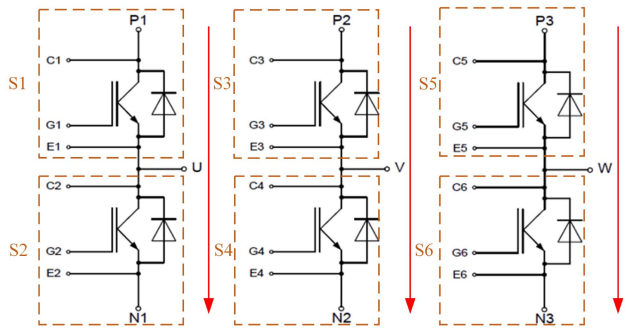


Fig. 13. Schematic diagram of the current path.

of R_{thjhs}. DUT3-S1, DUT3-S3, DUT3-S4, and DUT6-S4 get the failure line with 105% V_{CEsat} at N_f = 177 912, 178 544, 182 777, and 176 689, respectively.

However, for DUT5 and DUT7 performed PC+HV-H3TRB, things are entirely different. The development of V_{CEsat} and R_{thjhs} for DUT5 and DUT7 is displayed in Fig. 15 in the following text. DUT5 and DUT7 failed by solder layer degradation, indicating that the failure mode has changed from bond wire fatigue to solder layer degradation.

DUT5-S4 and DUT7-S2 failed by solder layer degradation at N_f = 134 306 and 153 942, respectively. DUT7-S4 reached the failure criterion of V_{CEsat} at N_f = 152 023, yet R_{thjhs} also almost reached the failure criterion. When comparing the V_{CEsat} and R_{thjhs} development trend of DUT7-S4, we found that R_{thjhs} increases at $N_f \approx$ 124 k, earlier than the increment of V_{CEsat} at $N_f \approx$ 128 k. The development of R_{thjhs} results in a higher junction temperature T_j at the chip surface and feet of the bond wire, as illustrated in (1) [11], finally leading to bond wire fatigue

$$T_j \uparrow = T_c + (R_{\mathrm{thjhs}} \times P) = T_c + (R_{\mathrm{thjhs}} \uparrow \times I \times V_{\mathrm{CEsat}}) \quad (1)$$

Another finding is that the thermal resistance R_{thjhs} of DUT5 and DUT7 increases at an early stage (DUT5-S3, DUT5-S4, and DUT7-S2, especially obvious for DUT5-S4). This phenomenon was also discussed in the previous literature [9] in which DUTs are performed HV-H3TRB first and transferred to standard PCT. The lifetime is then compared with that of purely new DUTs. It reveals that the DUTs preaged with HV-H3TRB have a shorter lifetime and the root cause is the thermal resistance increment at the early stage, which is verified by transient thermal impedance Z_{th} at different cycles. In addition, humidity can also influence the pressure on the TIM and the swelling of housing materials [15].

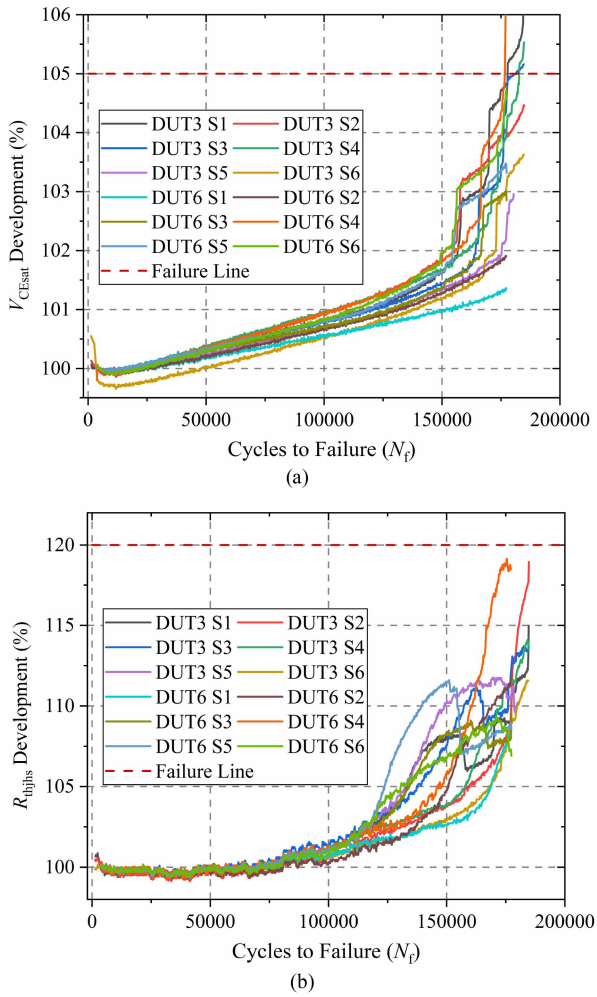


Fig. 14. V_{CEsat} and R_{thjhs} development during standard PCT. (a) V_{CEsat} development. (b) R_{thjhs} development.

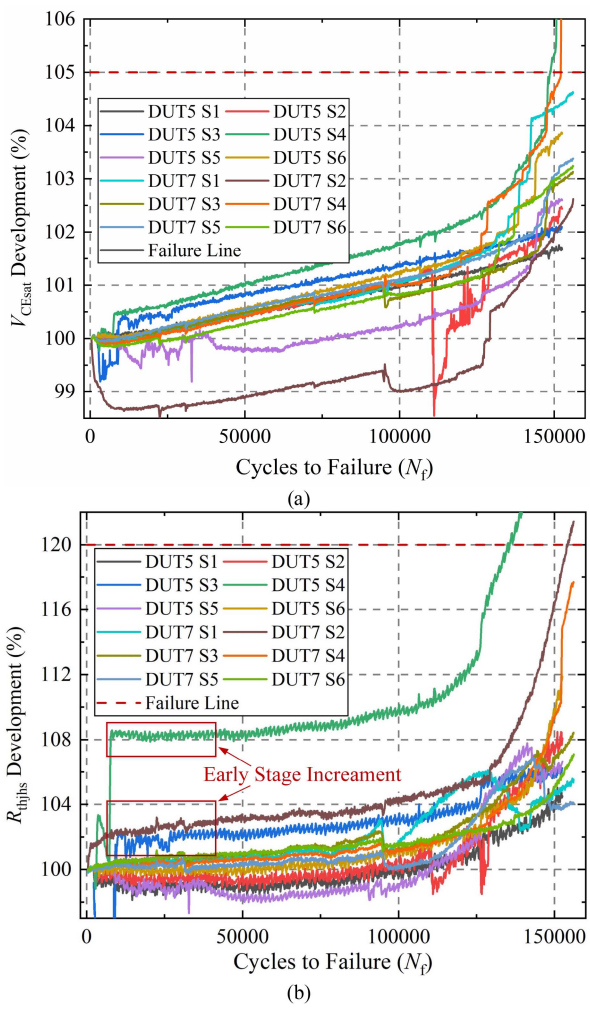


Fig. 15. V_{CEsat} and R_{thjhs} development during PC+HV-H3TRB. (a) V_{Cesat} development. (b) R_{thjhs} development.

Since the DUTs in this article are performed PC+HV-H3TRB in which large load current, high blocking voltage, ambient temperature, and ambient humidity couple firmly and simultaneously (as shown in Fig. 16); the temperature—humidity—mechanical coupling inside DUT may be more severe. There are totally two kinds of stresses applied to DUTs in the proposed PC+HV-H3TRB test setup: one is the physical stress with electrical–temperature–humidity—mechanical multiphysics field coupling, which is induced by load current, temperature, and humidity. This stress may cause a larger stress/strain at the bond wire feet compared with the standard thermomechanical stress because hygroscopic swelling is also introduced by humidity. This stress causes thermal resistance R_{thjhs} increment phenomenon at an early stage as well (in Fig. 15) because moisture changes the thermal characteristics parameters of materials (e.g., thermal capacity and thermal conductivity). The other is the chemical stress with voltage, temperature, and humidity in which ions migrate and deposit, causing a sign of corrosion (in Figs. 20 and 21). In the PC+HV-H3TRB test, two stresses are competing with each other. For longer test time (corresponds to lower ΔT_j and $T_{j\max}$ of power cycling), chemical stress becomes the dominant role, while for shorter test time (corresponds to higher ΔT_j and $T_{j\max}$ of power cycling), physical stress is the dominant role. Although two stresses are concurrent, the test condition is limited (illustrated in Section IV-A) to coincide with the practical failure mechanism.

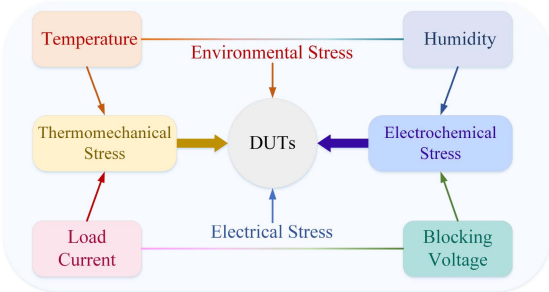


Fig. 16. Multistress coupling to DUTs under PC+HV-H3TRB test.

Literature [16] reported that failure usually occurs at the lower bridge of DUTs because of electric—thermal coupling. Thus,

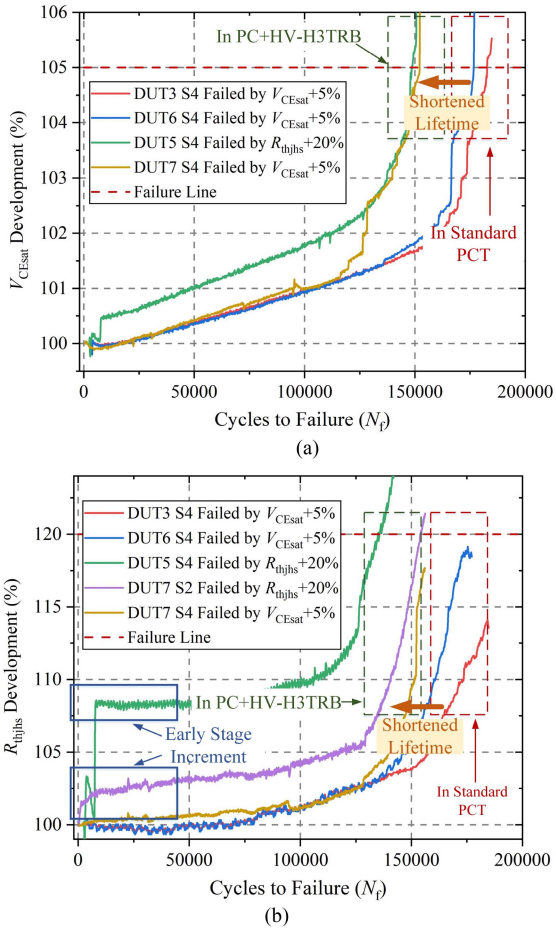


Fig. 17. Comparison of standard PCT and PC+HV-H3TRB for DUTs. (a) V_{Cesat} development. (b) R_{thjhs} development.

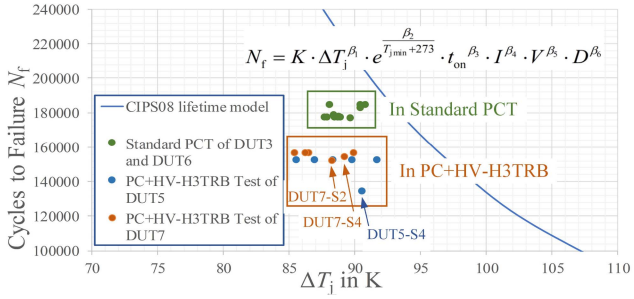


Fig. 18. Lifetime comparison of DUTs and CIPS08 model.

several switches (DUT3-S4, DUT6-S4, DUT5-S4, DUT7-S2, and DUT7-S4) are selected to compare V_{Cesat} and R_{thjhs} parameters. In Fig. 17, the proposed PC+HV-H3TRB shortens the lifetime of DUTs, and PC+HV-H3TRB may become a more severe reliability test than the standard PCT. It is due to the failure mode changing from bond wire fatigue to solder degradation.

Furthermore, the lifetime of the CIPS2008 model [17], [18], DUTs performed standard PCT, and PC+HV-H3TRB are compared in Fig. 18. The lifetime of the CIPS2008 model calculates

TABLE I
LIFETIME COMPARISON OF FAILED SWITCHES

Switch Number	Failure Mode	Cycles to Failure(N_f)	Performed Test
DUT3-S1	+5%V_{CEsat} increment	177 912	Standard PCT
DUT3-S3	+5%V_{CEsat} increment	178 544	Standard PCT
DUT3-S4	+5%V_{CEsat} increment	182 777	Standard PCT
DUT6-S4	+5%V_{CEsat} increment	176 689	Standard PCT
DUT5-S4	+20%R_{thjhs} increment	134 306	PC+HV-H3TRB
DUT7-S2	+20%R_{thjhs} increment	153 942	PC+HV-H3TRB
DUT7-S4	+5%V_{CEsat} increment	152 023	PC+HV-H3TRB

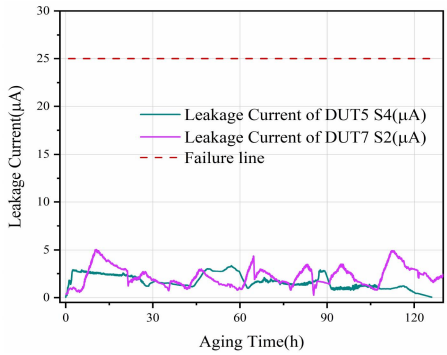


Fig. 19. Leakage current monitored during PC+HV-H3TRB.

by the following equation, where basis lifetime $K = 9.30 \times 10^{14}$, $\beta_1 = -4.416$, $\beta_2 = 1285$, $\beta_3 = -0.463$, $\beta_4 = -0.716$, $\beta_5 = -0.761$, $\beta_6 = -0.5$, minimum junction temperature $T_{\mathrm{jmin}} = 60$ °C, power-ON time $t_{\mathrm{on}} = 1$ s, blocking voltage $V_{\mathrm{BD}} = 7.5$, current per bond wire $I \approx 608/(20 \times 3) = 10.13$ A, and diameter of bond wire $D \approx 400$ μm

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{\beta_2}{T_{jmin}+273}} \cdot t_{\mathrm{on}}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad (2)$$

The lifetime for DUTs performed standard PCT is 176 689(DUT6-S4), 177 912(DUT3-S1), 178 544(DUT3-S3), and 182 777(DUT3-S4), respectively, and they match the CIPS2008 lifetime model well (gray dots and blue line). However, the lifetime of DUT5 and DUT7 (performed PC+HV-H3TRB, yellow and red dots) is 20k cycles lower, with the lifetime of 134 306(DUT5-S4) and 152 023(DUT7-S4) and 153 942(DUT7-S2).

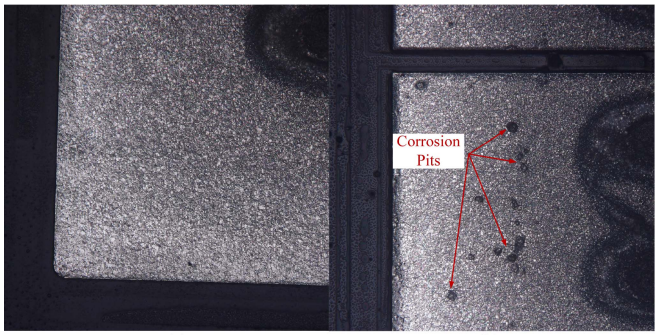
These tests end at an increment of R_{thjhs} by 30% or V_{CEsat} by 10% to see if more failure will occur, and switches that failed or not are included in Fig. 18 above. DUT5-S4, DUT7-S2, and DUT7-S4 are the only failed switches during the PC+HV-H3TRB test, indicating strong temperature–humidity–mechanical coupling at the lower bridge of DUTs.

The lifetime data are summarized in Table I for a better presentation of the experimental results.

Although high voltage applies to DUTs, the performance of leakage current of DUTs during PC+HV-H3TRB did not show any degradation signature in Fig. 19. In the last static parameters measurement, the leakage current I_{CES} decreases by 27.5%, and

TABLE II
GATE LEAKAGE CURRENT I_{GES} COMPARISON FOR DUT7 BEFORE AND AFTER PC+HV-H3TRB TEST

Device Number	Failure Information	I_{GES} before test(nA)	I_{GES} after test(nA)
DUT7-S1	Not Fail	4.4	3.1
DUT7-S2	+20%R_{thjhs} increment, N_f=153 942	4.6	2.5
DUT7-S3	Not Fail	4.5	4.3
DUT7-S4	+5%V_{CEsat} increment, N_f=152 023	3.3	35.9
DUT7-S5	Not Fail	4.1	3.9
DUT7-S6	Not Fail	4.6	3.6



(a) (b)

Fig. 20. Optical inspection comparison of chip surface topography. (a) DUT3-S2 after standard PCT. (b) DUT7-S6 after PC+HV-H3TRB.

breakdown voltage BV_{CES} increases by an average of 1.6% for DUT7 after the PC+HV-H3TRB test, indicating that the blocking capability does not degrade.

To ensure that the DUTs' failure is irrelevant to gate degradation, a gate leakage current I_{GES} for DUT7 is compared before and after the PC+HV-H3TRB test. The result is given in Table II, which showed an increment for DUT7-S4 and a decrease for DUT7-S2, indicating gate degradation is not the main reason for DUTs' failure.

However, when we remove the silica gel and optical inspect the chip surface for the failure analysis in Fig. 20, the corrosion pits are found at the chip surface, indicating that PC+HV-H3TRB has applied another electrochemical stress on the DUTs. This phenomenon is caused by moisture corrosion at the chip surface.

Furthermore, an SEM with Energy Dispersive X-Ray Analysis (EDX) was performed by HITACHI SU3800 to figure out the component content of these corrosion pits, as shown in Fig. 21. The bright part represents the presence of the element, while the dark part means the absence of the element. It reveals that sulfur and carbon are the two primary causes of this phenomenon. Since the chip surface is covered by silica gel, sulfur likely comes from silica gel. There are two circumstances here: one is that sulfur is carried by the silica gel itself, which is induced or contaminated during the manufacturing process. The other is that sulfur comes from the air outside silica gel, which diffuses into silica gel before the PC+HV-H3TRB test and further diffuses to the chip surface with high-temperature vapor. After employing SEM with EDX on the silica gel material, the results show that there is no sulfur found in the material (shown in Fig. 22), and the air is the potential source of sulfur.

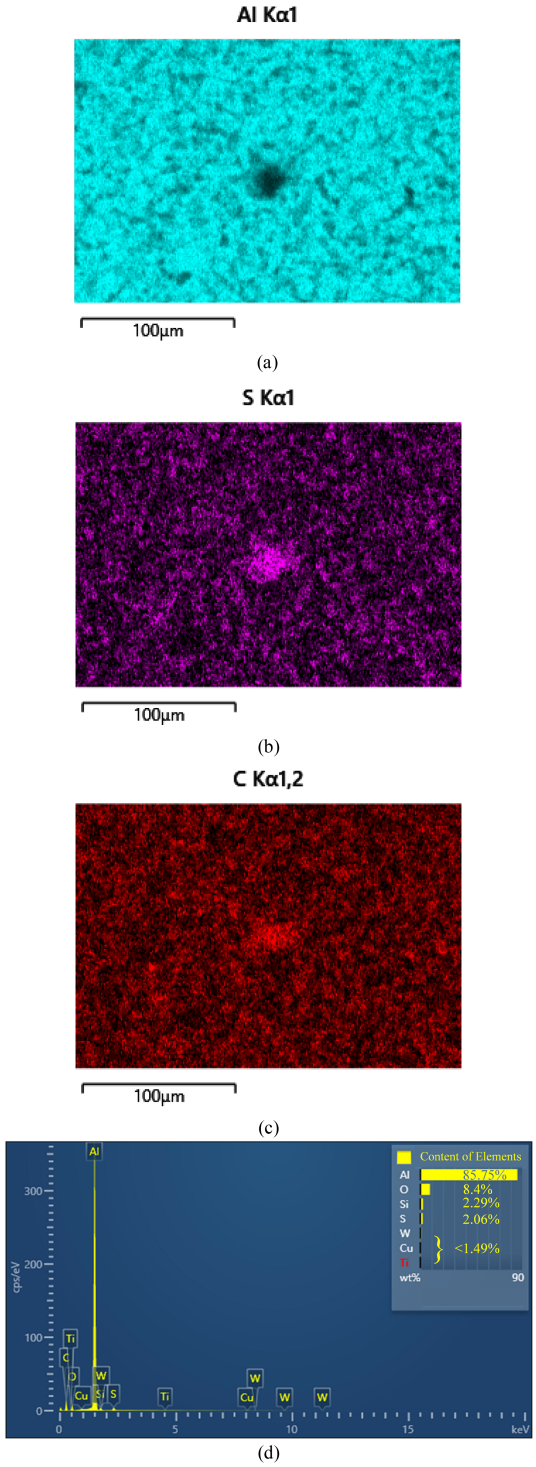


Fig. 21. SEM of the corrosion pit. (a) Aluminum distribution. (b) Sulfur distribution. (c) Carbon distribution. (d) Content of elements detected.

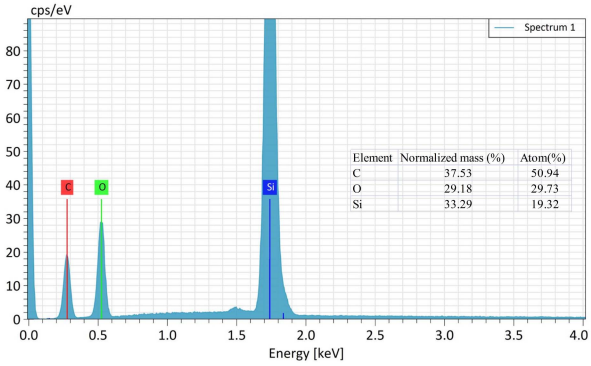


Fig. 22. Elements component analysis of silica gel material.

V. Conclusion

In this article, an advanced PC+HV-H3TRB test with high voltage, large current, high temperature, and high humidity is proposed to get closer to actual working conditions. The proposed test based on standard PCT integrates HV-H3TRB at the cooling stage to simultaneously apply the electrochemical and thermomechanical stress for power modules. Some preliminary conclusions can be drawn as follows.

1) The PC+HV-H3TRB test circuit, working principle, and implementation are proposed. The high-voltage isolation circuit and isolation modules are designed to assure precise measurement at the millivolt, microampere, and microsecond accuracy under high voltage.
2) A 6-kV/750-A prototype of PC+HV-H3TRB is constructed to verify the proposed scheme's feasibility and effectiveness. The noise evaluation and five points' (A–E) measurement in one cycle are illustrated. The parameters of Δt_1, Δt_2, and Δt_3 are set at 8 ms, 4 ms, and 50 ms to ensure an adequate time to block high voltage while keeping the accurate measurement.
3) Full-bridge power modules for electric vehicle use are tested and compared at the same test condition in standard PCT and the proposed PC+HV-H3TRB test. The failure mode indicates a transform from bond wire fatigue (in standard PCT) to solder degradation (in PC+HV-H3TRB). R_{thjhs} increases at an early stage in PC+HV-H3TRB, implying moisture invasion that influence the thermal resistance. This phenomenon leads to a 19.3% shorter lifetime of DUTs in PC+HV-H3TRB.
4) After optical inspection, the corrosion pits are found at the chip surface after PC+HV-H3TRB, implying that electrochemical corrosion is another failure mechanism caused by humidity, and subsequent SEM proves that the corrosion is caused by sulfur or carbon elements.

References

[1] T. Harder, "ECPE guideline AQG 324: Qualification of power modules for use in power electronics converter units (PCUs) in motor vehicles," 2018.
[2] IEC 60747-9:2019: Semiconductor devices Discrete devices—Part 9: Insulated gate bipolar transistors (IGBTs) [S], 2019.
[3] F. Hoffmann, M. Hanf, N. Kaminski, and S. Schmitt, "Investigation on the impact of thermo-mechanical stress on the humidity ruggedness of IGBTs by means of consecutive PCT and H3TRB testing," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 376–379.
[4] C. Zorn and N. Kaminski, "Temperature humidity bias (THB) testing on IGBT modules at high bias levels," in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–7.
[5] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (THB) testing on IGBT modules by high bias levels," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 385–388.
[6] H. Matsushima, H. Okino, K. Mochizuki, and R. Yamada, "Charge distribution in termination area of 4H-SiC diodes analyzed by measuring depletion-layer capacitance," in *Proc. Int. Conf. Solid State Devices Mater.*, 2015, pp. 500–501.
[7] V. Smet et al., "Ageing and failure modes of IGBT modules in high-temperature power cycling," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4931–4941, Oct. 2011.
[8] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.
[9] F. Hoffmann, N. Kaminski, and S. Schmitt, "Investigation on the impact of environmental stress on the thermo-mechanical reliability of IGBTs by means of consecutive H3TRB and PCT testing," in *Proc. 33rd Int. Symp. Power Semicond. Devices ICs*, 2021, pp. 371–374.
[10] E. Deng, J. Chen, Y. Zhao, Z. Zhao, and Y. Huang, "Power cycling capability of high power IGBT modules for flexible HVDC system," in *Proc. PCIM Eur. Digit. Days; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020, pp. 1–8.
[11] J. Chen, E. Deng, Y. Zhang, and Y. Huang, "Junction-to-case thermal resistance measurement and analysis of press-pack IGBTs under double-side cooling condition," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8543–8553, Jul. 2022.
[12] Y. Zhang et al., "Sequential V_{ce}(T) method for the accurate measurement of junction temperature distribution within press-pack IGBTs," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3735–3743, Apr. 2021.
[13] Y. Wang, E. Deng, L. Wu, Y. Yan, Y. Zhao, and Y. Huang, "Influence of humidity on the power cycling lifetime of SiC MOSFETs," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 12, no. 11, pp. 1781–1790, Nov. 2022, doi: 10.1109/TCPMT.2022.3223957.
[14] "ECPE guideline PSRRA 01, railway applications HV-H3TRB tests for power semiconductor," 2019.
[15] F. Wuest, O. Wittler, and M. Schneider-Ramelow, "Influence of temperature and humidity on power cycling capability of power modules," *Microelectron. Rel.*, vol. 114, Nov. 2020, Art. no. 113880.
[16] Y. Zhao, E. Deng, M. Pan, Y. Zhang, and Y. Huang, "Influence of thermal coupling on lifetime under power cycling test," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13641–13651, Nov. 2022.
[17] G. Zeng, L. Borucki, O. Wenzel, O. Schilling, and J. Lutz, "First results of development of a lifetime model for transfer molded discrete power devices," in *Proc. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2018, pp. 1–8.
[18] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules—Various factors influencing lifetime," in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, 2008, pp. 1–6.

Yanhao Wang was born in Chongqing, China, in 1996. He received the bachelor's and master's degrees in electrical engineering in 2018 and 2021, respectively, from North China Electric Power University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources.

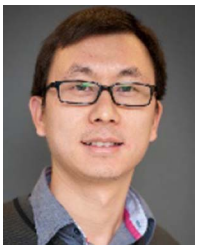
His main research interests include packaging and reliability of power devices, especially lifetime evaluation under multistress coupling.

Erping Deng (Member, IEEE) was born in Hunan province, China, in 1989. He received the bachelor's degree from the Harbin Institute of Technology, Harbin, China, in 2013, and the Ph.D degree from North China Electric Power University, Beijing, China, in 2018, both in electrical engineering.

He has been a Professor with the Hefei University of Technology, Hefei, China, since 2022. He was a University Lecturer with North China Electric Power University, Beijing, China, from 2018 to 2022, and a Postdoctor with the Chemnitz University of Technology, Germany, from 2018 to 2020. His main research interests include the packaging and reliability of high-voltage and high-power press pack IGBTs. He is also focused on the power cycling reliability, failure mechanism, lifetime modeling, and prediction of power devices.

Lixin Wu was born in Zhejiang Province, China, in 1998. He received the bachelor's degree in electrical engineering from Zhejiang Sci-Tech University, Hangzhou, China, in 2021. He is currently working toward the master's degree in electrical engineering with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources, North China Electric Power University, Beijing, China.

His main research interests include the packaging and reliability of high-power devices, especially the life assessment of actual inverter operating conditions.



Haiyang Cao was born in Hubei Province, China, in 1986. He received the B.Sc. degree in mechanical engineering from the Dalian University of Technology, Dalian, China, in 2008, and the M.Sc. degree in electromobility from the Chemnitz University of Technology, Chemnitz, Germany, in 2017.

He is currently a Technical Project Manager with Power Semiconductor Development Department, NIO, Hefei, China. He worked as a Senior Engineer with Packaging Advanced Team, Delta Power Electronic Center, Shanghai, China, from 2017 to 2020. His main research interests include power semiconductor module packaging and reliability.

Yuxing Yan was born in Yichang, China, in 1999. He received the bachelor's degree in electrical engineering from China Three Gorges University, Yichang, China, in 2021. He is currently working toward the M.D. degree in electrical engineering with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources, North China Electric Power University, Beijing, China.

His main research interests include packaging and reliability of power devices, especially the failure mechanism of high temperature tests.

Pin Zeng was born in Guangxi Province, China, in 1992. He received the B.Sc. degree in electrical and electronic engineering from the University of Nottingham Ningbo, Ningbo, China, in 2015, and the M.Sc. degree in power electronic, machines, and drives from the University of Manchester, Manchester, U.K., in 2016.

He is currently a Power Electronic Engineer with Power Semiconductor Design Department, NIO, Hefei, China. He worked as a Senior Application Engineer with Nexperia, Shanghai, China, from 2019 to 2021, and Electronic Engineer with Dynex Semiconductor, U.K., from 2016 to 2019. His main research interests include power semiconductor verification and application.

Yiming Zhang was born in Shandong province, China, in 1996. He received the bachelor's degree in electrical engineering from North China Electric Power University, Beijing, China, in 2017. He is currently working toward the Ph.D. degree in electrical engineering with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources, North China Electric Power University, Beijing, China.

His main research interests include the packaging and reliability of high-voltage and high-power electronics' devices.

Yushan Zhao was born in Hebei province, China, in 1993. He received the bachelor's degree in electrical engineering from Hangzhou Dianzi University, Hangzhou, China, in 2016, and the master's degree in electrical engineering from North China Electric Power University, Beijing, China, in 2019, where he is currently working toward the Ph.D. degree in electrical engineering with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources.

His main research interests include the packaging and reliability of electrical vehicles.

Yongzhang Huang (Member, IEEE) received the B.S. degree in engineering physics from the Department of Engineering Physics, Tsinghua University, Beijing, China, in 1984, and the Ph.D. degree in physics from the Chinese Academy of Sciences, Beijing, China, in 1991.

He is currently a Professor with North China Electric Power University, Beijing, China. His research interests include renewable energy power system, high-power electronic device and application, electric vehicle, and big data of power grid.