Letters

A Simple Switching-Event Dependent High-Frequency Sampling Method for Power Conversion System

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***Abstract*—Precise current and voltage sensing are challenging for digital control in high-frequency power conversion systems. Given that the power electronics circuitry is triggered repetitively by power device switching events, a switching-time-dependent sampling method is proposed to realize an equivalent high-frequency signal sampling with a low-speed analog digital converter (ADC) and digital controller. Two sampling modes are developed in the proposed methods in terms of sampling rates lower and higher than the digital controller clock frequency, respectively. A fast and simple signal reconstruction method is designed to ensure the feasibility of a low-cost processor. A series-resonant dual-active-bridge is taken as an example for the theoretical analysis and experimental verification. The resonant current and Miller plateau voltage in the topology are sampled to verify the potential of the proposed method for online parameter recognition of dc–dc converters and device behavior monitoring of power devices.**

***Index Terms*—Digital control, dual-active-bridge (DAB) converter, high-frequency sampling, power device monitoring.**

I. Introduction

DIGITAL control is critical for power electronic systems. To adaptively and intelligently realize those functions in power electronics systems, it is usually necessary to have various state feedback, such as current, voltage, or temperature [1]. An emerging challenge is to online digitize the high-frequency component of the current or voltage to collect more information, especially considering the increasing switching frequency in wide-bandgap-device based converter applications. Conventional signal digitization in power electronics is based on the classic Nyquist-Shannon sampling theorem [2], i.e., the sampling frequency should be at least higher than two times the highest signal frequency. In field power electronics applications, to extract desired timing or frequency information fast and simply, the sampling frequency is usually five or ten times higher. Under this constraint, the sampling and digitization of high-frequency signals become costly due to the expense of high-speed analog digital converters (ADCs) and controllers. Furthermore, as a typical design, an FPGA interface paired with high-speed ADC also increases the complexity of the control circuitry. These limitations significantly impede the application of advanced online modeling and monitoring techniques on both the device and converter levels.

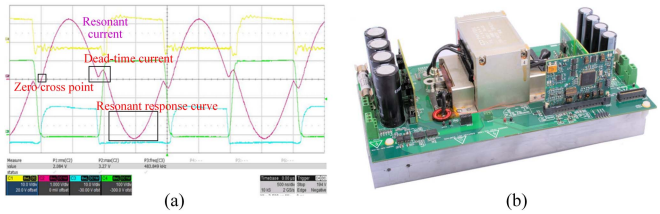

Fig. 1. CLLC converter of TI's reference design. (a) Current waveform. (b) Converter prototype.

On the device level, these techniques include device reliability monitoring [3], intelligent active gate drivers [4], and power loss estimations [5]. On the converter level, dc–dc converters are involved in this topic. For example, Fig. 1 shows the CLLLC converter of the Texas Instruments reference design [6]. Once the current can be accurately acquired, the ZCS/ZVS condition, power loss, actual inductance value, and other modeling information can be calculated and derived from the zero-cross point, dead-time current, and the response curve. However, to realize such functions, the requirement for high-speed ADC cannot be fulfilled in a single DSP control system, rendering the potential functions less feasible in field applications, regarding the constraint of the Nyquist-Shannon sampling theorem.

One reality behind the classic understanding of the Nyquist-Shannon sampling theorem is that the measured signal can be reconstructed with a lower sampling rate via a derivative from prior knowledge, which has recently received more and more attention. In [7], the converter model is leveraged to generate more sampling points from the original limited sampling

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points. In [8], the compressed sensing method is applied to gate-to-source voltage sampling. An interesting oscilloscope technique is implemented to realize a higher accuracy for periodic signals [9], where sampling points collected from several contiguous cycles in a periodic signal are combined to get high time-resolution results. As for power electronics applications, a repetitive feature can also be leveraged with much more flexibility. The switching event of power devices stimulates the power circuitry response, which is the basis of the discrete switching state analysis. Hence, in terms of power electronics circuitry, if the initial conditions and switching states in two time sections are the same, the circuitry responses should be no different, even though the two time sections are discontinuous and independent. One supporting example is that the gate-to-source voltage waveform is less different in several continuous cycles despite constantly changing the PWM duty cycle. However, considering the online sampling scenario for power electronics applications, the realization of limited computing resources and short execution time is the critical issue. Based on this feature, this letter presents a switching-event-dependent high-frequency current/voltage sampling and reconstruction method for a power conversion system. It should be noted that the proposed method is appropriate for signals with high-frequency components but with minimal variation cycle by cycle, where the high-frequency current or voltage in a dc–dc converter and the power device behavior at a switching instant are used as examples to study in this letter.

The rest of this letter is organized as follows. In Section II, the measurement circuitry for the proposed method is introduced. Then, the two sampling modes, i.e., basic mode and high-resolution (HR) mode, are presented and illustrated using examples. A step-by-step design process is given to apply this method from circuitry design to software implementation. A feasible and fast reconstruction approach with limited computing resources is proposed. The potential interference and noise issues are analyzed. Finally, experimental case studies are presented in Section III, i.e., the resonant current and driving voltage miller plateau in a series-resonant dual-active-bridge (SR-DAB) converter are online captured to validate the effectiveness of the proposed sampling method. Finally, the conclusion is summarized in Section IV.

II. Proposed Method

To illustrate the proposed sampling method, an SR-DAB converter is taken as an example where the resonant ac and gate-to-source voltage are sampled and digitized.

A. Sensing Circuitry Operation

The circuitry diagram for the proposed sampling method is shown in Fig. 2. First, the digital controller sends switching PWMs, i.e., $\mathrm{PWM_{sw}}$, to drive the SR-DAB converters. Two sampling modes (i.e., basic mode and HR mode) are designed to sample the resonant current I_{sr} and gate-to-source voltage V_{gs}, respectively. The resonant current I_{sr} is sampled by an internal ADC of the digital controller. The PWM signal $\mathrm{PWM_{trg\_bs}}$ is delayed from the switching PWM signal $\mathrm{PWM_{sw}}$ in basic mode. The delay time consists of a fixed delay time t_{ps_bs} and a varied delay time t_{add_bs}. And then, the $\mathrm{PWM_{trg\_bs}}$ is sent to trigger the sampling action of the internal ADC. In HR mode, the $\mathrm{PWM_{sw}}$ is delayed with a fixed delay time t_{ps_hr} to generate the signal $\mathrm{PWM_{trg\_hr0}}$. The $\mathrm{PWM_{trg\_hr0}}$ goes through a *retarder*, slowing down the slew rate to form V_{slope} and is then compared with a threshold voltage V_{th} from a PWM-based digital-analog converter (PWM-DAC). The V_{th} is determined by the duty cycle of a PWM signal $\mathrm{PWM_{cmp}}$. Hence the comparator output signal $\mathrm{PWM_{trg\_bs}}$ is delayed from $\mathrm{PWM_{trg\_hr}}$ with a varied delay time t_{add_bs}.

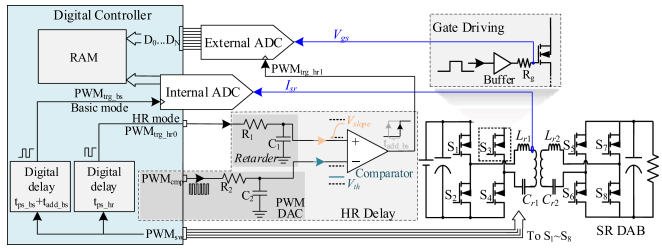

Fig. 2. Diagram of sampling circuitry of the proposed method.

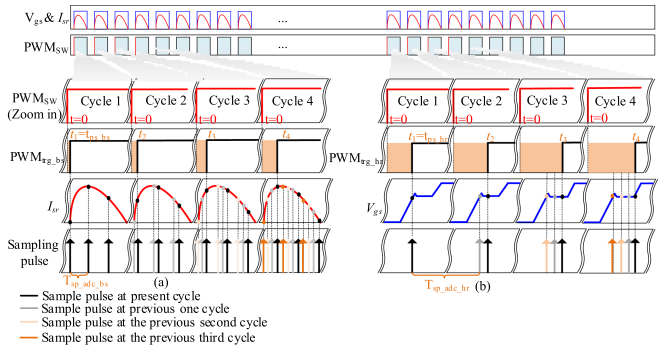

Fig. 3. Illustration of sampling process in basic mode and HR mode. (a) Basic mode for I_{sr}. (b) HR mode for V_{gs}.

B. Sampling Process

1) Basic Mode: Fig. 3 illustrates the sampling process of the proposed method, where the resonant current I_{sr} is sampled in basic mode, and the gate-to-source voltage signal V_{gs} is sampled in HR mode. The number of sampling points in one cycle is denoted as W. The number of cycles taken as one group is H. To simplify understanding, assume that a completed sampling and reconstruction operation contains four contiguous sampling periods, i.e., $\mathrm{H} = 4$. First, the instant when $\mathrm{PWM_{sw}}$ flips from low to high is set to $t = 0$ as a zero-time reference. In the basic mode, at cycle 1, $\mathrm{PWM_{trg\_bs}}$ flips at $t_1 = t_{ps\_bs}$, where t_{ps_bs} is used to locate the start point of the sampling window. When $\mathrm{PWM_{trg\_bs}}$ flips, the ADC begins a continuous sampling with the sampling time interval of internal ADC, denoted as $\mathrm{T_{sp\_adc\_bs}}$. Due to the limited sampling speed of the internal ADC, assume only three sampling points can locate within the sampling window ($W = 3$), which is not enough to reconstruct the profile of the resonant current I_{sr} accurately. At cycle 2, the

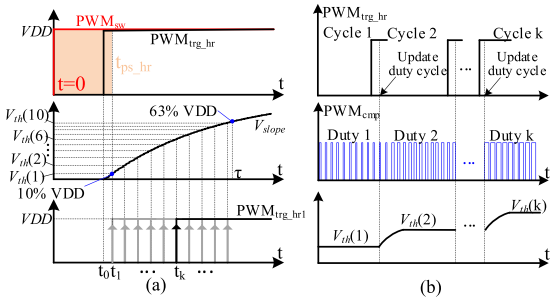

Fig. 4. Diagram of delay time generation procedure in HR mode.

$\mathrm{PWM_{sw}}$ flipping instant is still set to $t = 0$ as a time reference. A delay time t_{add_bs} is added to the original delay time t_{ps_bs}. The value of t_{add_bs} varies cycle by cycle. At cycle 2, $t_{add\_bs} = \mathrm{T_{sp\_adc\_bs}}/4$, and $\mathrm{PWM_{trg\_bs}}$ flips at $t_2 = t_{ps\_bs} + \mathrm{T_{sp\_adc\_bs}}/4$, hence there is an incremental delay time $\mathrm{T_{sp\_adc\_bs}}/4$. Then, the ADC executes the same sampling process, but three sample points are located at different positions in terms of a changed flipping time of $\mathrm{PWM_{trg\_bs}}$. At cycle 3, $\mathrm{PWM_{trg\_bs}}$ flips at $t_3 = t_{ps\_bs} + 2{\cdot}\mathrm{T_{sp\_adc\_bs}}/4$, and another three sampling points are obtained. At cycle 4, a similar process is conducted with a delay time $t_3 = t_{ps\_bs} + 3{\cdot}\mathrm{T_{sp\_adc\_bs}}/4$. Given the circuitry feature, the resonant current in the sampling window has the same curve in several contiguous cycles. Therefore, the 12 sampling points from 4 cycles can be equivalently taken as sampling points obtained from one cycle with a sampling time interval $\mathrm{T_{sp\_adc\_bs}}/4$. They can reconstruct I_{sr} by rearranging the sequence of the sampling points. It should be noted that in this case of basic mode, the flipping instant of $\mathrm{PWM_{trg\_bs}}$ has an added delay time of $\mathrm{T_{sp\_adc\_bs}}/4$ cycle by cycle, the minimum of which determines the equivalent sampling rate capability and is constrained by the clock frequency of the digital processor applied.

2) HR Mode: For applications that need higher sampling rates, the basic mode cannot support a very small time delay due to the limitation of digital clock frequency. Thus, an HR mode is designed to realize an ultra-high equivalent sampling rate. Fig. 3(b) illustrates the usage of HR mode where the Miller plateau of V_{gs} is measured. Since the signal duration of the Miller plateau is quite short, only one sampling point can be located in the sampling window at each cycle. A very short delay time should be added cycle by cycle to realize an interleaved sampling. Fig. 4(a) illustrates the short delay time generation process in HR mode. First, the rising edge of $\mathrm{PWM_{trg\_hr}}$ goes through the *retarder* in Fig. 2. The *retarder* can generate an RC step response V_{slope}, which can be expressed as follows:

$$\begin{cases} V_{\mathrm{slope}}(t) = \mathrm{VDD} \cdot [1 - e^{-\frac{1}{\tau}(t-t_0)}],\ t \geq t_0 \\ \tau = R_1 C_1 \end{cases} \tag{1}$$

where VDD is the power supply voltage value of the digital circuitry, and τ is the RC time constant. R_1 and C_1 are the resistor and capacitor of the *retarder* circuit, respectively. t_0 is the instant when $\mathrm{PWM_{trg\_hr}}$ flips. $V_{th}(k)$ is the voltage value of V_{th} at the cycle k generated from PWM DAC, which determines the delay time between $\mathrm{PWM_{trg\_hr0}}$ and $\mathrm{PWM_{trg\_hr1}}$ as

$$t_k = \ln\left(1 - \frac{V_{th}(k)}{\mathrm{VDD}}\right) R_1 C_1 + t_0. \tag{2}$$

The threshold voltages should be within 10% of $\mathrm{VDD}(V_{\mathrm{slope}}(\tau/10))$ to 63% of $\mathrm{VDD}(V_{\mathrm{slope}}(\tau))$ to avoid false triggering. Assume the required equivalent sample time is $\mathrm{T_{sp\_eq}}$ realized by signal reconstruction from a 10-cycle sampling. Because of the nonlinearity of V_{slope}, a nonuniform $V_{th}(k)$ is given as

$$V_{th}(k) = \mathrm{VDD} \cdot \left[1 - e^{-\frac{1}{\tau}(t_{ps} + (k-1)\mathrm{T_{sp\_eq}} - t_0)}\right],$$
$$\text{where } k = 1, 2, \ldots, 10. \tag{3}$$

Fig. 4(b) illustrates the specific operation process in HR mode. At cycle 1, $\mathrm{PWM_{cmp}}$ generates PWM with a designed duty cycle duty 1, filtered to $V_{th}(1)$ by the low-pass filter formed by R_1 and C_1. After sampling action is triggered, the PWM duty cycle should update immediately to ensure the next threshold voltage $V_{th}(2)$ is stable before the next rising edge of $\mathrm{PWM_{trg\_hr0}}$ arrives. To pursue a lower voltage ripple and shorter stable time on $V_{th}(k)$, a higher-order filter circuit like an *LC* filter or a HR DAC can replace the PWM DAC to provide the adjustable voltage $V_{th}(k)$.

C. Design Process

In this section, the design process of the proposed sampling method is described. First, the applicability of the desired sampling signal should be evaluated by checking whether the following conditions can be fulfilled.

1) The desired signal section should have a known time relationship with the switching time instant, but the time relationship has not to be a constant. For example, the gate-to-source voltage has a specific relationship with switching time, although the duty cycle and switching frequency may change. Generally, this condition is easily fulfilled in a power electronics circuit where the response is triggered by switching events.
2) The desired signal section should vary less in several contiguous cycles. Due to the high switching frequency from ten to hundreds of kilohertz in power converters, a steady process in a time scale of milliseconds can fulfill the requirement.
3) The real-time requirement for this signal acquisition can be compromised. The control, optimization, or monitoring is not necessarily updated cycle by cycle. For example, V_{gs} captured for power device lifetime online monitor is a suitable case to implement because taking tens of cycles to get one completed sampling result can be acceptable. Nevertheless, fault diagnosis applications may not be reasonable regarding the fast response time requirement.

Next, the target sample window with a duration $\mathrm{T_{signal}}$, the delay time to the switching instant t_{ps} for locating the sampling window, and the target sample interval $\mathrm{T_{sp\_eq}}$ should be identified according to a specific application. The $\mathrm{T_{sp\_eq}}$ is also the delay time added to the $\mathrm{PWM_{trg\_hr0}}$ cycle to cycle and

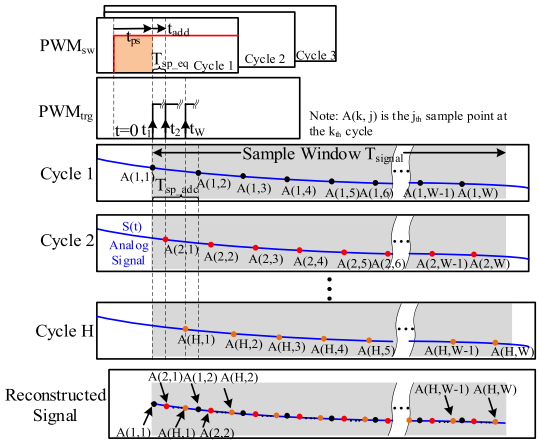

Fig. 5. Diagram of the general timing sequence for proposed sampling method.

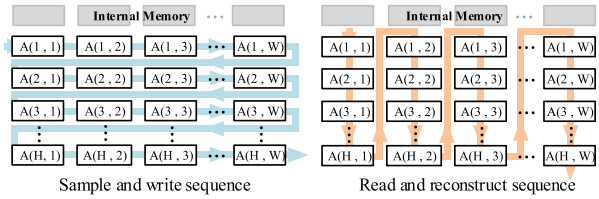

Fig. 6. Illustration of fast storage and reconstruction procedure.

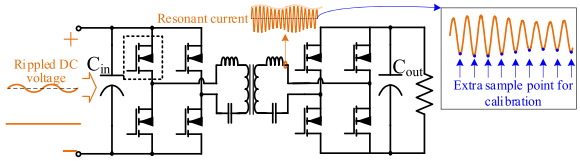

Fig. 7. Illustration of interference error mitigation approach.

determines the adoption of basic mode or HR mode as

$$\mathrm{T_{sp\_eq}} \le \frac{1}{f_{\mathrm{MPUCLK}}} \Rightarrow \text{HR Mode},$$
$$\mathrm{T_{sp\_eq}} > \frac{1}{f_{\mathrm{MPUCLK}}} \Rightarrow \text{Basic Mode} \tag{4}$$

where f_{MPUCLK} is the micro processor unit (MPU) clock frequency.

In basic mode, there is a tradeoff between the number of cycles used for reconstruction and the sampling speed of the ADC, as described in the following equation:

$$\mathrm{T_{sp\_eq}} = \frac{\mathrm{T_{sp\_adc\_bs}}}{\mathrm{H}}, \quad \mathrm{T_{sp\_adc\_bs}} = \frac{\mathrm{T_{signal}}}{\mathrm{W}} \tag{5}$$

where W is the number of sampling points in one cycle, and H is the number of cycles for one reconstruction. An extra expense on an ADC with a higher sampling speed (lower $\mathrm{T_{sp\_adc\_bs}}$) can bring a better real-time performance resulting from fewer cycles for reconstruction and vice versa.

In HR mode, since there is only one sampling point per cycle, the sampling window $\mathrm{T_{signal}}$ equals $\mathrm{W}\cdot\mathrm{T_{sp\_hr\_eq}}$, there is no special requirement for ADC sampling speed, but the main challenge in this mode is to add a delay time to $\mathrm{PWM_{trg\_hr0}}$ precisely cycle by cycle. To differentiate the threshold voltage $V_{th}(k)$ among cycles, only part of the V_{slope} can be leveraged, and a practical time range in the slope can be set from $\tau/10$ to τ. Therefore, the RC constant value selection should meet the following equation:

$$\frac{9\tau}{10} \ge (\mathrm{W}-1)\mathrm{T_{sp\_eq}}. \tag{6}$$

Finally, the signal sampling process is executed, and signal reconstruction is conducted subsequently. Fig. 5 shows the general signal sampling and reconstruction process of the proposed sampling method, where HR mode can be regarded as a particular case of $\mathrm{W} = 1$. The sampling points can be described as follows:

$$\begin{cases} \mathrm{A}(k,j) = \mathrm{S}[\mathrm{t_{ps}} + (k-1)\mathrm{T_{sp\_eq}} + (j-1)\cdot\mathrm{T_{sp}}], \\ k = 1\ldots\mathrm{H},\ j = 1\ldots\mathrm{W} \end{cases} \tag{7}$$

where S(t) is the function of the signal section. A(*k*,*j*) is the j_{th} sample point at the k_{th} cycle. Considering the digital storage structure and software realization, a simple and fast reconstruction approach is devised as shown in Fig. 6. First, a H×W size of memory is assigned for sampling result storage. In the sampling process, the sampling results are written to memory units horizontally with the original sampling sequence. For the reconstructing process, sampling points are read vertically from memory. Therefore, the reading sequence naturally follows the equivalent sampling sequence of the reconstructed signal with a sampling interval $\mathrm{T_{sp\_eq}}$. The memory can be refreshed every H-switching cycles to update the desired signal section continuously. Therefore, the reconstruction process does not add any extra calculation burden to the microprocessor. Furthermore, the reconstruction process matches well with the functionality of direct memory access in a microprocessor [10].

D. Noise and Interference Issue Discussion

Note that the main advantage of the proposed method is to realize a high-frequency waveform online sampling and digitalization with engineering applicable low-speed ADC. However, it has to acknowledge that there should be more considerations of measurement errors for the proposed sampling method. The white noise and interference are discussed in this part to clarify their influence on reconstruction.

For additive white noise in the time domain, the proposed method has the same performance as the conventional sampling method because the white noise is random, and hence there is no impact on noise level when sampling points from different cycles are reconstructed.

For the interference issue, taking DAB as an example, it is possible that an input or output dc voltage ripple coupled into a resonant current breaks the consistency among cycles as shown in Fig. 7. The resonant current has a periodic oscillation and may invalidate the proposed method.

Nevertheless, the impact of interference can be alleviated or neutralized. In the case of DAB resonant current, a well-designed dc voltage capacitor array can decouple each power stage on

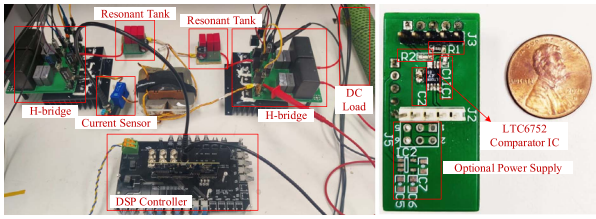

Fig. 8. Experimental prototype to test proposed sampling method. (a) SR-DAB setup. (b) Delay generator for HR mode.

TABLE I
EXPERIMENTAL PROTOTYPE CONFIGURATION

Circuitry Component(s)		Part number/ Parameters
SR-DAB circuitry	Resonant capacitance C_{r1}, C_{r2}	1 μF
	Resonant inductance L_{r1}, L_{r2}	37 μH
	Resonant frequency f_{sr}	26 kHz
	Switching frequency f_{sw}	26 kHz
Resonant current sampling	Sampling ADC	TMS320F28379 DSP internal 12bit ADC
	Sampling rate of ADC	600 kSPS
	Equivalent sampling rate	6 MSPS
	Number of sampling points in one cycle	16
	Number of cycles for reconstruction	10
V_{gs} sampling	Sampling ADC	LTC2236CUH 10bit ADC
	Retarder circuitry R_1, C_1	$R_1 = 500\ \Omega$, $C_1 = 100$ pF
	PWM DAC circuitry R_2, C_2	$R_2 = 100\ \Omega$, $C_2 = 0.1$ μF
	Real sampling rate	One sampling point per cycle
	Equivalent sampling rate	200 MSPS

a higher frequency band. Another method shown in Fig. 6 is adding one extra sampling point at the same cycle position to reflect the interference and calibrate sampling results via a digital approach.

III. EXPERIMENTAL VERIFICATION

Both the basic mode and HR mode of the proposed sampling method have been experimentally verified in a 120 V SR-DAB prototype as shown in Fig. 8(a). And the circuitry of the small delay time generator for HR mode is shown in Fig. 8(b). The critical circuitry and control parameters are summarized in Table I. To compare with conventional sampling and digitization solutions, the oscilloscope sampled data and adopted ADC sampled data in a single cycle are provided to represent the continuous sampling performance of ultra-high-speed ADC and general-purpose ADC, respectively.

First, the basic mode of the proposed sampling method is adopted to online sample the resonant current continuously and reconstruct one cycle current from sampling points in 10 cycles, as shown in Fig. 9. There are 16 sampling points in each cycle. Since some sampling points are outside the sampling window as a margin, there are 120 sampling points within the window. A TMS320F28379 DSP samples the resonant current with a sampling frequency of 600 kSPS. An equivalent sampling rate of 6 MSPS is realized by ten-cycle reconstruction. To compare the sampling performance straightforwardly, the resonant current is also recorded by an oscilloscope with a sampling frequency of

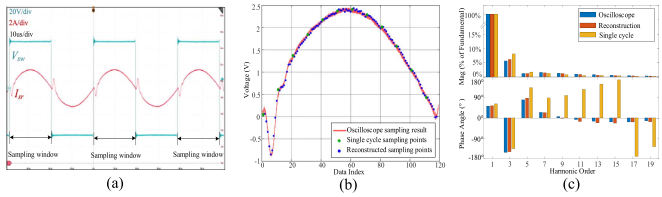

Fig. 9. Waveform and FFT of resonant current. (a) Oscilloscope sampling result. (b) Comparison of sampling results in time domain. (c) Comparison of sampling results in frequency domain.

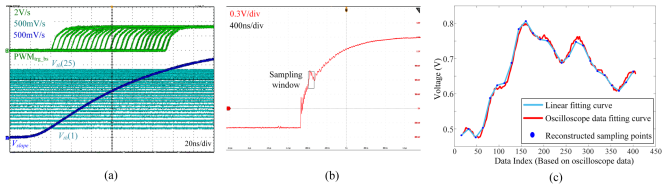

Fig. 10. Performance of HR mode for Miller plateau samplings. (a) Triggering signals in HR mode. (b) V_{gs} waveform at turn-ON transient sampled by oscilloscope. (c) Comparison of sampling results for V_{gs} at Miller plateau.

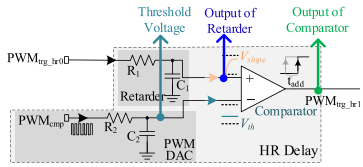

Fig. 11. Corresponding relationship of the curves in Fig. 10(a).

1 GSPS, and the FFT analysis is conducted on the oscilloscope results, reconstructed sampling results, and single-cycle sampling points. Note that a periodic continuation for the sampling result is applied to Fourier-series analysis. The resonant current within the sampling window is reconstructed from continuous sampling points in ten cycles. It can be seen that the sampling points in a single cycle are limited to reflect higher frequency components, especially the current distortion caused by the dead-time effect. While the current waveform reconstructed from ten cycle sampling points can well match oscilloscope data in time and frequency domains. The HR mode is also verified by reconstructing the Miller plateau from 25-cycle sampling points. Fig. 10(a) shows an overlapped waveform of 25 triggering signal waveforms from the circuitry in Fig. 11 of HR delay. It can be seen that the $\mathrm{PWM_{trg1}}$ rising edge has a 5 ns step incremental phase-shifting cycle to cycle with a threshold voltage $V_{th}(k)$ increased slower and slower to keep the triggering interval constant at 5 ns to realize an equivalent sampling rate up to 200 MSPS. Fig. 10(c) shows the Miller plateau from oscilloscope and HR mode samplings. It can be seen that reconstructed signals match well with oscilloscope sampling results.

IV. CONCLUSION

In this letter, a switching-event-dependent sampling method is proposed to reach a higher sampling frequency with lower-speed ADCs. For general applications, a digital controller in

basic mode can generate the trigging signal with incremental delay time. For applications demanding a sampling frequency higher than the digital controller clock, an HR mode is designed to generate a tiny delay time with a sampling circuitry. The design procedure is described in detail, and a fast reconstruction approach is covered to ensure feasibility. The potential noise issues are analyzed, and the corresponding depression solution is given. Finally, two experimental application examples on basic mode and HR mode are designed to present the potential of the proposed method on dc–dc converter online modeling and switching behavior monitoring. Future work could be expanded around these regions.

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