A Selective Common Mode Noise Mitigation Method Using Phase-Shifted Modulation for Four-Switch Buck–Boost DC/DC Converter

Yuning Bai, Sideng Hu, *Member, IEEE*, Zhi Yang, Mustafa Tahir, and Yongjian Zhi

***Abstract*—Wide bandgap power devices can work at higher switching frequencies compared to silicon competitors. It helps reduce the volume of passive components but brings more serious electromagnetic interference (EMI) noise issue. The increased noise filtering requirements may restrict the power density improvement. This article discusses the conducted EMI issue and noise filtering in the four-switch buck–boost (FSBB) dc/dc converter. The differential mode and common mode (CM) noise models embedded with noise source features are derived and analyzed. It is found that modifying the spectral distribution of the CM noise is a challenge when the duty cycles are fixed by voltage gain. Inspired by the CM model, a phase-shifted modulation method is proposed to achieve selective CM noise mitigation. The recommended operating range and the implementation process are presented. The theoretical modeling and the proposed method are verified through an FSBB converter with 48 V input and 100 kHz switching frequency, and experimental results validate that the proposed method can achieve 30% volume reduction of the CM filter.**

***Index Terms*—Common mode (CM) noise, four-switch buck–boost (FSBB) converter, phase shift, selective harmonic control.**

I. Introduction

NONISOLATED dc/dc converters are employed in a wide range of applications like consumer electronics and industrial and medical equipment [1]. Four-switch buck–boost (FSBB) converters are widely adopted in these fields, such as battery energy storage systems [2], photovoltaic application [3], microgrid [4], and universal serial bus power delivery [5]. The converter features in bidirectional energy transfer with either step-down or step-up voltage gain. Unlike the traditional buck–boost converter, the output voltage polarity is the same as the input. Thereby, it is also called noninverting buck–boost converter [6]. This topology can also be regarded as a basic unit and further combined into a multilevel converter to expand the voltage and power range [2], [7].

In recent years, with a large-scale commercial use of wide bandgap (WBG) devices, designers are inclined to develop FSBB converters with them [8], [9]. Compared with traditional silicon devices, WBG devices offer faster switching speeds and high switching frequency adaptability, with the potential to reduce the size of heat sinks and magnetic components. However, they also bring more serious conducted electromagnetic interference (EMI) challenges. The volume of EMI filters gets increased to meet the electromagnetic compatibility standard [10]. It could result in a much lower increase in power density than expected.

A lot of general methods have been published to suppress EMI noise and reduce the volume of filters. One idea is to replace the large passive filters with a smaller active EMI filter (AEF) [11]. In AEF, a noise detection circuit separates the EMI noise from the power circuits into low-voltage and low-current signals. Then, a signal processing circuit, which can be composed of operational amplifiers, generates compensation signals, and finally injects them back into the system [12]. Because the AEF only needs to deal with noises other than the full power, it can be made by small low-power circuits. For example, some AEFs take only printed circuit board and surface-mounted devices, which significantly reduces the size of the EMI filter [13].

Many control strategies are also developed, with the advantage of making fewer changes to the existing hardware. Considering that the noise is directly related to the power switching action, researchers try to select the proper switching sequence to reduce the noise voltage [14]. The idea is especially suitable for multiphase systems [15]. Because multiphase systems contain more control degrees of freedom, more control objectives can be achieved. By elaborately designing the switching sequence, the challenges of nonideal factors such as the dead time could also be overcome [16]. Some articles try to change the features of the carrier wave. By regulating the rising and falling order of the sawtooth waves, the switching noise can be mitigated [17].

Another kind of control strategy is the spread spectrum technology [18]. The method uses sinusoidal signal, chaotic signal, or other signals to modulate the switching frequency. As a result, the noise energy is dispersed to a wide frequency range, and the noise amplitude is cut down. Thus, the required filter's suppression ability, usually described by the insertion loss

Manuscript received 17 August 2022; revised 7 November 2022 and 4 January 2023; accepted 18 February 2023. Date of publication 22 February 2023; date of current version 20 April 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 52177199 and in part by the Zhejiang Provincial Natural Science Foundation of China under Grant LGG22E070013. Recommended for publication by Associate Editor Y. Siwakoti. *(Corresponding author: Sideng Hu.)*

Yuning Bai, Sideng Hu, Zhi Yang, and Mustafa Tahir are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: whyorwhnt@zju.edu.cn; husideng@zju.edu.cn; 11910100@zju.edu.cn; mustafatahir@zju.edu.cn).

Yongjian Zhi is with the CRRC Zhuzhou Institute Company Ltd., Zhuzhou 412001, China (e-mail: zhiyj@csrzic.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3247764.

Digital Object Identifier 10.1109/TPEL.2023.3247764

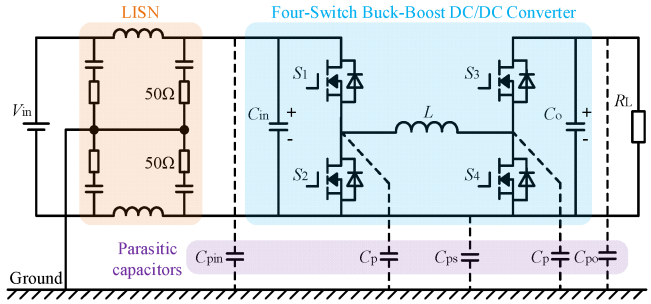

Fig. 1. Circuit diagram of the FSBB DC/DC converter system with parasitic capacitors.

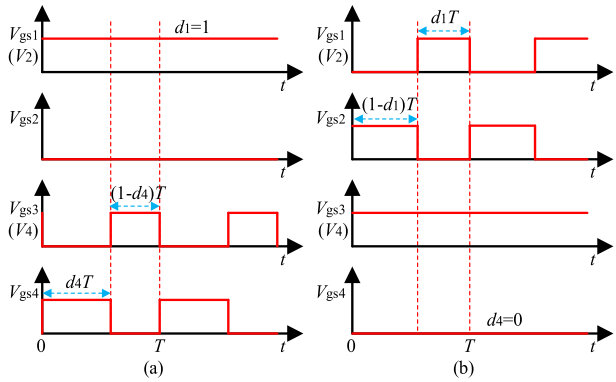

Fig. 2. Drive signals of S_1–S_4 in the conventional method. (a) Boost mode. (b) Buck mode.

(IL), is reduced. Designers can meet their needs with smaller components. The challenge of this scheme for dc/dc converter is the increasing output voltage ripple due to the changing switching frequency. Consequently, ample attention is required to design the output capacitor [19].

Noted that the high frequency brought by WBG devices not only leads to more serious noise but also provides opportunities for sophisticated design. By careful design of shielding, device integration and optimized placement, designers may significantly reduce the filter's volume [20], [21].

The above general approaches all can be applied to FSBB converters [22]. However, reducing EMI by using the converter's characteristics itself is still an open research question [23]. Besides, there is also a lack of noise models to guide the early design of filters. The motivation of this study is to develop a specialized method to mitigate conducted EMI and reduce the volume of the filter. The method is compatible with the above general schemes and can be used together to further improve performance. It can also be easily extended to multilevel structures. The article's contributions are summarized as follows.

1) The conducted EMI noise model of the FSBB converter is derived. The models can characterize noise sources and inspire the development of noise suppression strategies.
2) A common mode (CM) noise mitigation method for specified noise is proposed. The EMI noise on the selected harmonic order can be suppressed. Experiments show that it enables volume reduction of the CM filter.

The rest of this article is organized as follows. The basic working principle of the FSBB converter is introduced in Section II. Section III presents the noise models and the challenges faced by conventional modulation methods are briefly analyzed. Section IV presents the details of the proposed noise mitigation method. Some comments and the analysis for reducing the filter's volume are presented in Section V. The experimental verification is given in Section VI. Finally, Section VII concludes the article.

II. Basic Operation Principle of FSBB Converter

A. System's Structure and Converter's Topology

The FSBB converter system is shown in Fig. 1. Four power switches S_1–S_4 form two half-bridge structures and there is a power inductor L between them. The converter also includes input capacitor $C_{\rm in}$ and output capacitor $C_{\rm o}$. There are parasitic capacitors between each part of the converter and the reference ground [24], and the capacitances are generally hundreds of picofarads, including the input port to the ground capacitor $C_{\rm pin}$, the negative dc bus to the ground capacitor $C_{\rm ps}$, and the output port and load to the ground capacitor $C_{\rm po}$. To simplify the analysis, the parasitic capacitances at the midpoint of the two half-bridges are considered to be the same value, $C_{\rm p}$.

The conducted EMI noise can be captured by the line impedance stabilization network (LISN). Then, the signal is sent to an EMI receiver for measurement and recording. LISN consists of two fixed 50 Ω resistors and passive components. According to the application areas of the device under test, the values of these components need to be set according to corresponding standards [25].

B. Basic Operation Principle

The voltage gain G of the converter is defined as the ratio of output voltage $V_{\rm o}$ to input voltage $V_{\rm in}$. It can be controlled by the duty cycle d_1 and d_4 [26]

$$G = \frac{V_{\rm o}}{V_{\rm in}} = \frac{d_1}{1-d_4} \tag{1}$$

where d_1 is the duty cycle of S_1 and d_4 is for S_4. When $V_{\rm in}$ is lower than $V_{\rm o}$, the converter operates in boost mode, whereas if $V_{\rm in}$ is higher, it works in buck mode. Fig. 2 shows the driving signals $V_{\rm gs1}$–$V_{\rm gs4}$ of each switch, and T represents the duration of a switching cycle. Ideally, the logic of these drive signals would also describe the logic of the switch's withstand voltage. For example, when $V_{\rm gs1}$ is high, S_1 will turn ON. Then, the withstand voltage of S_2, namely V_2, has the same shape as $V_{\rm gs1}$, and the same is true for V_4.

C. Duty Cycle Limit

In practical applications, nonideal factors would limit the duty cycle generation, such as the nonzero rise and fall time of switching devices and the dead time for the half-bridge structure. For an FSBB converter, the duty cycles should satisfy

$$d_1, d_4 \in \{0,\ 1, [d_{\min}, d_{\max}]\} \tag{2}$$

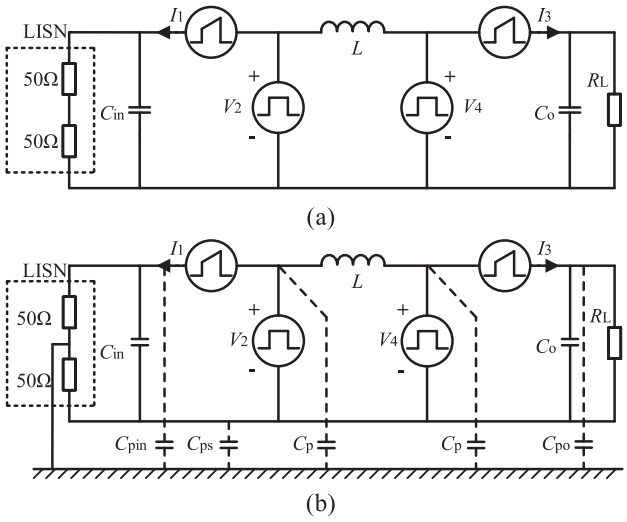

Fig. 3. FSBB system's equivalent circuits. (a) For DM noise modeling. (b) For CM noise modeling.

where $d_{\min}$ represents the exact minimum nonzero duty cycle that the converter can output, and its value depends on the specific hardware design. $d_{\max} = 1–d_{\min}$. For early-stage studies, a harsh value, $d_{\min} = 0.1$, is adopted by many researchers [26], [27].

III. Derived Noise Models

The conducted EMI noise of dc/dc converters can be separated into two components, which need to be analyzed separately and attenuated by corresponding filters [28]. The first component is called differential mode (DM) noise, and it flows through the positive and negative power lines. The second one is called CM noise, which propagates between the two power lines and the reference ground. The parasitic capacitors shown in Fig. 1 are the main path of CM noise propagation.

A. Modeling DM Noise

The target of noise modeling is to estimate and analyze the voltage signals to be collected by the LISN. Substitution theory is used to derive the noise model. As shown in Fig. 3(a), S_1 and S_3 are replaced by current sources I_1 and I_3, respectively, whereas S_2 and S_4 are replaced by voltage sources V_2 and V_4 [28]. The waveforms of these sources are completely consistent with the current or voltage of these switches. The DM noise flows through the positive and negative power lines, so there are no parasitic capacitors in the equivalent circuit.

Next, superposition theory is used to analyze the contribution of each source to the DM noise. The final DM noise model is derived as Fig. 4(a). The noise voltage collected by LISN is

$$V_{\mathrm{dm}}(\omega) = \frac{I_1(\omega)}{j\omega C_{\mathrm{in}} + \frac{1}{100}}. \tag{3}$$

According to the DM noise model in Fig. 4(a) and (3), some characteristics can be summarized. First, the dominant factor of DM noise is the current I_1, and it is independent of the

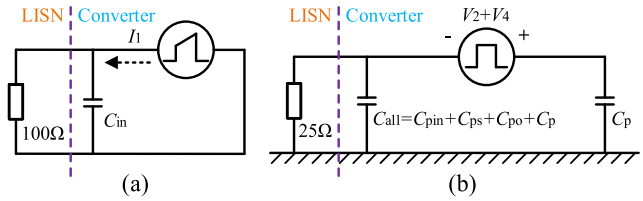

Fig. 4. (a) DM noise model. (b) CM noise model.

modulation methods. Even if other strategies outside the scope of this article are used [27], the conclusion is still applicable. In an early design stage, the time-domain and frequency-domain information of I_1 can be easily obtained through simulation. Then, DM noise can be obtained by (3) to help design DM filters.

Second, increasing C_{in} helps to reduce DM EMI. Designers can make a compromise between the noise and the capacitor's volume. On the other hand, this capacitance may be hundreds of microfarads. It makes the input impedance only a few ohms when considering DM noise. Designers need to choose a suitable filter structure according to the feature [29]. For example, a DM inductor is more effective than an X-capacitor.

B. Modeling CM Noise

Following the same steps as before, the CM equivalent circuit can be represented as Fig. 3(b). Further, the CM model is derived as Fig. 4(b). The CM noise voltage collected by LISN is

$$V_{\mathrm{cm}}(\omega) = \frac{25C_{\mathrm{all}}\left(V_2(\omega) + V_4(\omega)\right)}{25C_{\mathrm{all}} + C_{\mathrm{p}}\left(25 + j\omega C_{\mathrm{all}}\right)} \tag{4}$$

where $C_{\mathrm{all}} = C_{\mathrm{pin}} + C_{\mathrm{ps}} + C_{\mathrm{po}} + C_{\mathrm{p}}$.

It is seen that the spectrum of CM noise is determined by the sum of V_2 and V_4. Since C_{all} is usually only hundred picofarads, the input port shows high impedance when considering CM noise. A suitable filter structure needs to be selected, such as adding a Y-capacitor.

Special attention shall be paid to C_{po}. Although it is located at the converter's output port or the load side, its location in the model is parallel with the LISN. It means that adding a Y-capacitor at the output port is beneficial to reduce the CM EMI for the input side.

C. Challenge of Conventional Modulation Method

As discussed in Section II-B, in the conventional modulation method, V_2 and V_4 would not switch simultaneously. Therefore, the ac component in voltage that generates CM noise can be expressed as Fig. 5. In this figure, A is the voltage amplitude, which is equal to V_{in} in the buck mode and V_{o} in the boost mode. Similarly, D is the duty cycle and equals to d_1 or $(1–d_4)$. T represents the switching period, and fs is the control frequency, which meets $fs = 1/T$. n represents the multiple of control frequency and also means the order of switching harmonics. In the frequency domain, the amplitude of each harmonic can

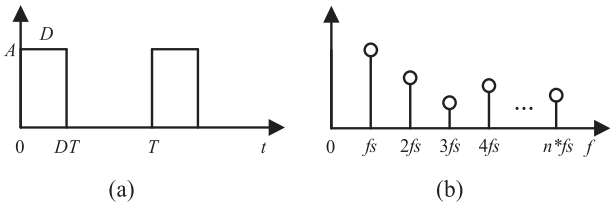

Fig. 5. Voltage waveforms in conventional modulation method. (a) Time domain. (b) Frequency domain.

be obtained by the Fourier series

$$|c_n| = \left| \frac{2}{T} \int_0^{DT} A e^{-jn\omega t} dt \right| = \left| \frac{A}{jn\pi} \left(1 - e^{-2jn\pi D}\right) \right| \tag{5}$$

where $n \geq 2$.

In the conventional method, there is only one control degree of freedom, i.e., the duty cycle. It is used to adjust the only control target, usually the output voltage. A fixed voltage target leads to a determined duty cycle D and further generates a fixed noise spectrum by (5). The noise filter has to be designed accordingly [25]. In general, there are limited methods to change the CM spectrum distribution, which creates obstacles for the joint optimization of software and hardware to further improve power density. In this article, a new solution is proposed, which is presented in the following section.

IV. Proposed CM Noise Mitigation Method

The phase-shifted modulation is attractive for the controller design. Some published researches succeed in soft switching [9], [30], and succeed in reducing the current stress of components [31]. In this section, a phase-shifted modulation method is proposed to modify the spectrum distribution of CM noise. An additional control degree of freedom, the phase shift ratio, is introduced to corporate with the conventional duty cycle. Thereby, with the output voltage regulation, another control target can be set to minimize the CM voltage at a selected frequency. The frequency is recommended to be set as the first harmonic entering the conducted EMI test range, which is 150 kHz–30 MHz in this article. This study will show that the proposed method is helpful to reduce the volume of CM filters.

A. Phase-Shifted Modulation

Fig. 6 shows the schematic diagram of the proposed modulation method. The phase shift ratio k is the first control degree of freedom. It is defined as the ratio of the delay time between V_{gs4} and V_{gs1} to the whole control cycle T, and $k \in [0, 1]$. d_1 is regulated as the second control degree of freedom. At this time, another duty cycle signal d_4 should be set according to (1) to ensure a controlled output voltage.

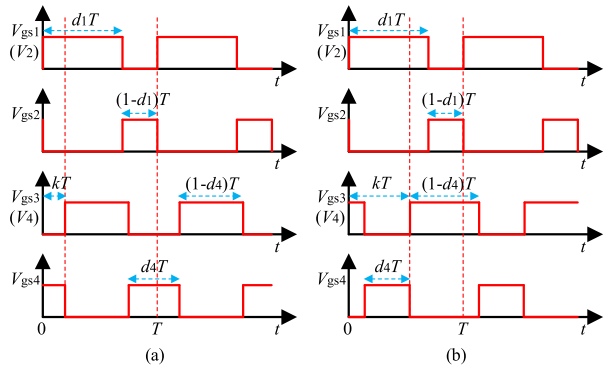

Fig. 6. Drive signals of S_1–S_4 in the proposed method. The definition of phase shift ratio k in this diagram is applicable to both buck mode and boost mode.

Based on (4), the CM noise is determined by the sum of V_2 and V_4. When the phase-shifted modulation is adopted, the spectrum of V_2 can be obtained by the Fourier series

$$C_{n,V2}\ (d_1) = \frac{2}{T} \int_0^{d_1 T} V_{\text{in}} e^{-jn\omega t} \mathrm{d}t \tag{6}$$

where the harmonic number meets $n \geq 2$.

Similarly, the spectrum of V_4 can be obtained. When $0 \leq k < d_4$, the following holds:

$$C_{n,V4}\ (d_1, k) = \frac{2}{T} \int_{kT}^{kT+(1-d_4)T} V_{\text{in}} G e^{-jn\omega t} \mathrm{d}t. \tag{7}$$

When $d_4 \leq k < 1$, the following holds:

$$C_{n,V4}\ (d_1, k) = \frac{2}{T} \left(\int_0^{kT-d_4T} V_{\text{in}} G e^{-jn\omega t} \mathrm{d}t + \int_{kT}^{T} V_{\text{in}} G e^{-jn\omega t} \mathrm{d}t \right). \tag{8}$$

Then, the CM noise can be calculated as (9) shown at the bottom of this page. If the harmonic order n and voltage gain G are given, the CM noise is determined by d_1 and k. It is easy to prove that in the definition domain, the function satisfies

$$C_{n,G}\ (d_1, k) = C_{n,G}\ \left(d_1, k + \frac{1}{n}\right). \tag{10}$$

It shows that (9) is a periodic function.

Fig. 7 depicts the CM voltage amplitude. The function value here is normalized based on V_{in}. When different combinations of d_1 and k are set, the amplitude of CM voltage can be adjusted within a range, and it is also possible to mitigate it to close to zero. Namely, suppressing a selected CM noise is equivalent to solving the following optimization problem:

$$\min_{d_1 \in [d_{\min}, d_{\max}],\ k \in [0,1]} \left| C_{n,G}\ (d_1, k) \right|. \tag{11}$$

$$C_{n,G}\ (d_1, k) = \begin{cases} -\frac{jV_{\text{in}}}{n\pi} \left(1 - e^{-2jn\pi d_1} - G\left(-1 + e^{\frac{-2jn\pi d_1}{G}}\right) e^{-2jn\pi k}\right), 0 \leq k < d_4 \\ -\frac{jV_{\text{in}}}{n\pi} \left(1 - e^{-2jn\pi d_1} + G\left(1 - e^{-2jn\pi} + e^{-2jn\pi k} - e^{\frac{-2jn\pi(d_1 + G(-1+k))}{G}}\right)\right), d_4 \leq k < 1 \end{cases} \tag{9}$$

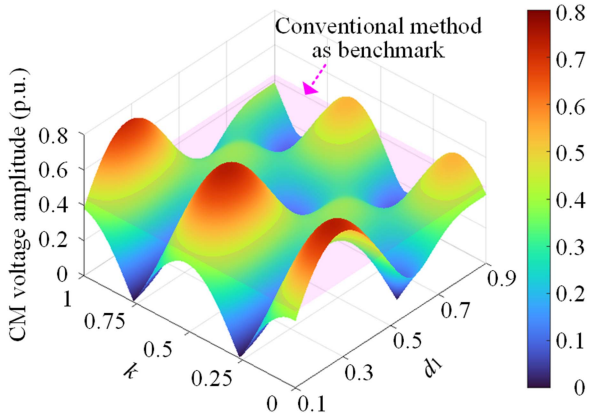

Fig. 7. Amplitude of CM voltage (second harmonic, $n = 2$) when voltage gain $G = 1.4$.

B. Solving Optimization Problems

The optimization problem (11) is very complex, and finding its analytical solution is a severe challenge. In practical application, a numerical solution could meet the needs of the control algorithm [32]. When a high-performance controller is adopted, the problem could be solved online by referring to some leading research [33], [34]. When a low-cost controller is used, it is easier to implement the real-time control based on the look-up table (LUT), which is built by an offline solution.

This study uses the differential evolution (DE) algorithm to obtain the numerical solution of the optimization problem offline [35]. Like some well-known optimization algorithms, DE is a random search algorithm based on swarm intelligence.

The algorithm starts with initializing a population containing N_{P} individuals and each of them represents a possible numerical solution of d_1 and k. Their coordinates are randomly generated and located in the two-dimensional solution space

$$\boldsymbol{x}_{i,w} = \left(\mathrm{Rand}\left[d_{\min}, d_{\max}\right], \mathrm{Rand}\left[0,1\right]\right) \tag{12}$$

where i means the number of individuals in the population, $i = 1, 2, \ldots, N_{\mathrm{P}}$, and w represents the rounds of evolution, $w \in [0, N_{\max}]$. $N_{\max}$ is the maximum number of iterations. Rand means to generate a random number within the parameter's range.

Next, the algorithm will start searching for the minimum value of the optimization problem (11). Specifically, the algorithm will iteratively update the coordinates of all individuals. The update contains three steps. The first step is called Mutation. The so-called mutant vector is obtained by

$$\boldsymbol{v}_{i,w+1} = \boldsymbol{x}_{\mathrm{best},w} + F\left(\boldsymbol{x}_{r1,w} - \boldsymbol{x}_{r2,w}\right) \tag{13}$$

where $\boldsymbol{x}_{\mathrm{best},w}$ is the coordinate that minimizes (11) in the wth generation. F is a parameter called mutation factor, and r_1 and r_2 are the numbers of two random individuals.

TABLE I
PARAMETERS OF DE ALGORITHM

Parameters	Value
Fitness function	(11)
Algorithm	DE/best/1/bin
Population size (N_{P})	100
Iteration number ($N_{\max}$)	300
Mutation factor (F)	0.6
Cross over rate (CR)	0.2

The second step is called Crossover, and the so-called trial vector is obtained through

$$\boldsymbol{u}_{j,i,w+1} = \begin{cases} \boldsymbol{v}_{j,i,w+1}, & \text{if } j = r_i \text{ or } \mathrm{Rand}\left[0,1\right] \le CR \\ \boldsymbol{x}_{j,i,w}, & \text{otherwise} \end{cases} \tag{14}$$

where j is a certain dimension of the coordinate, $j = 1$ or 2, and $r_i = 1$ or 2, randomly. CR is a parameter called crossover rate. This step aims to introduce new members to the population and expand the search range.

The third step is called Selection, according to

$$\boldsymbol{x}_{i,w+1} = \begin{cases} \boldsymbol{u}_{i,w+1}, & \text{if } f\left(\boldsymbol{u}_{i,w+1}\right) < f\left(\boldsymbol{x}_{i,w}\right) \\ \boldsymbol{x}_{i,w}, & \text{otherwise} \end{cases} \tag{15}$$

where $f()$ means substituting the coordinates into (11) to calculate its value. This step updates individuals, which makes the population constantly close to the searching target, namely the minimum value.

The algorithm parameters are presented in Table I. After iterating $N_{\max}$ times, $\boldsymbol{x}_{\mathrm{best},w}$ in the last round represents the numerical solution, including duty cycle d_1 and phase shift ratio k. When the solution is applied to the system, the selected nth CM noise will be mitigated. Noted that the optimization problem (11) may have multiple solutions. Therefore, for each selected n and G, DE needs to be executed repeatedly to ensure that there is no omission. The tradeoff among these results will be discussed in the following section.

C. Tradeoff Among Optimization Results

Solving (11) may obtain multiple solutions. For example, there may be six solutions for Fig. 7. According to (10), some of them are periodic, and this feature will be more pronounced when n is set with a large number. All of these solutions can suppress the selected CM noise but have different effects on the other converter performance. Different selection principles can be set according to the individual requirements. And finally, one of them can be chosen to regulate the FSBB system.

In this study, the inductor current ripple is taken as a criterion. The numerical solution leading to lower ripple is preferred to minimize magnetic losses.

When considering the position relationship of the driving signals, there are eight cases, which are summarized in Fig. 8. Different pulse distributions produce various inductor current

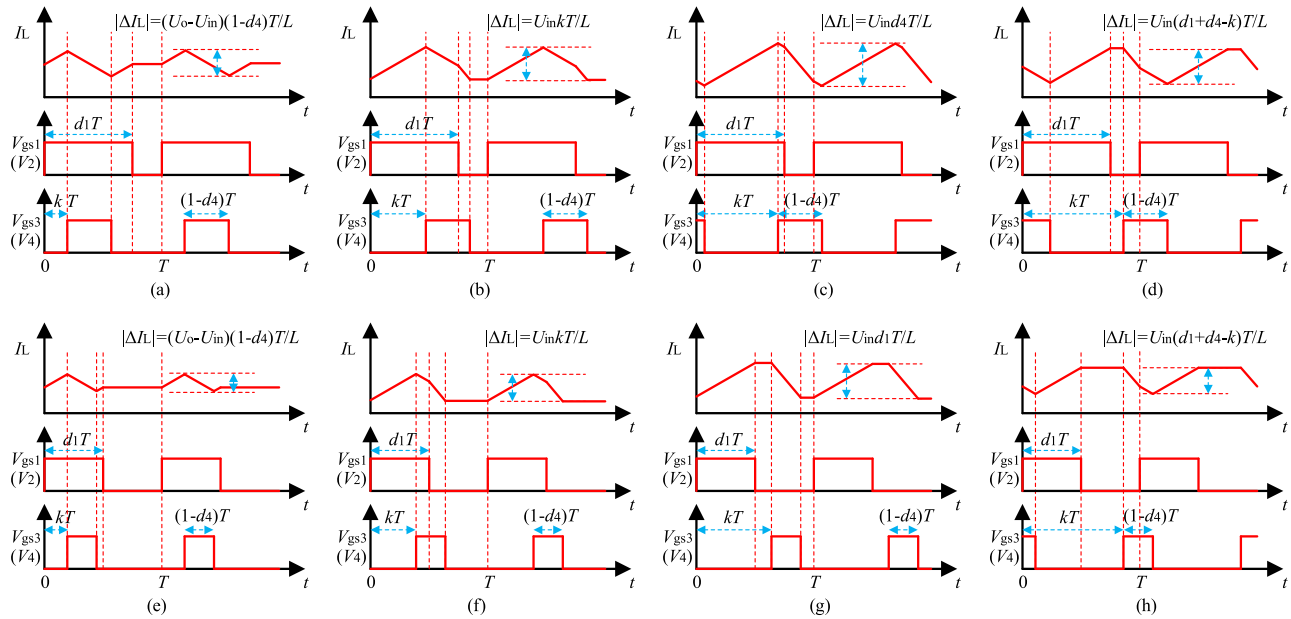

Fig. 8. Drive signals and inductor current waveforms in different solution space regions. (a) I: $d_1 > d_4$ and $0 <= k < d_1 + d_4 - 1$. (b) II: $d_1 > d_4$ and $d_1 + d_4 - 1 <= k < d_4$. (c) III: $d_1 > d_4$ and $d_4 <= k < d_1$. (d) IV: $d_1 > d_4$ and $d_1 <= k < 1$. (e) V: $d_1 < d_4$ and $0 <= k < d_1 + d_4 - 1$. (f) VI: $d_1 < d_4$ and $d_1 + d_4 - 1 <= k < d_1$. (g) VII: $d_1 < d_4$ and $d_1 <= k < d_4$. (h) VIII: $d_1 < d_4$ and $d_4 <= k < 1$.

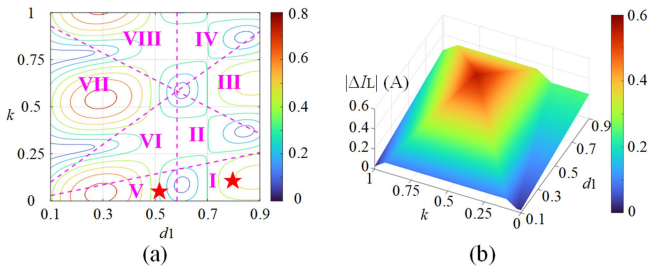

Fig. 9. (a) Solution space is divided according to the characteristics of inductor current ripple, and preferred regions are marked with stars. (b) Amplitude of inductor current ripple.

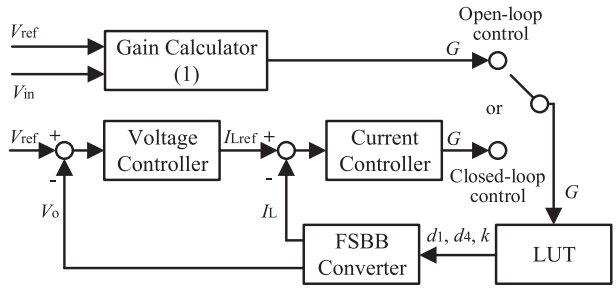

Fig. 10. Structure of the LUT-based control system.

characteristics, and the formulas of current ripple, $|\Delta I_{\mathrm{L}}|$, are marked in the figure. Their corresponding region in the solution space is shown in Fig. 9(a). Fig. 9(a) shows the contour map of CM voltage, and its parameters are the same as in Fig. 7. The current ripple is further calculated and shown in Fig. 9(b). The ripple in Regions I and V is lower. Therefore, the solutions in these regions will be taken as the final optimization results, whereas the others will be discarded.

D. LUT-Based Control System

The mitigation of CM noise with a fixed voltage gain is discussed before. And this section describes how this method is applied to a real-time control system with variable gain. The system structure is shown in Fig. 10. In this figure, V_{ref} is the output reference voltage, I_{L} is the inductor current, and I_{Lref} is its reference value.

The proposed method can be applied to the open-loop control or the closed-loop control. An LUT is used to convert the gain G to the duty cycle d_1 and phase shift ratio k. When the open-loop control is used, the gain can be calculated by (1) directly. When the closed-loop control is adopted, the current controller outputs voltage gains instead of duty cycles, which is different from the conventional control method. The controllers can adopt the proportional–integral regulator. Its design and tuning methods with voltage gain output can be found in [36].

During the real-time control, the input and output voltage may change. The voltage gain is various, and its range is $G \in [G_{\min}, G_{\max}]$. $G_{\min}$ is the minimum gain and $G_{\max}$ is the maximum value. They can be calculated by

$$\begin{cases} G_{\min} = \dfrac{V_{\mathrm{out,\ min}}}{V_{\mathrm{in,\ max}}} \\ G_{\max} = \dfrac{V_{\mathrm{out,\ max}}}{V_{\mathrm{in,\ min}}} \end{cases} \tag{16}$$

where $V_{\mathrm{in,max}}$ and $V_{\mathrm{in,min}}$ are the maximum and minimum input voltage of the converter, and $V_{\mathrm{out,max}}$ and $V_{\mathrm{out,min}}$ are the

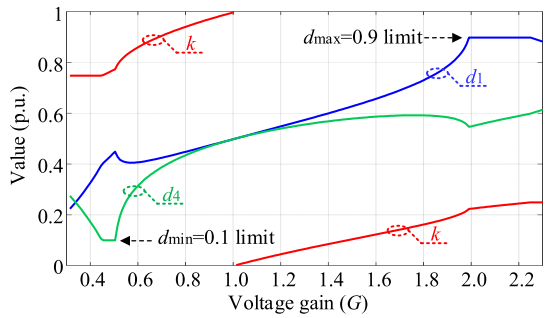

Fig. 11. LUT to mitigate the second-order CM noise.

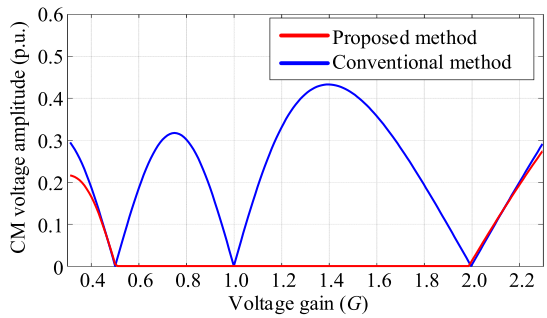

Fig. 12. Effect of the proposed method in second-order CM voltage mitigation.

maximum and minimum output voltage. For each G in this range, the optimization result of (11) needs to be obtained. Finally, all the results can be summarized into an LUT, which covers all voltage gain range. In order to obtain the continuous and smooth regulation capability, the LUT should have sufficient resolution. Therefore, the step G_{step} in the LUT should be small enough. In this study, $G_{\text{step}} = 0.01$.

Fig. 11 shows the LUT when mitigating the second-order CM noise, namely $n = 2$. When $G \in [0.51, 1.99]$, each parameter changes smoothly. Outside this range, d_1 or d_4 will touch the available duty cycle limit introduced in Section II-C, and its value will saturate.

E. Recommended Operating Range

Fig. 12 compares the amplitude of the CM voltage, namely $|V_2+V_4|$, with different modulation methods. The conventional one is calculated by (5), whereas the proposed one is by the function value of (11). The CM voltage of the conventional method will reach the maximum value around $G = 1.4$. As long as the CM filter is designed according to this point, it can provide sufficient suppression capability within the whole voltage range. For the proposed method, in the range of $G \in [0.51, 1.99]$, the scheme can significantly mitigate the CM voltage to close to zero. The mitigation helps to reduce the demand for filter's suppression capability and reduce its volume.

Comparing Figs. 11 and 12, when the duty cycle is saturated, the proposed method will no longer have advantages. That is, for $n = 2$,$G \in [0.51, 1.99]$ is the recommended operating range. Empirically, the larger the n, the longer the range. Table II summarizes some examples of recommended operation points. If a longer range is needed, it will be helpful to allow a relaxed $d_{\min}$ during the hardware design.

Note that Table II only lists examples that help reduce the filter's volume, and the application scenarios of the proposed method are not limited to it. For example, when a system is sensitive to the noise of a certain frequency, the proposed method can also be used to reduce the interference. At this time, f_s and n could be set as required.

TABLE II
EXAMPLES OF RECOMMENDED OPERATING RANGE

Switching frequency (f_s)	Recommended noise order (n)	Recommended gain range ($[G_{\min}, G_{\max}]$)
75 kHz $\le f_s <$ 150 kHz	2	[0.51, 1.99]
50 kHz $\le f_s <$ 75 kHz	3	[0.34, 2.96]
37.5 kHz $\le f_s <$ 50 kHz	4	[0.26, 3.90]
…	…	…

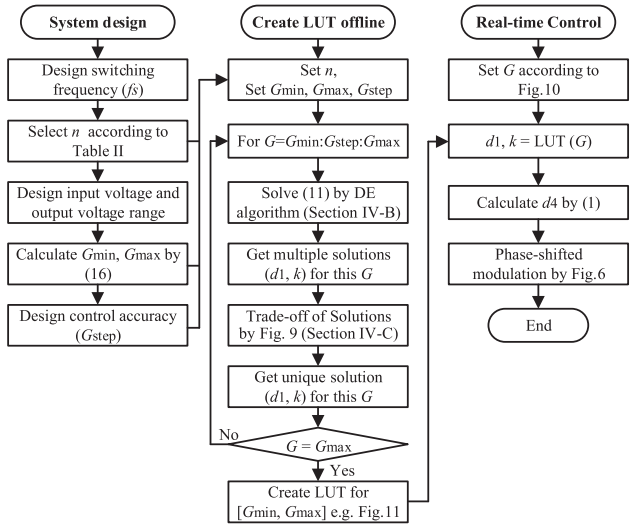

Fig. 13. Overall flowchart of the proposed method.

F. Implementation Flowchart

Fig. 13 shows the implementation flowchart of the proposed phase-shifted modulation method. The creation of LUT could be finished by a computer offline. A smaller G_{step} can achieve finer output voltage control, but it will be more time-consuming.

The real-time control is implemented by the controller of FSBB, such as a digital signal processor (DSP). Because d_1 and k contain a long decimal part, the processor with a higher clock resolution is recommended to help improve the accuracy of pulse position.

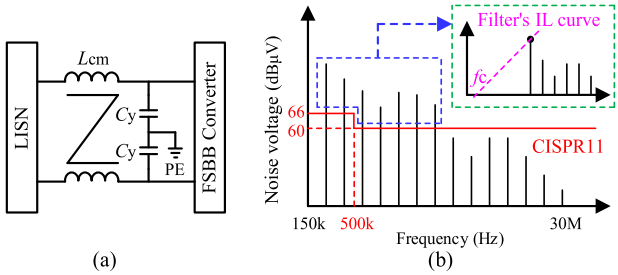

Fig. 14. (a) Structure of CM EMI filters. (b) Determination of filter's IL curve and corner frequency.

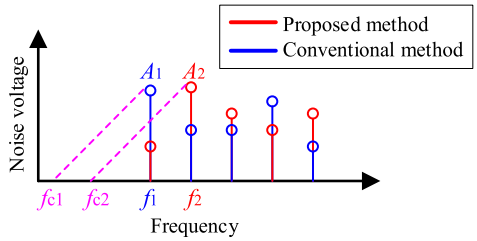

Fig. 15. EMI noise spectrums and the required corner frequency.

V. Discussion on the Proposed Method

A. Basic CM EMI Filters Design Method

Passive filters composed of CM inductors and Y-capacitors are commonly used to suppress CM EMI noise. The design process is reviewed here. Fig. 14(a) presents the structure of the one-stage CM filter. It can be cascaded to form a multistage filter. To simplify the analysis, this article only discusses the one-stage filter, but the conclusion can be easily extended to multistage structure.

The first step is to find the required IL. IL is used to describe the filter's performance to suppress noises, and it can be calculated by

$$IL = 10 \cdot \log\left(\frac{V_1}{V_2}\right) \tag{17}$$

where V_1 is the voltage on the LISN before the filter is installed, and V_2 is the voltage after installation. Fig. 14(b) shows the original noise of the converter, i.e., V_1. The CISPR11 standard limit can be regarded as the target of noise suppression, i.e., V_2. Therefore, the noise exceeding the limit, which is enclosed in the blue dotted box, needs to be suppressed by the filter.

The second step is to determine the corner frequency f_c of the filter. As shown in the green dotted box in Fig. 14(b), the IL of one-stage filter is a line with a slope of 40 dB/dec in the frequency domain. The line needs to be shifted from left to right along the X-axis until it first contacts the excess noise spectrum. At this time, it can be ensured that the IL provided by the filter is sufficient to meet the standard. And the intersection of the line and the X-axis is the filter's f_c.

The third step is to determine the inductance and capacitance, which meet the following relationship:

$$f_c = \frac{1}{2\pi\sqrt{L_{cm}C_y}} \tag{18}$$

where L_{cm} is the CM inductance and C_y is the Y-capacitance. C_y is determined by the leakage current limit in CISPR11 standard. Then, L_{cm} could be calculated according to (18). Obviously, higher f_c means lower C_y and L_{cm}, as well as smaller filter volume.

B. Benefits of Selective CM Noise Mitigation

The proposed method in this article can mitigate a selected CM noise, and it is recommended to select the first appearing peak that enters the EMI test range. This section discusses the benefits of this strategy for reducing the L_{cm}.

A noise spectrum of the conventional method is shown in Fig. 15. The amplitude of the first main noise to be suppressed is A_1 at the frequency f_1. According to the previous discussion, a filter with a corner frequency f_{c1} is required. After the proposed method is adopted, the noise energy at f_1 is mitigated, and the energy is allocated to a higher frequency. The noise at f_2 rises to A_2, and a filter with a corner frequency of f_{c2} is required. Then, the following formula holds:

$$\begin{cases} f_{c1} = f_1 \cdot 10^{-\frac{A_1}{40}} = nf_s \cdot 10^{-\frac{A_1}{40}} \\ f_{c2} = f_2 \cdot 10^{-\frac{A_2}{40}} = (n+1)\ f_s \cdot 10^{-\frac{A_2}{40}} \end{cases} \tag{19}$$

where f_s is the switching frequency of the converter.

Considering that the CM inductor contributes most of the volume of the filter, a same Y-capacitor C_y is used here to evaluate the change of inductance

$$\begin{cases} f_{c1} = \frac{1}{2\pi\sqrt{L_{cm1}C_y}} \\ f_{c2} = \frac{1}{2\pi\sqrt{L_{cm2}C_y}} \end{cases} \tag{20}$$

where L_{cm1} and L_{cm2} are the CM inductance corresponding to the spectrums, respectively. Next, the change of inductance can be calculated by

$$\rho = \frac{L_{cm1} - L_{cm2}}{L_{cm1}} \times 100\%. \tag{21}$$

Finally, (22) can be obtained by substituting (19) and (20) with (21)

$$\rho = \left(1 - \left(\frac{n}{n+1}\right)^2 \cdot 10^{\frac{A_2 - A_1}{20}}\right) \times 100\%. \tag{22}$$

Formula (22) can be used to estimate the reduction of inductance after adopting the proposed method. It is seen that the reduction is related to the harmonic order and the amplitude of the noise.

An example in an ideal case with $n = 2$ is presented here. Fig. 12 shows the effect of the second-order noise mitigation. The uninhibited noise, namely the blue curve, corresponds to A_1 in (22). The amplitude of the third-order harmonic may increase, as shown in Fig. 16, in which the red line corresponds to A_2. Then, the change of inductance can be calculated, and

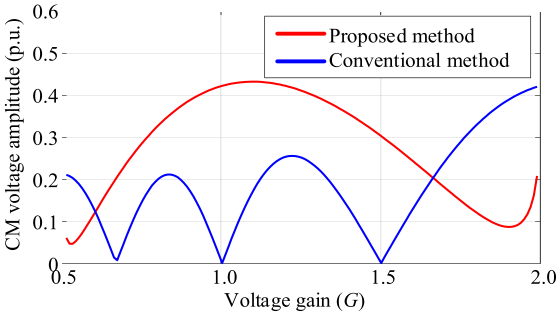

Fig. 16. Change of the third-order harmonic, when the second-order harmonic is mitigated ($n = 2$).

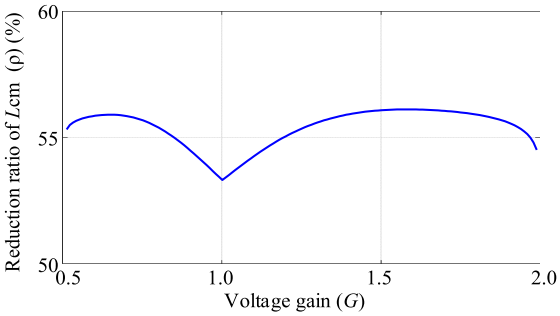

Fig. 17. Reduction of CM inductance, when the second-order harmonic is mitigated ($n = 2$).

the result is shown in Fig. 17. In the whole gain range, the CM inductance can be expected to be reduced by about 55% in an ideal case. It shows that although the amplitude of some higher order harmonics may increase, the proposed method can reduce the volume of the CM filter.

C. Evaluation of DE Algorithm

To solve the optimization problem (11), this study adopts the DE algorithm. In fact, any optimization algorithm that can find the minimum value of a function can be used, such as the well-known particle swarm optimization (PSO) algorithm. A brief evaluation and comparison is shown in this section.

As described in Section III-B, the DE algorithm has two control parameters F and CR, whereas PSO has three control parameters and the values used in this article are $C_1 = 1.6$, $C_2 = 1.2$, and $w = 0.5$. For the detailed principle of the PSO algorithm, refer to [35]. In the author's opinion, the parameter adjustment of DE may be easier owing to fewer parameters, whereas PSO with well-tuned parameters may show wider adaptability due to the more flexible configuration.

DE and PSO are used to create the LUTs. The programs are written by MATLAB and run in Intel Core i7-10700 processor. Fig. 18 shows the process of finding the minimum when setting $n = 2$, $G = 1.4$. Both algorithms converge rapidly. DE reaches the accuracy requirement of 10^{-15} after the 105th iteration, whereas PSO is faster with 85 iterations. The time consumption is listed in Table III. The actual time consumption of DE is shorter, 0.19 s.

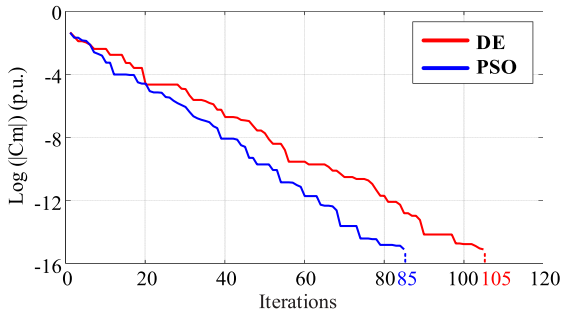

Fig. 18. Convergence in solving optimization problems.

TABLE III
COMPARISON BETWEEN DE AND PSO

Item	DE	PSO
Number of control parameters	2	3
Time consumption for once run	0.19 s	0.24 s
Time consumption for LUT n=2	149.04 s	274.42 s
Time consumption for LUT n=3	307.74 s	320.14 s
Time consumption for LUT n=4	409.42 s	353.61 s

And DE has advantages in some scenarios when creating the entire LUT, but it is not decisive.

The LUTs created by DE and PSO are almost identical. Therefore, optimization algorithm that is used to solve (11) only affects the offline time consumption and does not affect the performance of real-time noise mitigation.

D. Implementation Comments

To achieve the best performance, the noise mitigation method depends on the duty cycles and phase shift ratio with high accuracy [37]. Real-time processors with high clock frequency or low-cost processors with high-resolution pulsewidth modulation (HRPWM) function could meet the requirements [38]. At the design stage, users can convert the accurate data in LUT into an approximate value according to the output resolution of the processor, and then evaluate the mitigation capability by (9). In general, if the switching frequency is increased close to 1 MHz, the HRPWM function is required.

The proposed idea is suitable for FSBB converters and has the potential to be applied to other topologies. On the one hand, the idea could be directly extended to a multilevel structure consisting of FSBB units [2], [7], [39]. All units themselves shall be set to mitigate the noise at the same frequency. Further, the phase shift between multiple units may be used to suppress the other noises. On the other hand, when trying to extend the idea to a more general topology, the key point is to find the additional control degrees of freedom. Usually, the duty cycle is used to adjust the output voltage. If the switching frequency, the phase angle, or other variables could be regulated, there is an opportunity to mitigate CM voltage. In general, each additional

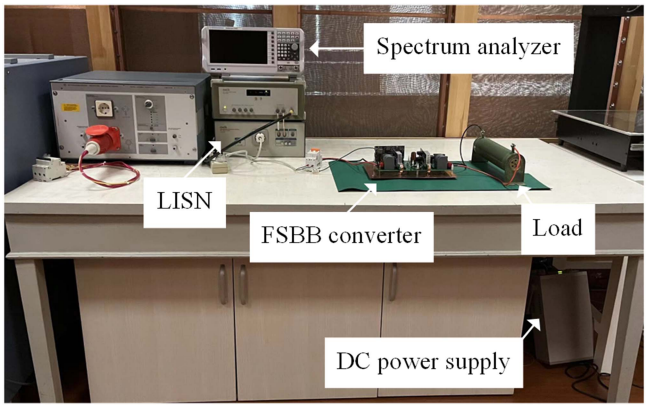

Fig. 19. Experimental setup.

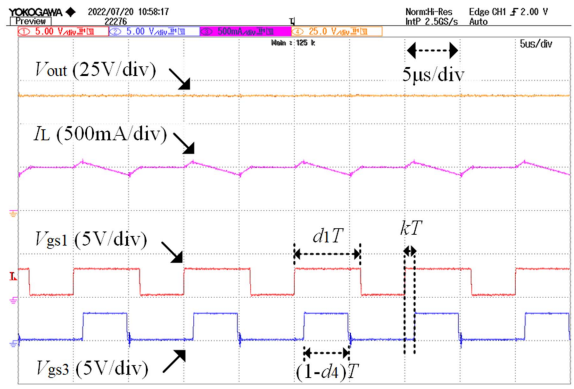

Fig. 20. Waveforms of the proposed phase-shifted modulation for the second-order CM noise mitigation ($n = 2$, $G = 1.4$).

TABLE IV
CONTROL PARAMETERS AND COMPONENT PARAMETERS

Parameters	Symbol	Value
Power switches	S_1–S_4	C3M0060065J
Control frequency	fs	100 kHz
Control cycle	T	10 μs
Inductance	L	490 μH
Output capacitance	C_o	50 μF
Input voltage	V_{in}	48 V
Load	R_L	100 Ω

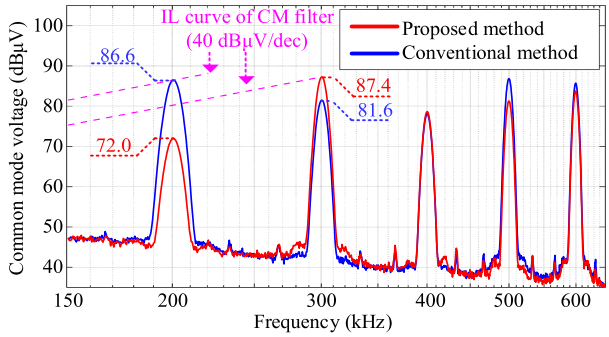

Fig. 21. CM noise spectrum demonstration for the proposed method in second-order noise mitigation.

control degree of freedom could suppress the CM noise at a selected frequency.

VI. EXPERIMENTAL VERIFICATION

The proposed method is tested on a laboratory prototype, shown in Fig. 19. The Rohde & Schwarz spectrum analyzer FPC1500 is used to collect noise signals. The real-time processor is TMS320F28388D from Texas Instruments, and its clock frequency is 200 MHz. Unless otherwise specified, the experimental parameters are as presented in Table IV.

A. Evaluation of CM Noise Mitigation

The first experiment takes the second-order CM noise as the mitigation target, i.e., $n = 2$. The open-loop control is adopted, and the output voltage gain is set to $G = 1.4$ as an example. According to Fig. 11, the duty cycle and phase shift ratio are set to $d_1 = 0.6018$ and $k = 0.086$.

Fig. 20 shows the key waveforms when using the proposed method. The drive signals V_{gs1} and V_{gs4} are directly measured from the DSP pins. It can be clearly seen that there is a phase shift determined by k between the two bridge arms. The waveform of inductor current also verifies the analysis of Section IV-C.

Fig. 21 verifies the mitigation of CM noise. The switching frequency is 100 kHz, so the noise at 200 kHz should be paid attention to when $n = 2$. The amplitude of the noise is mitigated from 86.6 to 72.0 dBμV. Theoretically, the noise can be more significantly suppressed. Nonetheless, the nonideal factors make it difficult to completely suppress the noise to zero in the experiment, such as the nonzero action time of the switches and the dead time in the half-bridge structure.

As discussed in Section V-B, when the second-order CM noise is mitigated, noise at other frequencies may increase, such as the noise at 300 kHz. The proposed method does not vanish the noise energy but changes its distribution. The lines with 40 dBμV/dec represent the filter's IL curve. The curve for the proposed method is on the right side along the X-axis. It means that the filter's corner frequency is higher, and its volume is lower. An experimental evaluation will be presented in the following section.

Fig. 22 evaluates the experimental results at different voltage gains. On the one hand, the proposed methods could always mitigate the CM noises. On the other hand, around the boundary value, such as $G = 0.6$ and $G = 1.9$, the noise mitigation is not as significant as other cases. The first reason is that the second-order CM noise itself is minor at these boundaries. The second reason is that it is assumed that all the parasitic capacitances C_p are with the same value to simplify the analysis in Section III-B. Noted, it is important to be equal rather than knowing specific values, because its equality guarantees the same noise ratio of V_2 and V_4. However, in the proof-of-concept prototype, the heat sinks

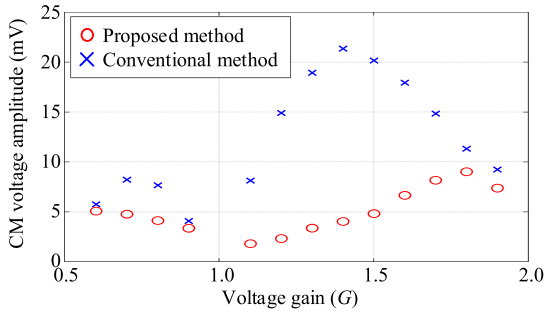

Fig. 22. Second-order CM noise migration demonstration with various voltage gain.

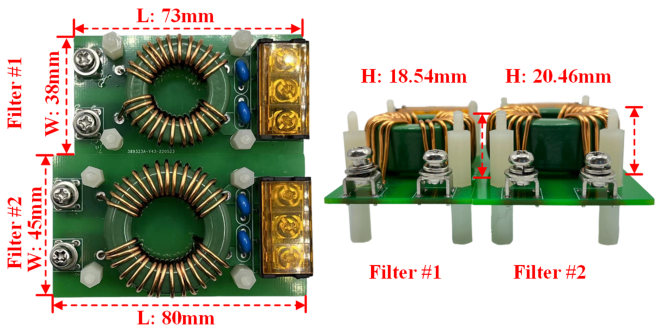

Fig. 23. Comparison of CM EMI filters. Filter #1 is used for the proposed method and Filter #2 is used for the conventional method.

of S_1 – S_4 are installed separately, which makes the parasitic capacitances unequal.

If it is necessary to further improve the mitigation capability, there are two feasible ways. The first way is to make all switches share the same heat sink in the hardware design stage, which is helpful to obtain equal C_p. The second way is to redesign the LUT according to the similar ideas in Section IV. At this time, it is necessary to adjust the minimum value target of (11), from the simple sum of V_2 and V_4 to the sum of V_2 and V_4 with proportions by their respective C_p.

B. Benefits of CM Noise Mitigation

In this section, the experiments evaluate the contribution to reducing the volume of the CM filter. Li et al. [40] provide a filter design and comparison method. It suggests that a pair of comparable CM inductors shall meet:

1) adopting the same core material;
2) adopting the same wire;
3) making with a similar perimeter utilization ratio, which equals to the length occupied by the windings divided by the available length.

According to this suggestion, two comparable CM filters are designed as shown in Fig. 23. The relative permeability of the cores is about 7000, and other parameters are listed in Table V.

The two filters were tested separately in the experiment, and the results are shown in Fig. 24. With the help of filters, the CM noise of both modulation strategies can be reduced below the standard limit. The first major noise at 200 kHz is mitigated by the proposed modulation method, which greatly reduces the demand for filter capability. The volume of the CM filter can be reduced from about 73 to 51 cm^3, achieving a 30% reduction.

TABLE V
PARAMETERS OF CM EMI FILTERS IN EXPERIMENTS

Parameters	Filter #1	Filter #2
Y-Capacitance (nF)	2.2	2.2
Inductance (mH)	2.32	1.48
Wire's diameter (mm)	1.3	1.3
Winding turns	15	13
Core's part number	TIANYUAN TYH7T38-22-15	TIANYUAN TYH7T31-19-13
Core's outer diameter (mm)	38	31
Core's inner diameter (mm)	22	19
Core's height (mm)	15	13
Perimeter utilization ratio	1.30	1.28
Filter's volume (cm^3)	73.656	51.430

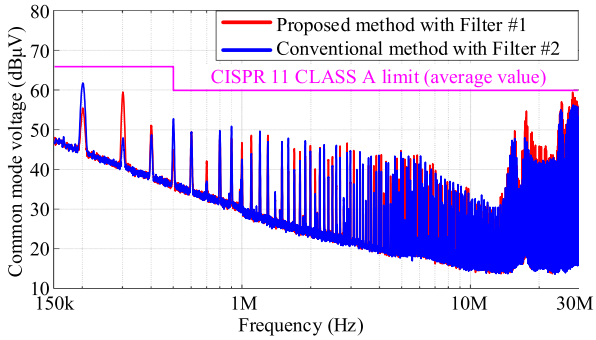

Fig. 24. CM noise spectrum with Filter #1 or #2. Both schemes meet the CISPR11 standard.

C. Selective CM Noise Mitigation

The switching frequency varies in different designs. Consequently, the first major noise in the test frequency range is also different. Therefore, the experiments in this section will show the mitigation of other selected noise.

Considering the switching frequency $f_s = 66.7$ kHz, the third harmonic, $n = 3$, is selected based on Table II. And $G = 1.2$ is taken as an example. The waveforms are shown in Fig. 25. The duty cycle and phase shift ratio are set to $d_1 = 0.3668$, $k = 0.0306$. It is seen that the third-order noise at 200 kHz is mitigated from 81.6 to 64.1 dBμV. The filter's IL curve is also shifted to the right side. A higher corner frequency and smaller volume can be expected.

When the switching frequency is set to 45 kHz, the fourth harmonic is selected, $n = 4$. The results are shown in Fig. 26. This is an example with $G = 1.6$. The duty cycle and phase shift ratio are set as $d_1 = 0.775$, $k = 0.27$. It is seen that the proposed

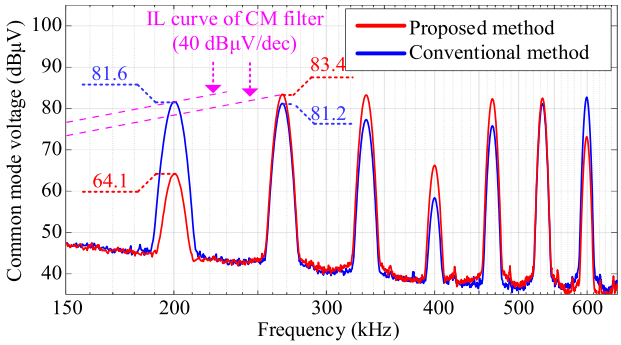

Fig. 25. CM noise spectrum demonstration for the proposed method in third-order noise mitigation.

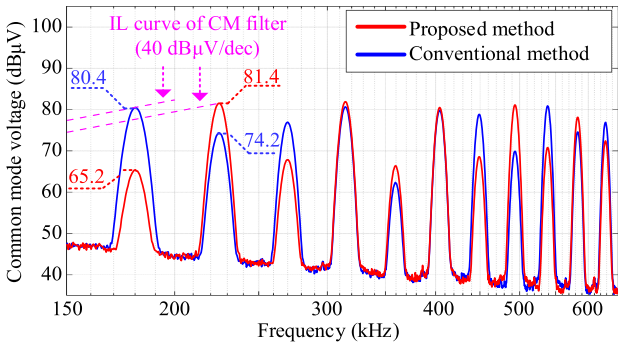

Fig. 26. CM noise spectrum demonstration for the proposed method in fourth-order noise mitigation.

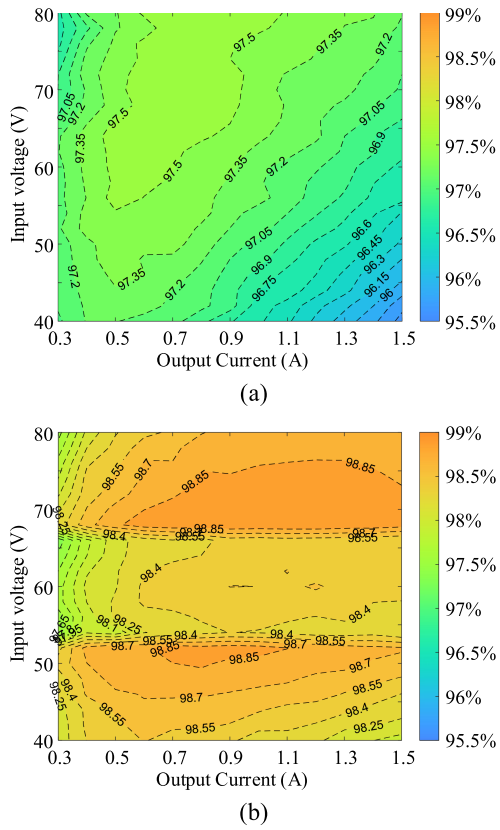

Fig. 27. Efficiency map. (a) Proposed method. (b) Conventional method.

method achieves a 15.2 dBμV reduction on the fourth-order CM noise at 180 kHz.

D. Efficiency Evaluation

The efficiency of the proposed method and the conventional method is evaluated. The conventional modulation method in [4] is used as a benchmark. Since the FSBB converter can both work in the boost mode or the buck mode, the conventional method needs to handle the transition between these modes. In other words, it needs to switch between a variety of different modulation schemes. It can be expected that the efficiency trend will be discontinuous at the switching point. Readers interested in conventional modulation methods could refer to [26] and [27]. For the proposed method, the LUT of $n = 2$ is used. And the phase-shifted modulation method is consistent throughout the voltage range.

The output voltage is fixed at 60 V, and Fig. 27 shows the experimental results. Noted that the loss of the auxiliary power supply is not included in them. Compared with conventional methods, the efficiency of the proposed method will be reduced by 1%–2%. The first reason for the reduced efficiency is that the proposed method uses additional switching actions to adjust the CM noise. The second reason is the increased conduction loss of the internal circulation. When S_2 and S_4 are turned ON at the same time, the inductor current will flow within the converter without connecting the load. The comparison results show that the proposed method is not recommended for high-efficiency-oriented scenarios. At the same time, attention should be paid to the design of the heat sink to ensure the compactness of the whole system.

VII. Conclusion

The conducted EMI noise of the FSBB dc/dc converter is discussed in this article. DM noise model and CM noise model are derived. The models show that the DM noise is related to the current flowing through S_1, whereas the CM noise is related to the sum of S_2 and S_4 voltages. The models provide tools to analyze the conducted EMI issues and guide the design of filters. And it may inspire the development of more control strategies or design methods.

A selective CM noise mitigation method is proposed. The implementation steps are presented in detail, and its recommended operating range is discussed. Experiments show that it can suppress the selected CM noise and help to reduce the volume of the CM filter. In future research, the optimization goal can be changed from minimizing the selected one to a compromise of multiple harmonics, which may further explore the potential of reducing the volume.

References

[1] S. Roy, A. N. M. W. Azad, S. Baidya, and F. Khan, "A comprehensive review on rectifiers, linear regulators, and switched-mode power processing techniques for biomedical sensors and implants utilizing in-body energy harvesting and external power delivery," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12721–12745, Nov. 2021.

[2] H. J. Ahmad and M. Hagiwara, "A compact high-power noninverting bidirectional buck–boost chopper for onboard battery energy storage systems," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1722–1735, Feb. 2022.

[3] C. Restrepo, B. Barrueto, D. Murillo-Yarce, J. Muñoz, E. Vidal-Idiarte, and R. Giral, "Improved model predictive current control of the versatile buck-boost converter for a photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 37, no. 3, pp. 1505–1519, Sep. 2022.

[4] X. Weng, Z. Zhao, K. Chen, L. Yuan, and Y. Jiang, "A nonlinear control method for bumpless mode transition in noninverting buck–boost converter," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2166–2178, Feb. 2021.

[5] J.-F. Chen, Z.-Y. Chen, and C.-M. Zhang, "Multi-mode control with GaN high operating frequency four-switch step-up/down converter," in *Proc. Int. Power Electron. Conf. - ECCE Asia*, Himeji, Japan, May 2022, pp. 477–484.

[6] D.-H. Kim and B.-K. Lee, "An enhanced control algorithm for improving the light-load-efficiency of noninverting synchronous buck-boost converters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3395–3399, May 2016.

[7] Z. Zhu et al., "Multimode smooth transition technique for three-level cascaded noninverting buck–boost DC–DC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14409–14419, Dec. 2021.

[8] Y. Bai, S. Hu, Z. Yang, Z. Zhu, and Y. Zhang, "Model predictive control for four-switch buck-boost converter based on tuning-free cost function with smooth mode transition," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6607–6618, Dec. 2022.

[9] Q. Liu, Q. Qian, M. Zheng, S. Xu, W. Sun, and T. Wang, "An improved quadrangle control method for four-switch buck-boost converter with reduced loss and decoupling strategy," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10827–10841, Sep. 2021.

[10] S. Natarajan, T. S. Babu, K. Balasubramanian, U. Subramaniam, and D. J. Almakhles, "A state-of-the-art review on conducted electromagnetic interference in non-isolated DC to DC converters," *IEEE Access*, vol. 8, pp. 2564–2577, 2020.

[11] B. Narayanasamy and F. Luo, "A survey of active EMI filters for conducted EMI noise reduction in power electronic converters," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 6, pp. 2040–2049, Dec. 2019.

[12] Y. Chu, S. Wang, and Q. Wang, "Modeling and stability analysis of active/hybrid common-mode EMI filters for DC/DC power converters," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6254–6263, Sep. 2016.

[13] Y. Zhou et al., "A novel neutral point-based active EMI filter for common mode noise attenuation," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10081–10085, Sep. 2022.

[14] W. Jiang, H. Jiang, S. Liu, S. Ji, and J. Wang, "A carrier-based discontinuous PWM strategy for T-type three-level converter with reduced common mode voltage, switching loss, and neutral point voltage control," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1761–1771, Feb. 2022.

[15] Z. Liu, P. Wang, W. Sun, Z. Shen, and D. Jiang, "Sawtooth carrier-based PWM methods with common-mode voltage reduction for symmetrical multiphase two-level inverters with odd phase number," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1171–1183, Jan. 2021.

[16] W. Deng, X. Zhang, and W. Xie, "A novel direct torque control strategy of two-level voltage source inverters for eliminating common-mode voltage spikes caused by dead-time effect," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2275–2284, Feb. 2023.

[17] D. Xu, M. Yang, Y. Chen, J. Long, and D. Xu, "EMI-regulated SiC-based motor drives with Markov chain pseudo-random frequency space vector pulse width modulation strategy," *IEEE Trans. Energy Convers.*, vol. 37, no. 4, pp. 2348–2358, Dec. 2022.

[18] R. Gamoudi, D. Elhak Chariag, and L. Sbita, "A review of spread-spectrum-based PWM techniques—A novel fast digital implementation," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10292–10307, Dec. 2018.

[19] F. Pareschi, R. Rovatti, and G. Setti, "EMI reduction via spread spectrum in DC/DC converters: State of the art, optimization, and tradeoffs," *IEEE Access*, vol. 3, pp. 2857–2874, 2015.

[20] P. B. Derkacz, J.-L. Schanen, P.-O. Jeannin, P. J. Chrzan, P. Musznicki, and M. Petit, "EMI mitigation of GaN power inverter leg by local shielding techniques," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11996–12004, Oct. 2022.

[21] F. C. Lee, S. Wang, and Q. Li, "Next generation of power supplies—Design for manufacturability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6462–6475, Dec. 2021.

[22] X. Zhang, Z. Wang, M. Cheng, S. Ding, and W. Wang, "The random PWM based bi-directional buck-boost cascade converter for electric vehicles," in *Proc. Int. Conf. Elect. Mach. Syst.*, Beijing, China, Aug. 2011, pp. 1–5.

[23] M. Zehelein, J. Portik, M. Nitzsche, P. Marx, and J. Roth-Stielow, "Reduction of the leakage currents by switching transition synchronization for a four-switch buck-boost converter," in *Proc. 10th Int. Conf. Power Electron. - ECCE Asia*, Busan, South Korea, May 2019, pp. 2217–2223.

[24] M. Sasaki, J. Imaoka, and M. Yamamoto, "An investigation on the relationship between CM noise and distribution of parasitic capacitance," in *Proc. Int. Power Electron. Conf. - ECCE Asia*, Himeji, Japan, May 2022, pp. 477–484.

[25] A. Ganjavi et al., "Common-mode current prediction and analysis in motor drive systems for the new frequency range of 2–150 kHz," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 74–90, Feb. 2022.

[26] N. Zhang, G. Zhang, and K. W. See, "Systematic derivation of dead-zone elimination strategies for the noninverting synchronous buck–boost converter," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3497–3508, Apr. 2018.

[27] Y. Bai, Z. Zhu, Z. Yang, S. Zha, and S. Hu, "Analysis and comparison of inductor current characteristics for non-inverting buck-boost converter with four-mode modulation," in *Proc. IEEE 5th Int. Elect. Energy Conf.*, Nanjing, China, May 2022, pp. 2534–2540.

[28] J. Yao, Y. Lai, Z. Ma, and S. Wang, "Advances in modeling and reduction of conducted and radiated EMI in non-isolated power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Phoenix, AZ, USA, Jun. 2021, pp. 2305–2312.

[29] V. Tarateeraseth, "EMI filter design: Part III: Selection of filter topology for optimal performance," *IEEE Electromagn. Compat. Mag.*, vol. 1, no. 2, pp. 60–73, Apr.–Jun. 2012.

[30] J. Fang, X. Ruan, X. Huang, R. Dong, X. Wu, and J. Lan, "A PWM plus phase-shift control for four-switch buck-boost converter to achieve ZVS in full input voltage and load range," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12698–12709, Dec. 2022.

[31] B. Shi, Z. Zhao, K. Li, G. Feng, S. Ji, and J. Zhou, "Design methodology for optimal phase-shift modulation of non-inverting buck-boost converters," *J. Power Electron.*, vol. 19, no. 5, pp. 1108–1121, Sep. 2019.

[32] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.

[33] J. Hao, G. Zhang, K. Yang, M. Wu, Y. Zheng, and W. Hu, "Online unified solution for selective harmonic elimination based on stochastic configuration network and Levenberg–Marquardt algorithm," *IEEE Trans. Ind. Electron.*, vol. 69, no. 10, pp. 10724–10734, Oct. 2022.

[34] M. Wu, H. Tian, Y. W. Li, G. Konstantinou, and K. Yang, "A composite selective harmonic elimination model predictive control for seven-level hybrid-clamped inverters with optimal switching patterns," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 274–284, Jan. 2021.

[35] A. M. Amjad and Z. Salam, "A review of soft computing methods for harmonics elimination PWM for inverters in renewable energy conversion systems," *Renewable Sustain. Energy Rev.*, vol. 33, pp. 141–153, May 2014.

[36] L. Callegaro, M. Ciobotaru, D. J. Pagano, E. Turano, and J. E. Fletcher, "A simple smooth transition technique for the noninverting buck–boost converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4906–4915, Jun. 2018.

[37] Z. Liu, Z. Huang, F. C. Lee, and Q. Li, "Digital-based interleaving control for GaN-based MHz CRM totem-pole PFC," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 808–814, Sep. 2016.

[38] "TMS320x280x, 2801x, 2804x high resolution pulse width modulator (HRPWM) reference guide," Texas Instruments Inc., Dallas, TX, USA, 2011. [Online]. Available: https://www.ti.com/lit/ug/spru924f/spru924f.pdf

[39] M. S. Khan, S. S. Nag, A. Das, and C. Yoon, "Analysis and control of an input-parallel output-series connected buck-boost DC-DC converter for electric vehicle powertrains," *IEEE Trans. Transp. Electrific.*, to be published, doi: 10.1109/TTE.2022.3216610.

[40] H. Li, Y. Ding, C. Zhang, Z. Yang, Z. Yang, and B. Zhang, "A compact EMI filter design by reducing the common-mode inductance with chaotic PWM technique," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 473–484, Jan. 2022.

[41] R. Whitt, Z. Yuan, A. I. Emon, F. Luo, and D. Huitink, "Electrothermal system design and evaluation of low EMI and thermally balanced 150 kW T-type traction inverter," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 538–547, Jan. 2023.

[42] G. Yu, J. Dong, T. B. Soeiro, G. Zhu, Y. Yao, and P. Bauer, "Three-mode variable-frequency ZVS modulation for four-switch buck+boost converters with ultra-high efficiency," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4805–4819, Apr. 2023.

Yuning Bai received the B.S. degree in electrical engineering and automation from North China Electric Power University, Beijing, China, in 2015, and the M.S. degree in electrical engineering from the North China University of Technology, Beijing, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with Zhejiang University, Hangzhou, China.

His research interests include model predictive control of motor drives and dc/dc converters, and analysis and suppression of conducted electromagnetic interference for dc/dc converters.

Sideng Hu (Member, IEEE) was born in China, in 1984. He received the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2011.

From August 2011 to August 2013, he was a Postdoctoral Researcher with the University of Michigan-Dearborn, Dearborn, MI, USA. Since September 2013, he has been with the College of Electrical Engineering, Zhejiang University, Hangzhou, China. His research interests include high-frequency dc/dc converters, soft-switching techniques, and vehicle electrification.

Zhi Yang received the B.S. degree in industrial automation from Hohai University, Nanjing, China, in 1997, and the M.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2005. He is currently working toward the Ph.D. degree in electrical engineering with Zhejiang University, Hangzhou, China.

He is currently the General Manager with the Intelligent Energy Research Institute, Wanbang Digital Energy Company, Ltd., Nanjing. His experience includes active power filter, variable-frequency drives, power quality analysis, and fast chargers of electric vehicle.

Mustafa Tahir received the B.Sc. degree in electrical engineering from the University of Engineering and Technology, Lahore, Pakistan, in 2015, and the M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with Zhejiang University, Hangzhou, China.

His research interests include wide bandgap devices characterization, modeling and applications, resonance analysis, energy storage, and power converters.

Mr. Tahir was the recipient of the Excellent Paper Award of the IACGN in 2019. He is a lifetime member as well as a Registered Engineer with the Pakistan Engineering Council.

Yongjian Zhi was born in Shangshui County, Henan, China, in July 1982. He received the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2013.

He is currently a Senior Design Engineer with CRRC Zhuzhou Institute Company Ltd., Zhuzhou, China. His research interests include electromagnetic compatibility and the suppression techniques of rail transport.