A Load Adaptive Digital Gate Driver IC With Integrated 500 ksps ADC for Drive Pattern Selection and Functional Safety Targeting Dependable SiC Application

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***Abstract*—A fully integrated load adaptive digital gate driver is proposed for high-speed and dependable SiC applications. It breaks the trade-OFF between surge/ringing and switching loss over a wide load range of 3–15 A by selecting the gate patterns stored in 8 channel 1.5 kb look up table (LUT). The principle of voltage ringing during turn-OFF of power devices is analyzed, and a method of temporarily controlling the gate current in the opposite direction is found to be effective. A proposed time resolution expansion technique allows the output of optimal waveforms based on theory without increasing the memory size, achieves the surge/ringing suppression of 51% and reduce the LUT size by 1/12. The integrated 500 ksps successive approximation register analog to digital converter (ADC) with steady sampling and automatic power supply voltage (VDD) selection schemes senses not only the load current, but also the surge and the short circuit for functional safety.**

***Index Terms*—Active gate driver, CMOS integrated circuits, load adaptive, overshoots, silicon carbide (SiC) MOSFETs, surge voltage, wireless power transfer.**

I. Introduction

APPLICATION of SiC power devices is in progress in various important motor drive and power supply systems typified by e-mobility. Compared to conventional power devices such as insulated gate bipolar transistor (IGBT), SiC achieves less switching loss thanks to its high slew rate capability for drain voltage and current, as well as less conduction loss. It allows high power density and compact system implementations, but the following three challenges manifest:

1) large radiation noise and conduction noise caused by voltage surge and successive ringing in combination with the high-voltage slew rate;
2) device performance degradation and failure owing to the repetitive application of surge voltage;
3) Degradation of overcurrent tolerance for short-circuit faults.

Electro magnetic interference (EMI) and reliability degradations are critically important for power electronics in public environments for which reliability is essential.

The active gate drive technique shown in Fig. 1 is one of the solutions for the first challenge, but the analog control scheme shown in Fig. 1(a) is less effective owing to the limited arbitrariness of the gate drive waveform [1]. For example, reference [1] can only control dv_d/dt due to reverse recover current (I_{RR}) of SuperJunction MOSFETs and cannot control current or voltage ringing. In addition, the analog feedback for faster control increases costs. Lobsiger and Kolar [2] controlled an IGBT dv_d/dt of 2 V/ns and Wangm et al. [3] and Noge et al. [4] controlled the rising current waveform of SiC-MOSFETs connected in parallel by feedback. However, a 14 V 320 MHz wideband operational amplifier is required in [3] and 220 MHz wideband operational amplifier with output voltage range of 20 V is required in [4], making chip integration difficult, which is required for applications such as EV motors. The implementation in a discrete configuration also increases area and cost. The gate driver [5] for GaN devices is successfully integrated with 4 V 500 MHz bandwidth operational amplifiers in a CMOS to control dv_d/dt with feedback. However, this technology cannot be applied to SiC-MOSFETs because the gate voltage of 4 V required to drive GaN is lower than the 18–25 V required for SiC-MOSFETs.

The digital gate drive shown in Fig. 1(b) is an attractive solution [6], [7], [8], [9], [10], [11], [12], [13], because arbitrary control of gate voltage can regulate various power device characteristics such as dv_d/dt, di_d/dt, and current-voltage ringing. However, the ON-chip implementation with a single waveform

Manuscript received 14 September 2022; revised 15 December 2022; accepted 7 February 2023. Date of publication 13 February 2023; date of current version 20 April 2023. Recommended for publication by Associate Editor K. Wada. *(Corresponding author: Shusuke Kawai.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3244200.

Digital Object Identifier 10.1109/TPEL.2023.3244200

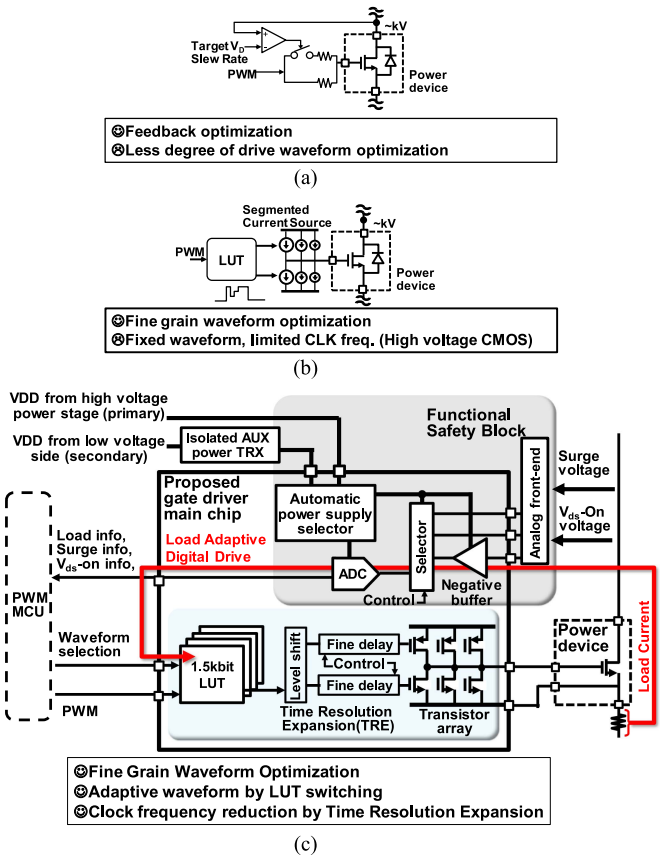


Fig. 1. Conventional and proposed active gate driver. (a) Conventional analog active gate driver. (b) Conventional digital gate driver. (c) Proposed Load Adaptive Digital Gate Driver IC w/ Functional Safety Feature.

look up table (LUT) [6] was insufficient for the motor drive applications in which the load current varies in the order of sub-1 ms [5]. Even another FPGA-based digital implementation has not demonstrated real-time load current tracking [7]. An example of load application is given in [8], However, an external measuring instrument is used to detect the load and output digital data to the gate driver IC.

In the case of the digital-based approach, it is necessary to find a waveform to drive the gate of the power device that can suppress ringing. In [6] and [9], waveforms are searched manually. No theoretical support has been provided for these optimal waveforms, making it difficult to apply this research to other devices. Miyazaki et al. [10] derived the optimal waveform using a simulated annealing algorithm. However, it requires 2500 measurements. Cheng et al. [8] also required a measurement time of 187 to 594 s, and there is no theoretical support for the generated waveforms [8]. As a result, the optimal waveform in [8] is complex and requires a large memory when storing the data in the chip. Raviola and Fiori [11] used a driver that can generate positive and negative binary gate currents, and the optimal waveform is generated by feedback using an ADC. However, the switching voltage is as low as 48 V and has not been demonstrated at switching hundreds of volts, as required for e-mobility. Also, the absolute value of dv_d/dt for switching by active gate is 1.5 V/ns, which is slow compared to the dv_d/dt of more than 10 V/ns shown in the SiC-MOSFET data sheet [12]. Theoretical analysis and simulation were not sufficiently performed in [11], and as a result, only the drain voltage undershoot at turn-ON has been demonstrated, and active gate technology has not been demonstrated in the drain voltage overshoot at turn-OFF. In [13], current and voltage slew rates are sensed by analog circuits and feedback signals are generated using the FPGA. The waveform is output to the gate of the power device by a mixed analog-digital circuit that includes an operational amplifier and a DAC to achieve 800 V switching. However, a 300 MHz operational amplifier is required for the output stage. The devices used for the measurement are IGBTs, which operate slower than SiC-MOSFETs, and the controlled dv_d/dt is as low as 1 V/ns.

Some references derive the ringing theoretically from the waveform [7], [14], [15]. Turn-ON current ringing is analyzed in [14], but there is no literature that analyzes turn-OFF voltage ringing in detail. A theoretical analysis of turn-OFF voltage ringing is performed for SiC-MOSFET in [7], but it is incomplete because it does not take into account the nonlinearity of the capacitor unique to SiC-MOSFETs. Cao et al. [15] mentioned the analysis of SiC-MOSFET turn-OFF and capacitance nonlinearity, but the verification by simulation is incomplete. As a result, no gate current patterns are shown in the simulations to break the trade-OFF between surge voltage and losses. In addition, no experiment results are shown to break the trade-OFF.

The second and third problems related to device degradation can be solved by an external controller in the case of IGBTs because of their relatively slow operation. However, SiC-MOSFETs are more sensitive to short circuits that cause thermal breakdown because the current density of the chip is higher than that of IGBTs, requiring a gate driver IC to complete fast detection and protection.

This article proposes a load-adaptive gate driver IC that solves issues related to surge voltage-induced noise and device gradients [16]. In this article, theoretical analysis, simulation, and measurements are comprehensively performed to generate optimal waveforms for turn-OFF voltage surge reduction. The theoretical analysis and simulation of turn-OFF considering capacitor nonlinearity, which has not been done before, is performed. The gate waveform that reduces surge voltage is derived from theoretical analysis and simulation. The optimal waveforms are generated by measurements using the results of simulation and theoretical analysis. The proposed chip is fabricated and the optimum waveform is supplied to the power device. The switching that breaks the tradeoff between surge voltage and losses is demonstrated experimentally using SiC-MOSFETs as the power device. The proposed load adaptive digital gate driver is shown in in Fig. 1. The IC implements the 3-bit segmented current sources, each consisting of a transistor array, to pull-up and pull-down the gate, the 1.5 kb LUT to store multiple gate drive patterns, the assisting schemes to expand the time resolution of the gate current and reduce the LUT size, and the multipurpose 500 ksps successive approximation register (SAR) ADC whose concept is shown in [17], an isolated power supply and automatic power supply voltage (VDD) selector is also implemented. The load

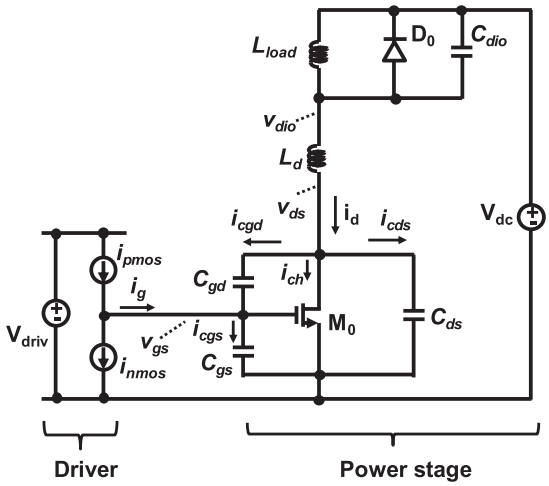


Fig. 2. Equivalent circuit of the power device and power stage.

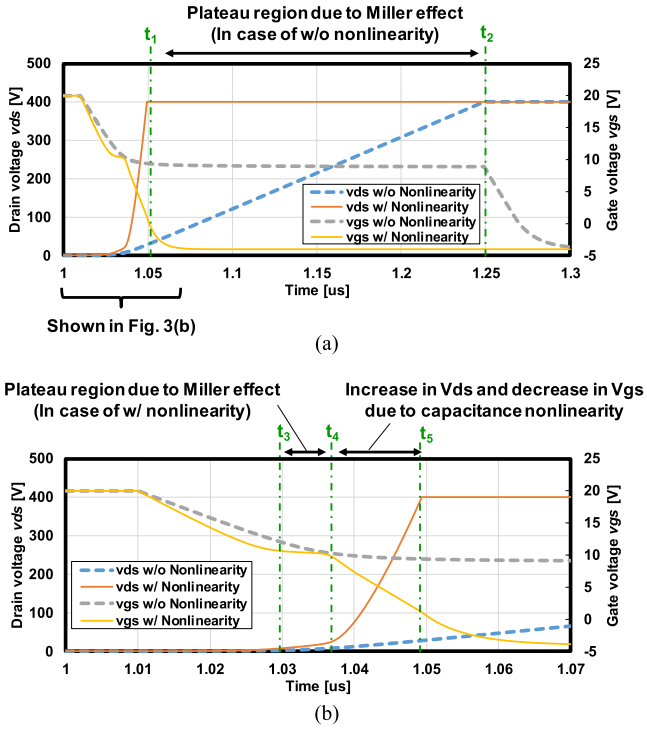


Fig. 3. Simulation results of turn-OFF waveforms with and without consideration of capacitor nonlinearity. (a) Simulation results of turn-OFF using the circuit in Fig. 2. (b) The enlarged view of a portion of Fig. 3(a).

adaptive digital gate driver was monolithically integrated for the first time ever, making it possible to break the tradeoff between surge/ringing noise and switching loss of SiC-MOSFETs for a wide variety of load varying applications.

The rest of this article is organized as follows. In Section II, the optimal gate current pattern is derived by performing a turn-OFF voltage ringing analysis that takes into account the nonlinearity of parasitic capacitance. Section III describes the driver circuit to output the derived optimal gate current pattern with less memory. Section IV presents the sampling front-end circuit for detecting surge voltage, ON-voltage, and drain current. The isolated power supply circuit is also shown in Section IV. The measurement result is shown in Section V. Finally, Section VI concludes this article.

II. Turn-Off Voltage Ringing Analysis

In this section, the optimal gate current pattern is derived by performing a turn-OFF voltage ringing analysis that takes into account the nonlinearity of parasitic capacitance. First, it is explained what is different from the conventional switching waveforms [18], [19] when capacitor nonlinearities of the SiC-MOSFETs are taken into account. Next, an analysis of turn-OFF voltage ringing considering capacitor nonlinearity and gate current waveforms that reduce ringing are shown. Fig. 2 shows the equivalent circuit of the power device and power stage. Fig. 3 shows what is different from the conventional switching waveforms [18], [19] by considering the nonlinearity of the capacitor. Fig. 3(a) shows simulation results of turn-OFF using the circuit in Fig. 2. Fig. 3(b) is an enlarged view of a portion of Fig. 3(a). The simulator is Cadence Spectre and the device is TW070J120B [12]. For simplicity of discussion, the inductance L_d is set to 0. The dotted line in Fig. 3(a) and (b) shows the result when the nonlinearity of the capacitor is not considered, and the solid line shows the result when the nonlinearity of the capacitance is considered. As shown in Fig. 3(a), when nonlinearities in capacitance are not considered, the gate voltage does not change because the capacitance C_{gd} increases due to the Miller effect from time t_1 to t_2, when the drain voltage increases [18], [19]. On the other hand, considering the nonlinearity of capacitance, as shown in Fig. 3(b), the period during which the gate voltage does not change due to the Miller effect begins at time t_3 and ends at time t_4. From time t_4 to t_5, the drain voltage rises sharply and the gate voltage also decreases due to the capacitance nonlinearity.

The analysis of turn-OFF voltage ringing also needs to take into account the rapid increase in drain voltage and decrease in gate voltage due to capacitance nonlinearity.

The following is an analysis of turn-OFF voltage ringing and identification of gate waveforms that reduce ringing, taking into account the nonlinearities described previously. Fig. 4 shows the simulation results using the circuit in Fig. 2 when the inductance L_d is set to 10 nH. The currents i_g, i_d, i_{ch}, and i_{cds} are the gate current, drain current, channel current, and parasitic drain-source capacitance current, respectively. The voltages v_{ds}, v_{dio}, and v_{gs} are the drain and gate voltages of transistor M_0 and the anode voltage of diode D_0, respectively. The g(Abs) in Fig. 4 is an absolute value of gain defined by dv_{ds}/dv_{gs}. In Fig. 4, C_{ds}, C_{gd}, and C_{ds} show the time variation of capacitance, where $(1+g)C_{gd}$ is the gate-to-drain capacitance that takes into account the Miller effect.

The turn-OFF operation is described below with reference to Fig. 4. It is briefly described up to the beginning of the Miller plateau region, which is described in other literature [18], [19], and then the subsequent characteristics are explained in detail. The gate current i_g begins to flow from time t_a, at time t_b the power device M_0 transitions from the intertripolar region to

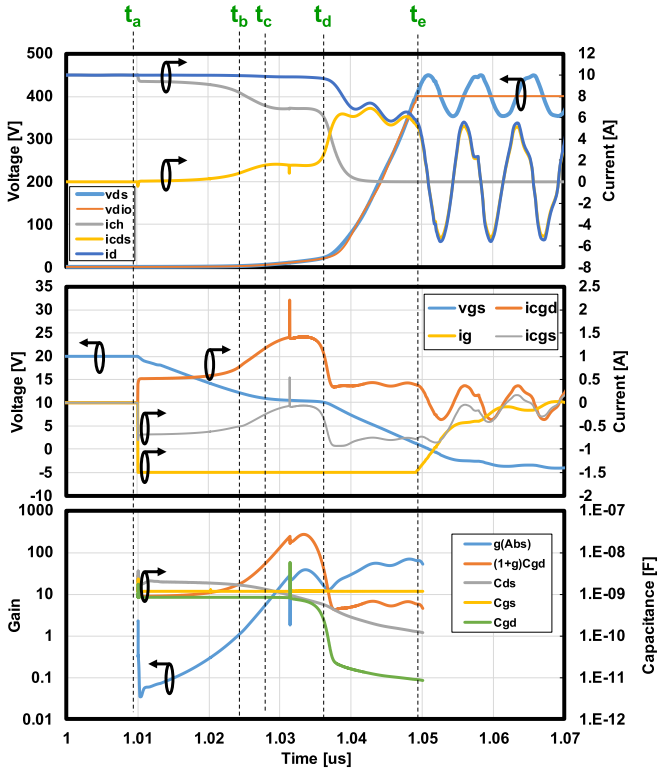


Fig. 4. Simulation results with nonlinearity of capacitors are considered and parasitic inductance is included.

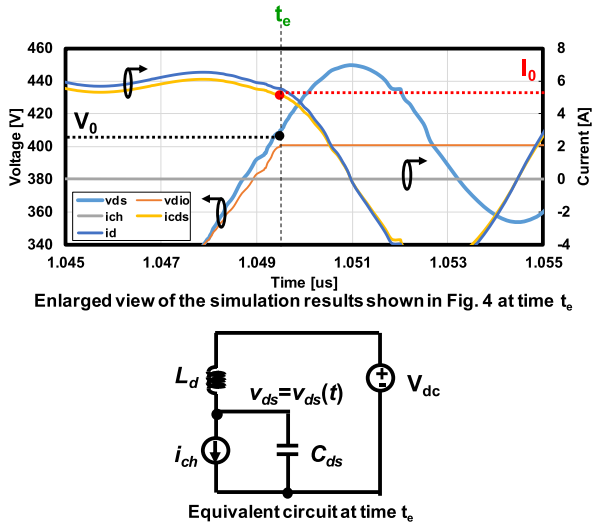


Fig. 5. Simulation results zoomed in at time t_e where drain voltage resonance starts and equivalent circuit at time t_e.

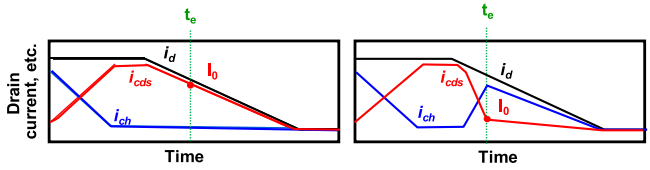


Fig. 6. Outlines of the channel current i_{ch}, drain current i_d, and current flowing in the capacitance C_{ds}.

the saturation region, and at time t_c the Miller plateau region begins [18], [19]. In the Miller plateau region, the capacitance $(1 + C_{gd})$, which takes into account the miller effect, becomes much larger than the capacitance C_{gs}, and most of the gate current i_g flows through the capacitance C_{ds}. From time t_c to t_d, the drain voltage v_{ds} slowly increases. The capacitance C_{gd} of SiC-MOSFET has a drain voltage dependence, and as the drain voltage increases, the capacitance C_{gd} rapidly decreases [12]. Then, at time t_d, the capacitance C_{gs} becomes larger than the capacitance $(1 + g)C_{gd}$, even considering the Miller effect. The gate current i_g starts to flow into the capacitance C_{gs}, and the gate voltage v_{gs} decreases. Even if the drain voltage does not reach the power supply voltage V_{dc} of the power stage, the miller plateau region ends at time t_d. As the gate voltage v_{gs} decreases, the channel current i_{ch} decreases and the current flowing in the capacitance C_{ds} increases.

When the gate voltage v_{gs} reaches the threshold voltage, the channel current i_{ch} becomes almost zero, and most of the current i_d flows into the capacitance C_{ds}. Since the capacitance C_{ds} also decreases with increasing drain voltage v_{ds} [12], the drain voltage v_{ds} and the diode voltage v_{dio} increase rapidly. At time t_e, diode D_0 begins to conduct. Here, a resonant circuit is formed and ringing occurs in the drain voltage v_{ds}. Fig. 5 shows simulation results magnified around time t_e and the equivalent circuit at time t_e. Since capacitance C_{gd} is an order of magnitude smaller than C_{ds} at time t_e, as shown in Fig. 4, the capacitance C_{gd} is ignored in Fig. 5 to simplify the discussion. In the equivalent circuit shown in Fig. 5, the drain voltage v_{ds} is $v_{ds}(t)$, and furthermore, the current source i_{ch} becomes almost zero at time t_e, so the following equation is obtained. Time t_e in Fig. 5 corresponds to $t = 0$ in

$$C_{ds}\frac{d^2 v_{ds}\,(t)}{dt^2} - \frac{V_{dc} - v_{ds}\,(t)}{L_d} = 0 \tag{1}$$

$$v_{ds}\ (0) = V_0 \tag{2}$$

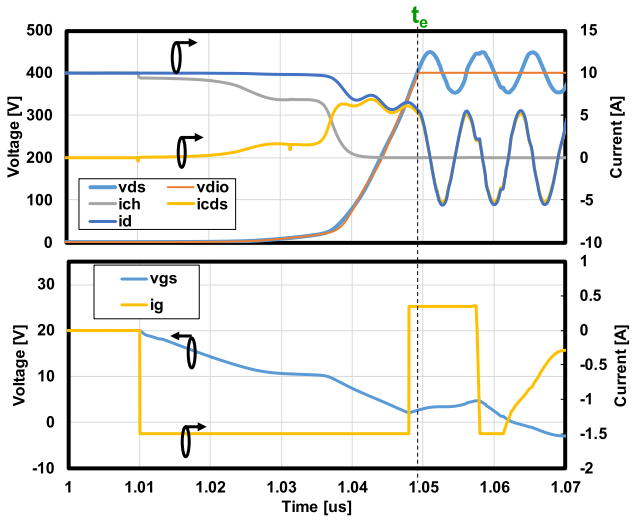
$$\frac{dv_{ds}\,(0)}{dt} = \frac{I_0}{C_{ds}}. \tag{3}$$

The initial values of the drain voltage v_{ds} and the current in the capacitance C_{ds} are V_0 and I_0, as shown in Fig. 5. The drain voltage v_{ds} is expressed by the following equation:

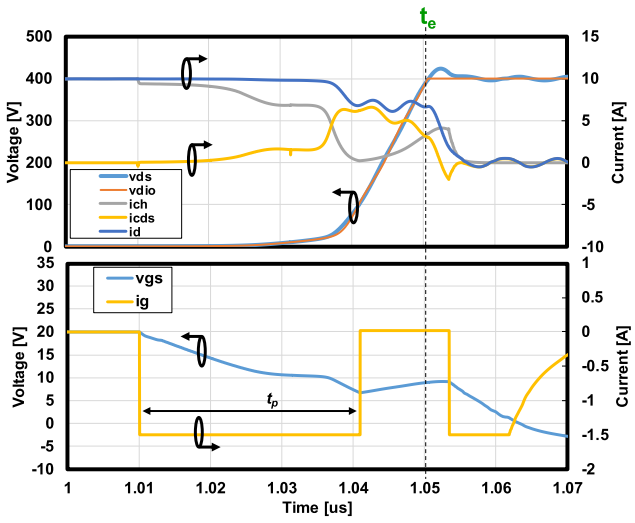
$$v_{ds}\ (t) = \sqrt{(V_0 - V_{dc})^2 + \left(\frac{I_0}{C_{ds}\omega}\right)^2}\ \sin(\omega t + \varphi) + V_{dc} \tag{4}$$

$$\omega = 1/2\pi\sqrt{L_d C_{ds}}. \tag{5}$$

From (4), it can be seen that to reduce the amplitude of the resonance voltage, the initial current I_0 of the capacitance C_{ds} should be reduced. Fig. 6 shows the outlines of the channel current i_{ch}, drain current i_d, and current flowing in the capacitance C_{ds}. The left figure in Fig. 6 shows the waveform without current i_{ch} control, while the right figure shows an example with



(a)



(b)

Fig. 7. Simulation results with controlled channel current and reduced ringing, and simulation results with uncontrolled channel current. (a) The simulation results showing an example of uncontrolled channel current. (b) The simulation example of controllable channel currents, showing successful reduction of surge voltage.

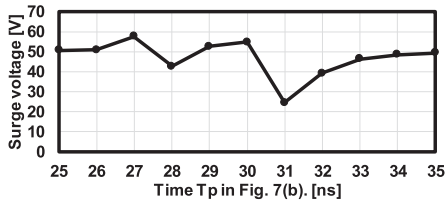


Fig. 8. Simulation results of the relationship between the time Tp, when the gate current starts to flow in the reverse direction, and the surge voltage.

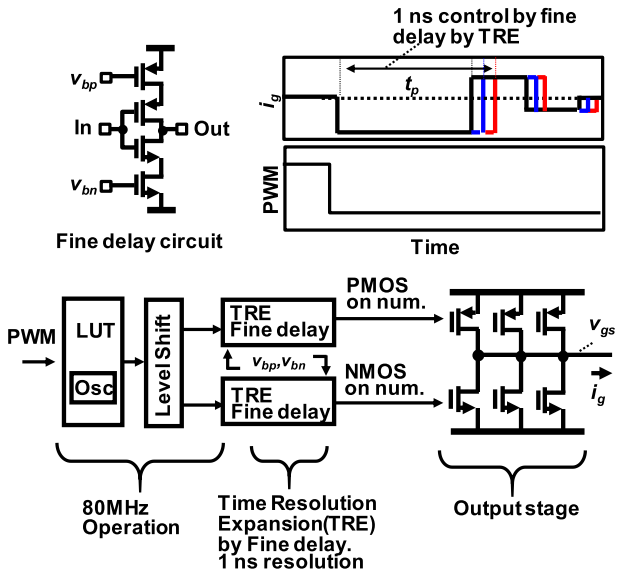


Fig. 9. Proposed gate driver with TRE.

current i_{ch} control. To reduce the initial value current I_0, the channel current i_{ch} should be increased, as shown in Fig. 6. This can be accomplished by temporarily flowing the gate current i_g in the opposite direction and increasing the gate voltage v_{gs} above the threshold voltage. The following describes how the gate current i_g is controlled to control the channel current i_{ch}. The requirement to control the gate current i_g prior to time t_e in order to control the channel current is illustrated in Fig. 7. The simulation results showing an example of uncontrolled channel current i_{ch} are shown in Fig. 7(a). Fig. 7(b) shows an example where the channel current i_{ch} is controllable. Fig. 7(b) also shows that the surge voltage has been successfully reduced. As shown in Fig. 7(a), even if the gate current i_g flows in the opposite direction just before time t_e when resonance begins, the current i_{cds} flowing through the capacitance C_{ds} cannot be reduced. This is because the gate voltage v_{gs} is much lower than the threshold voltage just before resonance starts. Therefore, the gate current i_g shown in Fig. 7(b) is desirable. By flowing the gate current i_g in the reverse direction around the point where the gate voltage v_{gs} falls below the threshold voltage, holding the gate voltage at a value slightly below the threshold voltage, the channel current i_{ch} can be changed, and the initial value current in the capacitance can be reduced.

III. Proposed Gate Driver Design With Time Expansion Technique

As described in Section II, a gate waveform signal is required to drive the gate current i_g in the opposite direction. The relationship between the time t_p in Fig. 7 and the maximum surge voltage is shown in Fig. 8. The t_p is the time when the gate current begins to flow in the reverse direction. The surge voltage shows the difference between the drain voltage and the main circuit dc voltage of 400 V. The time t_p is set to 31 ns in the simulation shown in Fig. 7. As shown in Fig. 8, when t_p changes by 1 ns, the surge voltage changes significantly. Therefore, controlling t_p by 1 ns is necessary.

Fig. 9 shows the proposed gate driver with time resolution expansion (TRE). A 1 GHz clock is necessary to control 1 ns in a digital circuit. Generating the 1 GHz clock in the low-cost

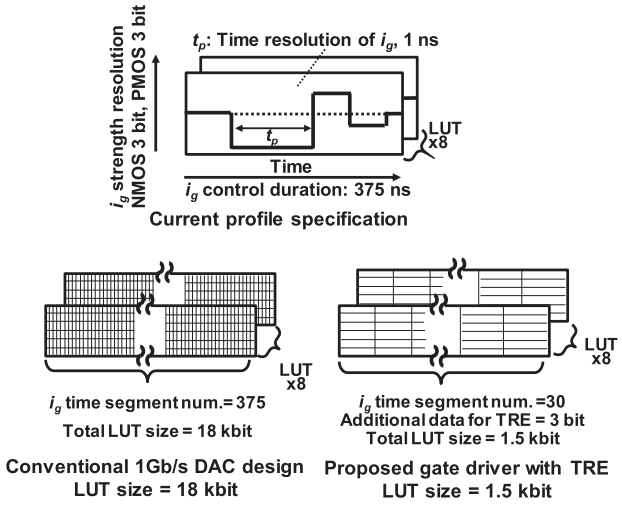


Fig. 10. LUT size specifications and comparison of LUT size with and without TRE.

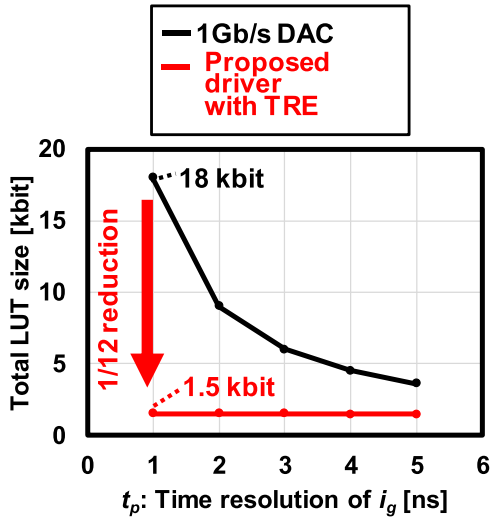


Fig. 11. Relationship of the time resolution and the required LUT size.

High Voltage CMOS process for gate drivers is not feasible in terms of area, power consumption and skew. As shown in Fig. 9, the TRE scheme proposed here introduces fine tunable delay circuits between the level shifter (LS) and the output stage. The fine delay is adjusted in a circuit with a current source connected between the PMOS or NMOS of the inverter and the power supply, as shown at upper left in Fig. 9. The fine delay circuit is enabled after the first falling edge of the PWM signal. The time t_p can be controlled in 1 ns increments by TRE. The output stage shown in Fig. 9 can output current fast for a time resolution of 1 ns, which has been confirmed by simulations that take parasitic resistance and parasitic capacitance into account. If the value of parasitic inductance between the power device and the gate driver becomes large, ringing may occur in the gate current and the intended active gate waveform may not be input to the power device. The inductance of the parasitic gate loop should be minimized by using TO247-4L with a Kelvin Source provided in the power device package.

The TRE scheme also keeps the clock frequency of the LUT at 80 MHz and LUT is significantly reduced in size by using TRE. The effect of the LUT on compactness is shown in Fig. 10. The current profile specifications are shown at the top of Fig. 10. The specification of the LUT includes the ability to store 6 bits (3 NMOS and 3 PMOS bits) of i_g amplitude information with a resolution of 1 ns. The total control interval is 375 ns. As shown at lower left in Fig. 10, if a conventional DAC [7] is used without the proposed TRE technique, data in 1 ns increments is required, resulting in a total LUT size of 18 kbit. On the other hand, when using TRE, 12.5 ns segment data is sufficient. The time of one segment, 12.5 ns, is controlled using fine delay at 1 ns intervals. With 3 bits, 12.5 ns can be adjusted in less than 1 ns. Even considering the additional 3 bits needed for TRE, the total LUT size is reduced to 1.5 k. Fig. 11 shows the time resolution and the required LUT size. When using a conventional 1 GS/s DAC, the smaller the required t_p resolution, the larger the LUT size. On the other hand, when TRE is used, the increase in the required LUT size can be suppressed. By using TRE, the required LUT size can be reduced to 1/12 of that using a conventional DAC. The LUT size of 3 kbits or less can be integrated into a CMOS process using digital circuits.

In the gate driver IC used in this article, NMOS and PMOS may conduct simultaneously for a very short time, causing a large current to flow. To prevent the wiring in the IC from being disconnected due to the large current, the PMOS and NMOS in the IC are connected with thick wiring.

IV. Design of Proposed Sampling Front-End and Isolated Power Supply

This section describes the circuit configuration of the sampling front-end and isolated power supply. By sensing the load current of the SiC-MOSFET, the LUT can be switched as a signal indicating the load status. The V_{ds}-ON voltage can be used for short-circuit detection. By monitoring the surge voltage, information on the overvoltage applied to the SiC-MOSFET can be obtained and used to determine reliability. Isolated power transmission was also included to achieve functional safety, a concept presented in the literature [17]. The ON-chip ADC, selector and buffer circuits can be powered via isolated power transmission.

A. Load Current Sensing

Fig. 12 shows the schematics of sampling front-end (FE) for the load current sensing, the surge monitoring, and the V_{ds}-ON (short-circuit) monitoring with the integrated 500 ksps SAR ADC. The load current is detected by the resistor $R_{\rm sense}$ introduced in the source terminal of the low-side SiC-MOSFET, but both the positive and the negative voltages appear on $v_{R\rm sense}$ because of the current commutation. To sense both of them, an inverting amplifier is integrated on the chip and the offset voltage v_{ref} is applied. The sample timing of the ADC is set to 4 μs past the SiC voltage transient (steady sampling) so as to be unaffected by the switching noise of the 400 V power stage.

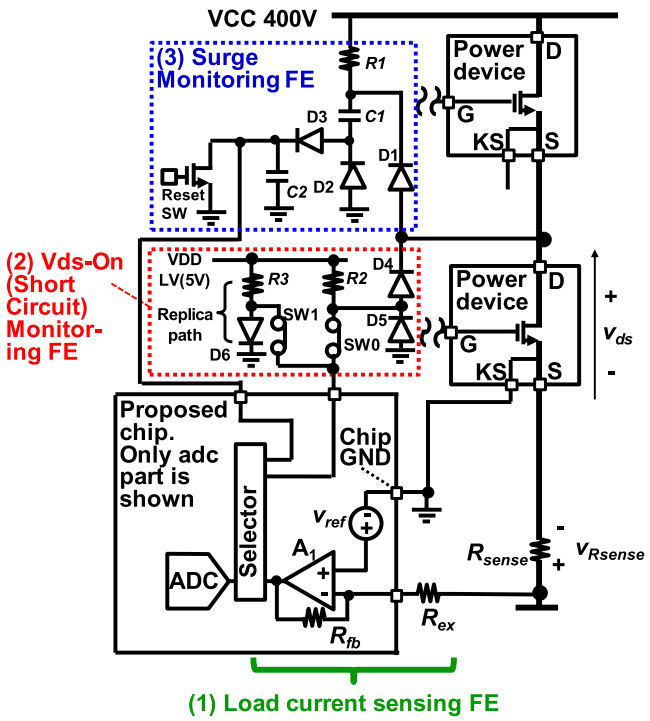


Fig. 12. Surge monitoring circuit, Vds-ON monitoring circuit, load current detection circuit.

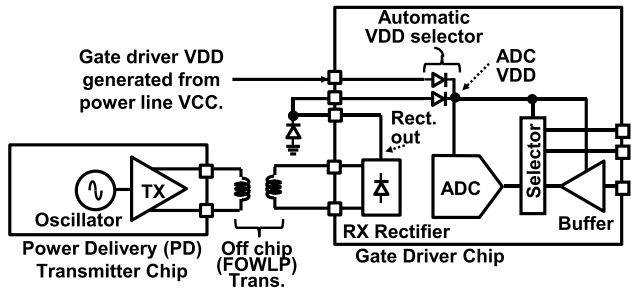


Fig. 13. Isolated power supply circuits.

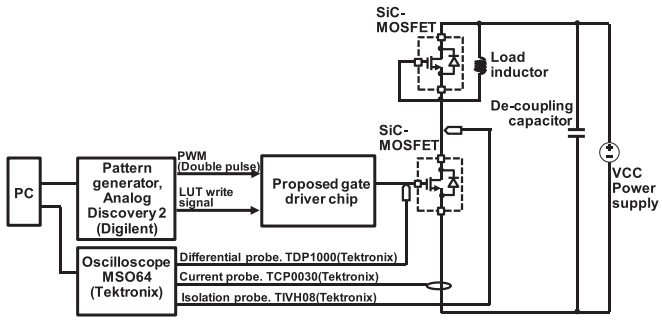


Fig. 14. Measurement setup.

B. Surge Monitoring

To detect the surge voltage, a peak hold surge sampling frontend composed of the OFF-chip high-voltage diode, dividing sample capacitors, and the reset switch was also implemented as a surge monitoring FE, as shown in Fig. 12. In the initial state, resistor R_1 biases the voltage on the cathode of D_1 to VCC of 400 V. When a surge occurs in the drain voltage of a low-side power device and the voltage becomes greater than 400 V, the cathode side of diode D_1 becomes equal to the surge voltage. The surge voltage larger than 400 V is divided by capacitors C_1 and C_2 to match the 5 V ADC input inside the chip. Diodes D_2 and D_3 are located to provide the current path when capacitors C_1 and C_2 are discharged by the reset switch. The detected surge voltage can be used to predict device performance degradation or failure due to repeated application of surge voltage.

C. V_{ds}-On (Short-Circuit) Monitoring

On-state V_{ds} (V_{ds}-ON) is also observed to detect the short-circuit fault. Fig. 12 also shows the V_{ds}-ON (short-circuit) monitoring front end. The Resistor R_2 biases the cathode of diode D_5 to 5 V. When the low-side power device turns ON, the drain voltage v_{ds} of the power device is lower than 5 V. Then, diode D_4 turns ON and the anode of diode D_4 is the same as the drain voltage of the power device. Diode D_4 turns OFF when the low-side power device turns OFF and the ADC input voltage never exceeds 5 V. With the proposed circuit, the ON-voltage of diode D_4 is added to the V_{ds}-ON voltage. Therefore, a replica circuit consisting of resistor R_3 and diode D_6 is prepared. By measuring the difference between the voltage at the anode of diode D_6 and the voltage at the anode of diode D_4, the effect of the ON-voltage of the diode can be eliminated.

D. Isolated Power Supply

As shown in Fig. 13, the receiver for the auxiliary isolated power transfer and the automatic VDD selector for the ADC and sensing frontend are integrated for functional safety. Power supply of the gate driver IC is typically provided from the VCC in the high-voltage domain through a step-down converter. But in terms of functional safety, the monitoring circuits should keep operating for diagnosis and safe system shutdown in case faults, including short circuit, occur in the high-voltage domain, and the power supply is lost. Isolated power transfer is realized over a differential transformer implemented by a cost- and power-efficient fan out wafer level package process [17]. The automatic VDD selector consists of two diodes and outputs to the ADC whichever is the higher of the voltage generated from the high-voltage domain and the voltage transmitted wirelessly.

V. Measurement Results

The gate driver test chip was fabricated in 0.5 μm CMOS with 40 V high-voltage transistors for the segmented current source. The performance is verified by using the device SCT3080KR [20], a 1.2 kV SiC-MOSFET. The device SCT3080KR has a TO-247-4L package and a Kelvin source. To avoid unwanted oscillations occurring in the gate voltage, a device with a package with less parasitic inductance was selected. The double pulse tests were performed under 400 V VCC. Fig. 14 shows the measurement setup. The signal to write the LUT and the PWM signal are generated using Analog Discovery 2 from Digilent.

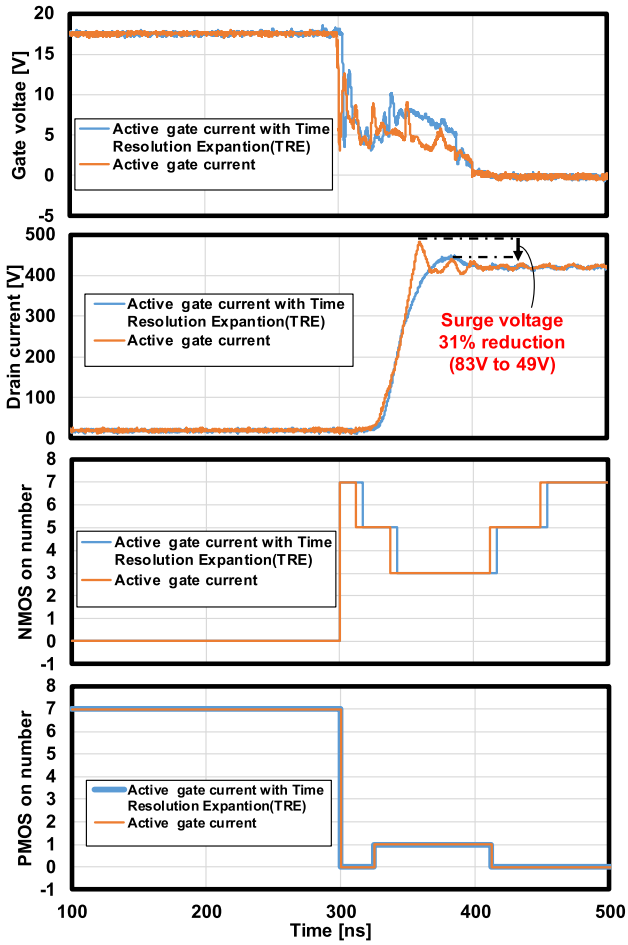


Fig. 15. Measured turn-OFF waveforms with and without TRE.

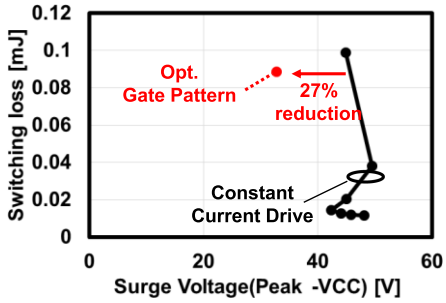


Fig. 16. Measured surge voltage and switching losses at 3 A drain current.

The oscilloscope used to measure gate voltage, drain voltage, and drain current is a Tektronix MSO64. The oscilloscope and pattern generator are controlled by a PC. Fig. 15 shows the drain voltage waveform of the optimized gate pattern with and without TRE. The TRE is adopted for the NMOS turn-ON pattern. TRE enhances the optimization and compresses the surge by 31%(83 to 49 V). Measured surge voltage and switching losses for drain currents of 3 and 15 A are shown in Figs. 16 and 17. The constant current drive in Figs. 16 and 17 represents the case where the gate is driven without changing the current value in the time direction. Compared to the constant current drive, the proposed gate pattern

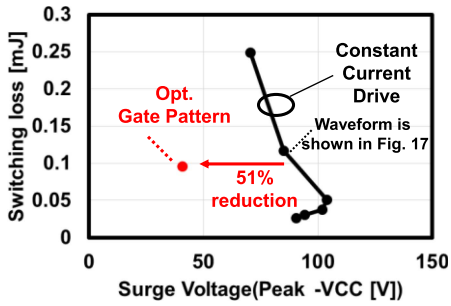


Fig. 17. Measured surge voltage and switching losses at 15 A drain current.

achieves 51% and 27% surge reduction for the same level of switching loss at the load current of 15 and 3 A, respectively.

Fig. 18 shows the switching waveforms using the proposed method and the conventional driving method at a drain current of 15 A. Using the proposed method, the surge voltage is reduced by 51% from 85 to 40.1 V. At time t_x in Fig. 18, the PMOS is turned ON. However, six NMOS are also turned ON. In this article, the current value of 1 segment of PMOS and 1 segment of NMOS were designed as 522 and 153 mA, respectively. Therefore, at time t_x, the current flows from the gate of the power device to the driver direction. At time t_y in Fig. 18, the number of NMOS on is reduced to 3. From time t_y, the current is flowing toward the gate of the power device. The gate current is flowing in the reverse direction before time t_z, when the resonant circuit is formed. The ringing of the drain voltage is successfully reduced. The dv_d/dt from 10% to 90% drain voltage increase with active gate control in Fig. 18 is 16 V/ ns.

The following shows the method of generating a gate current pattern that breaks the trade-OFF between surge voltage and losses in the measurement. The waveform generation was done manually with the measurement system shown in Fig. 14, observing switching losses and surge voltages. As shown in the simulation and theoretical analysis in Section II, there are two important aspects of the gate waveform that reduce the surge voltage. The first is to inject the gate current in the reverse direction shortly before the drain voltage reaches the power stage supply voltage, and the second is to keep the gate voltage value close to the threshold voltage value when injecting the gate current in the reverse direction. The method of how these two aspects are achieved with an active gate waveform is explained below.

First, the method to keep the gate voltage value close to the threshold voltage value when injecting the gate current in the reverse direction is described. Discharging the gate charge with a large gate current when turning OFF the power device is desirable in terms of turn-OFF delay reduction and switching loss reduction. Therefore, in the waveform shown in Fig. 18, when the gate current draw starts at time t_v, the gate charge is discharged at the maximum current that the driver can provide. On the other hand, as shown in Section II, the surge voltage cannot be reduced if the gate voltage is not close to the threshold voltage value when injecting the reverse current. If the gate charge continues to be discharged at a large gate current, the gate

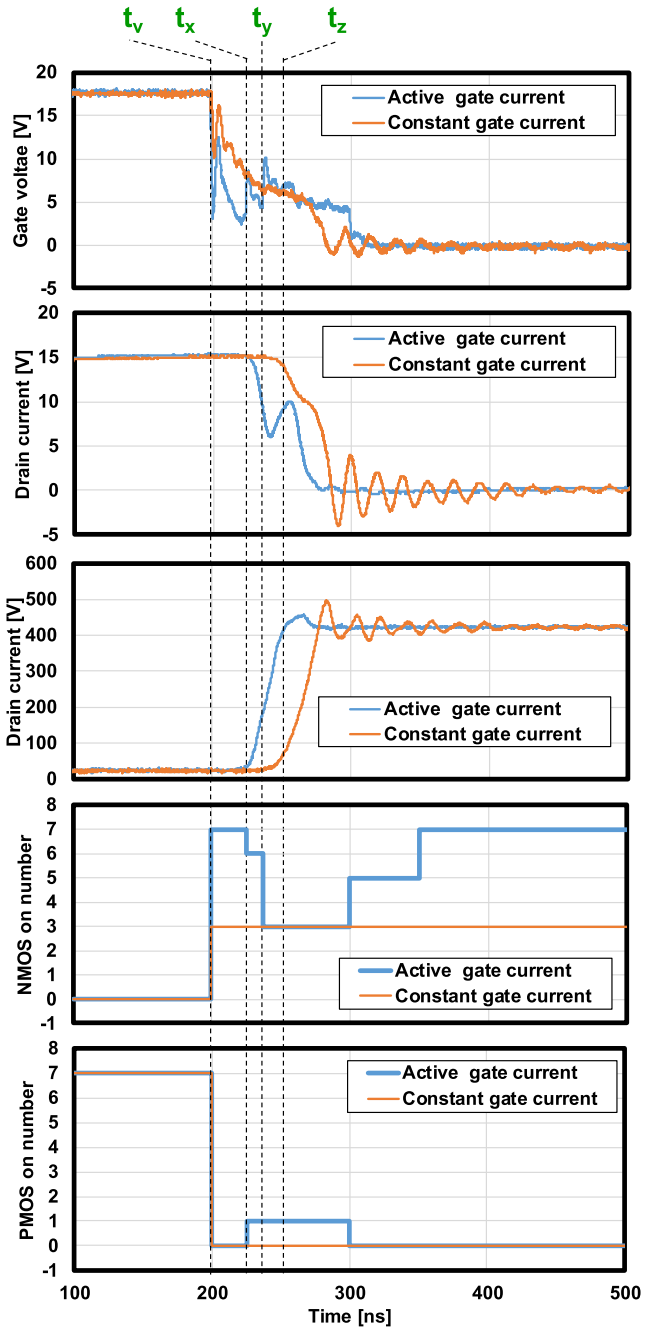


Fig. 18. Measured switching waveforms using the proposed method and the conventional driving method at a drain current of 15 A.

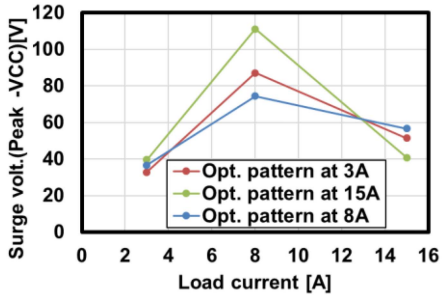


Fig. 19. Relationship of the surge voltage and load current for each optimized gate pattern.

voltage falls far below the threshold voltage value at the time of injecting the reverse current. As a result, the surge voltage cannot be reduced even if the gate voltage is injected in the reverse direction, as shown in Fig. 7(a) in one example. The gate current should be varied to keep the gate voltage close to the value of the threshold voltage at the timing of injecting current in the reverse direction. At the time t_x when the gate voltage becomes close to the value of the threshold voltage, the driving force of NMOS is reduced and the driving force of PMOS is increased so that the gate voltage remains close to the value of the threshold voltage.

Next, the timing of injecting the gate current in the reverse direction is described. According to the simulation results shown in Fig. 7 and the theoretical analysis in Section II, injecting gate current in the reverse direction just before the drain voltage matches the power stage supply voltage does not reduce the surge voltage. Injecting gate current at an earlier timing enables the surge voltage to be reduced. In the simulation shown in Fig. 7(b), the surge voltage is successfully reduced when the gate current is injected in the reverse direction at the timing when the drain voltage reaches 100 V instead of when the drain voltage reaches the power stage voltage of 400 V. In the measurement, the gate current must be injected in the reverse direction at an earlier time as in the simulation, not just before the drain voltage matches the power stage voltage. In this measurement, the surge voltage was successfully reduced by injecting the gate current in the reverse direction at the time t_y shown in Fig. 18, when the drain voltage reached 200 V. With respect to the timing of injecting the gate current in the reverse direction, the difference between the simulation and the actual measurement is considered to be the difference in the nonlinearity of the capacitance of the device used.

Fig. 19 shows the relationship of the surge voltage and load current for each optimized gate pattern. As shown in Fig. 19, the gate pattern optimized at a specific load current is not the best in other current ranges, and therefore, the load adaptation is obviously effective.

Fig. 20 shows the dynamic load adaptation. The measurement circuit is shown in the lower left corner of Fig. 19. The load current is detected by sensing the drain current i_d after SiC-MOSFET turn-ON. The ADC shown in Fig. 19 detects the drain current i_d flowing in the SiC-MOSFET by sensing the voltage across the resistor R_{sense}. One of the LUTs is selected according to the output value of the ADC, and the gate current i_g defined by the selected LUT is output to the SiC-MOSFET. The time waveforms of drain voltage v_{ds}, drain current i_d, and gate voltage v_{gs} are shown at lower right in Fig. 20. A double pulse signal is used as input. The drain current i_d is 3 A at the first switching shown by the red frame at lower right in Fig. 20. In the second switching, shown by the blue frame at lower right in Fig. 20, the drain current i_d is 6 A. A magnified view of the first switching waveform is shown at upper left in Fig. 20, and a magnified view of the waveform during the second switching is shown at upper right in Fig. 20. In the first switching with drain current $i_d =$

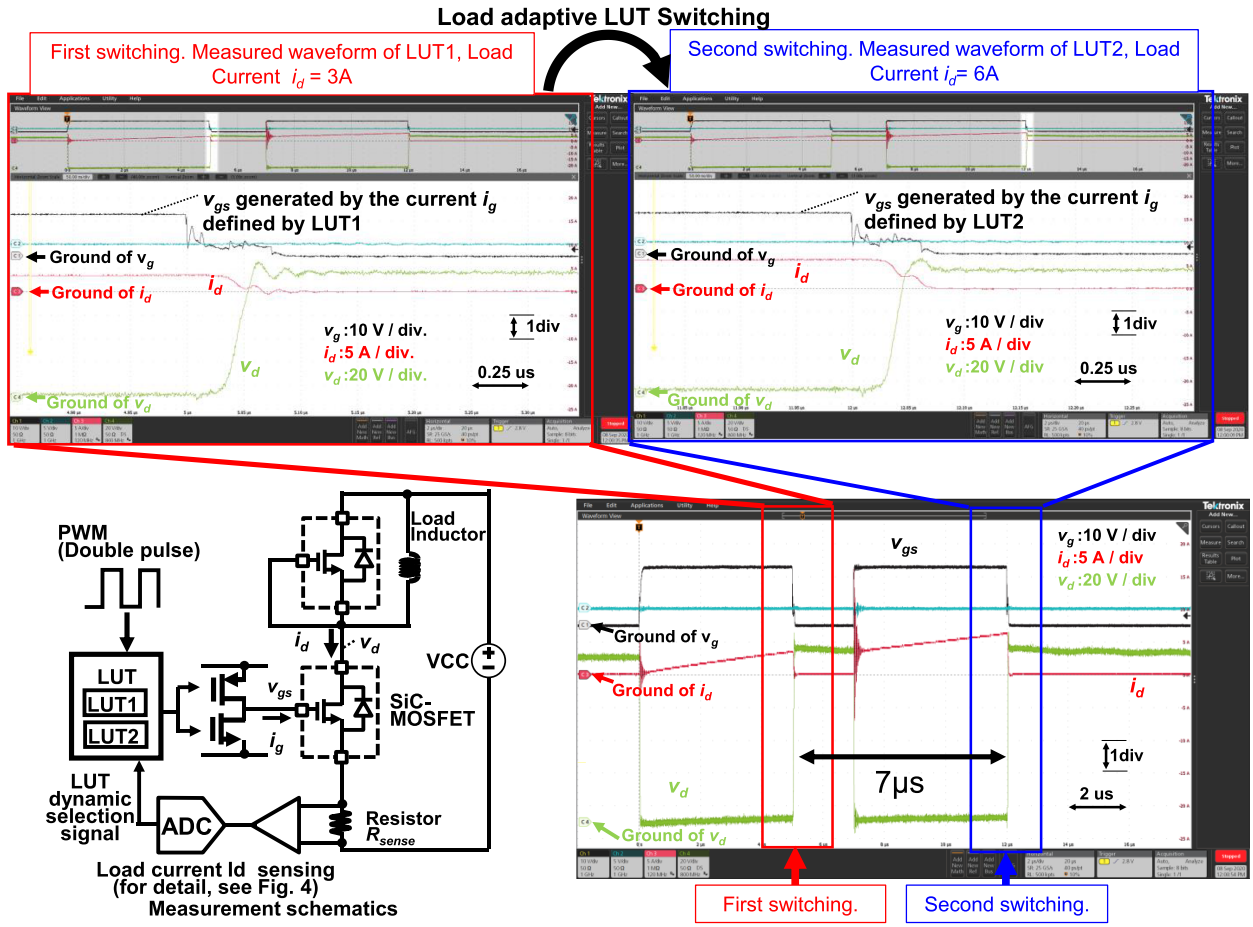


Fig. 20. Measured result of dynamic load adaption.

3 A, the gate current i_g defined by LUT1 is supplied to the gate of the SiC-MOSFET. In the second switching, the output of the ADC changes because the drain current i_d has increased from 3 to 6 A. The LUT2 is selected by the ADC changes because the drain current i_d has increased from 3 to 6 A. The LUT2 is selected by the ADC output and the gate current i_g defined by LUT2 is supplied to the gate of the SiC-MOSFET. The patterns of LUT1 and LUT2 are shown on the left in Fig. 21. The waveforms of the gate voltage v_{gs} during the first and second switching are overlaid on the right in Fig. 21. As shown on the right in Fig. 21, the gate voltage v_{gs} is different between the first and second switching. Different LUTs are successfully selected and output according to the drain current i_d. As shown at lower right in Fig. 20, the time between the first and second switching is 7 μs. During the time of 7 μs, the ADC detects the drain current, the LUT switches, and the gate waveform is successfully replaced. Since the pulse carrier frequency for motor drive is typically less than 20 kHz, the loop response of the chip is fast enough for load adaptation. In this scheme, the drain current i_d is sensed at a transient current one pulse ahead of the target transient current, and so the drain current variation must be slow enough relative to the PWM carrier frequency to achieve proper control. Since this relationship holds true for many motor applications, this scheme is acceptable.

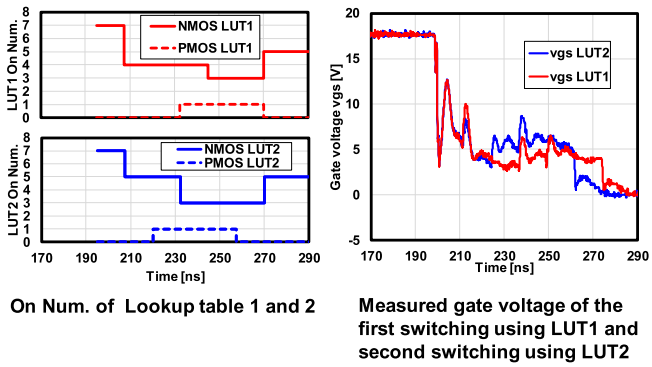


Fig. 21. On number of MOS stored in LUT1 and LUT2 used to measure the dynamic load adoption shown in Fig. 19. The measured waveforms of the gate voltages of the first and second switching overlaid.

The measurement results of the three sampling FEs are presented in Fig. 22. The measured result of the load current sampling FE is shown at upper left in Fig. 22. The blue line shows the analog drain current waveform. This current waveform is obtained from the calculation by measuring the differential voltage of the resistor R_{sense} by differential probe. The orange line shows the output code of the ADC. The ADC output code matches the

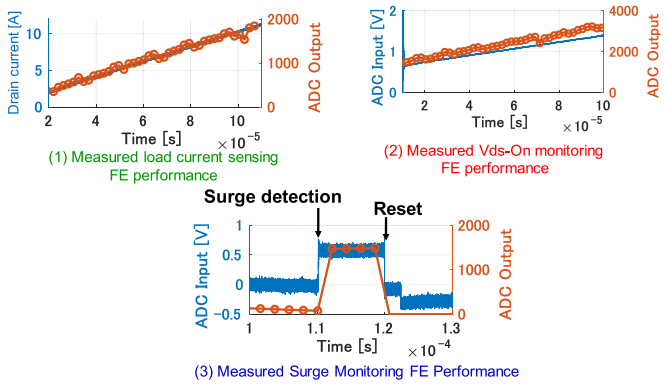


Fig. 22. Measured result of sampling front-end.

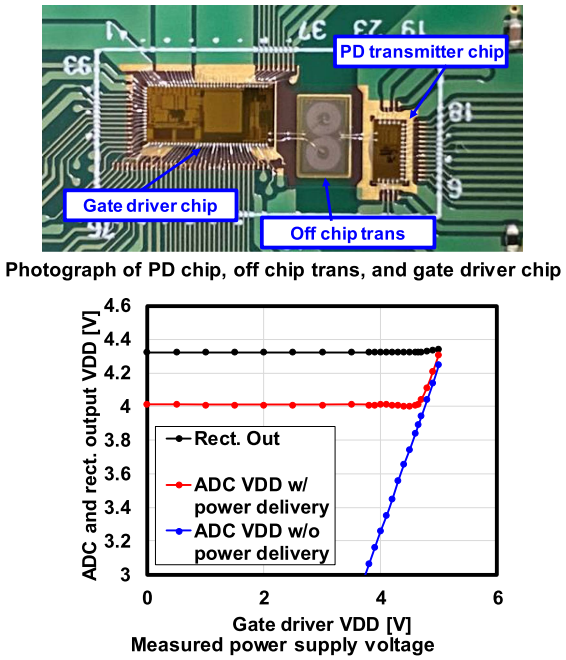


Fig. 23. Photograph and measured results of isolated power transfer.

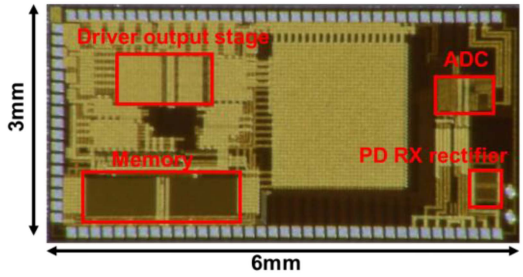


Fig. 24. Chip micrograph.

TABLE I
COMPARISON TABLE

	[6] TPE 2018	[10] TPE 2017	[1] ISSCC 2019	[7] TIE 2020	[2] TPE 2015	[9] TPE 2021	[11] TPE 2022	[15] TCAS 2022	This Work
Control strategy	Digital	Digital	Analog	Digital	Analog	Digital	Digital	Digital	Digital
#LUT	1 (on chip)	1 (off chip)	NA	8 (off chip)	NA	1 (on chip)	NA	NA	8 (on chip)
Load adaptive	No	No	Yes	No	Yes	No	Yes	No	Yes
Integrated ADC	No	No	NA	No	No	No	No	No	Yes
Time resolution expansion	Yes	No	NA	No	No	Yes	No	No	Yes
Time step	150 ps	40 ns	Continuous	Unknown	Continuous	100 ps	250 ps	Continuous	1 ns
Simultaneous PMOS NMOS Cont.	Yes	No	No	No	No	Yes	No	No	Yes
Power supply of driver	+5 V / 0 V	+15 V / 0 V	+10 V / 0 V	+20 V / -5 V	+14 V / -10 V	+5 V / 0 V	NA	+15V / -5V	+18 V / 0 V
Process(gate driver chip)	Unknown	40 V, 0.18 um BCD	18 V, 0.13 um CMOS	Discrete	Discrete	0.18um HV-CMOS	Discrete	0.18um BCD	40 V, 0.5 um CMOS
Target device	40 V GaN (EPC2015)	1200 V IGBT ,SiC(SCH2080KR)	600 V SJ-MOS*4 (TK8A60W5)	1200 V SiC (CAS120M12BM2)	1200 V IGBT (FF300R12MS4)	600V GaN (GS66508P)	75V N-ch (FDB031N08)	1200 V SiC (C3M0016120K)	1200 V SiC (SCT3080KR)
Driver output current	NA	756mA	NA	NA	NA	NA	NA	NA	3.6 A
Turn-off SR*3,4 when active gate is applied	2 V / ns*1	6 V / ns*1	-4.5 V / ns*2	18 V / ns*1	2 V / ns*	100 V / ns	-1.5 V / ns*1,*2	12 V / ns*1	16 V/ ns
Target of active gate control	Turn-on I_d surge, Turn -off V_d surge.	Turn-on I_d surge, Turn off V_d surge.	Turn-on V_d slew rate	Turn-on I_d surge, Turn off V_d surge	Turn-on I_d/V_d SR*3,Turn-off I_d/V_d SR*3	Turn-on I_d surge,	Turn-on V_d surge.	Turn-off V_d surge.	Turn-off V_d surge.
Experimental results that breaks the trade-off between loss and surge	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes

*1Estimated from figure.
*2Turn on slew rate.
*3Slew Rate (dv_d/dt). Speed when drain voltage changes from 10% to 90%.
*4Superjunction MOSFET

measurement result of the drain current. The load current sensing FE is also used for the dynamic LUT adaptation, as shown in Fig. 20. The measurement result of the V_{ds}-ON monitoring FE is shown at upper right in Fig. 22. The blue line shows the analog voltage of the ADC input. This input voltage is the same as the anode voltage of diode D_4. The orange line is the ADC output code. The ADC output code matches the measurement result of the analog V_{ds}-ON voltage. The measurement result of the surge monitoring FE is shown at the bottom of Fig. 22. The blue line is the ADC input voltage, which is the same as the voltage of capacitor C_2. The orange line is the ADC output code. The surge voltage is successfully detected by the surge monitoring FE circuit and the ADC output code matches the analog input voltage. By using the proposed sampling FE, the V_{ds}-ON voltage and the surge voltage sensing during the SiC switching is acceptable, and very fast short-circuit protection in 2 μs, which is limited by the ADC sampling rate, is achieved.

The measured results of the receiver for the auxiliary isolated power transfer and the automatic VDD selector are shown in Fig. 23. Shown on the left in Fig. 23 are the OFF-chip transformer, the power delivery (PD) transmitter chip, and the gate driver chip. The PD transmitter chip was fabricated in 130 nm CMOS process. The chip provides over 10 mW power consumption with enough margin. The measured ADC VDD and rectifier output voltage are shown on the right in Fig. 23. Without using the PD chip, the ADC VDD is decreased, as shown by the blue line in Fig. 23. When the PD chip is operating, the PD chip is constantly sending power. The ADC operates with the power acquired from the PD chip through wireless power transmission in the case that the power from VCC to the gate driver is interrupted. As shown by the red line in Fig. 23, the ADC VDD keeps the minimum requirement of 4.0 V by using the power transfer circuit.

Fig. 24 shows the photograph of the test chip fabricated in 0.5 μm CMOS with 40 V HV transistors. The chip size is 6 mm $\times$

3 mm. Table I shows the Comparison table. In this article, eight LUTs were integrated on a chip to demonstrate surge voltage reduction for a 1200 V SiC application. As shown in Table I, the slew rate or dv_d/dt of the power device with the active gate technology in this article is 16 V/ns, which is slower than the switching rate with GaN devices, however the same or faster than the other works SiC-MOSFET, IGBT and Si-MOSFET devices. The driver IC in this article can output active gate waveforms and suppress surge voltage under switching conditions where the drain voltage slew rate is more than 10 V/ns. The proposed driver IC successfully breaks the trade-OFF between surge voltage and power consumption. The function to switch the optimum waveform following the load current of the power device was realized in a single chip. The load adaptive gate waveform output was demonstrated using proposed digital gate driver with a high degree of freedom of waveform.

VI. Conclusion

A fully integrated load adaptive digital gate driver with an ON-chip ADC for functional safety is demonstrated for SiC-MOSFETs. The turn-OFF behavior of SiC-MOSFETs is analyzed by simulation, and it is shown that injecting the gate current in the reverse direction is effective in reducing the surge voltage. Measured surge voltage was reduced by 51% without increasing losses. The optimized current patterns stored in the ON-chip LUT reduce surge voltage without increasing the switching loss. The sampling FE for functional safety successfully monitors the load current, surge voltage, and V_{ds}-ON voltage of the power device.

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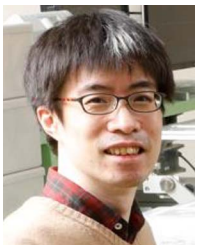

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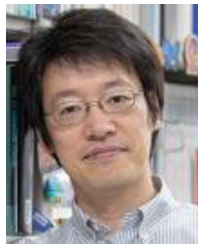

Hiroki Ishikuro (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1994, 1996, and 1999, respectively.

In 1999, he was with the System LSI Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was involved in the development of CMOS RF and mixed-signal circuits for wireless interface chips. In 2006, he was with the Department of Electrical Engineering, Keio University, Yokohama, Japan, as an Assistant Professor, where he focused on high-speed inductive-coupling links for three-dimensional chip integration and noncontact connector. He is currently a Professor with Keio University, where he focuses on the mixed-signal circuit and system designs for extremely low-power interfaces.

Dr. Ishikuro is a member of the Technical Program Committee for the Symposium on VLSI Circuits.