Letters

Simple Enhancement of Series–Series-Compensated Inductive Wireless Power Transfer Links Operating With Load-Independent Voltage Output at Fixed Frequency to Attain Zero Inverter Phase Angle

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***Abstract*—It is well-known that series–series-compensated resonant inductive wireless power transfer links (SS-IWPTL) may be designed to attain load-independent voltage output (for given operating frequency and coupling coefficient. Unfortunately, the corresponding inverter output impedance is either highly inductive or highly capacitive (inductive region is typically preferred due to natural zero-voltage switching of inverter transistors), significantly increasing inverter volt-ampere (VA) rating. The letter demonstrates that designing the SS-IWPTL for operation in the capacitive region and then adding a shunt inductor across ac-side terminals of either inverter or rectifier allow attaining inverter zero-phase angle, thus minimizing its VA rating.**

***Index Terms*—Inductive wireless power transfer link (IWPTL), load-independent voltage output (LIVO), series–series compensation, zero-phase angle (ZPA).**

I. Introduction

INDUCTIVE wireless power transfer technology is rapidly gaining popularity nowadays, being applied to systems where the conventional power transfer is impossible or undesirable [1], [2]. In some applications (e.g., power transfer though rigid barriers [3], electric vehicles charging with automatic alignment [4], etc.), coil's coupling coefficient remains nearly constant and known, allowing the inductive wireless power transfer link (IWPTL) to attain load-independent voltage output (LIVO) without feedback [5], [6]. It was shown in [7] that, in SS-IWPTLs, arbitrary LIVO may be attained for given coil inductances, coupling factor, and operation frequency. Unfortunately, LIVO operation of series–series-compensated resonant inductive wireless power transfer link (SS-IWPTL) imposes either highly inductive (typically preferred due to natural zero-voltage switching (ZVS) of inverter switches) or highly capacitive output impedance of transmitting inverter, significantly increasing its volt-ampere (VA) rating [8]. In order to minimize the impedance, series-inductance plus parallel capacitance is typically added to either primary or secondary compensation networks, forming *LCC*-S [9] or S-*LCC* [10] compensated IWPTLs. Unfortunately, full-rating inductor and shunt capacitor addition significantly increase compensation network size and alleviates efficiency due to increased circulating currents. Inspired by the recent work [11], this letter suggests to operate the SS-IWPTL in capacitive rather than inductive region and minimize the inverter output impedance by adding an inductor, connected across either inverter or rectifier terminals. As a result, reactive current consumed by the network is supplied by the additional inductor, while inverter VA rating is minimized. The improvement is attained at the expense of some physical size increase and potentially insignificant efficiency degradation.

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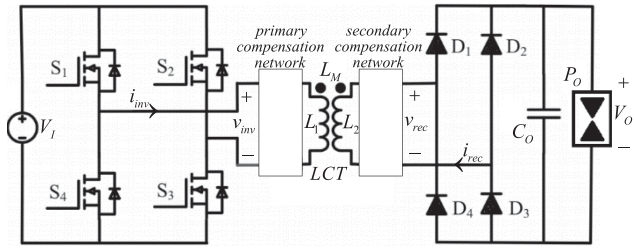

Fig. 1. Typical IWPTL structure.

II. Design for LIVO

Typical IWPTL feeding a power load P_O is shown in Fig. 1 with V_I and V_O denoting the input and output dc voltages, L_1, L_2, and L_M symbolizing the primary, secondary, and mutual inductances of the loosely coupled transformer (LCT) coils, and C_O standing for the load filter capacitance. The inverter is operated at constant frequency $\omega = 2\pi/T$ so that

$$v_{\text{inv}}(t) = \begin{cases} V_I, & 0 < t \le 0.5T \\ -V_I, & 0.5T < t \le T. \end{cases} \tag{1}$$

Voltage–current relations of LCT in Fig. 1 are described by the following set of equations (neglecting coil's series equivalent

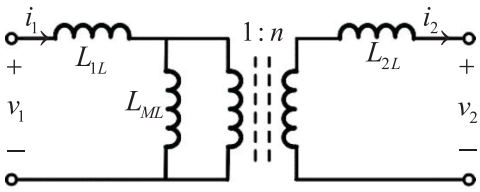

Fig. 2. Generalized ideal-transformer-based LCT equivalent circuit.

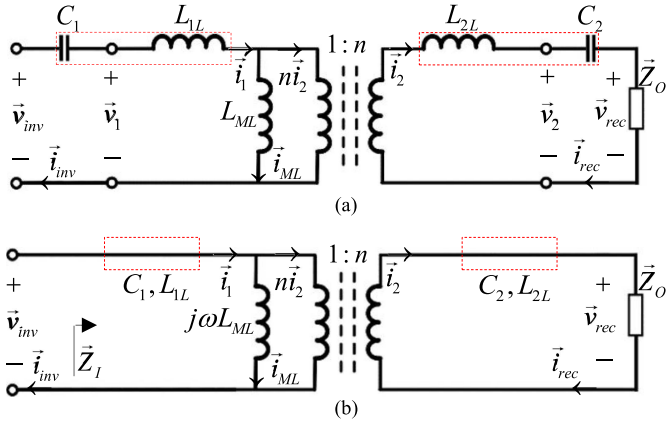

Fig. 3. SS compensation of the LCT to attain LIVO. (a) SS-compensated LCT. (b) Resulting first-harmonic equivalent circuit.

resistances for brevity):

$$v_1(t) = L_1 \frac{di_1(t)}{dt} - L_M \frac{di_2(t)}{dt}$$
$$v_2(t) = L_M \frac{di_1(t)}{dt} - L_2 \frac{di_2(t)}{dt}, \quad L_M = k\sqrt{L_1 L_2} \tag{2}$$

where $0 \le k \le 1$ denotes the coupling coefficient, while v_1, i_1 and v_2, i_2 represent the input and output LCT voltages and currents, respectively [7]. As shown in [12], (2) may be realized by generalized ideal-transformer-based equivalent circuit, as shown in Fig. 2, where

$$L_{1L} = \left(1 - \frac{k}{\alpha}\right) L_1, \quad L_{2L} = (1 - \alpha k)\, L_2,$$
$$L_{ML} = \frac{k}{\alpha} L_1, \quad n = \alpha \sqrt{\frac{L_2}{L_1}} \tag{3}$$

for a constant arbitrary α. Series leakage elements L_{1L} and L_{2L} are typically considered inductive [i.e., L_{1L}, $L_{2L} > 0$ in (3)], imposing

$$1 - k\alpha^{-1} > 0, \quad 1 - \alpha k > 0. \tag{4}$$

Eliminating series leakage inductances by resonating them at operating frequency ω with series compensating capacitances

$$C_1^{-1} = \omega^2 L_{1L} = \omega^2 \left(1 - k\alpha^{-1}\right) L_1$$
$$C_2^{-1} = \omega^2 L_{2L} = \omega^2 \left(1 - \alpha k\right) L_2 \tag{5}$$

as shown in Fig. 3(a), yields the electrical first-harmonic equivalent circuit of SS-compensated LCT, as depicted in Fig. 3(b).

The resulting voltage gain given by

$$G_V = \frac{|\vec{v}_{\text{rec}}|}{|\vec{v}_{\text{inv}}|} = |n| = \left|\alpha \sqrt{L_1^{-1} L_2}\right| \tag{6}$$

is obviously load independent. Hence, in order to obtain a certain load gain value G_V^*, α should be selected as follows:

$$\alpha = \pm G_V^* \sqrt{L_1 L_2^{-1}}. \tag{7}$$

As shown in [13], rectifier input impedance (at LIVO frequency) $\vec{Z}_O$ is slightly inductive (i.e., $\vec{Z}_O = V_O^2/P_O + jX_O$), yet may be well-approximated as pure resistive in practice [14]. Referring consequently to Figs. 1 and 3, secondary current phasor is given by

$$\vec{i}_2 = \vec{i}_{\text{rec}} = \frac{\pi}{2} \frac{P_O}{V_O}. \tag{8}$$

Inverter current phasor is then found as [cf. (3), (7), and Fig. 3]

$$\vec{i}_{\text{inv}} = \vec{i}_1 = n\vec{i}_2 + \vec{i}_{ML} = \frac{\pi}{2} G_V^* \frac{P_O}{V_O} - j \frac{4}{\pi} \frac{V_O}{j\omega k \sqrt{L_1 L_2}} \tag{9}$$

with corresponding magnitude given by

$$I_{\text{inv}}^{\text{SS}} = \left|\vec{i}_{\text{inv}}\right| = \frac{\pi}{2} G_V^* \frac{P_O}{V_O} \sqrt{1 + \left(\frac{8}{\pi^2} \frac{V_O^2/P_O}{G_V^* \omega k \sqrt{L_1 L_2}}\right)^2}. \tag{10}$$

Inverter apparent power is obtained as follows:

$$\vec{S}_{\text{inv}} = \frac{1}{2} \vec{v}_{\text{inv}} \vec{i}_{\text{inv}}^{\,*} = \underbrace{P_O}_{P_{\text{inv}}} + j \underbrace{\frac{8}{\pi^2} \frac{V_O^2}{G_V^* \omega L_M}}_{Q_{\text{inv}}} \tag{11}$$

and corresponding VA rating is then given by

$$S_{\text{inv}}^{\text{SS}} = \left|\vec{S}_{\text{inv}}\right| = P_O \sqrt{1 + \left(\frac{8}{\pi^2} \frac{V_O^2/P_O}{G_V^* \omega L_M}\right)^2}. \tag{12}$$

III. Attaining Zero-Phase Angle (ZPA)

Inverter output impedance at operating frequency and corresponding phase angle in Fig. 3 are given by [cf. (2), (3), (7)]

$$\vec{Z}_I = \frac{8}{\pi^2} \frac{V_O^2/P_O}{n^2} \left\| j\omega L_{ML} = \frac{8}{\pi^2} \frac{V_O^2/P_O}{\left(G_V^*\right)^2} \right\| j\omega L_M \frac{\text{sgn}(\alpha)}{G_V^*},$$
$$\arg \vec{Z}_I = \tan^{-1}\left(\frac{8}{\pi^2} \frac{V_O^2/P_O}{\alpha k \omega L_2}\right) = \text{sgn}(\alpha)$$
$$\cdot \tan^{-1}\left(\frac{8}{\pi^2} \frac{V_O^2/P_O}{G_V^* \omega L_M}\right). \tag{13}$$

In case, $\alpha > 0$ is selected in (7) (prior art), its value should reside within the range

$$k \le \alpha \le k^{-1} \tag{14}$$

to satisfy (4) [7]. Corresponding inverter phase angle in (13) is then positive (i.e., the output impedance is inductive), allowing

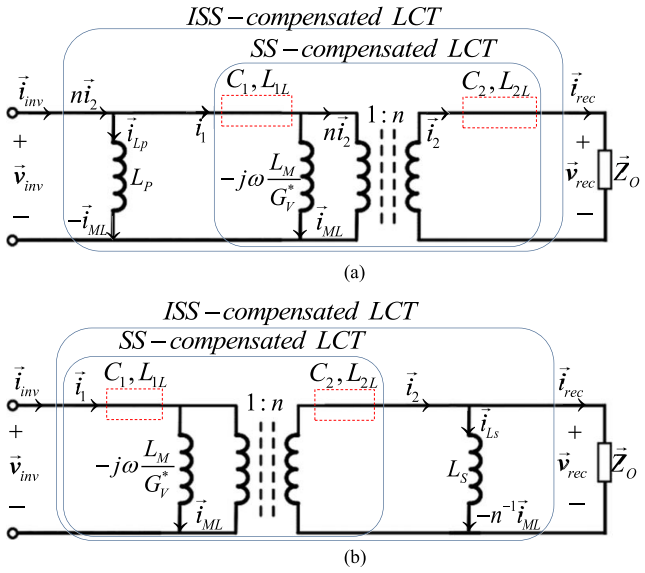

Fig. 4. ISS compensation of the LCT to attain LIVO and ZPA. (a) Primary-side compensation. (b) Secondary-side compensation.

attaining ZVS. However, when

$$G_V^* \omega L_M >> \frac{8}{\pi^2} V_O^2 / P_O \tag{15}$$

does not hold, the inverter provides significant reactive current to the resonant network, resulting in VA rating aggravation. In order to minimize inverter phase angle (consequently reducing VA rating), additional compensating capacitance may be connected across either inverter or rectifier terminals to resonate with L_{ML} at operating frequency. Unfortunately, addition of shunt capacitance across a switched voltage source/load is undesirable due to high imposed *dv/dt*. Consequently, a series inductance must be inserted between shunt compensating capacitance and ac-side terminals of the inverter (or rectifier). Unfortunately, additional series inductance has to withstand full-rating inverter (or rectifier) current, while parallel compensating capacitance gives rise to high circulating currents, deteriorating the efficiency [9], [10].

On the other hand, if $\alpha < 0$ is selected in (7) (original contribution), then (4) is satisfied unconditionally. Corresponding inverter phase angle in (13) is then negative (i.e., the impedance $\vec{Z}_I$ in Fig. 3(b) is capacitive) since L_{ML} in (3) attains a negative value, i.e., equivalent to a capacitance

$$C_{ML} = -\frac{\alpha}{\omega^2 k L_1} = \frac{G_V^*}{\omega^2 L_M} \tag{16}$$

at operating frequency. Consequently, additional compensating inductance may be connected across either inverter [L_P, cf. Fig. 4(a)] or rectifier [L_S, cf. Fig. 4(b)] terminals to resonate with C_{ML} at operating frequency, i.e.,

$$L_P = |L_{ML}| = \frac{1}{\omega^2 C_{ML}} = \frac{L_M}{G_V^*}, \quad L_S = n^2 |L_{ML}| = G_V^* L_M \tag{17}$$

respectively, to minimize the inverter phase angle. The resulting compensation network is referred to as inductor + SS = ISS compensation in Fig. 4. Referring to Figs. 1 and 4(a), secondary current phasors are given by (8), while compensating inductance current phasor is given by

$$\vec{i}_{Lp} = -\vec{i}_{ML} = j\frac{4}{\pi}\frac{V_O}{j\omega k\sqrt{L_1 L_2}}. \tag{18}$$

Thus, inverter current phasor is obtained as [cf. (3), (7)]

$$\vec{i}_{\text{inv}} = \underbrace{n\vec{i}_2 + \vec{i}_{ML}}_{\vec{i}_1} + \underbrace{(-\vec{i}_{ML})}_{\vec{i}_{Lp}} = n\vec{i}_2 = \frac{\pi}{2} G_V^* V_O^2 / P_O = I_{\text{inv}}^{\text{ISS}}. \tag{19}$$

Inverter apparent power is obtained as follows:

$$\vec{S}_{\text{inv}} = \frac{1}{2}\vec{v}_{\text{inv}}\vec{i}_{\text{inv}}^* = P_O = S_{\text{inv}}^{\text{ISS}} \tag{20}$$

which is also corresponding VA rating. A similar result may be obtained from Fig. 4(b) as well. Comparing (12) and (20), the following is well-evident: inverter feeding an SS-compensated LCT supplies both load power (active) and power drawn by L_{ML} (reactive). On the other hand, inverter driving an ISS-compensated LCT supplies the reflected load power (active) only, while the power drawn by L_{ML} (reactive) is supplied by compensating inductance. Consequently, inverter VA rating reduction ratio (RRR) is given by

$$\text{RRR} = \frac{S_{\text{inv}}^{\text{ISS}}}{S_{\text{inv}}^{\text{SS}}} = \left(1 + \left(\frac{8}{\pi^2}\frac{V_O^2/P_O}{G_V^* \omega L_M}\right)^2\right)^{-0.5} < 1. \tag{21}$$

IV. Remarks

A. Influence on Losses

Comparing Figs. 3 and 4(a), it may be concluded that primary and secondary LCT current phasors are similar; hence, corresponding losses are similar as well. In case of SS compensation, inverter conduction losses are estimated as follows:

$$P_{\text{loss,inv}}^{\text{SS}} = r_{\text{sw,ss}} \left(I_{\text{inv}}^{\text{SS}}\right)^2 = r_{\text{sw,ss}} \left(\left(\frac{\pi}{2} G_V^* \frac{P_O}{V_O}\right)^2 + \left(\frac{4}{\pi}\frac{V_O}{\omega L_M}\right)^2\right) \tag{22}$$

where $r_{\text{sw,ss}}$ denotes the inverter switch (rated at least $I_{\text{inv}}^{\text{SS}}$) equivalent series resistance. On the other hand, in case of ISS compensation, inverter and compensating inductance conduction losses are estimated as follows:

$$P_{\text{loss,inv}}^{\text{ISS}} = r_{\text{sw,iss}} \left(I_{\text{inv}}^{\text{ISS}}\right)^2 = r_{\text{sw,iss}} \left(\frac{\pi}{2} G_V^* \frac{P_O}{V_O}\right)^2$$

$$P_{\text{loss,}Lp}^{\text{ISS}} = \frac{r_{Lp}}{2} \left(I_{Lp}^{\text{ISS}}\right)^2 = \frac{r_{Lp}}{2} \left(\frac{4}{\pi}\frac{V_O}{\omega L_M}\right)^2 \tag{23}$$

where $r_{\text{sw,iss}}$ and r_{Lp} denote the inverter switch (rated at least $I_{\text{inv}}^{\text{ISS}}$) and compensating inductance equivalent series resistances. Consequently, if

$$P_{\text{loss,inv}}^{\text{ISS}} + P_{\text{loss,}Lp}^{\text{ISS}} \approx P_{\text{loss,inv}}^{\text{SS}} \tag{24}$$

then shunt inductor addition does not deteriorate the efficiency.

TABLE I
SYSTEM PARAMETER VALUES

Parameter	Value	Units
P_O	250	W
V_I	200	V
L_1, L_2	180	μH
G_V^*	1	--
k	0.71	--
ω	2π·124.5	Krad/s

B. DC Component Elimination

It should be emphasized that the current flowing through compensating inductance may contain a dc component due to practical inverter or rectifier nonsymmetry. Hence, a capacitor possessing impedance valued much larger than that of the compensating inductance (at operating frequency) may be placed in series with it in order to block the dc current flow while preserving the above analysis accuracy. Alternatively, corresponding inductor current feedback adjusting inverter output may be utilized, requiring an extra current sensor.

V. EXAMPLE

Consider the SS-IWPTL designed in [6] and [8] for through-glass power delivery system into enclosed compartment. The corresponding parameter values are summarized in Table I. The system is intended to operate with unity load-independent voltage gain, i.e., $|\alpha| = 1$ [cf. (7)].

A. Series–Series Compensation

According to (5) with $\alpha = 1$, compensating capacitors pair is selected as $C_1 = C_2 = 31.3$ nF. According to (11), expected inverter apparent power is 250 W + j320VAR, indicating VA rating of 407 VA. Inverter rms current is obtained as 2.27 A_{rms}, formed by active and reactive components of 1.39 A_{rms} and 1.8 A_{rms}, respectively.

B. Series–Series + Primary Shunt Inductor Compensation

According to (5) with $\alpha = -1$, compensating capacitors pair is selected as $C_1 = C_2 = 5.3$ nF while compensating inductance is selected cf. (17) as $L_P = 127.8$ μF. According to (20), expected inverter apparent power is 250 W, indicating a similar VA rating. Inverter rms current is obtained as 1.39 A_{rms}, formed by active component only, while the 1.8 A_{rms} reactive component (i.e., 320 VAR of reactive power) is supplied to the network by compensating inductance. The RRR is then 1.39/2.27 ≈ 0.6, well-supported by (21)

C. Simulations

Fig. 5 depicts simulations results of the above example, where Fig. 5(a) presents waveforms obtained from first-harmonic-approximated linear equivalent circuit, while Fig. 5(b) demonstrates corresponding switched-circuit outcomes. It is well-evident that unity voltage gain, operational regions, and above-calculated analytical rms current values are accurately supported by simulations, as shown in Fig. 5(a). Even though

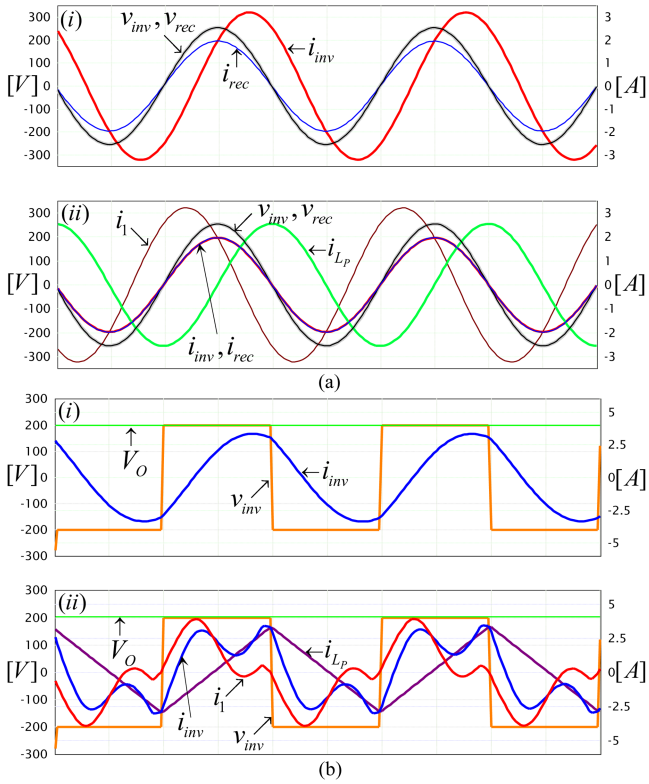

Fig. 5. Simulations, time scale 2 μs/div. (i) SS-IWPTL. (ii) ISS-IWPTL. (a) First-harmonic approximation. (b) Switched model.

the LCT primary-side current i_1 of ISS-IWPTL is capacitive, it is compensated by shunt inductance current i_{Lp} (triangle shaped in reality due to inverter-imposed square-wave voltage, as expected) so that inverter current $i_{\rm inv}$ is minimized and ZVS is retained, as desired.

D. Experiments

In order to experimentally validate the presented analysis and simulation outcomes, the prototype presented in [6] and [8] was employed. The inverter was realized utilizing 650 V, 150 mΩ TPH3206PSB gallium nitride field-effect transistors driven by Silicon Labs SI8273AB1 isolated drivers. Switching signals were generated by Texas Instruments F28335 digital signal processor-based control card. The receiving-side rectifier was realized by means of Microsemi APT40DQ120BG ultrafast soft recovery diodes. The WPT link was fed from IT61517D ITECH high-voltage dc power supply and terminated by Maynuo M9715B dc electronic load, operated in constant power mode. Fig. 6 depicts the corresponding experimental results, where Fig. 6(a) presents the primary ac-side voltage and current along with secondary dc-side voltage of SS-compensated IWPTL and Fig. 6(b) presents the primary ac-side voltage, inverter, and compensating inductance currents along with secondary dc-side voltage of primary-side-inductance ISS-compensated IWPTL. It may be concluded that unity-gain operation is sustained and current waveforms accurately follow the corresponding simulations.

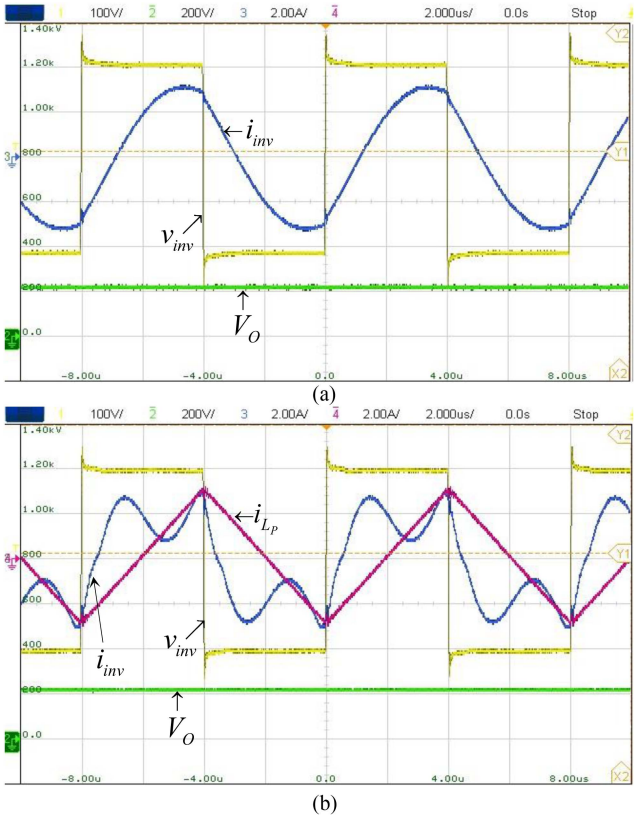

Fig. 6. Experimental results. Time scale: 2 μs/div. (a) SS-IWPTL. (b) ISS-IWPTL.

VI. Conclusion

In this letter, capacitive region of operation was selected for an SS-IWPTL attaining LIVO and additional compensation shunt inductor was applied. As a result, output characteristics of the system remained nearly unchanged, while inverter VA rating was minimized by diverting the reactive power from the inverter to the additional inductor.

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