Real-Time Extraction of SiC MOSFETs' Degradation Features Under Improved Accelerated Power Cycling Tests for DC-SSPC Application

Bin Yu, *Member, IEEE*, and Li Wang, *Member, IEEE*

***Abstract*—The SiC MOSFET is a key component of the dc solid-state power controller (DC-SSPC). The reliability of DC-SSPCs can be improved by real-time online monitoring of the degradation of SiC MOSFETs. At present, the degradation of SiC MOSFETs can be indirectly monitored using thermosensitive electrical parameters (TSEPs); however, their degradation can cause nonnegligible measurement errors. Another limitation is that one type of TSEPs can only reflect a certain form of the degradation process. On this basis, in this article, the real-time extraction method of SiC MOSFETs' degradation features under improved accelerated power cycling tests for DC-SSPC application (i.e., average and standard deviation of the ON-state resistance change rate (*avgk* and *stdk*) of the improved accelerated power cycling test) is proposed. The *avgk* and *stdk* can be easily obtained by simple calculations. This method can not only directly monitor the severe degradation of bonding wires, but it can also monitor the severe degradation of the solder layer without measuring the junction temperature (T_J). Compared with the traditional solder layer degradation feature extraction method using thermal resistance, for which T_J is essential, the monitoring results using the proposed method are not affected by the degradation of TSEPs. Finally, the effectiveness of the proposed method is verified by experimental results.**

***Index Terms*—Degradation features, ON-sate resistance change rate, real-time, SiC MOSFET , solid-state power controller.**

I. Introduction

SINCE SiC MOSFETs have the characteristics of smaller ON-resistance(R_{dson}) and the ability to withstand high temperatures and antiradiation compared to Si-based devices, they are preferred and used more in the modern dc solid-state power controller (DC-SSPC) [1], [2], [3], [4]. Consequently, the power density and reliability of the DC-SSPC can be improved. As more and more attention is paid to the long-term reliability of DC-SSPCs, research interest is increasing in online health status monitoring technology [5], [6]. The SiC MOSFET, as the critical component of DC-SSPCs, undertakes the task of switching ON and OFF high-power loads, which will cause the large junction temperature swing (ΔT_J) in the SiC die [7], [8]. As the significant ΔT_J change is the main factor causing the degradation of SiC MOSFET [9], [10], the real-time monitoring of the degradation of SiC MOSFETs for DC-SSPCs is essential for the long-term safe operation of DC-SSPCs [5].

The accelerated power cycling test (APCT) is often used to evaluate the degradation mechanism of power devices [10], [11], [12]. Different working modes will produce other degradation mechanisms; therefore, it is necessary to set up the suitable APCT according to the actual working modes of the power devices. The conventional APCT can be divided into two types, i.e., ac APCT (AC-APCT) and dc APCT (DC-APCT), according to the difference in the driver voltage during the heating phase of the APCT (HP-APCT) [12]. In the AC-APCT, the driver voltage during the HP-APCT is controlled by the pulsewidth modulation signals. It presents the high-frequency varying in positive and negative voltages (or zero voltage), which is consistent with the working modes of the high-frequency converter [13]. In the DC-APCT, the driver voltage always has a positive value during the HP-APCT. However, in the cooling phase of the APCT (CP-APCT), the driving voltage is switched to zero or a negative value, or the driving voltage still has a positive value where the drain current (I_d) is only milliampere level [13], [14]. The two APCTs mentioned above are unsuitable for the operating conditions of DC-SSPCs. As the switching device, DC-SSPC will be in the steady ON-state for a long time after the load is connected, and the current of power device for DC-SSPCs (i.e., I_d) will vary from several amperes (i.e., low rated current) to dozens of ampere (i.e., overcurrent to protect the wire from the overheating damage) [2], [8], [15], [16], [17]. The low rated current means low power loss, leading to the small ΔT_J in the die of the power device, which can be used as the CP-APCT. In contrast, the high overcurrent means high power loss, leading to the large ΔT_J in the die of the power device, which can be used as the HP-APCT. Keeping the above-mentioned in view, this type of working mode of DC-SSPCs means that one cycle of the dc accelerated power test has been carried out on its power device. Therefore, the dc accelerated power test based on DC-SSPC working modes is different from the conventional DC-APCT in terms of the setting of the cooling phase. Moreover, the gate oxide layer of the current commercial

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SiC MOSFETs has defects, which are more vulnerable to the drive voltage and lead to damage or unstable performance of SiC MOSFETs [18], [19], [20]. Therefore, in this article, the DC-SSPC working modes are refined into the improved dc APCT (ImDC-APCT).

Another problem is how to simply and effectively extract the degradation features online for real-time monitoring of the degradation degree of SiC MOSFETs. For SiC MOSFETs, both the package degradation [10], [11] and the die degradation (e.g., gate oxide layer degradation) [18] exist simultaneously. If one degradation feature, which reflects the above-mentioned primary degradation mode of the SiC MOSFET for DC-SSPCs, can be extracted in real-time, then the health status of SiC MOSFETs can be evaluated based on degradation features. Then, effective measures can be taken in advance to improve the reliability of the DC-SSPC. In the existing research, one degradation feature is only used to reflect one degradation mode of SiC MOSFETs, and the influence of other degradation modes on this feature is ignored [11], [21]. This research method is conducive to studying the weakness of SiC MOSFETs. However, multiple degradation modes of SiC MOSFETs are always coinciding and interrelated [10]. One problem is that other degradation modes may also affect one degradation feature that is used to evaluate a particular degradation mode. Therefore, it is difficult to use one feature for a reliable assessment of the degradation status of SiC MOSFETs [22], [23]. In addition, even without considering the interrelated effects of multiple degradation modes, multiple degradation features must be monitored online simultaneously to fully understand the health status of SiC MOSFETs. It increases the complexity and cost of the monitoring circuit and is not convenient for practical applications.

In order to understand these above-mentioned limitations more clearly, the traditional degradation features are discussed in this paragraph. Thermal resistance ($R_{\rm th}$) is often used as an essential feature to reflect solder layer degradation [11]. The thermosensitive electrical parameter (TSEP), such as the ON-state resistance ($R_{d\rm son}$), the ON-state voltage ($V_{d\rm son}$), the forward voltage of the reverse diode, and threshold voltage ($V_{\rm th}$), is usually used to indirectly measure the $R_{\rm th}$ without destroying the SiC MOSFET package [18], [24], [25]. In order to obtain $R_{\rm th}$ indirectly, it is necessary to first obtain the calibration curve of the TSEP to the T_J. However, the die and bonding wire degradation of SiC MOSFETs will cause the above-mentioned calibration curve errors, which will cause the $R_{\rm th}$ unacceptable measurement error [10], [18], [26].

The $R_{d\rm son}$ during the cooling phase of the ImDC-APCT($R_{d\rm son\,L}$) can be accurately measured online by the drain–source voltage clamp circuit [5]. Therefore, it can be used to evaluate the bonding wire degradation and the die degradation [9]. However, the power loss of the SiC MOSFET during the cooling phase is small, which is insufficient to cause its self-heating. So, it is usually not used to evaluate the degradation of the solder layer and the thermal interface material (TIM). As mentioned above, $V_{\rm th}$ is the feature reflecting the degradation of the SiC die, yet it cannot be measured online for the DC-SSPC working mode. Hence, it is also not the ideal feature to comprehensively reflect the SiC MOSFET's degradation trend.

It is worth noting that both the SiC die degradation (i.e., the threshold voltage degradation) and the bonding wire degradation will increase the $R_{d\rm son}$ during the heating phase of the ImDC-APCT ($R_{d\rm son\,H}$). In addition, both the TIM degradation and the solder layer degradation will cause the $R_{\rm th}$ to increase, which in turn will lead to an increase in T_J , and finally, the $R_{d\rm son\,H}$ will also be increased. Thus, $R_{d\rm son\,H}$ is an outstanding feature that can fully reflect the degradation of SiC MOSFETs. In this research, $R_{d\rm son\,H}$ is often used as a TSEP to measure the T_J indirectly [5], [27], and it is rarely used for the evaluation of the degradation status of SiC MOSFET. In [28], although $R_{d\rm son\,H}$ is used to evaluate the SiC MOSFET health status, the degradation information of the bonding wire and the solder layer cannot be recognized. Therefore, it is difficult to comprehensively understand the SiC MOSFETs health status, and reasonable health management measures cannot be taken in advance.

Keeping in view the limitations of the traditional condition monitoring method, in this article, the real-time extraction method of SiC MOSFETs' degradation features under ImDC-APCT for the DC-SSPC is proposed. This method can directly monitor the severe degradation of the bonding wire and the solder layer without measuring the junction temperature. Compared with the traditional method of using $R_{\rm th}$ to monitor the solder layer degradation, this method has the advantage that the monitoring results are not affected by the TSEP degradation. In Section II, first, the ImDC-APCT principle is introduced in detail, then, the influence of the main degradation modes (i.e., $V_{\rm th}$ degradation, TIM degradation, bonding wire degradation, and solder layer degradation) of SiC MOSFETs on the $R_{d\rm son}$ during the heating phase is comprehensively analyzed, and finally, the implementation and verification processes of the proposed method are presented in detail. In Section III, the test platform is described in detail. In Section IV, the 650 V/17 mΩ (Part #: sct3017al) commercial SiC MOSFET from Rohm Co., Ltd. is used with the device under test (DUT) to verify the effectiveness of the proposed method. Finally, Section V concludes this article.

II. Proposed Degradation Monitoring Method of SiC MOSFETs

The principle of the ImDC-APCT designed for the operating characteristics of the DC-SSPC is introduced. Furthermore, the influence of the main degradation modes of SiC MOSFETs on the $R_{d\rm son}$ is comprehensively analyzed to comprehend its possible limitation, with the aim of modeling the $R_{d\rm son}$ for the degradation feature extraction of SiC MOSFETs. On this basis, the proposed method for the real-time extraction of SiC MOSFETs' degradation features using the average of the $R_{d\rm son\,H}$ change rate (*avgk*) and the standard deviation of the $R_{d\rm son\,H}$ change rate (*stdk*) is described. Finally, the verification process of the proposed method is also analyzed.

A. Improved DC Accelerated Power Cycling Test

As discussed in Section I, when the two operating states of DC-SSPCs are combined in the one-time cycle, an ImDC-APCT derived from the actual operating state of the DC-SSPC is proposed.

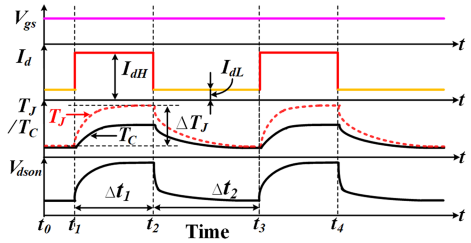


Fig. 1. Operating waveform of the ImDC-APCT of SiC MOSFETs.

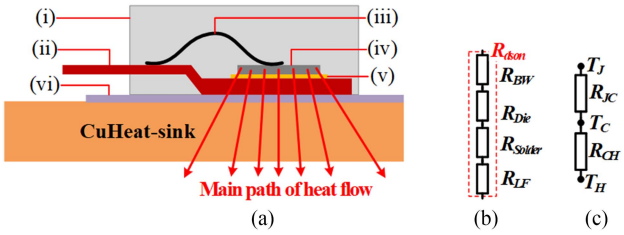


Fig. 2. Physical structure of the SiC MOSFET with the To247 package considering the main heat flow path (a) and its equivalent R_{dson} (b) and equivalent thermal resistance (c).

Fig. 1 shows the operating waveform of the ImDC-APCT of SiC MOSFETs, and the operating principle is described as follows.

t_1–t_2: The DC-SSPC overcurrent operating state is simulated, i.e., the SiC MOSFET is ON-state with a large enough heating current I_{dH}, keeping enough time $\triangle t_1$ to enable the SiC MOSFET to enter the thermally stable steady state.

t_2–t_3: The rated current operating state of the DC-SSPC is simulated, i.e., a low cooling current I_{dL} is applied to SiC MOSFETs and maintained for a long enough time $\triangle t_2$ to completely cool down SiC MOSFETs. Due to the low I_{dL} value, the T_J and case temperature (T_C) are approximately equal at t_3.

After t_3, a new power cycling has been performed again.

In the complete power cycling period, the drive voltage of the SiC MOSFET has been maintained at a relatively high value (e.g., 18 V), and $\triangle T_J$ is large enough to achieve the accelerated degradation of SiC MOSFETs. Since the standard MIL-STD-1760D has to be implemented when the DC-SSPC is applied, the time $\triangle t_1$ and $\triangle t_2$ (shown in Fig. 1) selection should also be based on the standard (the detailed analysis is presented in Section IV). The I_{dH} value will be determined by the R_{dson} and R_{JC} of the actual DUT, so that the $\triangle T_J$ of the DUT in the heating phase is higher than 80 °C. When the I_{dL} value is selected, there are two things to be considered: First, throughout the life time of the DUT, the power loss of the DUT is low, so that the DUT can be cooled in the cooling phase, i.e., at the end of the cooling phase of the DUT, the T_J is approximately equal to the T_C; and second, the I_{dL} value is large enough that it can be simulated as the real rated working current of the DC-SSPC, e.g., several amperes.

B. Influence of the Main Degradation Modes of SiC mosfets on the on-State Resistance

Fig. 2 shows the SiC MOSFET physical structure with the To247 package, considering the primary heat flow path (a) and its equivalent R_{dson} (b) and equivalent thermal resistance (c). In Fig. 2(a), (i)–(vi) represent the mold resin, the lead frame, the bonding wire, the SiC die, the solder layer, and the TIM, respectively. In Fig. 2(b), R_{BW} represents the bonding wire resistance, R_{Die} represents the SiC die resistance, R_{Solder} represents the solder layer resistance, and R_{LF} represents the lead frame resistance. It should be noted that the lead frame is composed of copper with a large cross-sectional area through the current; herein, the R_{LF} value is small and not easily affected by degradation. Fig. 2(c) shows the equivalent steady-state thermal resistance of the SiC MOSFET considering the entire heat flow path, where R_{JC} is the junction-case thermal resistance, R_{CH} is the TIM thermal resistance, and T_H is the CuHeat-sink temperature. In this section, the effect of several main degradation modes of the SiC MOSFET on the R_{dson} will be comprehensively analyzed according to Fig. 2.

1) Influence of Gate Oxide and TIM Degradation on $\mathrm{R_{ds}}_{on}$*:* First, the influence of gate oxide degradation on the R_{dson} is analyzed. According to Aichinger et al. [29], the SiC die resistance (R_{Die}) is typically composed of three major components

$$R_{\mathrm{Die}} = R_{\mathrm{chan}} + R_{\mathrm{JFET}} + \mathrm{R_{epi}} \tag{1}$$

where R_{chan} is the channel resistance, R_{JFET} is the junction-field-effect-transistor (JFET) resistance, and R_{epi} is the epitaxial layer resistance of the drift region.

According to Aichinger et al. [29] and Yang et al. [30], in SiC MOSFETs, the R_{chan} can make up to 50% of the total die resistance due to the lower inversion carrier mobility at the gate oxide layer interface and the depletion of charge density due to enhanced electron trapping. When the effect of temperature [10] is taken into account, R_{chan} can be expressed as follows:

$$R_{\mathrm{chan}} = L_{\mathrm{CH}}(T_J + 273)^k / \left[300^k Z \mu_0 C_{\mathrm{ox}} \left(V_{gs} - V_{\mathrm{th}}\right)\right] \tag{2}$$

where L_{CH} is the channel length, Z is the channel width, C_{ox} is the specific capacitance of the gate oxide layer, μ_0 is a constant related to electron mobility and semiconductor processing, V_{gs} is the driving voltage, and the index k varies from 1 to 2.5.

As a consequence, the R_{Die} of SiC MOSFETs is more sensitive to V_{gs} and V_{th}. When high electric field intensity and thermal stress are applied to the gate oxide layer interface, the V_{th} drift is observed, leading to a change in R_{chan} and thus affecting R_{Die}.

As described in Section II-A, in the ImDC-APCT, the SiC MOSFET gate has been subjected to a high positive drive voltage. Since defects exist at the gate oxide layer interface, the positive V_{th} shift phenomenon will occur more frequently. Therefore, according to (1), R_{Die} will increase. Moreover, R_{Die} increase will lead to an increase in power loss, causing an increase in T_J, which in turn further causes an increase in R_{Die} .

Fig. 3 depicts the V_{th} degradation phenomenon based on the actual SiC MOSFET test result (i.e., sct3017al) on the ImDC-APCT platform (presented in Section III). It can be seen that as the number of APCTs (i.e., i) increases, V_{th} gradually increases [i.e., V_{th} is increased by 0.34 V (0.34 V = 5.51 V − 5.17 V)]. Since the drive voltage of SiC MOSFETs is usually higher (in this article, $V_{gs} = 18$ V), if only the V_{th} degradation is considered, according to (2), the R_{chan} will increase by about 2.7% [2.7% = 0.34 V/(18 V − 5.51 V)], and this small increase also demonstrate the maturing SiC manufacturing technology.

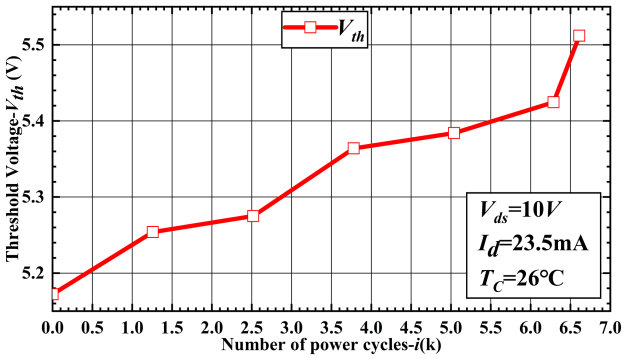


Fig. 3. $V_{\rm th}$ value at different numbers of power cycles based on the actual SiC MOSFET test result.

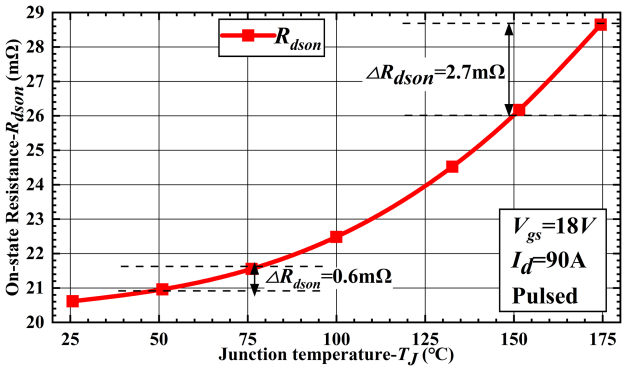


Fig. 4. R_{dson} of undegraded SiC MOSFET at diferent T_J values and $I_d = 90$ A.

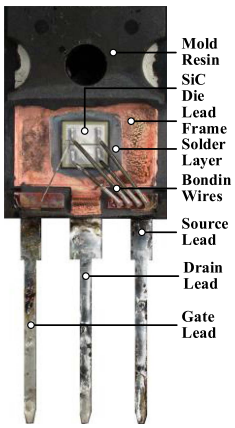


Fig. 5. Inner structure of the decapsulated DUT (DUT is 1# SiC MOSFET).

Second, according to Fig. 2(c), the relationship between the $R_{\rm CH}$ and the T_J can be obtained as follows:

$$T_J = I_d V_{\rm dson}\left(R_{\rm JC} + R_{\rm CH}\right) + T_H. \tag{3}$$

From (3), the TIM degradation will directly lead to an increase in $R_{\rm CH}$ and ultimately cause an increase in T_J. Combining 1) and (2), it can be seen that the TIM degradation will eventually lead to an increase in the R_{dson}.

In addition, another factor that motivates us to use the R_{dson} to monitor the degradation of SiC MOSFET will be explained here. Fig. 4 shows the R_{dson} value of the undegraded SiC MOSFET under the different T_J values and the constant I_d (i.e., $I_d = 90$ A), and it was obtained using the "short pulse current method" [5]. From Fig. 4, the higher the T_J, the greater the R_{dson} change (ΔR_{dson}) during the same ΔT_J. For example, when the T_J increases from 50 to 75 °C, the ΔR_{dson} is only 0.6 mΩ. Nevertheless, when the T_J increases from 150 to 175 °C, the ΔR_{dson} increases to 2.7 mΩ, which is 4.5 times the ΔR_{dson} under the low T_J value.

During the HP-APCT, the T_J is high (e.g., varying from 150 to 175 °C); hence, the $V_{\rm th}$ and the TIM degradation are easier to observe by monitoring the $R_{dson\,H}$. During the CP-APCT, the T_J is approximately equal to the T_C, which is controlled by a water cooling system and kept at a constant value; therefore, the $V_{\rm th}$ degradation can be monitored using $R_{dson\,L}$, whereas the TIM degradation has little influence on the $R_{dson\,L}$ due to the low power loss.

2) Influence of the Bonding Wire Degradation on $\rm R_{ds\,on}$*:* First, the external package of the DUT (DUT is 1# SiC MOSFET tested in Section IV) needs to be decapsulated using the laser equipment and the acid solution to ensure that the inner structure of the DUT is not damaged. The size of each layer of the DUT is measured and listed in Table I. In Fig. 5, the inner structure of the decapsulated DUT is shown. In addition, the material properties of each layer of the DUT are also presented in Table II, which is the basis for subsequent theoretical calculations. For a brand-new bonding wire, its resistance value can be expressed as follows:

$$R_{\rm BW} = \rho_{\rm BW}\frac{l_{\rm BW}}{A_{\rm BW}} \tag{4}$$

where $\rho_{\rm BW}, l_{\rm BW}$, and $A_{\rm BW}$ represent the resistivity, length, and cross-sectional area of the bonding wire, respectively.

Due to the mismatch of coefficients of thermal expansion among SiC dies, aluminum bonding wires, and solder layers, the bonding wire connection and the solder layer are the weakest and most easily degraded parts in the APCT [31]. Heel part cracks, interface cracks, delamination, lift-offs, and fracture are more likely to occur than internal voids in the bonding wire [10]. Generally, the degradation process of the bonding wire degradation is gradually developed from cracks and delamination to the final lift-offs or fracture, which will cause a decrease in the total cross-sectional area through the current, and as a result, the $R_{\rm BW}$ will inevitably increase gradually.

Before the bonding wire is about to be lifted off, the contact part between the bonding wire and the SiC die has been loosened, and therefore, the thermal shock caused by the APCT will contribute to irregular changes in the cross-sectional area through the current. The irregular change caused by the bonding wire degradation is not a maddening thing. We can identify the degradation process by using the mathematics standard deviation.

When the bonding wire is finally lifted off or fractured, the contact area will suddenly drop to zero. It is bound to be observed that the $R_{\rm BW}$, especially the $R_{\rm BW}$ in the cooling phase, suddenly increases, which can be used to detect the bonding wire lift-off phenomenon [18], [32]. In [32], the diagram of the bonding wire lift-off was displayed. It can be seen that the bonding wire

TABLE I
DIMENSION INFORMATION OF EACH PART OF THE DUT (I.E., SCT3017AL)

Structure item	Material	Length (mm)	Width (mm)	Height (mm)	Diameter (mm)
Die	SiC	4.8	4.8	0.33	
Solder layer	Pb Sn Ag	6.8	6.8	0.07	
Lead frame	Cu	17	14	2	6.6
Bonding wire	Al	10/7/10			0.375/0.05

Note: The diameter of source bonding wires is 0.375 mm, and their lengths are 10 and 7 mm, respectively. The diameter of the gate bonding wire is 0.05 mm.

TABLE II
RELATED PROPERTY PARAMETERS OF THE DUT (I.E., SCT3017AL) PACKAGING MATERIAL

Material	Thermal conductivity [W/(m·K)]	Specific heat capacity [J/(kg·K)]	Resistivity (μΩ·m)	Density (kg·m^{-3})	Poisson ratio	Young modulus (GPa)	Coefficient of thermal expansion (10^{-6}/K)
SiC	490	690	0	3216	0.45	749	4.3
Pb Sn Ag	35	150	0.2083	9000	0.4	10	21
Cu	400	385	0.0172	8960	0.35	110	17
Al	238	900	0.0283	2700	0.33	70	23

lift-off will cause the current initially borne by the lifted-off bonding wire to transfer to these remaining bonding wires that are well bonded. Thereby, it leads to a decrease in the total A_{BW} value. As a result, the sudden $R_{d\mathrm{son}}$ increase phenomenon can be manifested. In addition, with the increase in the number of lifted-off bonding wires, the current density of bonding wires will increase rapidly, which will increase the temperature of the SiC die and bonding wires during the heating phase and accelerate the bonding wire degradation speed [10]. For example., according to Tables I and II and (4), the resistances of the brand-new longer source bonding wire and shorter bonding wire can be calculated as 2.564 and 1.795 mΩ, respectively, and the total resistance of bonding wires is about 0.5278 mΩ [0.5278 mΩ = (0.5∗2.564 mΩ + 0.5∗1.795 mΩ)/(0.5∗2.564 mΩ∗0.5∗1.795 mΩ)]. When only one longer bonding wire is lifted off and the degradation of other bonding wires is not considered, at least 0.14 mΩ increases in R_{BW}, which is easy to observe in $R_{d\mathrm{son}L}$.

Then, the thermal–mechanical coupling simulation based on the multiphysical field simulation software Comsol Multiphysics is carried out to analyze the stress on the bonding wire under the power cycling. Fig. 6 shows the simulation result of the internal temperature distribution of the DUT at the end of the heating phase, and Fig. 7 shows the simulation result of the stress distribution of the internal structure of the DUT at the heating phase. According to Figs. 6 and 7, due to the temperature gradient and the difference in the thermal expansion coefficients among each layer material of the DUT, greater stress and an obvious deformation ($\Delta\lambda$) will be generated on the bonding wire. It is a fundamental reason for the bonding wire degradation and the irregular change in the $R_{d\mathrm{son}}$.

3) Influence of Solder Layer Degradation on $\mathrm{R_{ds}}_{on}$*:* The main degradation modes of the solder layer are layer cracks, voids, and delamination [32], [33], which will lead to a reduction in the contact area between the SiC die and the lead frame [see Fig. 2(a)]. On the one hand, this will directly cause an increase in R_{Solder}; on the other hand, it will also cause an increase in R_{JC}, which indirectly leads to an increase in R_{Die} according to (1) and (2), and this increase is more obvious than the increase in R_{Solder} .

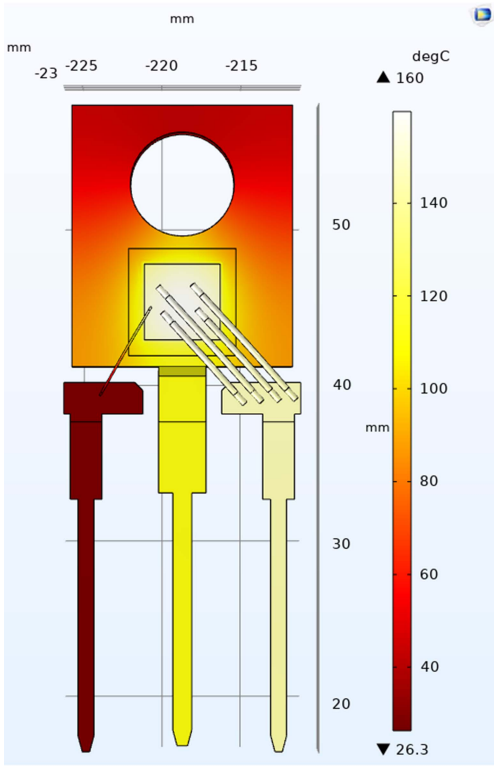


Fig. 6. Simulation result of the internal temperature distribution of the DUT at the end of the heating phase.

Similar to the analysis when the bonding wire is severely degraded (i.e., delamination), each thermal shock will cause the irregular change in the contact area between the solder layer and the SiC die, which will not only lead to an irregular change in R_{Solder} but also cause an irregular change in T_J during the heating phase due to the irregular change in R_{JC} , and finally, the R_{Die} irregular change of the heating phase will be shown. Different from the bonding wire, due to the large contact area between the solder layer and the SiC die and the effect of gravity, even if the solder layer is severely degraded, it is difficult to be

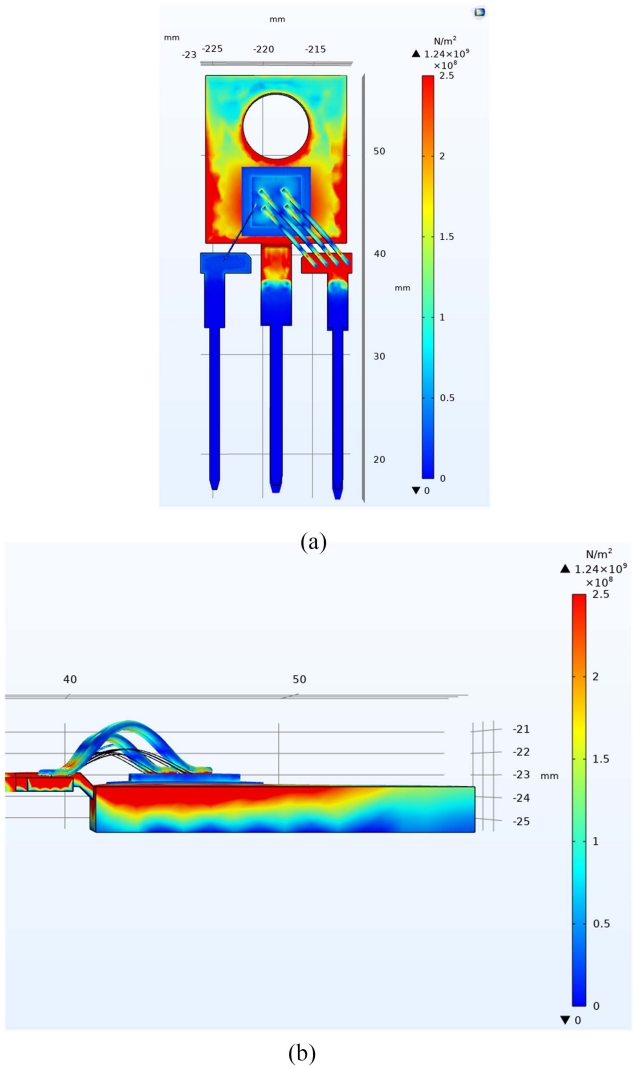


Fig. 7. Simulation result of the stress distribution in the internal structure of the DUT at the heating phase. (a) Front view. (b) Axis view. (c) Left view.

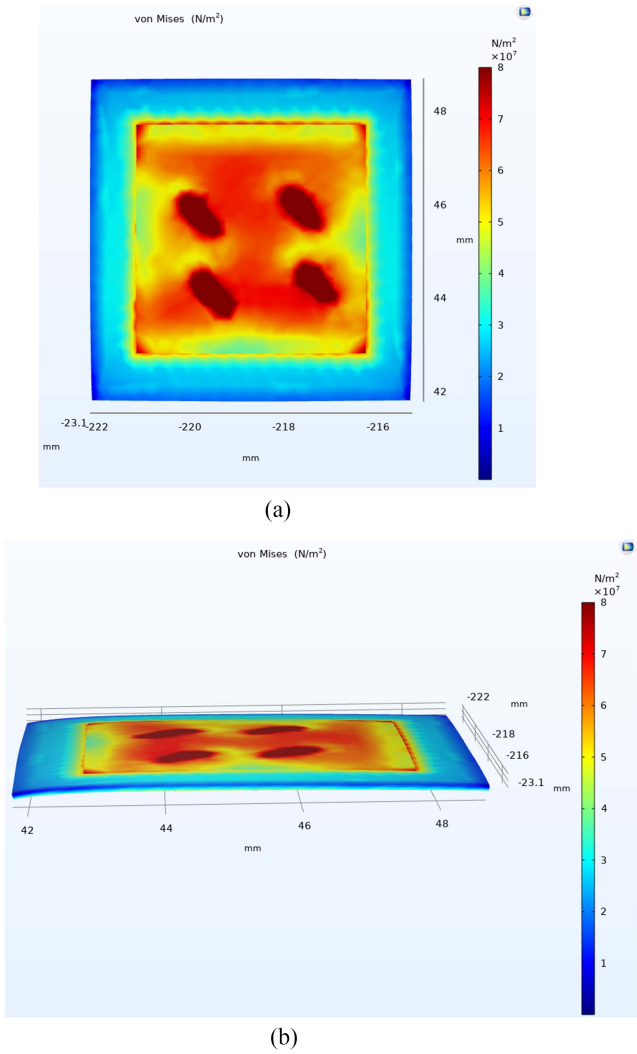


Fig. 8. Simulation result of the stress distribution of the internal structure of the DUT at the heating phase. (a) Front view. (b) Axis view. (c) Left view.

lifted off (i.e., wholly separated from the SiC die). Therefore, as the degradation becomes more and more serious, this irregular change becomes more evident and can be observed all the time. Similarly, it is also detected using the standard deviation in mathematics. In [33], a cross-sectional view of the delamination of the solder layer was given. It can be seen that the delamination of the solder layer will lead to poor contact between the SiC die and the lead frame, so when the thermal shock comes, the irregular changes in the R_{dson} can be monitored.

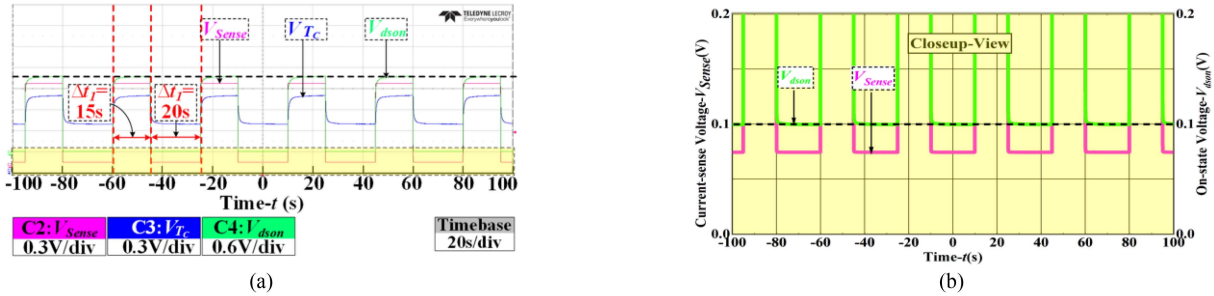
However, the R_{Solder} value is minimal, and it is difficult to observe the solder layer degradation status through the $R_{dson\,L}$. For example, for a brand-new solder layer, its resistance value can be expressed as follows:

$$R_{\text{Solder}} = \rho_{\text{Solder}} \frac{h_{\text{Solder}}}{A_{\text{Solder}}} \tag{5}$$

where ρ_{Solder}, h_{Solder}, and A_{Solder} represent the solder layer's resistivity, thickness, and cross-sectional area, respectively.

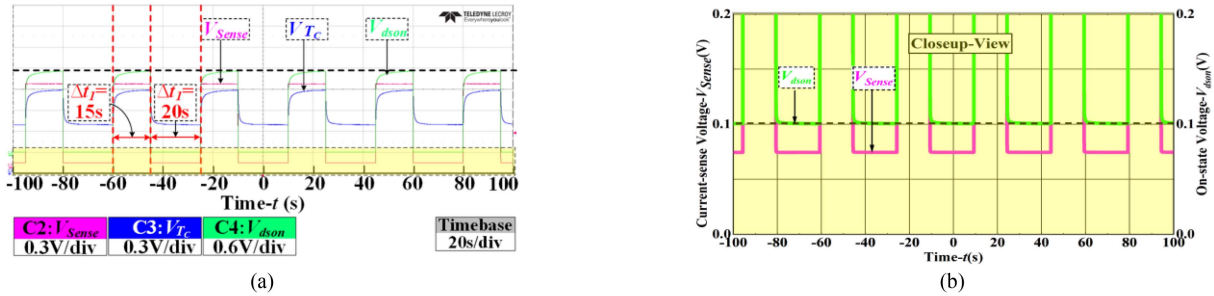
According to Tables I and II and (5), the resistance of the brand-new solder layer ($R_{\text{Solder-new}}$) can be calculated as $R_{\text{Solder-new}} = (\rho_{\text{Solder}} * h_{\text{Solder}})/A_{\text{Solder}} = 0.2083\ \mu\Omega\cdot\text{m} * 70\ \mu\text{m}/(4.8\ \text{mm} * 4.8\ \text{mm}) = 0.64\ \mu\Omega$, which is small and only 0.0012 times the total resistance of bonding wires (i.e., 0.0012 $= 0.64\ \mu\Omega/\ 0.5278\ \text{m}\Omega$). Suppose the influence of the A_{Solder} change on the R_{JC} is not considered temporarily. In that case, a bold assumption is made that A_{Solder} is reduced to 0.5 times the original value and ρ_{Solder} increased to ten times its original value due to the delamination and voids, and the change in the h_{Solder} is ignored, but even then, the R_{Solder} of the degraded solder layer ($R_{\text{Solder-deg}}$) is small, i.e., $R_{\text{Solder-deg}} = 10 * 2 * R_{\text{Solder-new}} = 20 * 0.64\ \mu\Omega = 12.8\ \mu\Omega$, and it is about 0.09 times ($0.09 = 12.8\ \mu\Omega/0.14\ \text{m}\Omega$) the change in the $R_{dson\,L}$ caused by the lift-off of one bonding wire and is not easy to be observed in the $R_{dson\,L}$.

Similarly, the solder layer stress distribution based on the Comsol Multiphysics software is shown in Fig. 8. From Fig. 8, the vertical surface downward stress generated at the contact position between the bonding wire and SiC die will be transferred to the solder layer. In addition, the larger stress from the edge of the



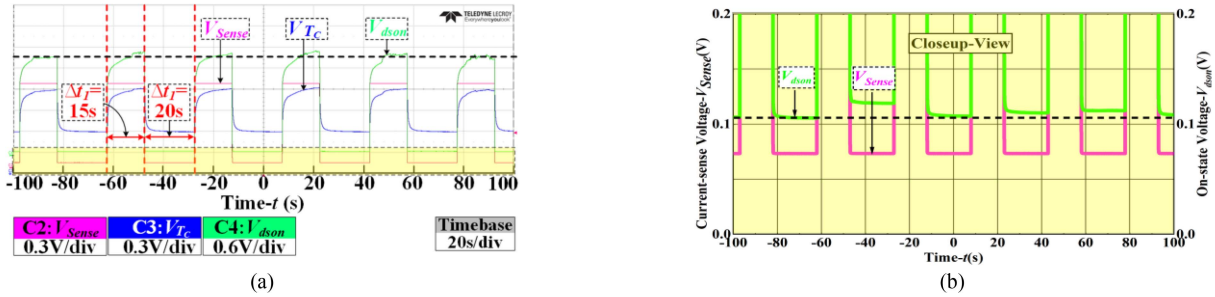
(a) (b)

Fig. 9. Test waveform of the actual SiC MOSFET (i.e., sct3017al) without degradation and performed on the ImDC-APCT platform (presented in Section III) (a) and its close-up view (b).



(a) (b)

Fig. 10. Test waveform of the actual SiC MOSFET (i.e., sct3017al) with slight degradation and performed on the ImDC-APCT platform (presented in Section III) (a) and its close-up view (b).



(a) (b)

Fig. 11. Test waveform of the actual SiC MOSFET (i.e., sct3017al) with serious degradation and performed on the ImDC-APCT platform (presented in Section III) (a) and its close-up view (b).

contact surface between the solder layer and the SiC die and the obvious deformation can be observed. From Fig. 8, the gradually increasing deformation from the center to the edge indicates that the solder layer is most likely to be degraded from the edge and gradually extend, eventually evolving into delamination and more voids, leading to SiC die failure. In the process of gradual delamination of the solder layer, more prominent deformation can be caused, and therefore, the effective contact area between the SiC die and the solder layer will be irregular during the next several power cycles. The irregular changes in thermal resistance R_{JC} will lead to the irregular change in R_{dsonH}. Moreover, since the solder layer will not eventually be lifted off like the bonding wire, irregular change will always exist, and the degree of irregularity will continue to increase.

Some experimental results that prompted us to propose the innovative monitoring method in this article are shown in Figs. 9–11, which are the test waveform of the actual SiC MOSFET (i.e., sct3017al) with different degradation levels performed on the ImDC-APCT platform (presented in Section III) and their respective close-up views, where the horizontal black dotted lines marked are used as the reference line. According to the position of the reference line, the changing trend of the V_{dson} can be observed intuitively. The solid lines in green, pink, and blue represent the V_{dson}, the current-sense resistance voltage (V_{Sence}, represents I_d), and the thermal resistance voltage (V_{TC}, represents T_C), respectively.

According to Figs. 9 and 10, compared to the undegraded SiC MOSFET, when the SiC MOSFET is slightly degraded, there is a certain increase in the R_{dson}, whereas the R_{dson} value in several consecutive cycles is basically the same. When the SiC MOSFET is severely degraded, as shown in Fig. 11, both the R_{dsonH} and the R_{dsonL} in several consecutive cycles have noticeable irregular changes. Based on the analysis mentioned above, the irregular change in the R_{dsonH} is mainly caused by the severe degradation of the solder layer and the bonding wire; yet, in the cooling phase, the R_{Solder} is so small that

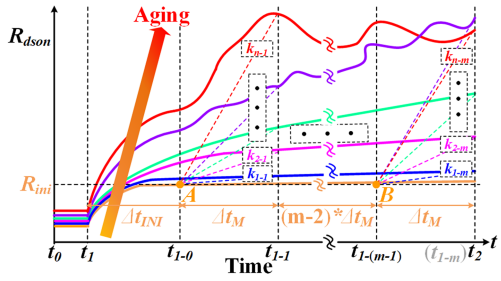


Fig. 12. Schematic diagram of the theoretical degradation process of $R_{dson\,H}$ and its change rate k_{i-j}.

the R_{BW} mainly contributes to the irregular change in the $R_{dson\,L}$.

C. Proposed Method of on-State Resistance-Change-Rate-Based Real-Time Degradation Feature Extraction for SiC mosfets

According to the above-mentioned analysis, in the ImDC-APCT of the SiC MOSFET, the T_J during the heating phase is higher, and when the V_{th}, the solder layer, the bonding wire, and the TIM are degraded, they are easily reflected in the $R_{dson\,H}$ of the SiC MOSFET; hence, the real-time degradation monitoring of the SiC MOSFET can be performed through a simple mathematics calculation on the $R_{dson\,H}$ (e.g., standard deviation), which can be used as degradation features. In this section, the proposed method will be described in detail.

1) Implementation Process of the Proposed Method: According to the above-mentioned theoretical analysis, when the brand-new SiC MOSFET is tested on the ImDC-APCT platform, its degradation process can be described as follows. First, in the initial stage of the SiC MOSFET degradation, the SiC die quickly enters the thermal steady state during the heating phase, and the change in the $R_{dson\,H}$ is extremely small during the thermal steady state. Then, as the degradation level deepens, it will take a long time for the SiC die to enter the thermal steady state during the heating phase. Moreover, the change in the $R_{dson\,H}$ becomes larger during the thermally stable steady state. In the final stage of the SiC MOSFET degradation, due to the severe degradation of bonding wires, the solder layer, and the TIM, it is almost difficult for the SiC die in the heating phase to enter the true thermally stable steady state. The $R_{dson\,H}$ in the heating phase will change drastically and irregularly. In order to facilitate the analysis of the proposed method, the entire above-mentioned degradation process is shown in Fig. 12, where the solid orange line and the solid red line, respectively, represent the change in the R_{dsonH} of the brand-new SiC MOSFET and the completely degraded SiC MOSFET during the heating phase. The other colored solid lines represent the change in the $R_{dson\,H}$ of SiC MOSFETs under the degradation states, and the degradation degree gradually deepens along the direction of the red arrow (i.e., marked in "Aging" in Fig. 12). According to Fig. 12, the proposed method for real-time degradation monitoring of the SiC MOSFET using the change rate of the R_{dsonH} can be clearly described.

In Fig. 12, the period from t_1 to t_2 is the complete heating time, which is represented as $\triangle t_1$ in Fig. 1; t_1 is the time at which the SiC MOSFET starts to heat at each accelerated power cycle, and the time at which the brand-new SiC MOSFET has entered the thermally stable steady state is represented as $t_{1\text{-}0}$, i.e., the change in the T_J is small from this moment to the end time of the heating phase, and as a consequence, the $R_{dson\,H}$ change is also very small. Herein, the R_{dson} at $t_{1\text{-}0}$ is represented as R_{ini}, and the time interval between $t_{1\text{-}0}$ and t_1 is represented as t_{INI}. It should be noted that the time is divided into m parts, and each time period is $\triangle t_M$

$$\bigcap_{j=1}^{m} \frac{t_{1-j} - t_{1-(j-1)}}{\Delta t_M} = 1 \tag{6}$$

where $t_{1\text{-}j}$ represents the end time of each $\triangle t_M$, and j increases from 1 to m according to the step size 1.

According to (7), the $R_{dson\,H}$ change rate (k_{i-j}) from $R_{dson\,H}$ at the jth $\triangle t_M$ under the ith cycle to R_{ini} can be calculated as follows:

$$k_{i-j} = \left(R_{i-j} - R_{ini}\right)/\Delta t_M \tag{7}$$

where R_{i-j} is the $R_{dson\,H}$ at t_{1-j} of the ith cycle, and the number of cycles i increases from 1 to n according to the step size 1 (n is the cycle number at which SiC MOSFETs are completely degraded).

It can be seen that at the initial stage of degradation, the closer the time to t_{i-j}, the larger its k_{i-j} value (i.e., $k_{i-1}<k_{i-2}<,\ldots,<k_{i-m}$); however, the significant difference among them cannot be seen due to the lower degradation level. As the degradation level deepens, the k_{i-j} change trend can be seen clearly, i.e., with the increase in i, $k_{i-j}>k_{\,(i-1)-j}$, and $(k_{i-m}-k_{i-1})>(k_{(i-1)-m}-k_{(i-1)-j})$. At the end stage of the degradation, with the increase in i, the larger irregular change can be seen in Fig. 12, and $k_{\,(i-1)-j} < k_{i-j}$ and $k_{i-m} < k_{i-1}$ will occur in some cycles. It is difficult to comprehensively monitor the SiC MOSFET degradation level by comparing the k_{i-j} value, which drives us to develop a new method to monitor the SiC MOSFET degradation state.

First, in order to reduce the impact of the k_{i-j} irregular change on the evaluation of the SiC MOSFET degradation level, the average value of these k_{i-j} in each cycle (i.e., k_i) is calculated as follows:

$$k_i = \frac{1}{m}\sum_{j=1}^{m} k_{i-j}. \tag{8}$$

Then, the average value ($avgk_i$) and the standard deviation ($stdk_i$) of k_i for r ($r = 12, \ldots, m$) adjacent cycles can be obtained as follows:

$$avgk_i = \frac{1}{r}\sum_{i=i}^{i+r-1} k_i \tag{9}$$

$$stdk_i \sqrt{\sum_{i=i}^{i+r-1} \left(k_i - avgk_i\right)^2 / r}. \tag{10}$$

The $avgk_i$ and $stdk_i$ can be used to carry out more comprehensive monitoring of the degradation state of SiC MOSFETs , which is explained in detail as follows.

According to the above-mentioned analysis, as the degradation progresses, $avgk_i$ gradually increases. However, when the bonding wire, the solder layer, and the TIM are severely degraded due to the irregular change in the $R_{dson\,H}$, it is still difficult to fully evaluate the degradation state of SiC MOSFETs only using $avgk_i$. If the $avgk_i$ and the $stdk_i$ are considered together, the degradation process of SiC MOSFETs will be revealed more clearly.

This is because when the first bonding wire is about to be lifted off, the thermal shock in the several adjacent cycles will cause an irregular change in the contact area between the bonding wire and the SiC die, leading to the irregular change in the R_{dsonH}. Thus, the corresponding $stdk_i$ value will be larger than the previous $stdk_i$ value, and it will also be larger than the $stdk_i$ value after this bonding wire is lifted off but before the next bonding wire is lifted off. Based on this, $stdk_i$ can be used to monitor the time when the bonding wire is severely degraded. When the solder layer is severely degraded, the delamination phenomenon becomes more prominent, the thermal shock in several adjacent cycles will cause a larger irregular change in the contact area between the SiC die and the lead frame, resulting in the irregular change in the T_J, and finally, the irregular change in $R_{dson\,H}$ can be seen. Due to the pressure applied to the package of SiC MOSFETs for heat dissipation, the solder layer is difficult to separate entirely from the SiC die, and the large $stdk_i$ value will be obtained based on the mathematical meaning of the standard deviation. Keeping in view the above-mentioned analysis, the $stdk_i$ can be used to monitor the time when the solder layer is severely degraded. In addition, when the bonding wire and the solder layer are severely degraded, the overall increase trend of the $avgk_i$ is also more apparent.

In summary, in this article, $avgk_i$ is used as a feature to evaluate the degradation level of SiC MOSFETs, whereas $stdk_i$ can be identified as another feature of the severe degradation of the bonding wire and the solder layer.

2) Verification Process of the Proposed Method: Commonly used and direct verification methods are the following. First, when the severely degraded state of the bonding wire and the solder layer is monitored by the proposed method, the experiment is stopped immediately. Then, the package of the DUT is opened, and the scanning electronic microscopy (SEM) inspection is performed. It is possible to judge whether or not the bonding wire and the solder layer are severely degraded through the analysis of the cross-sectional SEM images. This verification method can verify the effectiveness of the proposed method, whereas the bonding wire lift-off and the solder layer delamination are not synchronized. Therefore, when the bonding wire is lifted off, the test is stopped, and the package of the DUT will be damaged to obtain SEM images; at this time, the solder layer delamination may not have yet occurred. In order to obtain SEM images of the solder layer delamination, the new DUT will be used, and a new round of tests needs to be performed. Similarly, if the solder layer delamination has occurred first, the repeated steps are performed again. In order to verify the effectiveness of the proposed method, a large number of tests are performed, and therefore, the verification process is costly and time-consuming.

If the real-time monitored data are used to verify the effectiveness of the proposed method, the test will not be forced to terminate, so that time and costs can be saved. Based on this understanding and combined with the analysis presented in Section II-B, the real-time monitored data in ImDC-APCT is fully excavated, and it can be found that the $R_{dson\,L}$ can be used to verify the severe degradation of the bonding wire. In this way, the overall test time and cost can be saved. Nevertheless, in order to thoroughly verify the effectiveness of the proposed method, it is still necessary for the DUT to be decapsulated and then analyzed for failure under the microscope.

And then, there is another issue that needs more attention, i.e., the V_{dson} of the SiC MOSFET in the cooling phase (i.e., $V_{dson\,L}$) is low (this is because the I_d and the $R_{dson\,L}$ are low) and the change in the V_{dsonL} caused by the degradation is low; therefore, the accurate ON-state voltage measurement circuit needs to be applied to the ImDC-APCT. Fortunately, the innovative drain–source voltage clamp circuit (i.e., innovative drain-source voltage clamp circuit based on a zener diode (IDZD)) proposed in [5] can be used to obtain $V_{dson\,L}$ accurately.

III. Measurement Setup

Fig. 13(a) and (b) shows the schematic diagram and actual experimental platform, respectively, for verifying the proposed method. The SiC MOSFET with the To247 package from Rohm Semiconductor (i.e., sct3017al) is used as the DUT in this article. As shown in Fig. 13(b), the experimental platform consists of the dc power supply $V_{\rm DC}$ (q), the fuse (e), the electronic load $R_{E\rm Load}$ (r), the DC-SSPC, the water cooling system, the external heating system, the measurement system, and the data acquisition system. The DC-SSPC is composed of the dc bus capacitor board (f), the SiC MOSFET Q (t), CuHeat-sink (m), the control board (h), and the power board containing the current-sense resistance $R_{\rm Sense}$, the diode D, the line inductance $L_{\rm line}$, and the drive circuit (g). The external heating system is made up of the hot plate (n) and the CuHeat-sink (m), where the SiC MOSFET can be pressed against the CuHeat-sink by the crimping device (u), and the T_J can be increased from 25 to 175 °C. The water cooling system is composed of the constant temperature water bath (o) and the water cooling row heat exchanger with the cooling exhaust fan (p). The constant water temperature heated by the constant temperature water bath flows into the CuHeat-sink to provide a constant ambient temperature for the SiC MOSFET in the ImDC-APCT. Since the constant temperature water bath cannot be used to cool water, the heat generated in the SiC MOSFET during heating phase will be dissipated by the water cooling row heat exchanger. The measurement system is composed of the temperature transmitter (j) for measuring the temperature of the CuHeat-sink and the test board (i), which contains the T_C measurement circuit based on the positive temperature coefficient of thermal resistance R_T (i.e., PT100), the I_d measurement circuit based on the $R_{\rm Sense}$, and the V_{dson} measurement circuit based on the IDZD.

If the DUT is directly soldered to the means printed circuit board (PCB), two problems have to be faced. First, a large layout area and a thick copper layer on the PCB are required, which increases the costs and design difficulty. Another problem is that the DUT needs to be replaced multiple times in the ImDC-APCT, and the soldering method for the DUT is very

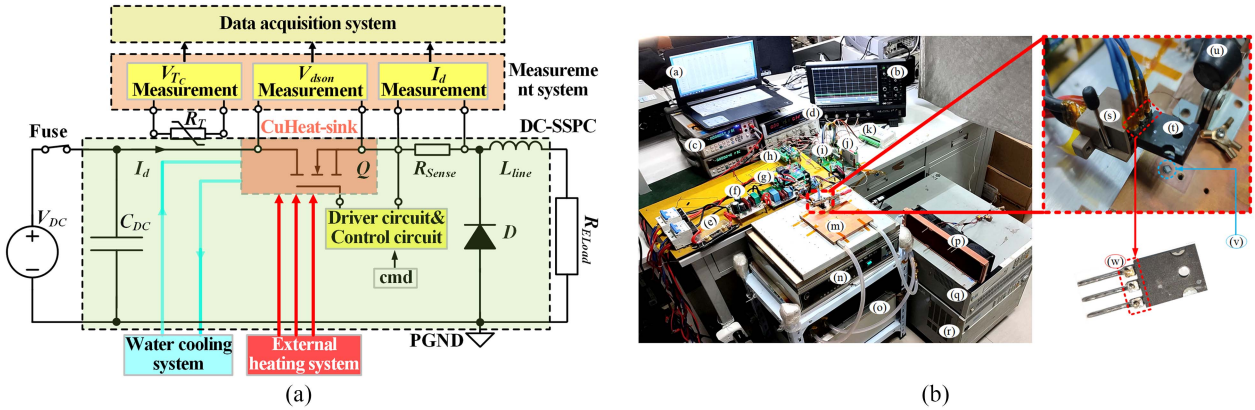


Fig. 13. Schematic diagram (a) and actual experimental platform (b) for verifying the proposed method.

disadvantageous, which may cause damage to other devices due to repeated disassembly. If the lead of the SiC MOSFET is pressed into the test socket [Fig. 13(b)–(s)] without any measures to reduce the contact resistance, a nonnegligible measurement error will be introduced due to the contact resistance. Fortunately, the IDZD presented in [5] has the differential input characteristic, and therefore, in this article, the connector plugin is soldered on the lead near the package of the DUT, and the drain and the source of the DUT can be directly connected to the input of the IDZD. In this way, the problem of the contact resistance of the test socket is solved, which makes it easier to replace the DUT; thereby, the test efficiency is improved.

The data acquisition system is made up of a high-precision data acquisition board, 8AD PRO [see Fig. 13(b)-(a)], a high-precision oscilloscope, HD4096 [see Fig. 13(b)-(b)], and a high-precision digital multimeter, 34410A [see Fig. 13(b)-(c)], where the high precision data acquisition board 8AD PRO has a 24-b analog-to-digital converter with an accuracy of 0.1%. Therefore, the data of the I_d, T_C, and V_{dson} of the SiC MOSFET can be accurately acquired in real-time and stored on a hard disk. However, the data acquisition card has a lower sampling frequency, only 1 kHz, and therefore, the dynamic effects of the SiC MOSFET can be obtained using the high-precision oscilloscope HD4096. The high-precision multimeter 34410A can be used to accurately obtain the static parameters of the SiC MOSFET and the calibration for other measurement instruments.

Overall, these high-precision measurement instruments and the use of highly accurate ON-state voltage measurement circuits (i.e., IDZD) ensure highly accurate characteristics of the measurement data, which is the basis for the study of the real-time degradation monitoring methods.

IV. Experimental Verification

In this section, the detailed parameter settings of the ImDC-APCT and the reason for the parameter settings are described. Afterward, the comprehensive analysis of the test results and the comparative observation under the microscope verify that the $avgk_i$ can be used as a feature to evaluate the degradation level of the SiC MOSFET and the $stdk_i$ can be used as a feature to identify the severe degradation of the solder layer and the bonding wire.

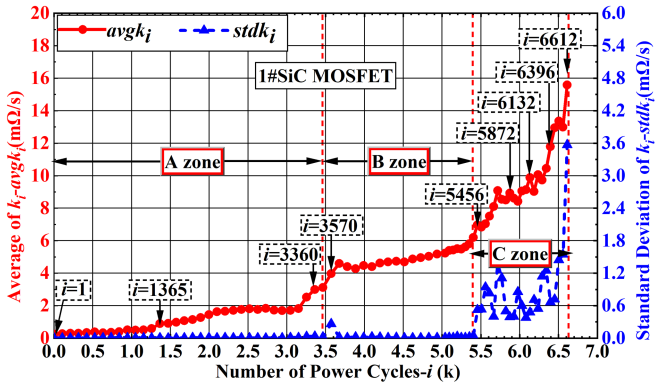


Fig. 14. $avgk_i$ and $stdk_i$ of 1# SiC MOSFET at different numbers of power cycles.

According to the standard MIL-STD-1760D [34], DC-SSPCs can withstand several times the rated load and the duration time can range from several seconds to several tens of seconds. Therefore, in this article, $\triangle t_1 = 15$ s and $\triangle t_2 = 20$ s (as shown in Figs. 1 and 9–11) were selected. In the initial stage of the degradation of SiC MOSFET , it completely entered the thermal steady preparation state within 5 s, hereby, $T_{\mathrm{INI}} = 5$ s (shown in Fig. 12). For the value of the $\triangle t_M$ (shown in Fig. 12), if its value is too small, more computing resources will be needed, and if the value is too large, the degradation level of the SiC MOSFET will not be accurately reflected. According to the thermal response time of the sct3017al given in the datasheet and the TIM, the T_J during the initial stage of the degradation can remain stable within 1 s, so, $\triangle t_M = 1$ s, correspondingly, $m = 10$. In order to obtain the average value and standard deviation of the k_i for real-time monitoring of the degradation level of the SiC MOSFET, where $r = 10$, the $avgk_i$ and $stdk_i$ can be obtained using a few calculation resources. Taking into account the changes in the operating environment temperature of the DC-SSPC and the repeatability of the test results, two water temperatures flowing into the CuHeat-sink (T_A) are given, i.e., $T_A = 26$ °C and $T_A = 61$ °C. 1# SiC MOSFET is tested at $T_A = 26$ °C, $I_{dH} = 90$ A, and $I_{dL} = 5$ A, and test results are shown in Figs. 14 –16. 2#SiC MOSFET is tested at $T_A = 61$ °C, $I_{dH} = 80$ A, and $I_{dL} = 5$A, and test results are shown in Figs. 17 –19.

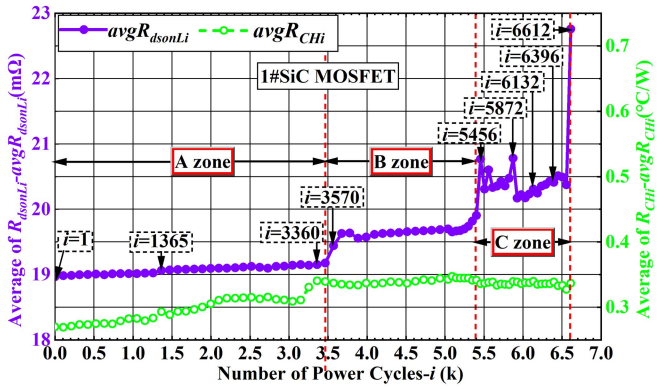


Fig. 15. $avgR_{dson\,Li}$ and $avgR_{\mathrm{CH}\,i}$ of 1# SiC MOSFET at different numbers of power cycles.

Figs. 14 and 17 depict the $avgk_i$ (solid red line, left y-axis) and the $stdk_i$ (solid blue line, right y-axis), calculated from the real-time monitored data from the ith cycle to the $(i+9)$th cycle, at different cycles (i, x-axis). In Figs. 15 and 18, the average value of the $R_{dson\,Li}$ (i.e., $avgR_{dson\,Li}$, purple solid line, left y-axis) and the steady-state thermal resistance of the TIM during the heating stage ($R_{\mathrm{CH}\,i}$) (i.e., $avgR_{\mathrm{CH}\,i}$, solid cyan line, right y-axis), which are calculated from the real-time monitored data from the ith cycle to the $(i+9)$th cycle, at different cycles (i, x-axis) are shown. Figs. 16 and 19 show the real-time monitored $R_{dson\,i}$ waveform from i-th cycle to $(i + 9)$-th cycle (Fig. 16(a) and Fig. 19(a)) and its closeup-view marked yellow (Fig. 16(b) and Fig. 19(b)), where the value of the $R_{dson\,i}$ is shown in left y axis. In order to facilitate analysis, the entire life cycle of SiC MOSFETs is divided into three zones, i.e., the slow degradation zone (A zone), the accelerated degradation zone (B zone), and the severe degradation zone (C zone). According to the experimental results presented in this article, the status in which the $stdk_i$ is eight times higher than the initial value for the first time and has no continuity is taken as the starting point for entering a slightly degraded status, and the reoccurrence of the state in which the $stdk_i$ is eight times higher than the initial value and lasts for a long time is taken as the starting point of the severe degradation status and also as the ending point of the slight degradation.

Some conclusions can be drawn through the analysis of the above-mentioned figures.

A. *Degradation Trend Monitoring Using* avgk$_i$

From Figs. 14 and 17, it can be seen that with an increase in i, $avgki$ gradually increases, and from the A zone to the C zone, the time taken becomes shorter and shorter and the increasing amount is getting larger and larger. For 1# SiC MOSFET, the A zone in Fig. 14 accounts for 52.4% of the entire life cycle, i.e., the end of the A zone is $i = 3465$, and the total entire life cycle is $i = 6612$, thereby, $52.4\% = 3465/6612$; however, $avgk_i$ increases from 0.252 to 3.118 mΩ/s, which is an increase of 11.4 times relative to its initial value (i.e., $11.4 = (3.118\ \mathrm{m\Omega/s} - 0.252\ \mathrm{m\Omega/s})/0.252\ \mathrm{m\Omega/s}$). The C zone accounts for 18.3% of the entire life cycle ($18.3\% = (6612-5404)/6612$), and $avgk_i$ increases from 6.202 to 15.579 mΩ/s, which is about 37.2 times its initial value (i.e., $37.2 = (15.579\ \mathrm{m\Omega/s} - 6.202\ \mathrm{m\Omega/s})/0.252\ \mathrm{m\Omega/s}$). There are similar test results for 2#SiC MOSFET. In Fig. 17, A zone accounts for 71.0% of the entire life cycle (i.e., $71.0\% = 3251/4578$) and $avgk_i$ increases only by nine times (i.e., $9 = (2.617\ \mathrm{m\Omega/s} - 0.262\ \mathrm{m\Omega/s})/0.262\ \mathrm{m\Omega}$ /s), whereas the C zone accounts for 11.4% (i.e., $11.4\% = (4578-4058)/4578$), and $avgki$ increases by about 35 times ($35 = (14.558 - 5.378\ \mathrm{m\Omega/s})/0.262\ \mathrm{m\Omega/s}$). Therefore, $avgk_i$ can be used to evaluate the SiC MOSFET degradation trend.

B. *TIM in A Zone Degradation Monitoring Using* avgk$_i$

Although the study of the bonding wire degradation and the solder layer degradation is significant to the SiC MOSFET reliability and has also received more attention, the test results presented in this article show that the TIM will also suffer from the degradation. According to the analysis presented in Section II-C.2, only in the high power loss mode, the TIM degradation can be identified, and in the low power loss mode, the degradation of the SiC die, the bonding wire, and the solder layers can be identified. Regardless of 1# SiC MOSFET (refer to Fig. 15) or 2# SiC MOSFET (refer to Fig. 18), the $R_{dson\,Li}$ in the A zone increases slowly, with no large-scale sudden increase or irregular change, i.e., for 1# SiC MOSFET and 2# SiC MOSFET, the $R_{\mathrm{CH}\,i}$ only increases 1.1% and 1.5%, respectively; therefore, the degradation level of the SiC die, the bonding wire, and the solder layer is low.

However, the corresponding $avgk_i$ and $avgR_{\mathrm{CH}\,i}$ are increased by 11.4 times ($11.4 = (3.118\ \mathrm{m\Omega/s} - 0.252\ \mathrm{m\Omega/s})/0.252\ \mathrm{m\Omega/s}$), 25.9% ($25.9\% = (0.340\ ^\circ\mathrm{C/W} - 0.270\ ^\circ\mathrm{C/W})/0.270\ ^\circ\mathrm{C/W}$), and 8.9 times ($8.9 = 2.617\ \mathrm{m\Omega/s} - 0.262\ \mathrm{m\Omega/s})/0.262\ \mathrm{m\Omega/s}$), 24.5% ($24.5\% = (0.330 - 0.265\ ^\circ\mathrm{C/W})/0.265\ ^\circ\mathrm{C/W}$), respectively; moreover, $avgk_i$ and $avgR_{\mathrm{CH}\,i}$ have similar increasing trends. Thus, $avgk_i$ can reflect the TIM degradation in the A zone very well. Through the real-time monitoring of $avgk_i$, the TIM can be proactively maintained or renewed in time, improving the system reliability.

C. *Severe Degraded Bonding Wire and Solder Layer Monitoring Using* stdk$_i$

According to Fig. 15, at $i = 3570$, the $R_{dson\,L}$ increases by 1.4% ($1.4\% = (19.44\ \mathrm{m\Omega} - 19.17\ \mathrm{m\Omega})/19.17\ \mathrm{m\Omega}$) suddenly; however, in the entire A zone, the $R_{dson\,L}$ only increases by 1.1% ($1.1\% = (19.17\ \mathrm{m\Omega} - 18.97\ \mathrm{m\Omega})/18.97\ \mathrm{m\Omega}$), and therefore, at $i = 3570$, the first bonding wire has been severely degraded and the lift-off is about to occur. From Fig. 14, the $stdk_i$ at $i = 3570$ suddenly increases by 11.1 times ($11.1 = (0.266\ \mathrm{m\Omega/s} - 0.022\ \mathrm{m\Omega/s})/0.022\ \mathrm{m\Omega/s}$), however, $stdk_i$ within the period of time before and after $i = 3570$ (before the second bonding wire is lifted off) has small values, whose maximum value is much smaller than the value at $i = 3570$.

A similar phenomenon is found in the 2# SiC MOSFET.

According to Fig. 18, in the entire A zone, the increase in R_{dsonL} is only 1.5% ($1.5\% = (20.24 - 19.95\ \mathrm{m\Omega})/19.95\ \mathrm{m\Omega}$), whereas at $i = 3307$, an increase of 2.2% ($2.2\% = (20.68 - 20.24\ \mathrm{m\Omega})/20.24\ \mathrm{m\Omega}$) is monitored, so at $i = 3307$, the first bonding wire has been severely degraded and is about to be lifted off.

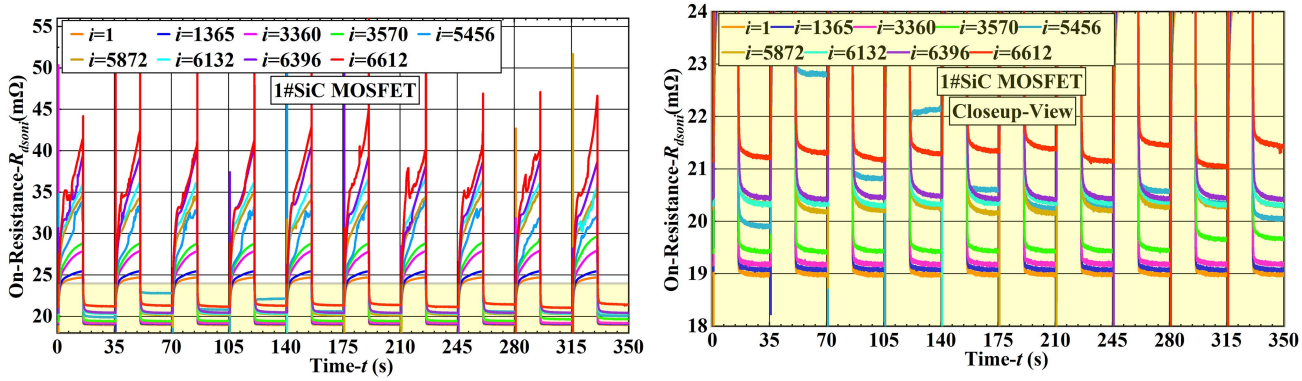


Fig. 16. Real-time monitored $R_{dson\,i}$ waveform of the 1# SiC MOSFET from the ith cycle to the $(i+9)$th cycle (a). Its closeup view is marked in yellow in (a) and (b).

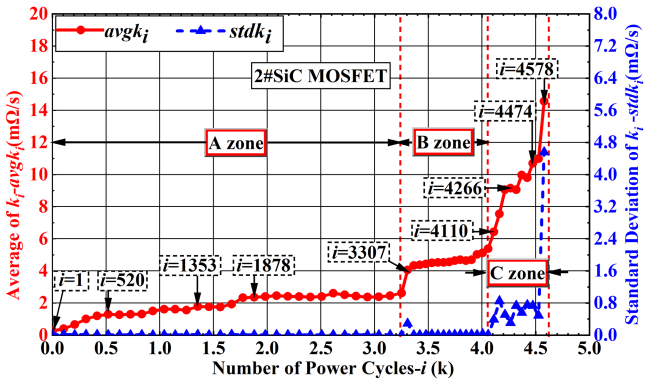


Fig. 17. $avgk_i$ and $stdk_i$ of 2# SiC MOSFET at diferent numbers of power cycles.

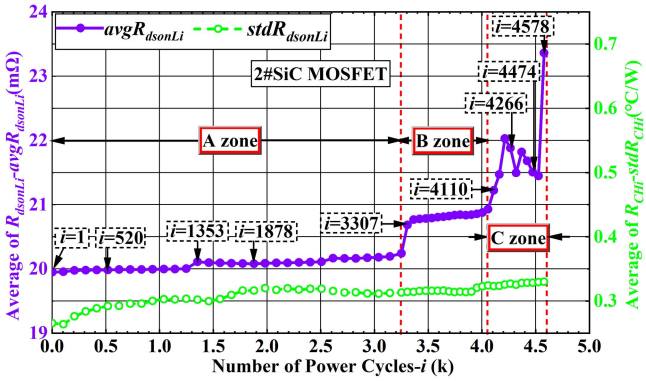


Fig. 18. $avgR_{dson\,Li}$ and $avgR_{CH\,i}$ of 2# SiC MOSFET at diferent numbers of power cycles.

Correspondingly, from Fig. 17, it can be seen that $stdk_i$ suddenly increased by 57.2 times (57.2 = (0.291−0.005 mΩ/ s)/0.005 mΩ/s), and it is much larger than other values near it.

Thereby, $stdk_i$ can be used to monitor the bonding wire lift-off.

In the C zone, the $R_{dson\,L}$ has both a sudden increase and severe irregular changes, which can be clearly seen in Figs. 14 and 17. The $stdk_i$ can maintain a large value in the C zone, e.g., for 1# SiC MOSFET, the $stdk_i$ varies from 0.379 to 3.570 mΩ/s, and for 2# SiC MOSFET, the $stdk_i$ varies from 0.316 to 4.557 mΩ/s. Both of these are much higher than the values when the bonding wire and solder layer are not severely degraded (i.e., the values in the A zone and B zone).

Although the TIM has also been degraded, according to the analysis presented in Section II, the TIM degradation cannot be reflected on $R_{dson\,L}$; thereby, the above-mentioned phenomenon observed in $R_{dson\,L}$ is mainly caused by the severe degradation of the solder layer, leading to a poor contact between the SiC die and the lead frame.

In addition, from Figs. 16 and 19, when the bonding wire and the solder layer are severely degraded, compared with the initial waveform where the SiC MOSFET is not degraded, the real-time monitored $R_{dson\,i}$ waveform becomes very irregular, which is also the main motivation for us to propose a new method to real-time monitor the severe degradation of the bonding wire and the solder layer using $stdk_i$.

D. Experimental Verification Based on Microscope Observation

Fig. 20 shows that the bonding wire degradation status observed under the optical microscope after 1 # SiC MOSFET is decapsulated. Fig. 21 shows the appearance of the brand-new bonding wire perfectly bonded on the SiC die. It can be seen from Fig. 20 that two long bonding wires have been lifted off from the SiC die surface. In addition, although the shorter bonding wires have not been lifted off, compared with the bonding state of the brand-new bonding wire in Fig. 20, they have also been seriously degraded and will be lifted off. In this state, combined with the deformation of the bonding wire based on the thermal–mechanical coupling simulation in the Comsol Mutiphysics software (shown in Fig. 7), in the near several power cycles, the contact area between the bonding wire and the SiC die will change irregularly, which will lead to the irregular change in the $R_{dson\,H}$ and the $R_{dson\,L}$.

Fig. 22 shows the solder layer degradation status of 1 # SiC MOSFET, and the left picture is photographed using the optical microscope under dark light, and the right picture is photographed using the scanning electron microscope. Fig. 23 shows the picture of the brand-new solder layer taken by the scanning electron microscope. According to the result shown

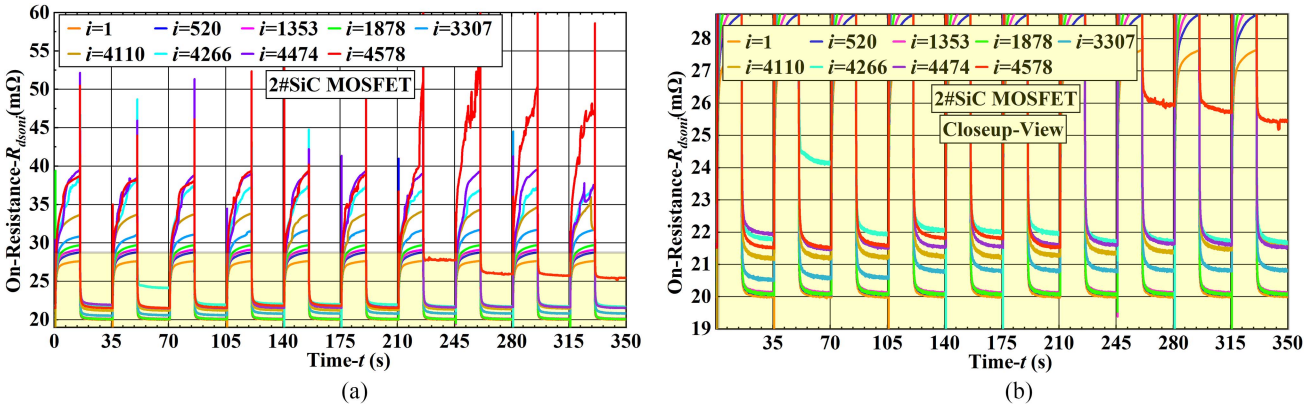


Fig. 19. Real-time monitored $R_{dson\,i}$ waveform of the 1# SiC MOSFET from the ith cycle to the $(i+9)$th cycle (a) and its closeup view marked yellow in (a) and (b).

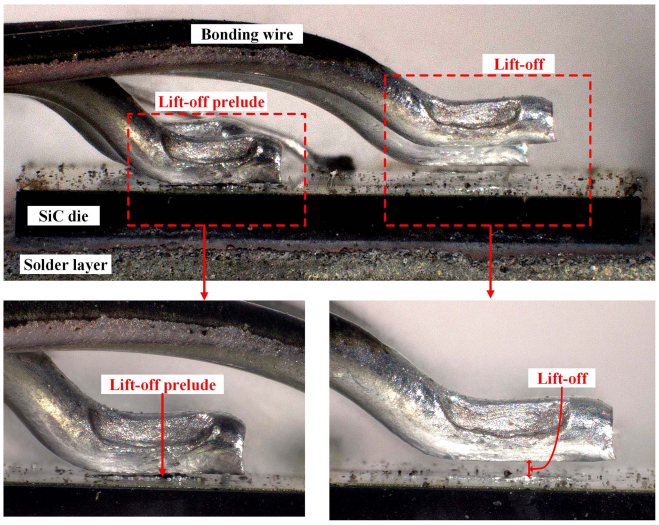


Fig. 20. Bonding wire degradation status of 1# SiC MOSFET observed under the optical microscope.

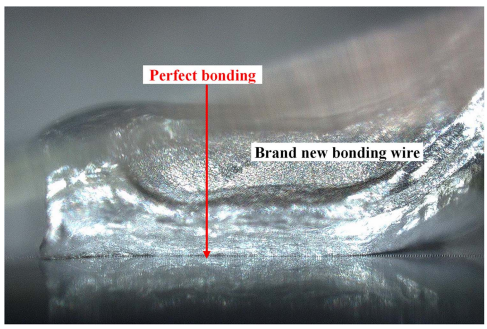


Fig. 21. Appearance of the brand-new bonding wire perfectly bonded on the SiC die.

in Fig. 22, serious delamination has occurred on the contact surface between the solder layer and SiC die, and melting traces can also be observed on the metal layer on the SiC die surface. Compared with the brand-new solder layer shown in Fig. 23, a lot of voids and serious delaminations can be observed under the scanning electron microscope. The material structure of the solder layer is not as "tight" as the brand-new solder layer, thus, the conductivity and thermal conductivity of the solder layer (i.e., the resistivity, heat transfer coefficient, etc.) will also deteriorate. According to the solder layer deformation in the thermal–mechanical coupling simulation (shown in Fig. 8), the effective contact area between the solder layer and the SiC die will change irregularly in the near several power cycles, and the resistivity and heat transfer coefficient may also change irregularly. Herein, the serious degradation of the solder layer will make a significant contribution to the irregular change of the $R_{dson\,H}$.

V. Conclusion

In this article, a method for the real-time extraction of SiC MOSFETs' degradation features in the ImDC-APCT for DC-SSPC application is presented and comprehensively analyzed. The proposed method can effectively monitor the main degradation process of SiC MOSFETs in real-time, such as the SiC die degradation, the bonding wire degradation, the solder layer degradation, and the TIM degradation. Moreover, the severe degradation of the bonding wire and solder layer can be monitored without the junction temperature information, which is a predominant feature and critical improvement of the proposed solution.

First, the ImDC-APCT of SiC MOSFETs is described, and its operation principle is analyzed in detail. After that, the influence of the SiC die degradation, the TIM degradation, the bonding wire degradation, and the solder layer degradation on $R_{dson\,H}$ is comprehensively analyzed. Some theoretical calculations and thermal–mechanical coupling simulation are also performed to explain the reasons behind it. Based on this, the operation principle and theoretical verification process of the proposed method for the real-time degradation monitoring of the SiC MOSFET for the DC-SSPC, in which the average value (*avgk*) and standard deviation (*stdk*) of the R_{dsonH} change rate are used as degradation features, are described in detail and comprehensively analyzed. And the severe degradation monitoring of the bonding wire and the solder layer using *stdk* and *avgk* has also been explained. Then, the experiment platform used to verify the proposed method is also particularly described and a detailed design guideline is

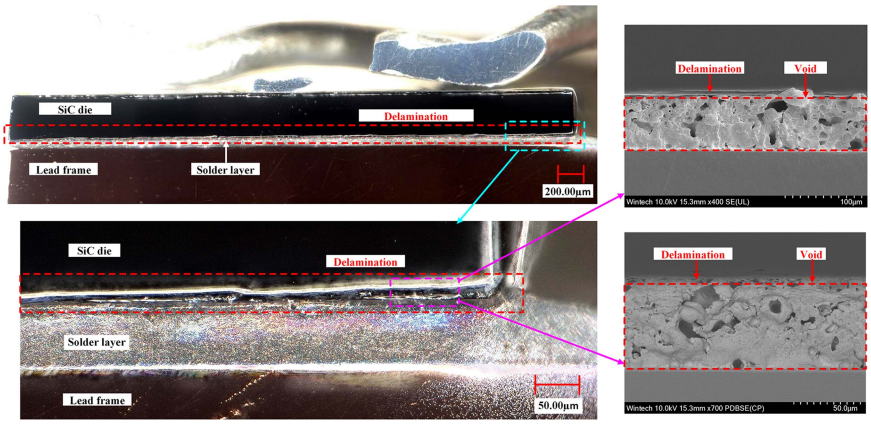


Fig. 22. Solder layer degradation status of 1# SiC MOSFET. The left picture is photographed using the optical microscope under the dark light. The right picture is photographed using the scanning electron microscope.

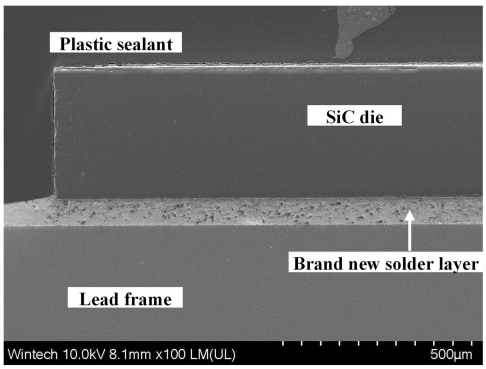


Fig. 23. Brand-new solder layer picture taken by the scanning electron microscope.

also given. Finally, the SiC MOSFET is tested on the above-mentioned experiment platform, and the proposed method has been verified using the monitoring data and the microscope observations.

In summary, since R_{dson} can be easily measured by the highly accurate drain–source voltage clamp circuit (i.e., IDZD) and the *stdk* and the *avgk* can be obtained through simple calculations, the proposed method for the real-time degradation monitoring of SiC MOSFETs in DC-SSPCs can be easily implemented.

The junction temperature (T_J) information of SiC MOSFETs cannot be obtained directly using this proposed method; however, it can easily monitor the severe degradation of the bonding wire and the solder layer, and thereby, proactive maintenance can be performed to improve the reliability and reduce the maintenance costs. In addition, for the traditional method of monitoring the solder layer degradation, the TSEPs need to be used, and the calibration process is also needed for the accurate T_J measurement, which will consume a lot of software computing resources, hardware resources, and experiment time. The proposed method in this article can effectively overcome these shortcomings.

The *avgk* can also be used as the degradation feature of the SiC MOSFET in the DC-SSPC for fault diagnosis and real-time remaining useful life prediction. When the method proposed in this article is used in the APCT, the SiC MOSFET degradation state can be judged in real time, and the test can be ended at the appropriate time; therefore, the security and efficiency of the test will be improved. In the future, more valuable characteristic indicators from the R_{dson} waveform of a single power cycle will be extracted and applied to the health status monitoring of the SiC MOSFET in the real DC-SSPC application. In addition, for the traditional DC-APCT operating condition, the lift-off of the bonding wire and the delamination of the solder layer are also relatively common failure models according to the analysis presented in Section I, and the method proposed in this article can also be adopted.

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