Influence of Junction-Capacitance and Dead-Time on Dual-Active-Bridge Actual Soft-Switching-Range: Analytic Analysis and Solution

Zhe Wang, *Student Member, IEEE*, Chi Li, *Member, IEEE*, Jiye Liu, *Student Member, IEEE*, and Zedong Zheng, *Senior Member, IEEE*

***Abstract*—Dual active bridges (DABs) may lose zero voltage switching (ZVS) operation when the junction capacitance of semiconductors cannot be fully charged or discharged within dead time. The influence above is more serious especially under light load because the switching current is small. The aim of this article is to analyze the influence of the junction capacitance and dead time on the ZVS range of DAB and propose a novel modulation to eliminate the influence. It is concluded that DAB has an inherent non-ZVS region due to the influence of junction capacitance and dead time. Besides, the exact ZVS range of DAB is given when the junction capacitance and dead time are considered. In view of the influence of junction capacitance and dead time, this article proposed a mixed-mode modulation, which enables DAB to avoid operating in non-ZVS region. Finally, a 4.5 kW rated prototype is made and experimental results are presented to verify the previous conclusions. The efficiency with the proposed method can be up to 4% higher under light load than that with the traditional method ignoring nonideal factors.**

***Index Terms*—Dead time, dual active bridge (DAB), junction capacitance, modulation, soft switching.**

I. Introduction

THE dual active bridge (DAB) was proposed in the 1990s [1], and it is getting more and more attention from researchers for the advantages of flexible control, high efficiency, high power density, etc. With the development of semiconductor devices, the application range of the DAB grows rapidly such as energy storage systems [2], [3], automotive applications [4], [5], solid-state transformers [6], [7], microgrids [8], [9], [10], etc.

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Zhe Wang, Chi Li, and Zedong Zheng are with the State Key Laboratory of Control and Simulation of Power Systems and Generation Equipments, Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: wangzhe19@mails.tsinghua.edu.cn; chi.li.2014@ieee.org; zzd@tsinghua.edu.cn).

Jiye Liu is with the Beijing Relpow Technology Co., Ltd, Beijing 100096, China (e-mail: liujiye13@126.com).

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DAB converters adopt phase-shifting control methods including single phase-shifting modulation [11], [12], extended phase-shifting modulation [13], dual phase-shifting modulation [14] and triple phase-shifting modulation [15], [16], [17], [18], [19]. Among them, the triple phase-shifting modulation is the most general modulation of DAB, and the others are the special cases of the triple phase-shifting modulation. Based on the triple phase-shifting modulation, researchers carried out global optimizations on targets such as the minimum reactive power [15], [16], the minimum effective value of high-frequency current [17], [18], and the minimum current stress [19] respectively, which broadens the soft-switching range of DAB converter and improves efficiency.

The ZVS characteristic is of great significance to reduce switching loss and improve efficiency. In most of the existing researches on DAB modulation methods, the influences of nonideal factors, such as dead time of converter and junction capacitance of device are not considered. It is considered that when the drain current (or collector current) of the device is not less than zero, another device of the same bridge can realize ZVS operation. Ignoring the nonideal factors, ZVS operation can be realized in full voltage gain and full power range by using triple phase-shifting modulation [19]. However, the actual converter contains nonideal factors unavoidably. Only when the switching current amplitude is large enough, the junction capacitance of the device can be fully charged and discharged in the dead time. Ignoring nonideal factors will lead to the misjudgment of the ZVS range, increasing the switching loss, and affecting the electromagnetic compatibility performance. DAB high-frequency voltage also produces distortion due to the influence of nonideal factors [20], which affects the power transmission characteristics. According to the research in [21], due to the influence of nonideal factors, DAB will lose the ZVS operation at light load, and the loss at the light load will be more than half of that at rated power, which decreases the efficiency in light load greatly.

In view of the influence of nonideal factors such as dead time and junction capacitance, scholars have done some studies by analyzing the stored energy in phase-shifting inductor [22], the stored charge in junction capacitance [23], [24], and the inductor current waveform in switching process [25], respectively, and presented different discriminant methods for the ZVS

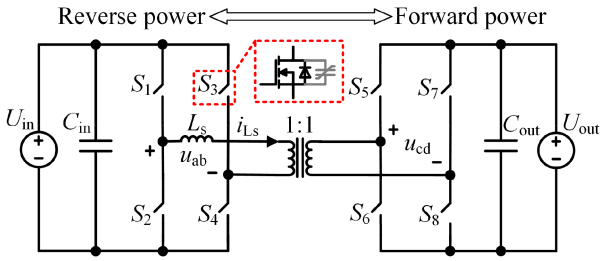

Fig. 1. Circuit of DAB.

conditions. However, the literatures above are all analyzed under a specific operating mode or a specific voltage gain, and the exact ZVS range of the converter in the full operating region is not given. Yan et al. [26] in University of Tennessee realized the ZVS operation by increasing the switching current amplitude, but the converter still lost the ZVS operation under certain voltage gain and transmission power conditions. Haneda and Akagi [27] in Tokyo Institute of Technology proposed a novel discontinuous mode of DAB, which can increase the converter efficiency in a wide load range. However, this method is not suitable for the situation when the voltage gain is not equal to the transformer turn ratio. In [28], [29], and [31], ZVS is realized by adding hardware circuits which are complicated and costly.

In this article, the influence of nonideal factors on the ZVS range is analyzed comprehensively. Besides, a mixed modulations, which requires switching between different modes, are proposed to realize ZVS operation in the wide voltage gain and load range. At present, a lot of literature has proved the feasibility of DAB working in frequent mode switching state [32], [33], [34], [35], [36].

The main contributions of this article lie in three aspects are as follows.

1) Based on the comprehensive analysis of the influence of nonideal factors, the exact ZVS region of DAB is given.
2) The dead time is optimized and a smallest non-ZVS region is obtained.
3) A novel mixed-mode modulation is proposed, which makes DAB avoid operating at non-ZVS region and realizes the ZVS operation in the wide voltage gain and load range.

The rest of this article is organized as follows: In Section II, the basic operation principle of DAB is illustrated. In Section III, the influence of nonideal factors on the ZVS range is analyzed. In Section IV, a novel mixed-mode modulation is proposed. In Section V, a 4.5-kW rated prototype is made, and experimental results are presented to verify the previous conclusions.

II. Topology Operation Principle

A. Operation Principle of DAB

Fig. 1 shows the topology of the DAB, which includes the primary bridge (S_1-S_4), the secondary bridge (S_5-S_8), the ideal transformer, the phase shift inductor L_s, the input capacitor C_{in}, and the output capacitor C_{out}. The square waveforms generated by the primary side and the secondary side are defined as u_{ab} and u_{cd}, respectively. The power transmitted from the primary side to the secondary side is defined as forward power, and vice versa is defined as reverse power. The input and output voltages are defined as U_{in} and U_{out}, respectively. The voltage gain d is defined as

$$d = U_{out}/U_{in}. \tag{1}$$

The base values of voltage, current, time, and power are defined as follows:

$$\begin{cases} U_{base} = U_{in} \\ I_{base} = U_{in}/(2f_sL_s) \\ T_{base} = T_s/2 \\ P_{base} = U_{in}U_{out}/(8f_sL_s) \end{cases} \tag{2}$$

where f_s is the switching frequency and T_s is the switching period. In this article, X(p.u.) represents the normalized value of X. To simplify the analysis, the following assumptions are made.

1) The losses of the inductors, capacitors, semiconductors, transformers, etc., are ignored.
2) The turn ratio of the ideal transformer is 1:1, and the magnetizing inductor is large enough (the magnetizing current can be ignored).
3) The bus capacitor is large enough, and the input voltage U_{in} and output voltage U_{out} are stable dc values.

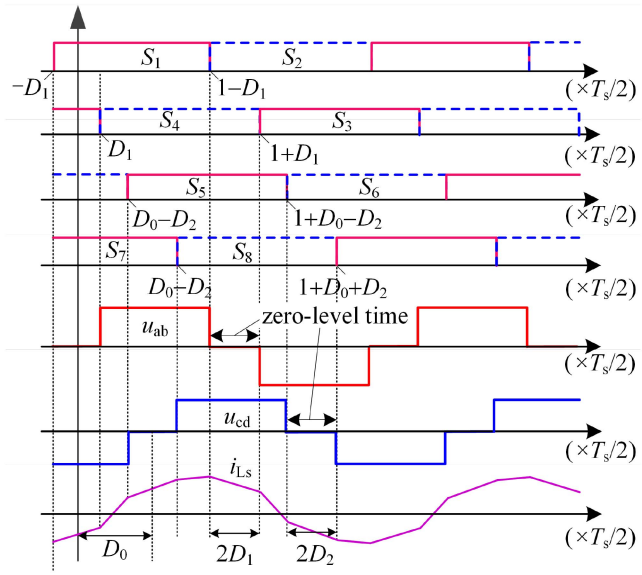

Fig. 2. Triple phase-shifting control waveforms of DAB.

B. Triple-Phase Shift Modulation Strategy

The triple phase-shifting control waveforms are shown in Fig. 2. The driving signals of the upper and lower MOSFETs of the same bridge arm are complementary. The triple-phase shift strategy includes three degrees of freedom, which are the primary phase shift ratio D_1, the secondary phase shift ratio D_2, and the external phase shift D_0. The phase shift ratios D_1 and D_2 are defined as the ratios of the zero-level time of u_{ab} and u_{cd} to the whole period T_s, respectively. The external phase shift ratio

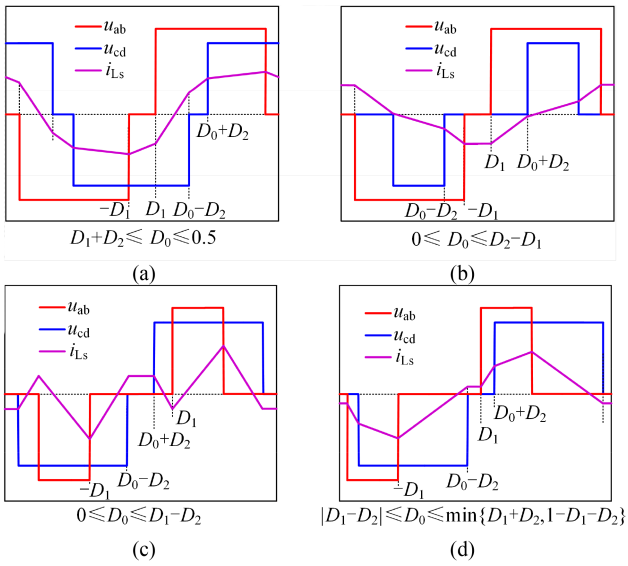

Fig. 3. Basic waveforms of the four modes when the power is forward and the voltage gain d is less than 1. (a) Mode A. (b) Mode B. (c) Mode C. (d) Mode D.

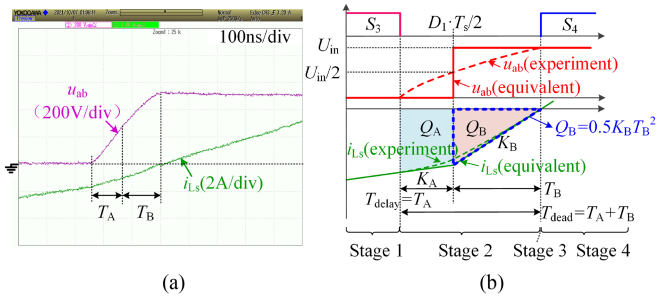

Fig. 4. ZVS transient waveforms of DAB. (a) Experiment waveforms. (b) Equivalent waveforms.

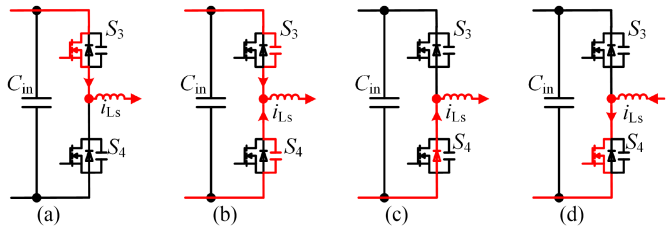

Fig. 5. Equivalent circuits of the four stages. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4.

D_0 is defined as the ratio of the time difference of the u_{ab} and u_{cd} centers to the half period.

To simplify the analysis, take the forward power and voltage gain d less than 1 case for example, and similar results can be obtained by simple transformations in other cases. According to the existing research results [16], the forward and voltage gain d less than 1 case has 4 practical modes, and the basic waveforms of these modes are shown in Fig. 3. The normalized analytic expressions of the turn-ON current and the transmission power of these modes are given in Tables II and III in Appendix, respectively.

III. Analysis of ZVS Range Considering Nonideal Factors

The ZVS operation can decrease the switching loss of semiconductors and increase efficiency. However, the nonideal factors, such as junction capacitance and dead time are not fully considered in the existing research causing the misjudgment of the ZVS range and decreasing the converter's efficiency. In this section, the influences of junction capacitance and dead time on the ZVS range are analyzed, and the actual ZVS range of DAB is derived when the junction capacitance and dead time are considered.

A. Influence of Junction Capacitance

Take the time $D_1 \times T_s/2$ in Fig. 2 for example to analyze the turn-ON transient of MOSFET S_4. The junction capacitances of switches S_3 and S_4 are defined as $C_{\text{oss\_S3}}$ and $C_{\text{oss\_S4}}$, which vary nonlinearly with the drain-source voltage. The experiment and its equivalent ZVS transient waveforms are shown in Fig. 4. The ZVS transient includes 4 stages, and the equivalent circuits of the four stages are shown in Fig. 5.

1) *Stage 1*: In this stage, the leakage inductor current i_{Ls} flows through the channel of MOSFET S_3, and the turn-OFF process has not yet started.
2) *Stage 2*: At the beginning of this stage, the channel of S_3 shuts down, and the junction capacitances $C_{\text{oss\_S3}}$ and $C_{\text{oss\_S4}}$ are resonant with the leakage inductor L_s. The voltage u_{ab} starts increasing until the junction capacitance $C_{\text{oss\_S4}}$ discharges to zero voltage.
3) *Stage 3*: When the junction capacitance $C_{\text{oss\_S4}}$ discharges to zero voltage, stage 3 starts and the leakage inductor current i_{Ls} flows through the parallel diode of S_4.
4) *Stage 4*: In this stage, the leakage inductor current i_{Ls} flows through the channel of MOSFET S_4. Because the drain-source voltage of S_4 has already decreased to zero, the turn-ON loss can be ignored and the ZVS operation is realized.

It can be seen that according to the analysis of turn-ON transient, the increasing process of voltage u_{ab} is slow due to the influence of junction capacitance. Besides, the junction capacitance varies nonlinearly with the drain-source voltage, so the waveform of voltage u_{ab} cannot be described by simple analytic expressions. Therefore, the waveform of voltage u_{ab} is piecewise linearized for the sake of analysis. When the actual waveform of u_{ab} is smaller than $U_{\text{in}}/2$, its value is assumed to be zero, and vice versa it is assumed to be U_{in}. The times of the two processes are defined as T_A and T_B, respectively. The slopes of i_{Ls} in the two processes are defined as $K_A = U_{\text{out}}/L_s$ and $K_B = (U_{\text{in}} + U_{\text{out}})/L_s$, respectively. For the sake of illustration, the critical dead time $T_{\text{dead\_cri}}$ is defined as the time required for the junction capacitance to discharge completely, that is

$$T_{\text{dead\_cri}} = T_A + T_B. \tag{3}$$

The ZVS conditions in Fig. 4 contain an implicit condition

$$T_{\text{dead}} = T_{\text{dead\_cri}} \tag{4}$$

where T_{dead} is the dead time. That is to say, S_4 turns ON at the time when $i_{Ls} = 0$. This implicit condition means the dead time T_{dead} is a value that varies with the operating modes, which is difficult to implement in practical application. The implicit condition (4) is just for the convenience of analysis and it will be released in Section III-B.

The same assumption is also suitable for the waveform of u_{cd}. Therefore, the waveforms of u_{ab} and u_{cd} can also be seen as ideal square waveforms. It is worth noting that, the high-frequency voltage u_{ab} and u_{cd} will not change immediately after the device control signal changes due to the influence of junction capacitance, and there is a delay time $T_{\text{delay}} = T_A$.

The charging or discharging charges of S_3 and S_4 in the process of u_{ab} increasing from 0 to $U_{\text{in}}/2$ and increasing from $U_{\text{in}}/2$ to U_{in} are defined as Q_A and Q_B, respectively [17], [24]. Therefore, the expressions of Q_A and Q_B can be derived by integrating i_{Ls} in time T_A and T_B

$$Q_A = \int_{T_A} i_{Ls} dt = \left| i_{Ls}\left(D_1 T_s/2\right)\right| T_A + U_{\text{out}}/L_s \cdot T_A^2/2 \tag{5}$$

$$\begin{aligned} Q_B &= \int_{T_B} i_{Ls} dt \\ &= \left| i_{Ls}\left(D_1 T_s/2\right)\right| T_B - \left(U_{\text{in}} + U_{\text{out}}\right)/L_s \cdot T_B^2/2 \end{aligned} \tag{6}$$

where $|i_{Ls}(D_1 T_s/2)|$, T_A, and T_B are the unknown variables while Q_A and Q_B are the know variables, which can be calculated by referring datasheet.

Take the SiC MOSFET C2M0040120D (Cree) for example to illustrate the calculation process of Q_A and Q_B. Assuming that the input voltage U_{in} is 1000V, the amplitude of u_{ab} is 1000 V. According to the datasheet, the junction capacitance varies with the voltage u_{ab} as is shown in Fig. 6(a). Because the switches S_3 and S_4 withstand the input voltage, the charge Q_A is equal to the charge Q_B due to symmetry, and their values are equal to the area in blue or red in Fig. 6(a). When the input voltage equals another value, the values of the charge Q_A and Q_B can also be calculated with the same method. Fig. 6(b) shows the curve of Q_A and Q_B changing with input voltage U_{in}.

Based on the analysis above, the critical ZVS condition of the time $D_1 \times T_s/2$ in Fig. 2 is that, when the leakage inductor current i_{Ls} increases to zero, the junction capacitance $C_{\text{oss\_S4}}$ discharges to zero voltage. The value of Q_B can be calculated by $0.5 K_{\text{B}} T_{\text{B}}{}^2$, and the critical leakage inductor current is as follows:

$$i_{Ls}\left(D_1 \cdot T_s/2\right) = I_{\text{cri}} = K_B T_B = \sqrt{2 Q_B \left(U_{\text{in}} + U_{\text{out}}\right)/L_s} \tag{7}$$

where I_{cri} is the critical value to realize ZVS operation. Only when the turn-ON current is larger than this value, the ZVS operation can be realized. According to (7), the higher the input and output voltage, the higher the charge stored in junction capacitance, the smaller the leakage inductor, the higher the requirements of the ZVS condition.

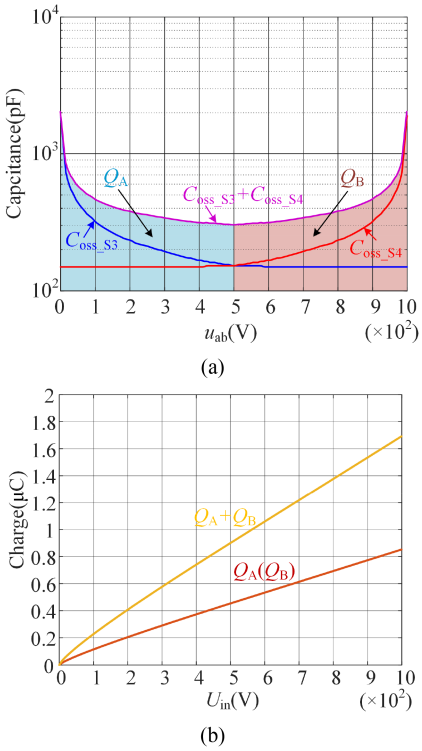

Fig. 6. Junction capacitance and the its stored charge. (a) Junction capacitance varies with the voltage u_{ab}. (b) Charge stored in junction capacitance.

DAB has multiple switching processes for each operating mode. The results of (7) can be generalized to each switching process of each mode. For the sake of illustration, the critical switching currents of primary side and secondary side are defined as $I_{P\_X\_\text{cri}}$ and $I_{S\_X\_\text{cri}}$ respectively, where X represents operation mode X ($X = A, B, C, D$). Then the following conclusions can be derived by critical ZVS condition and the expressions in Table II in Appendix.

1) In modes B and D, not all switches can realize ZVS operation when the influence of junction capacitance is considered. For mode B, i_{Ls} should be greater than 0 at time $(D_0 - D_2)*T_s/2$ and $(D_0 + D_2)*T_s/2$ to achieve ZVS operation. Put this condition into Table II in Appendix, then the phase shift ratio D_0 should be smaller than 0, which contradicts the forward transmission power. For mode D, i_{Ls} should be greater than 0 at time $(D_0 - D_2)*T_s/2$ and be smaller than 0 at time $D_1*T_s/2$. Put this condition into Table II in Appendix, we can also derive a contradiction.
2) In mode A and C, switches can realize ZVS operation if their switching currents are larger than critical currents $I_{P\_X\_\text{cri}}$ or $I_{S\_X\_\text{cri}}$ ($X = A, C$).

The expressions of these critical currents are as follows:

$$\begin{cases} I_{P\_A\_\text{cri}} = \sqrt{2 Q_{B(\text{Uin})}\left(U_{\text{in}} + U_{\text{out}}\right)/L_s} \\ I_{S\_A\_\text{cri}} = \sqrt{2 Q_{A(\text{Uout})}\left(U_{\text{in}} + U_{\text{out}}\right)/L_s} \\ I_{P\_C\_\text{cri}} = \max \\ \left\{\sqrt{2 Q_{B(\text{Uin})}\left(U_{\text{in}} - U_{\text{out}}\right)/L_s}, \sqrt{2 Q_{B(\text{Uin})} U_{\text{out}}/L_s}\right\} \\ I_{S\_C\_\text{cri}} = \sqrt{2 Q_{A(\text{Uout})} U_{\text{out}}/L_s} \end{cases} \tag{8}$$

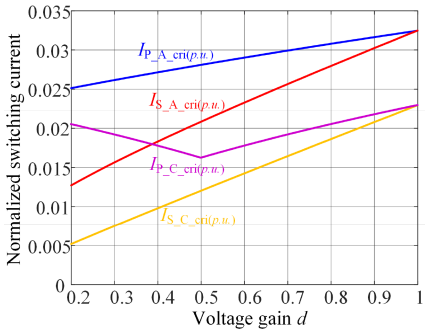

Fig. 7. Normalized critical switching currents when considering junction capacitance.

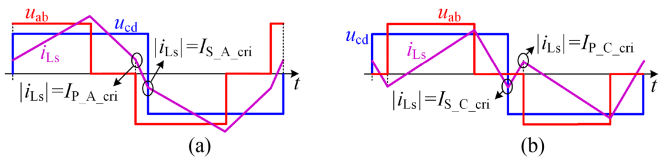

Fig. 8. Critical ZVS waveforms. (a) Mode A. (b) Mode C.

where $Q_{A(\mathrm{Uout})}$ and $Q_{B(\mathrm{Uin})}$ are the charging or discharging charges when the voltage is U_{in} and U_{out} in Fig. 6(a), respectively. According to (8), the normalized critical switching currents are plotted in Fig. 7.

Combing (8) and the expressions in Tables II and III in Appendix A, the normalized maximum ZVS power of mode A is 1, and the normalized minimum ZVS power $P_{A\_\mathrm{cri(p.u.)}}$ and the phase shift ratios of mode A are as follows:

$$\begin{cases} D_0 = I_{S\_A\_\mathrm{cri(p.u.)}} - 0.5d + 0.5 \\ D_1 = \left(2dD_0 - d - 2I_{P\_A\_\mathrm{cri(p.u.)}} + 1\right)/(2+2d) \\ D_2 = 0 \\ P_{A\_\mathrm{cri(p.u.)}} = 4(D_0 - D_0^2 - D_1^2) \end{cases}. \quad (9)$$

The critical ZVS waveform of this case is shown in Fig. 8(a). In the critical case, the absolute value of the switching current is equal to the critical current values $I_{P\_A\_\mathrm{cri}}$ and $I_{S\_A\_\mathrm{cri}}$.

Similarly, the normalized minimum ZVS power of mode C is 0. The normalized maximum ZVS power $P_{C\_\mathrm{cri(p.u.)}}$ and the phase shift ratios of mode C are shown in (10) and the critical waveform of this case is shown in Fig. 8(b)

$$\begin{cases} D_0 = \left(dD_1 - 0.5d - D_1 - I_{P\_C\_\mathrm{cri(p.u.)}} + 0.5\right)/d \\ D_1 = I_{S\_C\_\mathrm{cri(p.u.)}} - 0.5d + 0.5 \\ D_2 = 0 \\ P_{C\_\mathrm{cri(p.u.)}} = 4D_0(1-2D_1) \end{cases}. \quad (10)$$

Still, take the SiC K C2M0040120D (Cree) for example. Assuming that the input voltage U_{in} is 500 V, when the switching currents are larger than these critical currents in Fig. 7, the ZVS operation can be achieved. Therefore, the actual ZVS regions considering junction capacitance with critical dead time [implicit condition (4)] be derived in Fig. 9. The red dashed line [$P_{(\mathrm{p.u.})} = 2d(1-d)$] is the boundary between modes A and C, which can be derived easily by setting critical currents equal to 0 in (9) and (10). In ideal case, the critical ZVS region (or the boundary) of modes A and C is both the red dashed line and the ideal ZVS region is the whole power and whole voltage gain region. However, when considering junction capacitance, the critical ZVS boundaries of modes A and C are the upper and lower bounds of the light blue area, which means there is a non-ZVS region (the light blue area) inherently when considering junction capacitance.

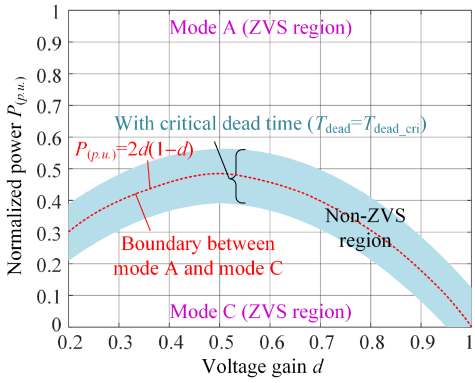

Fig. 9. Actual ZVS range when considering junction capacitance and critical dead time ($T_{\mathrm{dead}} = T_{\mathrm{dead\_cri}}$).

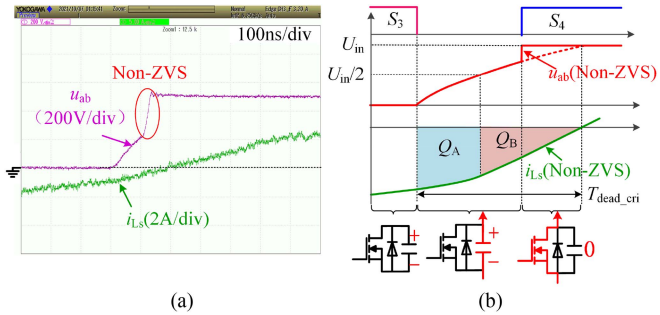

Fig. 10. Non-ZVS waveforms of critical case when $T_{\mathrm{dead}} < T_{\mathrm{dead\_cri}}$. (a) Experiment waveforms. (b) Equivalent waveforms.

B. Influence of Dead Time

Based on the previous analysis, this section will analyze the influence of dead time on the range of ZVS. Take the time $D_1 \times T_s/2$ in Fig. 2 for example to analyze the influence of dead time. When the switching current is equal to the critical current, it does not matter whether the dead time is larger or smaller than the critical dead time, the ZVS condition can't be achieved. These two cases will be examined separately as follows.

1) $T_{\mathrm{dead}} < T_{\mathrm{dead\_cri}}$: Fig. 10 shows the experiment and its equivalent ZVS transient waveforms when $T_{\mathrm{dead}} < T_{\mathrm{dead\_cri}}$. In this case, the absolute value of the switching current is equal to the critical ZVS current, and the junction capacitance can discharge to zero voltage. However, the switch S_4 is turned ON before its junction capacitance could fully discharge because the dead time is too short. In order to realize ZVS operation in the case of $T_{\mathrm{dead}} < T_{\mathrm{dead\_cri}}$, the absolute value of switching current $|i_{Ls}|$ should further increase (as shown by the solid green line in Fig. 11) until the junction capacitance could fully discharge to zero voltage within T_{dead}. The increased critical

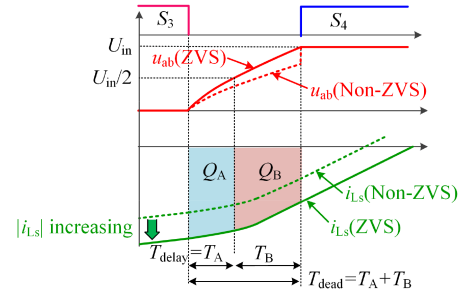

Fig. 11. Increased switching current to realize ZVS operation when $T_{\rm dead} < T_{\rm dead\_cri}$.

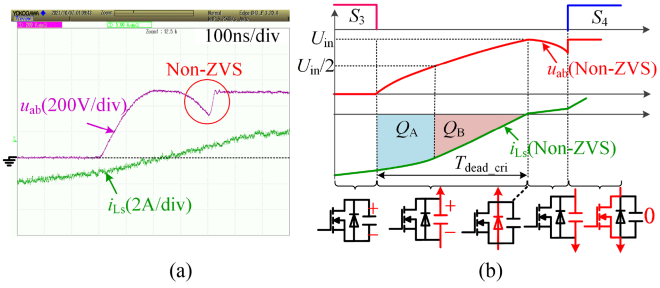

Fig. 12. Non-ZVS waveforms of critical case when $T_{\rm dead} > T_{\rm dead\_cri}$. (a) Experiment waveforms. (b) Equivalent waveforms.

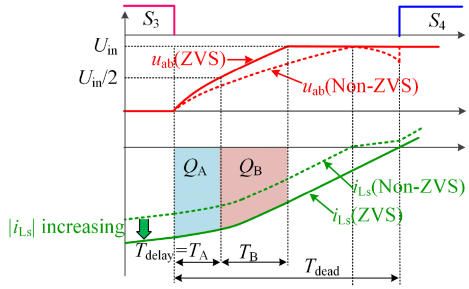

Fig. 13. Increased switching current to realize ZVS operation when $T_{\rm dead} > T_{\rm dead\_cri}$.

current $|i_{Ls}(D_1T_s/2)|$ in this case can be calculated by

$$\begin{cases} Q_A = \int_{T_A} i_{Ls}dt = |i_{Ls}\,(D_1T_s/2)|\,T_A + U_{\rm out}/L_s \cdot T_A^2/2 \\ Q_B = \int_{T_B} i_{Ls}dt \\ \quad = |i_{Ls}\,(D_1T_s/2)|\,T_B - (U_{\rm in}+U_{\rm out})/L_s \cdot T_B^2/2 \\ T_{\rm dead} = T_A + T_B \end{cases} \tag{11}$$

where T_A, T_B, and $|i_{Ls}(D_1T_s/2)|$ are the unknowns to be solved.

2) $T_{\rm dead} > T_{\rm dead\_cri}$: Fig. 12 shows the experiment and its equivalent ZVS transient waveforms when $T_{\rm dead} > T_{\rm dead\_cri}$. In this case, though the absolute value of the switching current is equal to the critical current, the junction capacitance is recharged after full discharge due to the long dead time. In order to realize ZVS operation in the case of $T_{\rm dead} > T_{\rm dead\_cri}$, the absolute value of switching current $|i_{Ls}|$ should further increase until the moment when i_{Ls} crosses zero is later than the turn-ON moment of S_4 (as shown by the solid green line in Fig. 13). The increased

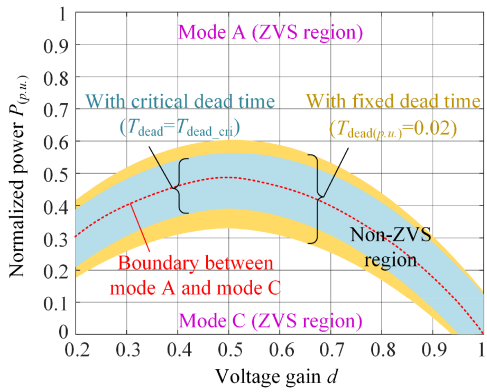

Fig. 14. Actual ZVS range when considering junction capacitance and fixed dead time ($T_{\rm dead(p.u.)} = 0.02$).

critical current $|i_{Ls}(D_1T_s/2)|$ in this case can be calculated by

$$\begin{cases} Q_A = \int_{T_A} i_{Ls}dt \\ \quad = |i_{Ls}\,(D_1T_s/2)|\,T_A + U_{\rm out}/L_s \cdot T_A^2 \Big/ 2 \\ |i_{Ls}\,(D_1T_s/2)| = (U_{\rm in}+U_{\rm out})/L_s \cdot (T_{\rm dead}-T_A) \end{cases} \tag{12}$$

where T_A and $|i_{Ls}(D_1T_s/2)|$ are the unknowns to be solved.

According to (11), (12) and the expressions in Appendix A, the non-ZVS region considering junction capacitance with fixed dead time can be plotted in Fig. 14. In Fig. 14, the dead time $T_{\rm dead(p.u.)}$ is set as 0.02 just for example, and the actual non-ZVS region will change with the dead time $T_{\rm dead(p.u.)}$. In the next section, the dead time will be optimized to get a minimum non-ZVS region. It is clear that the non-ZVS region is larger with fixed dead time.

C. Optimization of Dead Time

Though the non-ZVS region is smallest with the critical dead time $T_{\rm dead\_cri} = T_A + T_B$, the critical dead time varies with the voltage gain and power, which means the critical dead time is not a fixed time. In order to get a fixed dead time and at the same time make the non-ZVS region the smallest, this section will optimize the dead time.

According to (11) and (12), the critical ZVS currents under different voltage gain d and different normalized dead time $T_{\rm dead(p.u.)}$ are shown in Fig. 15.

According to (9), (10), and the critical ZVS currents in Fig. 15, the critical ZVS powers of modes A and C under different voltage gain d and different normalized dead time $T_{\rm dead(p.u.)}$ are shown in Fig. 16(a) and (b), respectively. When the normalized power is larger than the minimum ZVS power of mode A or smaller than the maximum ZVS power of mode C, the ZVS operation can be achieved. The region between the two critical ZVS powers is the non-ZVS region, which can be derived by taking the difference between the two critical ZVS powers [see Fig. 16(c)]. It can be seen the non-ZVS region changes with the dead time, and when the dead time is equal to the optimum dead time $T_{\rm dead\_opti(p.u.)}$ [as shown by the red box in Fig. 16(c)], the non-ZVS region is minimum.

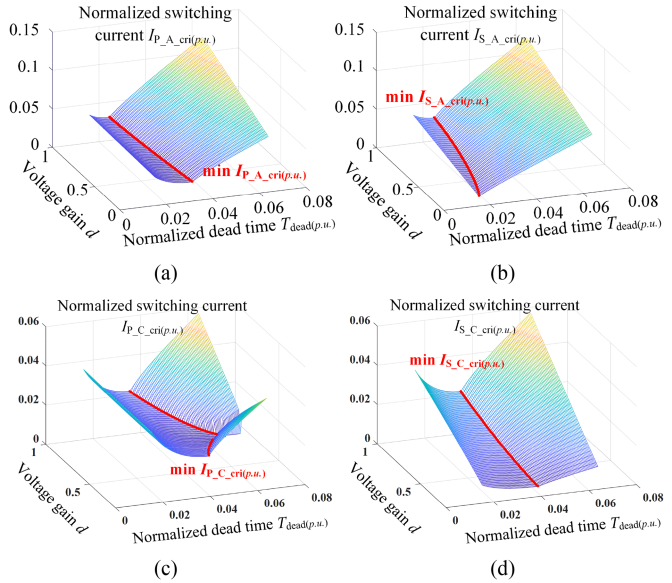

Fig. 15. Critical ZVS currents under different voltage gain d and different normalized dead time $T_{\mathrm{dead(p.u.)}}$. (a) Mode A primary side critical ZVS current $I_{P\_A\_\mathrm{cri(p.u.)}}$. (b) Mode A secondary side critical ZVS current $I_{\mathrm{S\_A\_cri(p.u.)}}$. (c) Mode C primary side critical ZVS current $I_{P\_C\_\mathrm{cri\,(p.u.)}}$. (d) Mode C secondary side critical ZVS current $I_{S\_C\_\mathrm{cri(p.u.)}}$.

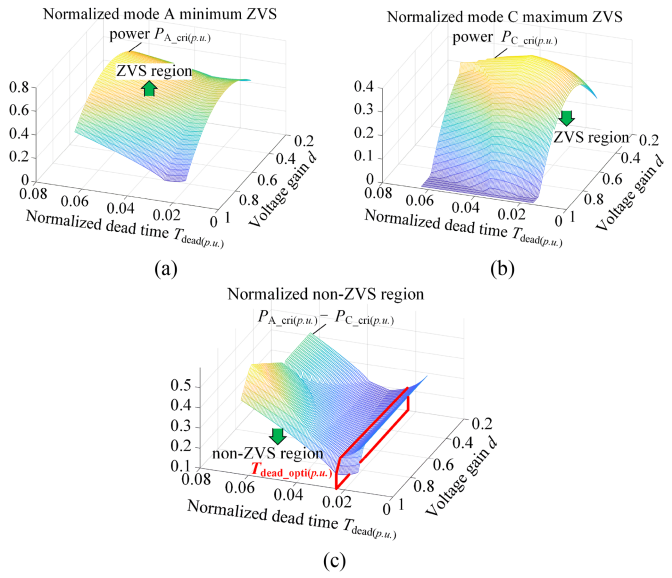

Fig. 16. ZVS region under different voltage gain d and different normalized dead time $T_{\mathrm{dead(p.u.)}}$. (a) ZVS region of mode A. (b) ZVS region of mode C. (c) Non-ZVS region.

Take the SiC MOSFET C2M0040120D (Cree) for example. Other devices can also calculate the corresponding optimum dead time $T_{\mathrm{dead\_opti(p.u.)}}$ and derive the corresponding actual ZVS region. After optimizing the dead time, the actual ZVS range of DAB considering junction capacitance with optimal dead time can be plotted in Fig. 17 by (9)–(12). After optimizing the dead time, the non-ZVS region is smaller than before. When the power is high, use mode A while when the power is low, use mode C. However, when the power is between the two critical ZVS power, part of the DAB switches will lose the ZVS condition.

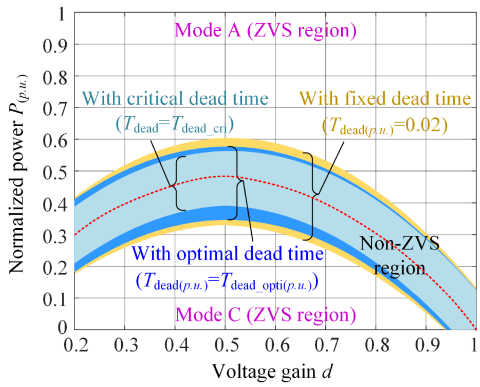

Fig. 17. Actual ZVS range when considering junction capacitance and optimal dead time ($T_{\mathrm{dead(p.u.)}} = T_{\mathrm{dead\_opti(p.u.)}}$).

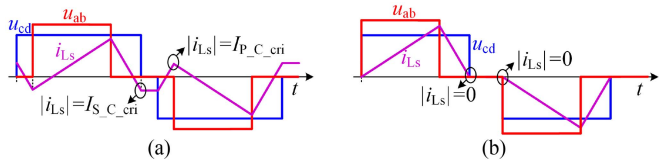

Fig. 18. Critical waveforms of mode C. (a) Considering nonideal factors. (b) Not considering nonideal factors.

IV. Mixed-Mode Modulation

Based on the analysis above, DAB can achieve ZVS operation in part of power region in modes A and C while lose ZVS condition in the rest region. In this section, a novel mixed-mode modulation is proposed, which makes DAB avoid operating at non-ZVS region and realizes the ZVS operation in the wide voltage gain and load range.

For the ZVS region in Fig. 17, the optimal current stress modulation is adopted and its derivation process and the control strategy are shown in Appendix B. Combing (18), (20), and (22) in Appendix B, the control strategy of the optimal current stress modulation in ZVS region considering nonideal factors can be obtained. The distinction between the optimal current stress modulations considering nonideal factors and that not considering nonideal factors is the value of critical switching currents. Take mode C for example. The critical waveforms of mode C when considering and not considering nonideal factors are shown in Fig. 18(a) and (b), respectively. In Fig. 18(a), the critical switching current when considering nonideal factors has enough value to discharge the junction capacitance while in Fig. 18(b), that of not considering nonideal factors is zero, which cannot discharge junction capacitance and may lose ZVS condition.

For the non-ZVS region in Fig. 17, this article proposed a mixed-mode modulation, which makes DAB avoid operating at non-ZVS region. The idea of the mixed-mode modulation is to let DAB operate at modes A and mode C alternately in multiple periods to achieve ZVS operation in the non-ZVS region. In this case, the average power in multiple periods is between the powers of mode A and C. The mixed-mode schematic diagram is shown in Fig. 19. Assuming the mixed-mode is $n = n_{\mathrm{A}} + n_{\mathrm{C}}$ periods, the mode C is n_C periods, and mode A is n_A periods.

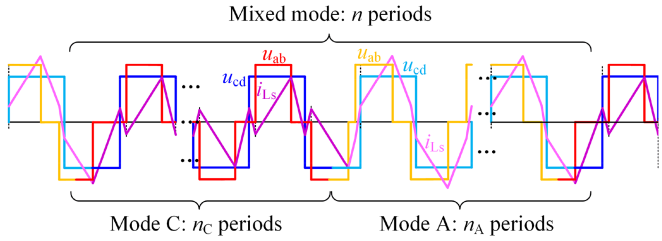

Fig. 19. Mixed-mode modulation's schematic diagram.

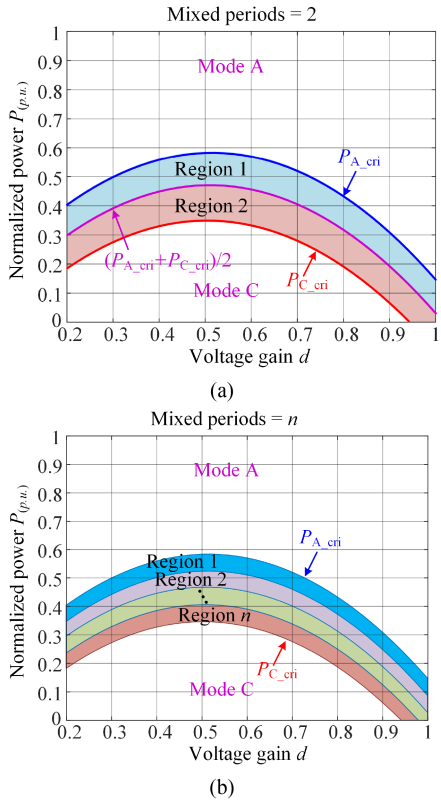

Fig. 20. Power distribution method. (a) When the mixed periods is 2. (b) When the mixed periods is n.

The normalized average power in n periods is as follows:

$$P_{\text{aver(p.u.)}} = \frac{n_C}{n} P_{\text{C(p.u.)}} + \frac{n_A}{n} P_{\text{A(p.u.)}}. \tag{13}$$

According to (20), the power distribution method can be get (see Fig. 20). Take the mixed periods $n = 2$ for example. The non-ZVS region can be divided into two parts, and the boundary between the two regions is $(P_{A\_\text{cri(p.u.)}} + P_{C\_\text{cri(p.u.)}})/2$. When the reference power $P_{\text{ref(p.u.)}}$ is at region 1, the power of mode C should equal the critical ZVS power $P_{C\_\text{cri(p.u.)}}$, and the power of mode A can be calculated by (13). When the reference power $P_{\text{ref(p.u.)}}$ is at region 2, the power of mode A should equal to the critical ZVS power $P_{\text{A\_cri(p.u.)}}$, and the power of mode C can be calculated by (13). Generally, when the mixed periods are n, the non-ZVS region can be divided into n parts. When the reference power $P_{\text{ref(p.u.)}}$ is at region $m(m < \text{n}/2)$, mode C is $n_C = m$ periods, and mode A is $n_A = n - m$ periods. The power distributions of modes A and C are as follows:

$$\begin{cases} P_{C\text{(p.u.)}} = P_{C\_\text{cri(p.u.)}} \\ P_{A\text{(p.u.)}} = \left(nP_{\text{ref(p.u.)}} - mP_{\text{C\_cri(p.u.)}}\right)/(n-m) \end{cases}. \tag{14}$$

When the reference power $P_{\text{ref(p.u.)}}$ is at region $m(m > \text{n}/2)$, the mode C is $n_C = m - 1$ periods, and mode A is $n_A = n - m + 1$ periods. The power distributions of modes A and C are as follows:

$$\begin{cases} P_{A\text{(p.u.)}} = P_{A\_\text{cri(p.u.)}} \\ P_{C\text{(p.u.)}} = \left[nP_{\text{ref(p.u.)}} - (n-m+1)P_{A\_\text{cri(p.u.)}}\right]/(m-1) \end{cases}. \tag{15}$$

It is worth noting that when the mixed periods n increase, the power change $\Delta P = |P_{A\text{(p.u.)}} - P_{C\text{(p.u.)}}|$ in the non-ZVS region is smaller. Meanwhile, lager mixed periods may cause a decrease in response time due to the response time of power changing from period T_s to period nT_s. Therefore, the mixed period n is a tradeoff between power ripple and response time. It is noted that the power change between two modes (with no dc bias of high-frequency currents or oscillation) can be done in a mixed period nT_s by adopting the method proposed in [32].

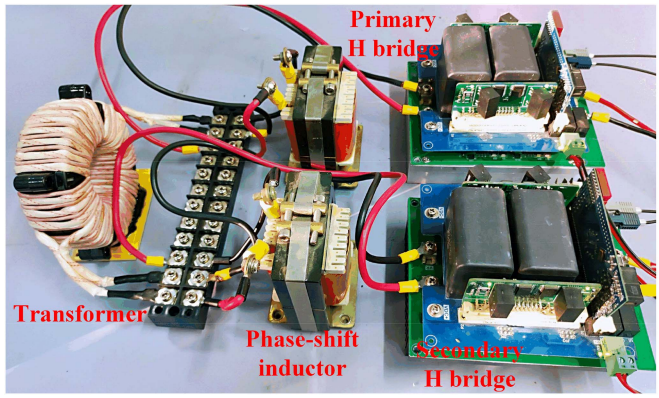

Fig. 21. Prototype.

V. Experimental Results

In order to verify the analysis in previous sections, experimental results are given in this section. The experiment prototype of the DAB converter is built by using SiC MOSFET C2M0040120D (Cree). The transformer adopts an amorphous magnetic core, the ratio is 1:1, and the operation frequency is 25 kHz. The value of phase shift inductance is 117 μH. The input voltage is 500 V, and the output voltage ranges from 200 to 500 V. The maximum power is 4.5 kW. The converter adopts the DSP TMS320F28335 (Texas Instrument) and the complicated part of the calculation can be put into offline calculation. The FPGA 10M08SAE144C8G (Altera) as controllers. Fig. 21 shows the actual prototype. Table I lists the parameters of the prototype.

A. Actual ZVS Range Considering Nonideal Factors

First, the influence of junction capacitance and dead time on ZVS operation is verified experimentally. Take mode C for example. Fig. 22 is the experimental waveforms of Fig. 18 in the previous section, and it shows the comparison of critical ZVS

TABLE I
DESIGN PARAMETERS OF THE PROTOTYPE

Parameter	Value
Input voltage U_{in}	500 V
Output voltage U_{out}	200–500 V
Maximum power P	4.5 kW
Phase shift inductance L_s	117 μH
Turn ratio	1:1
Input capacitance C_{in}	120 μF
Output capacitance C_{out}	120 μF
Switching frequency f	25 kHz

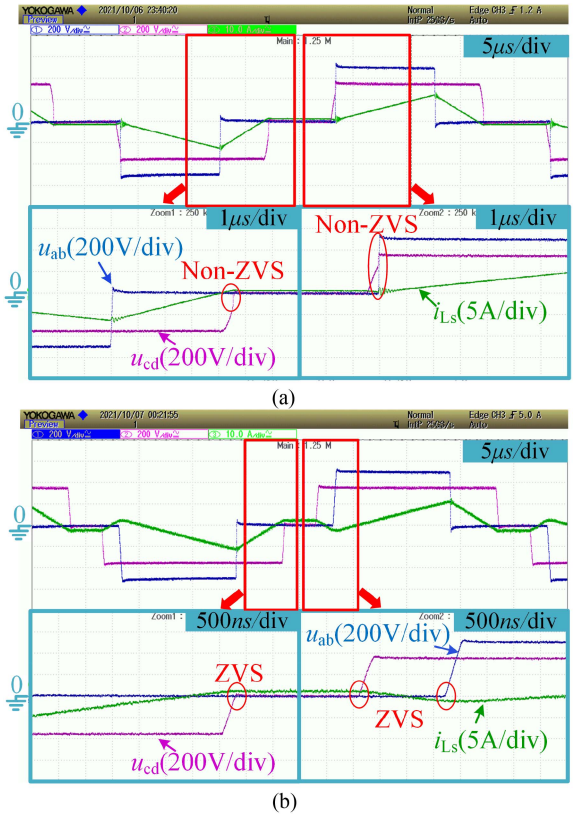

Fig. 22. Waveforms when $U_{out} = 350$ V, $d = 0.7$. (a) Not considering nonideal factors. (b) Considering nonideal factors.

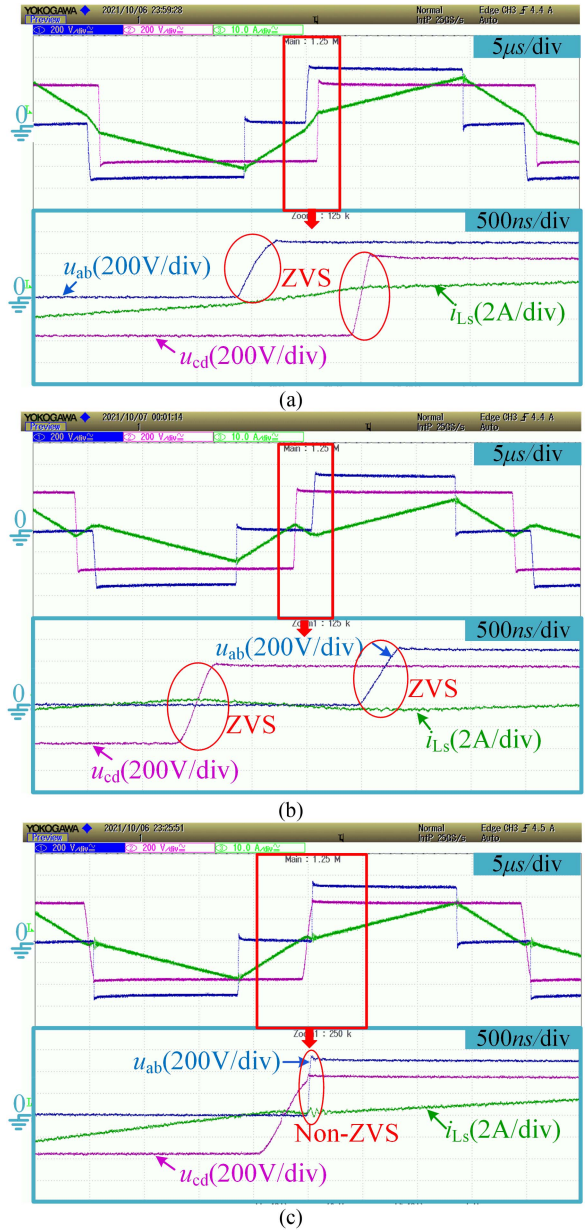

Fig. 23. Waveforms in ZVS region and non-ZVS region. (a) Critical ZVS waveforms of mode A in the ZVS region. (b) Critical ZVS waveforms of mode C in the ZVS region. (c) Waveforms in the non-ZVS region.

waveforms between not considering and considering nonideal factors when $U_{out} = 350$ V, $d = 0.7$.

In theory, when junction capacitance and dead time are not considered, as long as the absolute value of switching current is not less than 0, the ZVS operation can be realized. However, as is shown in Fig. 22(a), the converter has already lost ZVS operation in mode C when the nonideal factors are not taken into consideration, which verifies the conclusion of Fig. 18.

In fact, the absolute value of the switching current should be larger enough to charge or discharge junction capacitance. Fig. 22(b) shows the critical ZVS waveforms when considering nonideal factors. It can be seen that the absolute value with the proposed optimal current stress modulation is larger enough to discharge the junction capacitance, and the ZVS operation can be realized.

Then, verify the conclusion mentioned in Section III, that is, DAB has inherent non-ZVS operating regions when the non-ideal factors are considered. Fig. 23(a) and (b) shows the critical ZVS waveforms of mode A and C, respectively. The ZVS operation is realized in both two cases. Fig. 23(c) shows the waveforms of the non-ZVS region when adopting the optimal current stress modulation in Appendix B. It can be seen that there is an inherent non-ZVS region between modes A and C when considering nonideal factors.

B. Mixed-Mode Modulation Verification

In this section, the proposed mixed-mode modulation of DAB is experimentally verified, and the number of mixed periods n is

TABLE II
NORMALIZED ANALYTIC EXPRESSIONS OF SWITCHING CURRENT

Mode	Switching current			
	$-D_1$	D_1	D_0-D_2	D_0+D_2
A	$0.5\cdot[d(1-2D_0-2D_1)-(1-2D_1)]$	$0.5\cdot[d(1-2D_0+2D_1)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_0+2D_2)]$	$0.5\cdot[d(1-2D_2)-(1-2D_0-2D_2)]$
B	$0.5\cdot[d(1-2D_2)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1+2D_0-2D_2)]$	$0.5\cdot[d(1-2D_2)-(1-2D_0-2D_2)]$
C	$0.5\cdot[d(1-2D_0-2D_1)-(1-2D_1)]$	$0.5\cdot[d(1+2D_0-2D_1)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_1)]$
D	$0.5\cdot[d(1-2D_0-2D_1)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_1)]$	$0.5\cdot[d(1-2D_2)-(1-2D_0-2D_2)]$

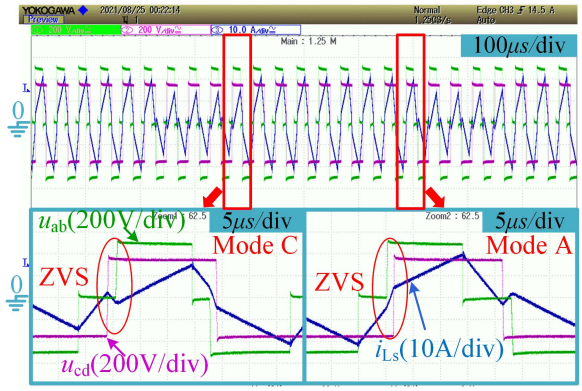

Fig. 24. Waveforms of the mixed-mode modulation.

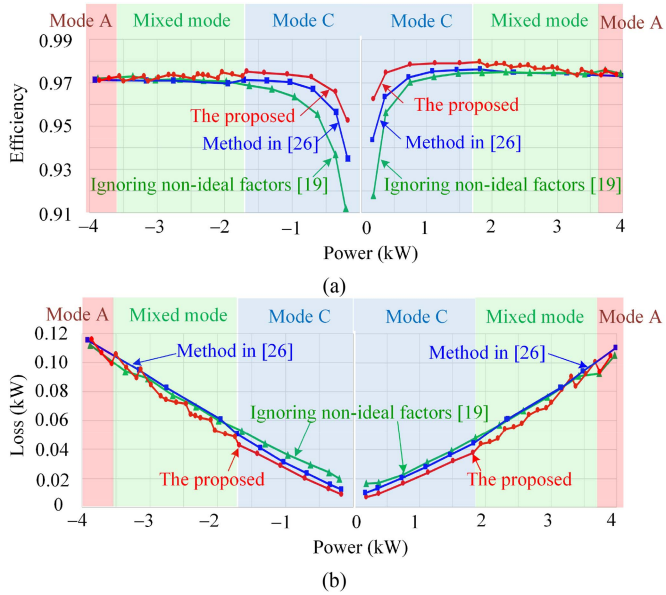

Fig. 25. Efficiency and loss.

set as 12 in this experiment. Taking forward power transmission as an example, the 12 mixed periods in Fig. 24 include eight mode A periods and four mode C periods. It can be seen that DAB can realize the ZVS operation and avoid operating in the nonZVS region with the proposed mixed-mode modulation, which fills the inherent non-ZVS region when considering nonideal factors.

C. Efficiency and Loss Analysis

In this section, the efficiency and loss measurement results of DAB converters with different modulation methods are compared under different voltage gains and output powers. The comparison object includes three modulation methods.

1) Optimal current stress modulation method without considering nonideal factors [19].
2) The modulation method in [26], which only considers the dead time effect, but ignores the junction capacitance
3) Modulation proposed in this article.

Fig. 25 shows the efficiency and loss of the three methods. The experiment condition is $U_{\text{in}} = 500\text{V}$, $U_{\text{out}} = 350\text{V}$.

The modulation method proposed in this article works in mode C when the load is light, in mixed-mode when the load is medium, and in mode A when the load is heavy. With the proposed optimal current stress modulation in the ZVS region and the mixed-mode modulation in the non-ZVS load, the DAB converter can achieve ZVS in a wide load range, so the efficiency is the highest and the loss is the lowest, especially under light load. The efficiency with the proposed method can be up to 4% higher under light load than that with the traditional method ignoring nonideal factors. When adopting the optimal current stress modulation method without considering nonideal factors, part of the DAB operation region losses ZVS operation under light and medium load, so the loss is the largest and the efficiency is the lowest. In [26], the dead time optimization is not carried out and the influence of junction capacitance is not considered, so the efficiency is lower than the method proposed in this article.

VI. CONCLUSION

The article analyzed the influence of nonideal factors on the ZVS range comprehensively, and the exact ZVS region is given when considering nonideal factors. Also, the dead time is optimized to achieve the smallest non-ZVS region. In view of the non-ZVS region, this article proposed a novel mixed-mode modulation, which enable DAB to operate with ZVS in a wide load and voltage gain range.

In conclusion, this article can provide a basis for judging the actual ZVS range of DAB, and provides a way to realize soft switching in a wide voltage gain and power range, which increases efficiency especially under light load. The efficiency with the proposed method can be up to 4% higher under light load than that with the method ignoring nonideal factors.

APPENDIX

A. Expressions of Switching Currents and Power

See Appendix Table II.

TABLE III
NORMALIZED ANALYTIC EXPRESSIONS OF POWER

Mode	Power
A	$4(D_0–D_0^2–D_1^2–D_2^2)$
B	$4D_0(1–2D_2)$
C	$4D_0(1–2D_1)$
D	$2[–D_0^2+2D_0–2(D_1+D_2)–(D_1–D_2)^2]$

B. Derivation of Optimal Current Stress Modulation in the ZVS Region

1) Mode A: According to Table II, among the four switching times, the inductor current i_{Ls} of mode A has the maximum absolute value at the time $-D_1T_s/2$. Therefore, the goal of the optimal current stress modulation is to solve the minimum value of $|i_{Ls(\text{p.u.})}| = |0.5\cdot[d(1-2D_0-2D_1)-(1-2D_1)]|$ under the condition of

$$\begin{cases} P_{(\text{p.u.})} = 4(D_0 - D_0^2 - D_1^2 - D_2^2) = P_{\text{ref(p.u.)}} \\ D_1 + D_2 \le D_0 \\ D_0 \le 0.5 \\ 0.5\left[d(1-2D_0+2D_1)-(1-2D_1)\right] \le -I_{P\_A\_\text{cri(p.u.)}} \\ 0.5\left[d(1-2D_2)-(1-2D_0+2D_2)\right] \ge I_{S\_A\_\text{cri(p.u.)}} \end{cases} \tag{16}$$

where $P_{\text{ref(p.u.)}}$ is the normalized reference power. Solving the question above, the control strategy of mode A can be derived as follows.

When

$$P_{\text{ref(p.u.)}} \le 1 - (2I_{S\_A\_\text{cri(p.u.)}} - d)^2 - \frac{2(d^2 - 2dI_{S\_A\_\text{cri(p.u.)}} + 2I_{P\_A\_\text{cri(p.u.)}} - 1)^2}{(1+d)^2} \tag{17}$$

then

$$\begin{aligned} D_0 &= I_{S\_A\_\text{cri(p.u.)}} - 0.5d + 0.5 \\ D_1 &= \sqrt{D_0 - D_0^2 - P_{\text{ref(p.u.)}}/4} \\ D_2 &= 0. \end{aligned} \tag{18}$$

When

$$P_{\text{ref(p.u.)}} > 1 - (2I_{S\_A\_\text{cri(p.u.)}} - d)^2 - \frac{2(d^2 - 2dI_{S\_A\_\text{cri(p.u.)}} + 2I_{P\_A\_\text{cri(p.u.)}} - 1)^2}{(1+d)^2} \tag{19}$$

then

$$\begin{aligned} D_0 &= \frac{2d^2 - 2d + 1 - d\sqrt{\left(1 - P_{\text{ref(p.u.)}}\right)(2d^2 - 2d + 1)}}{4d^2 - 4d + 2} \\ D_1 &= (0.5 - D_0)(1-d)/d \\ D_2 &= 0. \end{aligned} \tag{20}$$

2) Mode C: According to Table II, among the four switching times, the inductor current i_{Ls} of mode C has the maximum absolute value at the time $-D_1T_s/2$. Therefore, the goal of the optimal current stress modulation is to solve the minimum value of $|i_{Ls(\text{p.u.})}| = |0.5\cdot[d(1-2D_0-2D_1)-(1-2D_1)]|$ under the condition of (21)

$$\begin{cases} P_{(\text{p.u.})} = 4D_0(1-2D_1) = P_{\text{ref(p.u.)}} \\ 0 \le D_0 \\ D_0 \le D_1 - D_2 \\ 0.5\left[d(1+2D_0-2D_1)-(1-2D_1)\right] \le -I_{P\_C\_\text{cri(p.u.)}} \\ 0.5\left[d(1-2D_2)-(1-2D_1)\right] \ge I_{S\_C\_\text{cri(p.u.)}} \end{cases}. \tag{21}$$

Solving the question above, the control strategy of mode C can be derived

$$\begin{aligned} D_0 &= \frac{1 + 2dD_1 - d - 2D_1 - 2I_{P\_C\_\text{cri(p.u.)}}}{2d} \\ D_1 &= dD_2 - 0.5d + I_{S\_C\_\text{cri(p.u.)}} + 0.5 \\ D_2 &= \frac{\left[\begin{array}{l} 2I_{P\_C\_\text{cri(p.u.)}} + (4I_{S\_C\_\text{cri(p.u.)}} - 2d)(1-d) \\ +\sqrt{4I_{P\_C\_\text{cri(p.u.)}}^2 + 2P_{\text{ref(p.u.)}}d(1-d)} \end{array}\right]}{4d^2 - 4d}. \end{aligned} \tag{22}$$

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Zhe Wang (Student Member, IEEE) received the B.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with Tsinghua University, Beijing, China.

His research interests include high-step-up dc–dc converters and fuel cell vehicles.

Chi Li (Member, IEEE) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2015 and 2018, respectively.

From 2012 to 2018, he was a Research Assistant with the Center for Power Electronics Systems, Virginia Tech. In 2018, he was with Tsinghua University, where he is currently an Assistant Researcher with the Department of Electrical Engineering. His research interests include control and stability of grid-tied power electronics converters and systems, and solid-state transformers.

Jiye Liu (Student Member, IEEE) was born in Hebei, China, in 1993. He received the B.S. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2017 and 2022, respectively.

In 2022, he was with Beijing Relpow Technology Co., Ltd. His current research interests include multilevel converters, power electronic transformers, and application of wide bandgap devices.

Zedong Zheng (Senior Member, IEEE) was born in born in Shandong, China, in 1980. He received the B.S. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2003 and 2008, respectively.

He is currently an Associate Professor with the Department of Electrical Engineering, Tsinghua University. His current research interests include power electronics converters and high-performance motor control systems.