High Step-Up Gain Converter Based on Two-Phase Interleaved Coupled Inductor Without Right-Hand Plane Zero

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***Abstract*—This article proposed a novel two-phase interleaved coupled inductor (CI)-based high step-up gain converter without right half-plane (RHP) zeros for a wide operating range of duty cycle. A CI between input and output is used in the proposed converter to eliminate RHP zero. The energy of CI is transferred to an output capacitor when switch is ON to eliminate RHP zero. Furthermore, the converter has a wide operating range to eliminate RHP zero with a coefficient coupling of CI near one. Thus, the converter achieves a higher bandwidth and a wide range of control over output voltage. The small-signal model of the proposed converter is derived to verify the proposed claim. The single-loop voltage control is sufficient to regulate output voltage of the converter with a good stability margin and faster dynamic response for a wide range of load changes. In addition, the proposed converter has a high-voltage step-up gain and low voltage stress on switching devices compared with the boost converter. Moreover, interleaved operation at input side reduces ripple and increases power density. All theoretical findings are verified by simulation and experimental results. Experimental results are provided from implemented laboratory prototype of an input voltage of 24 V to an output voltage of 100 V and 200 W power.**

***Index Terms*—Coupled inductor (CI), high step-up gain, interleaved, nonminimum phase, right half-plane (RHP) zero, small-signal model.**

I. Introduction

THE demand for high step-up voltage gain dc–dc converters is increased in fields, such as dc microgrid, distributed generation system, and electric vehicle/hybrid electric vehicles [1], [2], [3], in recent years. Renewable energy sources (RES), such as photovoltaic (PV) panels and fuel cells, are low-voltage input sources, so it is impractical to directly connect the PV panel/fuel cell to the dc microgrid [4], [5]. Although the series connection of PV arrays is one way to increase voltage level, the total output power of PV modules is reduced because of uneven illumination intensity or module mismatch [6]. A high step-up gain dc–dc converter acts as a bridge between low-voltage input source, such as PV array/fuel cells and high step-up gain applications. However, boost dc–dc converter is not able to achieve high voltage gain of 10–20 times with high overall efficiency due to the parasitic parameters [7]. The main requirements for the satisfactory performance of high step-up gain converters are as follows:

1) desired voltage and power level,
2) stable operation and better dynamic response in the case of wide changes in load/ source, and
3) ripple in input current should be low, so it can significantly increase efficiency and lifetime of PV and fuel cells [4], [8].

Various nonisolated high step-up dc–dc topologies using coupled inductor (CI), switched capacitor, voltage multiplier, voltage lift technique, hybrid structure, and multilevel structure have been discovered in order to achieve high voltage gain and avoid extremely large duty ratio [4]. Among various nonisolated high step-up gain technique, CI is most popular. In order to implement, high voltage gain requires high turn ratio of CI. Utilizing high turns ratio of CI has drawback, such as big size of magnetic core, increases winding and core loss, large leakage inductance causes more voltage stress on switch, more current stress on switch due to input current ripples increases at high power, high conduction loss, and reduce converter efficiency. In hybrid combination of nonisolated boosting techniques, the combination of CI with other high step-up techniques is a well-known choice to achieve high voltage gain with reduce stress on switching devices and improved efficiency [4], [7], [9], [10].

Another major issue with boost converter is the presence of a right half-plane (RHP) zero in the control-to-output transfer function when operating in continuous conduction mode (CCM) [11], [12]. The presence of RHP zero makes the converter a nonminimum phase with relatively low bandwidth (BW) and slow dynamic performance. When the duty ratio steps up in the boost converter, the more energy is stored in the magnetizing inductance rather than being transferred to the output capacitor. Therefore, the output voltage initially decreases. This undesirable voltage dip makes the control scheme more complicated in real-time implementation. Crossover frequency should be designed at low frequency to meet the stability requirement in a close-loop control of boost converter. It results in a low

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BW, which is unsuitable for fast dynamic applications [5]. The high step-up gain dc–dc converters have to operate for wide range of control (load or input voltage disturbance) when it is used to step-up low input voltage source, such as PV array and fuel cell, to dc grid voltage level. In feedback controllers, the inverted initial responses created by an RHP zero cause the controller to generate erroneous driving signals, impeding system control. The zero and pole locations of transfer function in s-domain move with the variations of duty ratio. These movements would result in unsatisfactorily oscillatory and worst nonminimum-phase responses especially in RES applications with the requirement of wide range voltage regulation. In order to ensure the system stability, typical voltage loop controller cannot be designed to achieve desired dynamic response. The output voltage suffers slower and oscillatory response due to the low value of BW in the voltage-loop control. Therefore, it is difficult to design voltage controller to meet the high-performance requirement of high step-up gain converter in RES. Thus, to enhance close-loop BW and stability of the boost converter, elimination of RHP zero is important. New circuit topologies [11], [12], [13], [14], [15] or complex control [16], [17], [18] techniques are researched to eliminate RHP zero and its effect on the dynamic response of boost converter. To improve the dynamic response of high step-up gain converter due to the presence of RHP zero, dual-loop control technique in [19] and adaptive dual-loop control technique in [20] are implemented.

In [11], [21], and [22], magnetic coupling between the input inductor and the output filter inductor of the boost converter is provided to eliminate RHP zero. The magnetic coupling between the input and output inductors allows the energy to be transferred to the output capacitor even if the output diode is turned OFF. The introduction of magnetic coupling in boost converter transforms the RHP zeros into two zeros. The zero can be located on the left half-plane (LHP) by the proper selection of both inductor and coefficient of coupling (k). The limitation of this topology is that if the coefficient of coupling of a converter is taken one to keep zero far away from the RHP, it increased significant amount ripple in input and output currents [11], [21], [23]. It limits a value of k to 0.707 to eliminate RHP zero with appropriate amount of ripple [23]. To overcome a ripple issue of this topology, an additional *RC* damping network is connected in parallel with output capacitor in [23] and [24]. In [21], an integrated magnetic boost converter with input and output current ripple cancellations and RHP zero elimination has been proposed. In addition, third winding is used to cancel ripple in input current.

However, to satisfy the minimum-phase system requirement, the duty cycle variable range of the boost converter with magnetic coupled filter (BCMCF) is extremely narrow. In a wide range of control, the placements of zeros of this converter are observed to move from LHP to RHP and increase converter instability. The issue of low operating range of magnetic coupling to eliminate RHP zero due to ripple in input current is overcome by using interleaving technique and inverse coupling between two CIs in [15]. However, voltage gain is same as boost converter with more number of components count. In [14], the high step-up gain boost-forward converter is presented. In this converter, when the switch is ON, CI transfers energy to the output capacitor to eliminate RHP zero and also to enhance the voltage gain. The boost-forward converter provides higher voltage step-up gain than boost converter for same duty cycle. It also allows to use high value of coefficient of coupling near to one. However, increasing the value of k reduces the operating range of control to eliminate RHP zero. If the value of k is decreased to increase the operating range, the voltage gain of the converter is decreased and the converter needs to operate high duty cycle to restore same voltage gain. If the value of k is increased to restore the voltage gain, the ripple in input current increases. The presented converter has high value of ripple in input current due to the amplify action of CI. A high value of ripple in input current increases current stress, conduction losses, and reduce life span of PV array and fuel cell. This limits its application to high-power application.

To eliminate RHP zero, one another boost topology, tristate is developed in [18], [25], [26], and [27]. In tristate-based topology, output capacitor charging interval keeps constant by providing a freewheeling interval using an additional switch and a diode. The introduction of tristate improves dynamic response, but it requires more complex control circuit. Moreover, it has same gain as the boost converter. To eliminate RHP zero and improve the BW and stability margin, a minimum-phase bipolar converter is introduced for the easy operation of maximum power point tracking (MPPT) in [28]. This converter is implemented by combining the Cuk and SEPIC converters. However, this converter has step-up voltage gain same as boost converter with more components count. Another topology to eliminate RHP zero is presented, named KY converter, and it derivatives in [29]. It has same behavior as the buck converter with synchronous rectification, and hence, this converter possesses good load transient response, and output current is nonpulsating. Although KY converter has no RHP zero, in [30], to achieve a high voltage gain in this topology, several switched capacitor cells are used. Diode–capacitor-based high step-up gain converter without RHP zero is presented in [31]. In this, *RC* type damping network is connected with intermediate capacitors to locate zeros from RHP to LHP. However, two additional RC networks do not contribute to enhance the voltage gain. Moreover, additional components count increased cost and reduced efficiency. In [32], a third-order boost converter (TOBC) with a higher voltage gain is compared with the boost converter and minimum-phase characteristic. However, the operating range to eliminate RHP zero is as low as the converter cannot eliminate RHP zero for voltage gain more than three. Moreover, the uncommon ground between input and output leading to noise and diode reverse recovery problems.

Inspired by the above mentioned literature and the limitation of presented converters, a new converter is proposed to bridge this research gap in this article. The proposed converter combines a two-phase interleaved CI with voltage multiplier cells. The circuit arrangement is such that more energy of CI is transferred to output capacitor in forward mode than boost mode. Thus, an initial voltage dip in the output voltage eliminates when duty cycle increases due to step changed in a load. The proposed converter can eliminate RHP zero for a wide operating

range with coefficient coupling of CI near one compared with the boost-forward converter and BCMCF for same rating. The high ripple value in the input current due to magnetic coupling with a high value of k is reduced by applying the interleaving technique at the input side in the proposed converter. The proposed converter can achieve high voltage gain with low duty cycle in comparison to boost converter, boost-forward converter, and BCMCF. The proposed converter has the following distinct features.

1) The combination of CI with voltage multiplier cell increases voltage gain and reduces voltage stress on semiconductor devices. The converter can achieve a high step-up gain by either changing duty cycle or turn ratio of CI.
2) The proposed converter shifts zero in control to output voltage transfer function from RHP to LHP with an appropriate selection of parameters for a wide range of duty cycle with k near to one. Thus, the converter has higher BW and better dynamic response.
3) Single voltage-loop control is sufficient to regulate output voltage and to further enhance the dynamic response.
4) Due to the interleaving operation at the input side of the proposed converter, it requires a low value of inductance of CI to reduce ripple in input current than the boost-forward converter. The low value of inductance of CI reduces the size of a magnetic core, number of turns, and core and winding losses. It also reduces current stress on device and conduction losses, thus improving efficiency and increases power density.

The rest of this article is organized as follows. Section II discussed the proposed converter's construction and explained working principle. The performance parameters of the proposed converter are derived in Section II. A small-signal model of the proposed converter is derived in Section III. The small signal results analysis and controller design are discussed in Section III. Simulation results, frequency response analysis, and performance comparison are given in Section IV. The experimental results of the proposed converter of the laboratory prototype are presented in Section V. Finally, Section VI concludes this article.

II. Basic Principle and Construction of Proposed Converter

In this section, the basic principle and the construction of the proposed converter is explained. Fig. 1 shows the schematic diagram of the proposed converter. It consist of two CI (CI_1 and CI_2), two MOSFET switch (S_1 and S_2), multiplier capacitor (C_m), two output capacitors (C_{o1} and C_{o2}), multiplier diode (D_m), two output diodes (D_{o1} andD_{o2}), and load resistance (R_o). Primary winding of both CI with N_1 turns are employed in interleaved to reduce input current ripple. The secondary winding of both CI has turns of N_2. Secondary winding of the CI_1 with N_{s1} turns is connected in series with the output capacitor C_{o2} such way that it can transfer the energy of CI_1 in forward mode to output capacitor C_{o2}. Similarly, secondary

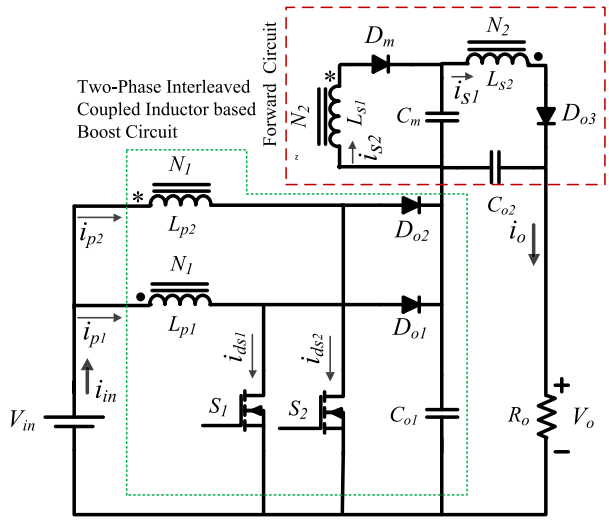

Fig. 1. Circuit diagram of the proposed converter.

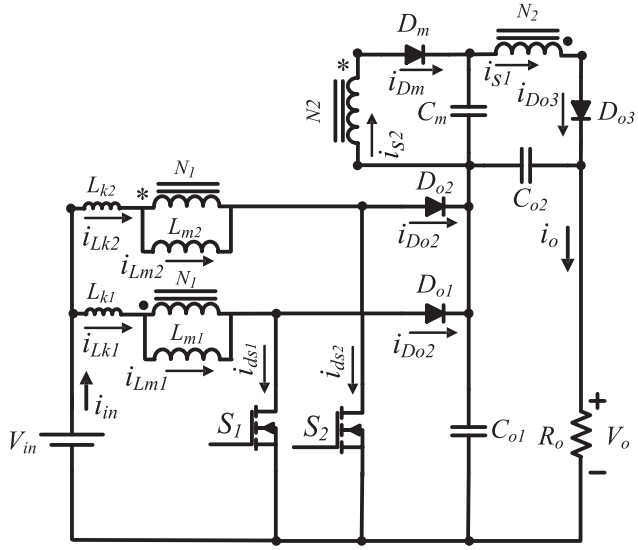

Fig. 2. Equivalent circuit diagram of the proposed converter.

winding of the CI_2 with N_{s2} turns is connected in series with multiplier capacitor C_m in such way that it can transfer the energy of CI_2 in forward mode and further extend the voltage gain. In Fig. 1, "•" and "∗" denotes the coupling references of the CI_1 and CI_2, respectively.

The equivalent circuit of the proposed converter is shown in Fig. 2. The CI is modeled as a combination of a magnetizing inductance (L_m), a leakage inductance (L_k), and an ideal transformer with the corresponding coupling coefficient of the CI k is equal to $L_m/(L_m + L_k)$. Turns ratio n of CI is N_2/N_1. The duty cycles of the power switches are interleaved with a 180° phase shift. Fig. 3 shows the key waveforms of the converter for duty cycle more than 50%. The converter has six modes of operation in one switching period. The working principle of a proposed converter is explained as follows.

Mode 1 [$t_0 - t_1$]: At t_0, the switch S_1 turns-ON and diode D_{o1} turns-OFF,as shown in Fig. 4(a). The switch S_2 remains

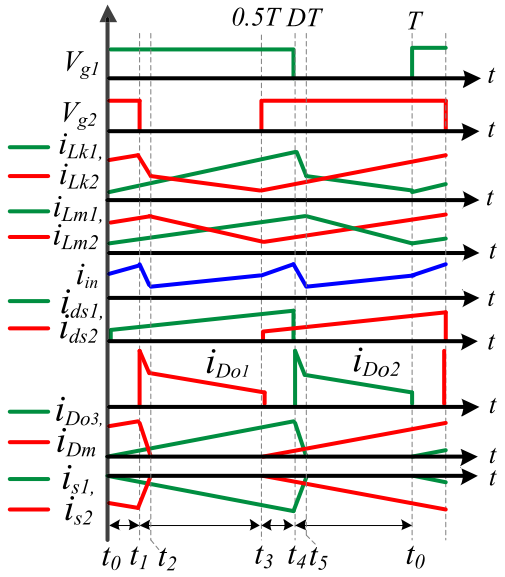

Fig. 3. Key waveforms of the proposed converter in one switching cycle.

ON and the dc input supply energized magnetizing inductance (L_{m1} and L_{m2}) of both CI. Diodes D_m and D_{o3} are conducting. The series combination of secondary winding of CI_1 and CI_2 with multiplier capacitor energized the output capacitor C_{o2} in forward mode. The equations are derived in this mode as follows:

$$\frac{di_{Lm1}}{dt} = \frac{di_{Lm2}}{dt} = \frac{v_{\text{in}}}{L_m} \tag{1}$$

$$\frac{dv_{cm}}{dt} = \frac{i_{Dm} - i_{Do3}}{c_m} \tag{2}$$

$$\frac{dv_{co2}}{dt} = \frac{i_{Do3} - i_o}{c_{o2}}. \tag{3}$$

Mode 2 [$t_1 - t_2$]: At t_1, the switch S_2 is turned OFF and diode D_{o2} is turned ON. Output diode (D_{o2}) and capacitor (C_{o2}) act as a clamp circuit and recycles the energy of leakage inductance of CI_1 to output capacitor C_{o1}, as shown in Fig. 4(b). Thus, it reduced the voltage spike on switch S_2 due to leakage inductance of CI. When leakage current (i_{Lk2}) is equal to magnetizing current (i_{Lm2}), this mode is ended.

Mode 3 [$t_2 - t_3$]: At t_2, the current through diode D_m is decreased to zero and turned OFF, as shown in Fig. 4(c). The dc input supply continue to energies magnetizing the inductance of CI_1. The series combination of a secondary winding of CI_1 with multiplier capacitor continue to energize the output capacitor C_{o2} in forward mode. The dc input supply series with L_{m2} of CI_2 and energized output capacitor C_{o1} in boost mode. Both output capacitor deliver energy to load. The state equation during this mode are as follows:

$$\frac{di_{Lm1}}{dt} = \frac{v_{\text{in}}}{L_m} \tag{4}$$

$$\frac{di_{Lm2}}{dt} = \frac{v_{\text{in}} - v_{co1}}{L_m} \tag{5}$$

$$\frac{dv_{cm}}{dt} = \frac{-i_{Do3}}{c_m} \tag{6}$$

$$\frac{dv_{co1}}{dt} = \frac{i_{Lm2} - i_o}{c_{o1}} \tag{7}$$

$$\frac{dv_{co2}}{dt} = \frac{i_{Do3} - i_o}{c_{o2}}. \tag{8}$$

Mode 4 [$t_3 - t_4$]: At t_3, the switch S_2 is turned ON, diode D_{o2} is turned OFF, and diode D_m is turned ON, as shown in Fig. 4(d). The dc input supply energized magnetizing inductance of both CI. The secondary winding of CI_2 starts to energize multiplier capacitor in forward mode. The series combination of secondary winding of CI_1 with multiplier capacitor continue to energize the output capacitor C_{o2} in forward mode. Both output capacitors deliver energy to load. The state equations of this mode are same, as expressed (1)–(3) in mode 1.

Mode 5 [$t_4 - t_5$]: At t_4, the switch S_1 is turned OFF, and the current through the diode D_{o1} starts to increase and diode D_{o3} start to decrease, as shown in Fig. 4(e). Output diode (D_{o1}) and capacitor (C_{o1}) act as clamp circuit and recycle the energy of leakage inductance of CI_2 to output capacitor C_{o1}, as shown in Fig. 4(e). Thus, it reduced the voltage spike on switch S_1 due to leakage inductance of CI. When leakage current (i_{Lk1}) is equal to magnetizing current (i_{Lm1}), this mode is ended.

Mode 6 [$t_5 - t_0$]: At t_5, the switch S_1 is turned OFF, D_{o3} is turn OFF, and diode D_{o1} starts to conduct, as shown in Fig. 4(f). The dc input supply series with L_{m1} of CI_1 energized output capacitor C_{o1} in boost mode. The switch S_2 remains in ON state and the dc input supply energized L_{m2} of CI_2. The secondary winding of CI_2 continues to energize capacitor C_m in forward mode. The equation is derived in this mode as follows:

$$\frac{di_{Lm1}}{dt} = \frac{v_{\text{in}} - v_{co1}}{L_m} \tag{9}$$

$$\frac{di_{Lm2}}{dt} = \frac{v_{\text{in}}}{L_m} \tag{10}$$

$$\frac{dv_{cm}}{dt} = \frac{i_{Dm}}{c_{o2}} \tag{11}$$

$$\frac{dv_{co1}}{dt} = \frac{i_{Lm1} - i_o}{c_{o1}} \tag{12}$$

$$\frac{dv_{co2}}{dt} = \frac{-i_o}{c_{o2}}. \tag{13}$$

The construction of the proposed converter is in such a way that the energy of inductance transferred in forward mode is more than boost mode to output capacitor. More average current flows in a forward path to the output capacitor due to a higher value of peak current of leakage inductance of CI. Thus, the proposed converter eliminates RHP zeros from control to output transfer function and better dynamic response. In addition, as two-phase interleaved structure input side of the proposed converter, the value of inductance of CI is also reduced in comparison to boost-forward converter for same ripple in input current.

III. Derivation of Performance Parameters

In this section, voltage gain and voltage stress on semiconductor devices of the proposed converter are derived for performance analysis.

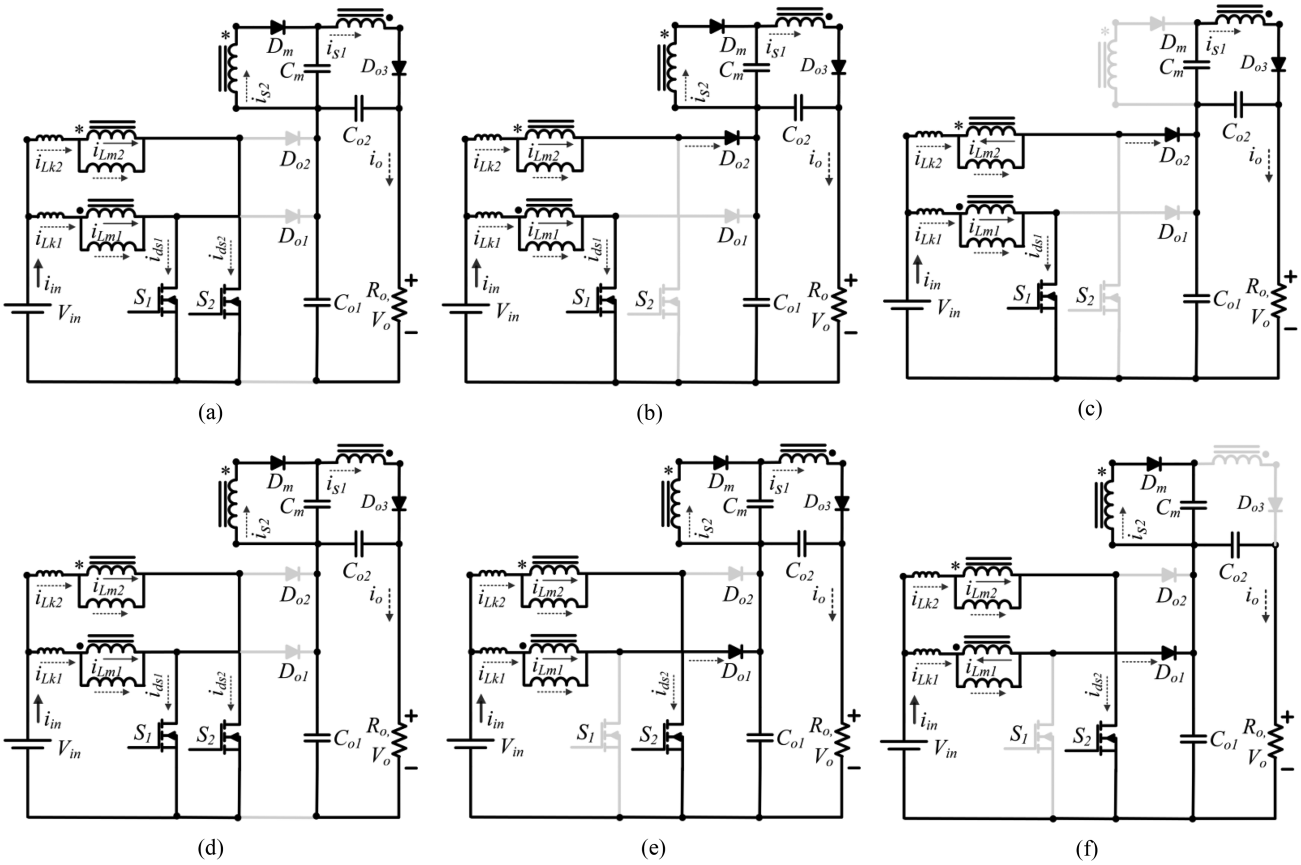

Fig. 4. Operating modes of the proposed converter in one switching cycle: (a) mode 1 $[t_0 - t_1]$, (b) mode 2 $[t_1 - t_2]$, (c) mode 3 $[t_2 - t_3]$, (d) mode 4 $[t_3 - t_4]$, (e) mode 5 $[t_4 - t_5]$, and (f) mode 6 $[t_5 - t_0]$.

A. *Voltage Gain of Proposed Converter*

In Fig. 4, modes 3 and 6 are considered to derive the voltage gain of the proposed converter. The voltage gain of the proposed converter is derived as follows.

When switch S_1 is ON and S_2 is OFF in mode 3, as shown in Fig. 4(c), the following equations are derived:

$$V_{\text{in}} = V_{Lm1\_\text{charge}} \tag{14}$$

$$V_{\text{in}} = V_{Lm2\_\text{discharge}} + V_{co1} \tag{15}$$

$$V_{Co2} = V_{Cm} + nV_{Lm1_{\text{charge}}} V_{Cm} = nV_{\text{in}} + V_{Cm}. \tag{16}$$

When switch S_2 is ON and S_1 is OFF in mode 6, as shown in Fig. 4(e), the following equations are derived:

$$V_{\text{in}} = V_{Lm2\_\text{charge}} \tag{17}$$

$$V_{\text{in}} = V_{Lm1\_\text{discharge}} + V_{co1} \tag{18}$$

$$V_{Cm} = nV_{Lm2\_\text{charge}}, V_{Cm} = nV_{\text{in}}. \tag{19}$$

Apply the volt–second balance principle to magnetizing inductance L_{m1} of CI_1

$$\int_0^D V_{Lm1\_\text{charge}} dt + \int_0^{1-D} V_{Lm1\_\text{discharge}} dt = 0. \tag{20}$$

Substitute (14) and (18) into (20), the voltage of the output capacitor V_{Co1} is derived and expressed as

$$\frac{V_{Co1}}{V_{\text{in}}} = \frac{1}{1-D}. \tag{21}$$

Apply the volt–second balance principle to magnetizing inductance L_{m2} of CI_2

$$\int_0^D V_{Lm2\_\text{charge}} dt + \int_0^{1-D} V_{Lm2\_\text{discharge}} dt = 0. \tag{22}$$

Substitute (15) and (19) into (22), the voltage of the multiplier capacitor V_m is derived and expressed as

$$V_{Cm} = nV_{\text{in}}. \tag{23}$$

Substitute (23) into (16), the voltage of the output capacitor V_{Co2} is derived and expressed as

$$\frac{V_{Co2}}{V_{\text{in}}} = 2n. \tag{24}$$

Voltage gain of the proposed converter is

$$\frac{V_o}{V_{\text{in}}} = \frac{V_{Co1} + V_{Co2}}{V_{\text{in}}}. \tag{25}$$

Substitute (21) and (24) into (25), the voltage gain is derived and expressed as

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} + 2n. \tag{26}$$

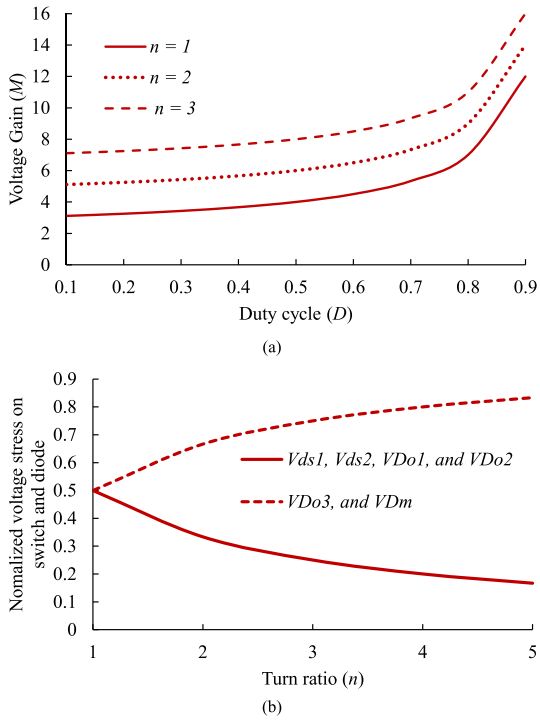

Fig. 5. Effect of turn ratio on performance parameters. (a) Curve of voltage gain versus duty ratio for different value of turn ratio. (b) Curve of voltage stress on power switch and diode versus turn ratio for duty cycle $D = 0.5$.

Equation (26) shows the voltage gain of the proposed converter. The gain of the converter can be increased by changing the turn ratio of CI or duty ratio. Fig. 5(a) shows the curve of the voltage gain of the proposed converter versus duty cycle for different turn ratio. It can be seen that the voltage gain of the converter is increased by changing turn ratio and duty cycle. The converter can be achieved high step-up voltage gain with low duty cycle using high turn ratio.

B. Voltage Stress on Semiconductor Device of Proposed Converter

In this section, the voltage stress on power switch and diode is derived. The voltage stress on both MOSFET switches S_1 and S_2 (V_{ds1} and V_{ds2}) is

$$V_{ds1} = V_{ds1} = \frac{V_{\text{in}}}{1-D} = \frac{V_o}{1+2n-2nD}. \tag{27}$$

The voltage stress on output diodes D_{o1} and D_{o2} ($V_{Do1}$and V_{Do2}) is

$$V_{Do1} = V_{Do2} = \frac{V_{\text{in}}}{1-D} = \frac{V_o}{1+2n-2nD}. \tag{28}$$

The voltage stress on multiplier diode D_m and output diode D_{o3} is

$$V_{Dm} = V_{Do3} = \frac{nV_{\text{in}}}{1-D} = \frac{nV_o}{1+2n-2nD}. \tag{29}$$

In (27), the voltage stress on the MOSFET is 50% of output voltage for $D = 0.5$ and $n = 1$ and decreases with increasing the turns ratio of CI, as shown in Fig. 5(b). In (28) and (29), the voltage stress of all output diodes is less than the output voltage. Fig. 5(b) shows that the voltage stress on diodes D_{o1} and D_{o2} decreases with increases number of turns ratio of CI. The maximum voltage stress is on diodes D_m and D_{o3}, and it increases with increasing the turns ratio of CI, as shown in Fig. 5(b).

The proposed converter can operate with high voltage gain and low voltage stress on switching devices compared with boost and boost-forward converter at same duty cycle.

IV. Small-Signal Model of Proposed Converter

The small-signal transfer function of the proposed converter in CCM is derived in this section to study the dynamic behavior and to design controller. The small-signal model of the proposed converter is derived using state-space averaging technique. The state-space averaged model of the converter is obtained under the following considerations.

1) Magnetizing inductance, leakage inductance, and coefficient coupling of both CI are considered equal, hence $L_{m1} = L_{m2} = L_m$ and $L_{k1} = L_{k2} = L_k$, $k_1 = k_2 = k$.
2) The input current is evenly shared in each phase. The current through each phase is $i_{Lm1} = i_{Lm2} = i_{Lm}$.
3) Semiconductor devices are considered ideal. Equivalent series resistances of all capacitors and CIs are neglected. The leakage inductance of CI is considered.
4) The input voltage is considered constant.

Independent state variables of the proposed converter are $x^T = [i_{Lm1},\ i_{Lm2},\ v_{Cm},\ v_{Co1},\ v_{Co2}]$. State equations are obtained for four modes (mode 1, mode 3, mode 4, and mode 6) of operation in previous Section II. The transient modes (mode 2 and mode 5) are not considered. Average current through each diode to derive state-space model is expressed as follows.

The average current through output diode D_{o1} and D_{o2} are

$$i_{Do1} = i_{Do2} = (1-d)i_{Lm}. \tag{30}$$

The average current through the multiplier diode D_m is

$$i_{Dm} = \frac{(nv_{\text{in}} - v_{cm})d^2T_s}{2L_{lk}}. \tag{31}$$

The average current through the output diode D_{o3} is

$$i_{Do3} = \frac{(2nv_{\text{in}} - v_{co2})d^2T_s}{2L_{lk}}. \tag{32}$$

The average large-signal model of the converter is derived by taking the average of all four interval state-space equations (1)–(13) and (30)–(32). It is expressed as follows.

State equation:

$$\dot{x} = Ax + Bu \tag{33}$$

where A is expressed in (34) and B is expressed in (35).

$$\begin{bmatrix} 0 & 0 & 0 & -\frac{1-d}{L_{m1}} & 0 \\ 0 & 0 & 0 & -\frac{1-d}{L_{m2}} & 0 \\ 0 & 0 & 0 & 0 & -\frac{d^2T_s}{2L_kC_m} \\ \frac{(1-d)}{C_{o1}} & \frac{(1-d)}{C_{o1}} & 0 & -\frac{1}{R_oC_{o1}} & -\frac{1}{R_oC_{o1}} \\ 0 & 0 & 0 & -\frac{1}{R_oC_{o2}} & -\frac{1}{R_oC_{o2}} - \frac{d^2T_s}{2L_kC_{o2}} \end{bmatrix} \tag{34}$$

$$\begin{bmatrix} \frac{1}{L_{m1}} & \frac{1}{L_{m2}} & \frac{nd^2T_s}{L_kC_m} & 0 & \frac{nd^2T_s}{L_kC_{o2}} \end{bmatrix}^T. \tag{35}$$

Output equation:

$$y = Cx \tag{36}$$

where C is expressed in the following:

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 1 \end{bmatrix}. \tag{37}$$

A. Steady-State Model

At equilibrium point, the deviation of state variable is zero and state variables and other variables represent the steady-state value. The steady-state model is obtained from (33) and (36). Substitute $\dot{i_{Lm1}} = \dot{i_{Lm2}} = \dot{v_{Cm}} = \dot{v_{Cmo1}} = \dot{v_{Co2}} = 0$, and substitute $i_{Lm1} = I_{Lm1}$, $i_{Lm2} = I_{Lm2}$, $v_{Cm} = V_{Cm}$, $v_{Co1} = V_{Co1}$, $v_{Co1} = V_{Co1}$, $v_{\text{in}} = V_{\text{in}}$, and $d = D$ in (33) and (36) to derive steady-state model. The steady-state voltage of output capacitor C_{o1} is derived from the steady-state model of the converter and expressed as follows:

$$\frac{V_{Co1}}{V_{\text{in}}} = \frac{1}{1-D}. \tag{38}$$

The steady-state voltage of output capacitor C_{o2} is derived from the steady-state model of the converter and expressed as follows:

$$\frac{V_{Co2}}{V_{\text{in}}} = \frac{2(nD^2T_s(1-D)R_o - L_{lk})}{(2L_k + D^2T_sR_o)(1-D)}. \tag{39}$$

The output voltage of the proposed converter is

$$\frac{V_o}{V_{\text{in}}} = \frac{V_{Co1} + V_{Co2}}{V_{\text{in}}}. \tag{40}$$

Substitute (38) and (39) into (40), the steady-state voltage gain (V_o/V_{in}) of the proposed converter is expressed as follows:

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} + \frac{2(nD^2T_s(1-D)R_o - L_k)}{(2L_k + D^2T_sR_o)(1-D)}. \tag{41}$$

In (41), the voltage gain of the converter is affected by leakage inductance, load resistance, and switching frequency. As the leakage inductance value of CI increases, the voltage gain of the proposed converter decreases, as shown in Fig. 6. If the k is one, the voltage gain of the converter is the same as expressed in (26).

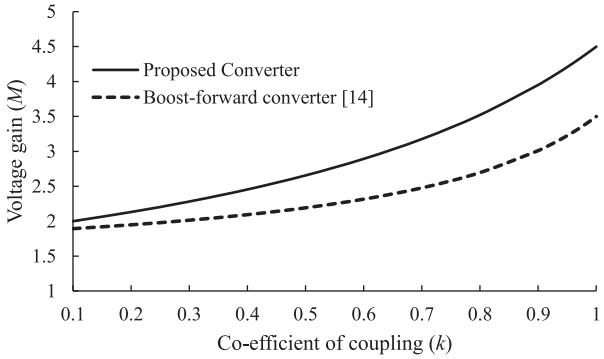

Fig. 6. Effect of co-efficient coupling (k) on voltage gain (M) of the proposed converter and boost-forward converter.

B. Small-Signal Model and Transfer Function

Applied perturbation to state variables and input signal in a large-signal model (33)–(36) at a steady-state operating point and then by comparing steady-state and small-signal quantity, the linearized small-signal model of the proposed converter is derived.

As symmetry structure of the proposed converter, the following condition is hold: $i_{Lm1} = i_{Lm2} = i_{\text{in}}/2$, and the original fifth order of the converter reduces to a fourth order [33], [34]. By considering input current i_{in} as state variable in place of i_{Lm1} and i_{Lm2} due to symmetry structure of the proposed converter, the small-signal model of the proposed converter is expressed as follows:

State equation:

$$\hat{\dot{x}} = A\hat{x} + B_1\hat{d} + B_2\hat{v_{\text{in}}} \tag{42}$$

where A is expressed in (43), B_1 and B_2 are expressed in (44)

$$\begin{bmatrix} 0 & 0 & -\frac{2(1-D)}{L_{m1}} & 0 \\ 0 & 0 & 0 & -\frac{d^2T_s}{2L_kC_m} \\ \frac{(1-D)}{C_{o1}} & 0 & -\frac{1}{R_oC_{o1}} & -\frac{1}{R_oC_{o1}} \\ 0 & 0 & -\frac{1}{R_oC_{o2}} & -\frac{1}{R_oC_{o2}} - \frac{D^2T_s}{2L_kC_{o2}} \end{bmatrix} \tag{43}$$

$$B_1 = \begin{bmatrix} \frac{2V_{co1}}{L_{m1}} \\ \frac{(2nV_{\text{in}} - V_{co2})DT_s}{L_kC_m} \\ -\frac{I_{Lm1} + I_{Lm2}}{C_{o1}} \\ \frac{(2nV_{\text{in}} - V_{co2})DT_s}{L_kC_{o2}} \end{bmatrix}, B_2 = \begin{bmatrix} \frac{2}{L_{m1}} \\ \frac{nD^2T_s}{L_kC_m} \\ 0 \\ \frac{nD^2T_s}{L_kC_{o2}} \end{bmatrix}. \tag{44}$$

Output equation: $\hat{y} = C\hat{x}$

$$\hat{v_o} = \hat{v_{c_{o1}}} + \hat{v_{c_{o2}}}. \tag{45}$$

The control-to-output voltage small-signal transfer function is derived from a small-signal model in (42) and (45) by considering input voltage is constant. The control-to-output voltage

small-signal transfer function is expressed as follows:

$$\frac{\hat{v_o}(s)}{\hat{d}(s)} = C(SI - A)^{-1}B_1$$

$$\frac{\hat{v_o}(s)}{\hat{d}(s)} = \frac{b_2 s^2 + b_1 s^1 + b_0}{a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{46}$$

where $b_2 = \dfrac{(2nV_{\text{in}} - V_{co2})DT_s}{L_k C_{o2}} - \dfrac{I_{Lm1} + I_{Lm2}}{C_{o1}}$

$$b_1 = \frac{2V_{co1}(1-D)}{C_{o1}L_m} - \frac{D^2 T_s (I_{Lm1} + I_{Lm2})}{2L_k C_{o1} C_{o2}}$$

$$b_0 = \frac{2V_{co1}(1-D)D^2T_s}{2L_m L_k C_{o1} C_{o2}} + \frac{2(2nV_{\text{in}} - V_{co2})(1-D)^2 DT_s}{L_m L_k C_{o1} C_{o2}}$$

$$a_3 = 1$$

$$a_2 = \frac{1}{R_o C_{o1}} + \frac{1}{R_o C_{o2}} + \frac{D^2 T_s}{2L_k C_{o2}}$$

$$a_1 = \frac{2(1-D)^2}{L_m C_{o1}} + \frac{D^2 T_s}{2R_o L_k C_{o1} C_{o2}}$$

$$a_0 = \frac{(1-D)^2}{L_m C_{o1}} \left(\frac{1}{R_o C_{o2}} + \frac{D^2 T_s}{2L_k C_{o2}} \right).$$

Equation (46) shows control-to-output voltage transfer function of the proposed converter. It can be seen that converter has two zeros. It can be seen in (46) that the transfer function has all coefficient of denominators are positive so all poles are on LHP of s plane. To make system stable and for minimum-phase characteristic, according to Routh–Hurtwitz criteria coefficient b_2, b_1 and b_0 of transfer function should be have same sign. The coefficient b_0 is positive so sign of all the coefficient should be positive. In order to eliminate RHP zero from the proposed converter, the following condition should be satisfied to make all coefficient positive:

$$\frac{C_{o1}}{C_{o2}} > \frac{(I_{Lm1} + I_{Lm2})L_k}{(2nV_{\text{in}} - V_{co2})DT_s} \tag{47}$$

$$C_{o2} > \frac{(I_{Lm1} + I_{Lm2})L_m D^2 T_s}{4nV_{\text{in}} L_k}. \tag{48}$$

The output capacitors of the proposed converter should be selected according to (47) and (48), which results in initially rise in V_{co2} compensates the initial dip in V_{co1}. It is equivalent to eliminating RHP zero from the control-to-output voltage transfer function. The operating range of the converter for which no RHP zero is derived from (48). As the input current is evenly shared in each phase, the operating range can be expressed in terms of coefficient of coupling (k) as follows:

$$D_{\text{proposed}} < \sqrt{\frac{4nV_{\text{in}} C_{o2}(1-k)}{kI_{\text{in}} T_s}}. \tag{49}$$

The operating range of the boost-forward converter for which no RHP zero is expressed as follows [14]:

$$D_{\text{boost-forward}} < \sqrt{\frac{2nV_{\text{in}} C_{o2}(1-k)}{kI_{\text{in}} T_s}}. \tag{50}$$

Taking ratio of (49) and (50), the following expression is derived:

$$\frac{D_{\text{proposed}}}{D_{\text{boost-forward}}} = \sqrt{2}. \tag{51}$$

TABLE I
SPECIFICATIONS AND COMPONENTS OF THE PROPOSED CONVERTER AND BOOST-FORWARD CONVERTER

Components / Parameters	Symbol	Values / Device Number
Input Voltage	V_{in}	24 V
Output Voltage	V_o	100 V (n = 1)
Output Power	P_o	200 W
Switching Frequency	f_{sw}	50 kHz
Proposed converter		
MOSFET Switches	S	IPP051N15N5 (150 V, 120 A, 5.1 $m\Omega$)
Diode	$D_{o1} - D_{o3}$,D_m	MBRD10100CT
Output Capacitor	C_{o1}	100 μF, 100 V Electrolytic Capacitor
Output Capacitor	C_{o2}	50 μF, 160 V Electrolytic Capacitor
Multiplier Capacitor	C_m	25 μF, 160 V Film Capacitor
Magnetising and Leakage Inductance of CI	L_m L_k	243 μH 7 μH
Turns Ratio ($N_2 : N_1$)	n	39:39 (n = 1)
Core Material of CI		Sendust Toroid Core KS130-125A
Boost-forward converter		
MOSFET Switches	S	IPP110N20NA (200 V, 88 A, 9.9 $m\Omega$)
Output Diode	$D_{o1} - D_{o2}$	MBRD10200CT
Output Capacitor	C_{o1}	100 μF, 160 V Electrolytic Capacitor
Output Capacitor	C_{o2}	2 x 25 μF, 250 V Film Capacitor
Magnetising and Leakage Inductance of CI	L_m L_k	486 μH 14 μH
Turns Ratio ($N_2 : N_1$)	n	53:53 (n = 1)
Core Material of CI		Sendust Toroid Core KS157-125A

It can be seen in (51) that the operating range of the proposed converter to eliminate RHP zero is more than boost-forward converter with same of k. Thus, the proposed converter has better dynamic response for a wide range of duty cycle than boost-forward converter. In the case of $k = 0.972$, elimination of RHP zero is possible in the proposed converter for duty cycle less than 0.911 and in the boost-forward for duty cycle less than 0.6441 for specification and parameters given in Table I. To operate converter for wide operating range to eliminate RHP zero require to decrease the value of co-efficient of coupling k in the proposed and boost-forward converter. As the k decreases, the gain of the converter is also decreased. However, the proposed converter has more gain for same value of k, as shown in Fig. 6. Hence, the proposed converter can operate for wide operating range to eliminate RHP zero compared with boost-forward converter for the same value of k.

The control-to-output voltage transfer function of the proposed converter has no RHP zero with coefficient of coupling near to one for wide operating range. Thus, the converter has more BW and internal stability for wide operating range. This makes design of closed-loop control circuit simple and easy to implement. It is possible to obtain desired dynamic response of the proposed converter using single-loop voltage control.

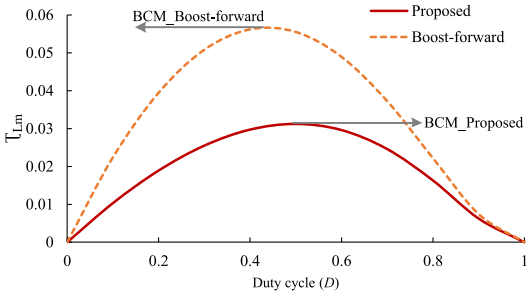

Fig. 7. Curve of normalized magnetizing inductance time constant τ_{Lm} versus duty cycle D of the proposed converter and boost-forward converter [14].

C. Small-Signal Model Analysis and Controller Design

The frequency response has been obtained of derived small-signal control to output voltage transfer function of the proposed converter in MATLAB for performance analysis. The analysis has been done using the parameters given in Table I. The boundary condition for the normalized magnetizing inductance time constant, τ_{Lm} is expressed as

$$\tau_{Lm} = \frac{L_m f_{sw}}{R} = \frac{D(1-D)^2}{(1+2n-2nD)^2}. \tag{52}$$

Fig. 7 shows the curve of τ_{Lm} versus D. The proposed converter is operated in CCM when τ_{Lm} is higher than the boundary value τ_{LmB}. It can be seen in Fig. 7 that the proposed converter required the low value of magnetizing inductance of CI for operation in CCM compared with the boost-forward converter. It reduces the size of magnetic core and number of turns, hence reduces core and winding losses. The proposed converter can work in CCM for wide range of load changes compared with the boost-forward converter for the same value of magnetizing inductance of CI and frequency. The magnetizing inductance of the CI is designed according to (52). To assure the CCM operation of this converter, the minimum value of the magnetizing inductance of CI is expressed as

$$L_{m_{\min}} = \frac{R_{o_{\max}} D(1-D)^2}{f_{sw}(1+2n-2nD)^2}. \tag{53}$$

According to (53), the minimum value of magnetizing inductance is 125 μH to assure CCM operation for a minimum load of 50 W. The CI of each phase of the converter is implemented with 250 μH to limit ripple of input current less than 50% at full load. The coefficient of coupling of CI of this converter is designed for 0.972. The value of L_m and L_k of CI are given in Table I. To eliminate RHP zero from control to output voltage transfer function of the proposed converter, output capacitors (C_{o1} and C_{o2}) are selected according to the condition derived in (47) and (48). C_{o2} should be greater than 40 μF and the ratio C_{o1}/C_{o2} should be greater than 2.24 to eliminate RHP zero. To satisfy the condition and to achieve small ripple in output voltage, C_{o1} and C_{o2} are selected as 100 and 50 μF, respectively. The converter has wide operating range up to 0.911 to operate without RHP zero with co-efficient coupling $k = 0.972$. It is derived using (49) for the specification and parameters given in Table I.

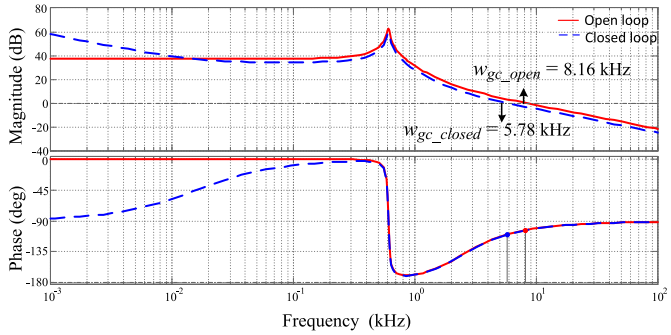

Fig. 8. Control-to-output voltage transfer function frequency response of the proposed converter in open-loop and closed-loop controls.

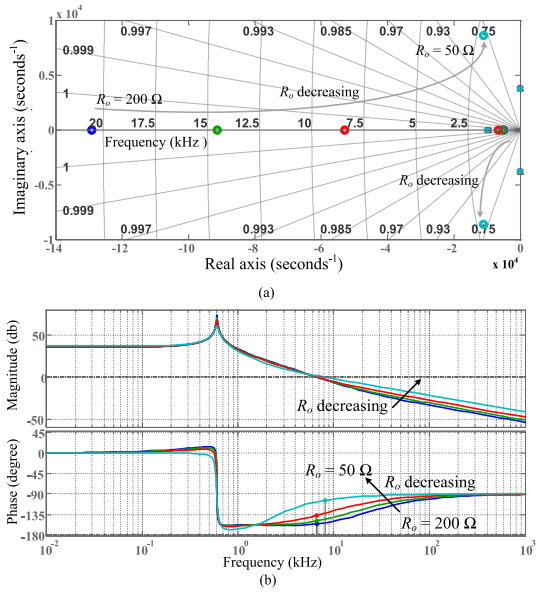

Fig. 9. Effect of different load resistance (50–200 Ω) on open-loop control-to-output voltage transfer function of the proposed converter: (a) pole-zero plot and (b) frequency response.

1) Small-Signal Model Analysis: In this section, frequency response are obtained from derived small-signal model of the proposed converter for the performance comparison. The control-to-output voltage transfer function of the proposed converter is obtained as follows:

$$G_{vd\_\text{open}}(s) = \frac{50\,786(s^2 + 2.25\times10^4 s + 1.98\times10^8)}{(s+10\,020)(s^2+192.9s+1.46\times10^7)}. \tag{54}$$

The control to output voltage transfer function of the proposed converter in (54) has no RHP zero. The open-loop frequency response of the proposed converter is shown in Fig. 8. The phase margin (PM) of the converter is 75.9° at crossover frequency 8.16 kHz and gain margin (GM) is infinity. The BW of the converter is 11.6 kHz in open-loop control. Fig. 9(a) and (b) shows the pole-zero maps and bode plot of the proposed converter using control-to-output voltage transfer function given in (46) for different load resistances from 50 to 200 Ω. It is observed in Fig. 9(a) that two zeros are located on LHP of s-plane as criteria of (47) and (48) are satisfied for different

load condition. As load increased, high-frequency zero moves further to low frequency while low-frequency zero moves toward high frequency. It can be seen in Fig. 9(b) that as load increased, the crossover frequency, BW, and PM are increased. In Fig. 9(a), the damping ratio of the converter is decreased with increased in load, thus settling time of converter is decreased with increased in load. There is no major effect of load resistance on the pole of transfer function.

2) Single-Loop Voltage Control With PI Controller Design: As the proposed converter has positive PM and GM, the single-loop voltage control with PI controller is implemented to regulate output voltage and to further improve the dynamic response under a load disturbance. The PI controller transfer function can be expressed as follows:

$$G_c(s) = k_p \frac{(Ts+1)}{Ts}. \tag{55}$$

The parameters of transfer function of the PI controller for closed-loop control of the proposed converter is obtained by using root locus pole placement technique in MATLAB. The proportional constant k_p is 69 and integral time constant T is 0.01, which are considered to make steady-state error near to 2% of output voltage with faster response. Loop transfer function of the proposed converter for closed-loop control is $G_{vd\_\text{loop}}(s) = G_{\text{pwm}}G_{vd\_\text{open}}(s)G_c(s)H(s)$, where $G_{vd\_\text{open}}(s)$ = open-loop transfer function of the proposed converter expressed in (54), $G_c(s)$ is PI controller transfer function, $G_{\text{pwm}}(s)$ = transfer function of PWM = $1/V_{\text{peak}}$ = 1/3.3, where V_{peak} is saw-tooth waveform's peak-to-peak voltage, and $H(s)$ = feedback transfer function of voltage sensor = 3.3/100. The loop transfer function $G_{vd\_\text{loop}}(s)$ for single-loop voltage control of the proposed converter is expressed as follows:

$$G_{vd\_\text{loop}}(s) = \frac{35042(s+100)(s^2+2.2\times10^4 s+1.97\times10^8)}{s(s+10020)(s^2+192.9s+1.45\times10^7)}. \tag{56}$$

Fig. 8 shows closed-loop frequency response of the proposed converter at full load. In closed-loop control, crossover frequency is 5.78 kHz, the converter achieved PM of 69.9°, and BW of converter is 8.16 kHz. Thus, closed-loop control of the converter achieved stable operation and faster dynamic response using single-loop control.

It can be seen that the proposed converter has high BW and good range of stability margin for wide range of control due to elimination of RHP zero. Hence, it is easy and simple to implement closed-loop control of the proposed converter using single-loop voltage control. It is possible to achieve regulated output voltage with faster response for wide range of control when the proposed converter is part of RES.

V. Simulation Results Analysis and Performance Comparison

In this section, the proposed converter is compared with boost converter and the other similar minimum-phase converters in terms of steady state and dynamic performance parameters. The analytical results are verified by the simulation results of the proposed converter using PSIM software. The simulation of the proposed converter, boost converter, and boost-forward converter is carried out for parameters given in Table I.

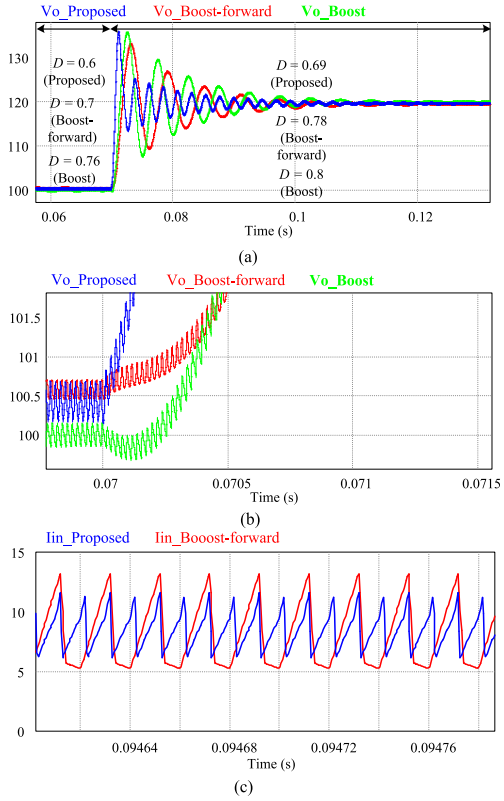

Fig. 10. Simulation results of the proposed converter, boost converter, and boost-forward converter. (a) Output voltage waveform when step changed in duty cycle. (b) Enlarged view of output voltage when step changed in duty cycle. (c) Input current waveform of the proposed converter and boost-forward converter at full load.

A. Simulation Results Analysis

In this section, the simulation waveform of the output voltage of the proposed converter, boost converter, and boost-forward converter are compared when step change in duty cycle. Fig. 10(a) shows the output voltage response of the proposed converter and compared converters. It can be seen in Fig. 10(a) that the proposed converter is operated with low duty cycle in comparison to compared converter to achieve an output voltage of 100 V. The proposed converter achieved rated output voltage of 100 V at $D = 0.6$ while boost converter at $D = 0.76$ and boost-forward converter at $D = 0.7$. It can be seen in Fig. 10(b) that the boost converter has negative voltage dip when step changed in duty cycle. It is due to the presence of RHP zero in its control to output voltage transfer function. The proposed converter and boost-forward converter have no negative voltage dip when step changed in duty cycle as the absence of RHP zero in control to output voltage transfer function. It can be seen in Fig. 10(a) that the proposed converter is reached to steady-state value faster than boost-forward converter. The ripple in input current is 50% in the proposed converter and 67% in boost-forward converter. Fig. 10(c) shows that the ripple in input current is reduced in the proposed converter compared with boost-forward converter.

TABLE II
FREQUENCY RESPONSE SPECIFICATION COMPARISON OF THE PROPOSED CONVERTER WITH BOOST AND BOOST-FORWARD CONVERTERS

Topology	Gain Crossover Frequency, w_{gc}	Phase Crossover Frequency, w_{pc}	Bandwidth	Phase Margin (degree)	Gain Margin (dB)	Stability
Proposed Converter	9 kHz	61 kHz	11.54 kHz	58	infinity	Stable
Boost Converter	5.93 kHz	0.4 kHz	-	-61	-39	Unstable
Boost-forward Converter (k = 0.972)	8.79 kHz	0.4 kHz	-	-132	-32	Unstable
Boost-forward Converter (k = 0.95)	8 kHz	27.5 kHz	10 kHz	33	6	Stable
Proposed Converter (closed loop control)	4.61 kHz	48 kHz	6.4 kHz	70	9.2	Stable

To reduce the ripple 50% in input current of boost-forward converter, the CI needs to design with high value magnetizing inductance L_m of 675 μH and $k = 0.944$. To achieve same voltage gain and ripple in input current, boost-forward converter needs to operate at $D = 0.72$. The output capacitor $C_{o1} =$ 100 μF and $C_{o2}=$ 75 μF of boost-forward converter should be considered to eliminate RHP zero condition accordingly, given in [14], and low value of ripple. As interleaved structure at input side of the proposed converter, it is designed with low value of magnetizing inductance of CI compared with the boost-forward converter for the same value voltage gain and ripple in input current. Hence, the proposed converter reduces the size of core, number of turns, and reduces related losses hence higher power density than boost-forward converter.

B. Frequency Response Analysis

In this section, the performance of the proposed converter is compared with boost and boost-forward converters in terms of stability margin and BW using bode plot. The open-loop frequency response of the proposed, boost, and boost-forward converters are obtained in PSIM software for the parameters given in Table I. It can be seen in Fig. 11(a) that boost converter is unstable as PM and GM both are negative. It can be seen in Fig. 11(b) that the boost-forward converter has negative PM and GM for coefficient of coupling 0.972. Boost-forward converter is operated without RHP zero for operating range below 0.644 for k = 0.972. It can be seen in Fig. 10(a), to achieve an output voltage of 100 V from 24 V, boost-forward is operated at $D = 0.7$, hence boost-forward has negative PM in frequency response. To eliminate RHP zero for wide operating range, boost-forward converter should be designed with further low value of coefficient coupling. If $k = 0.95$ is considered in (50), boost-forward converter can eliminate RHP zero at $D = 0.7$. In Fig. 11(c), boost-forward converter has positive PM and GM for $k = 0.95$. In Fig. 11(d), frequency response of the proposed converter has positive PM and GM for $k = 0.972$. Thus, the proposed converter is operated with a higher value of k than boost-forward converter for the same conditions. The proposed converter has no RHP zero in control-to-output voltage transfer function so it is simple and easy to design closed-loop control using single-loop control to regulate output voltage and to achieve designed dynamic response under a load disturbance. The closed-loop frequency response of the proposed converter is shown in Fig. 12. In the closed-loop control of the proposed converter, the parameters of PI controller is designed such that the converter achieved BW of 6.4 kHz and PM of 70° at 4.8 kHz. High BW reduced settling time. The performance comparison of the proposed converter in

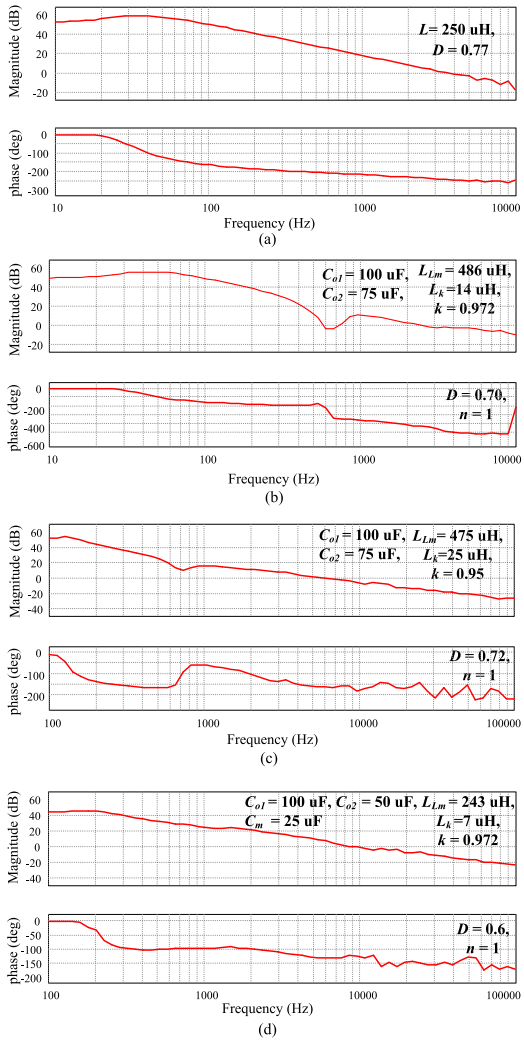

Fig. 11. Control-to-output voltage frequency response of the proposed converter and boost-forward converter. (a) Boost converter. (b) Boost-forward converter when coefficient of coupling (k) = 0.972. (c) Boost-forward converter when $k = 0.95$. (d) Proposed converter when $k = 0.972$.

TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH SIMILAR HIGH STEP-UP VOLTAGE GAIN DC–DC CONVERTER

High Step-Up Gain Topologies	Proposed Topology	Boost Converter	Boost-Forward Converter [14]	BCMCF [11]	Interleaved Tristate Boost Converter [26]	Second Order KY Converter [29]	Diode-Capacitor Converter [31]	TOBC [32]
Voltage Gain	$\frac{1}{1-D}+2n$	$\frac{1}{1-D}$	$\frac{1}{1-D}+n$	$\frac{1}{1-D}$	$\frac{D_b+D_o}{D_o}$	$1+2D$	$\frac{1+D}{1-D}$	$\frac{2-D}{1-D}$
Voltage Stress on Switch	$\frac{V_o}{1+2n-2nD}$	V_o	$\frac{V_o}{1+n-nD}$	V_o	V_o	$\frac{V_o}{1+2D}$	$\frac{V_o}{1+D}$	$\frac{V_o}{2-D}$
Maximum Voltage Stress on Diode	$\frac{nV_o}{1+2n-2nD}$	V_o	$\frac{nV_o}{1+n-nD}$	V_o	V_o	$\frac{V_o}{1+D}$	$\frac{2V_o}{1+D}$	$\frac{V_o}{2-D}$
Switch / Diode	2 / 4	1 / 1	1 / 2	1 / 1	4 / 4	4 / 2	1 / 2	1 / 2
Magnetic Core	2	1	1	1	2	1	2	1
Capacitors	3	1	2	2	1	3	5	2
Damping Resistor	-	-	-	-	-	-	2	-
Ripple in Input Current	Low	High	High	High	Low	Low	High	High
Non-minimum / Minimum Phase	Minimum	Non-minimum	Minimum	Minimum	Minimum	Minimum	Minimum	Minimum

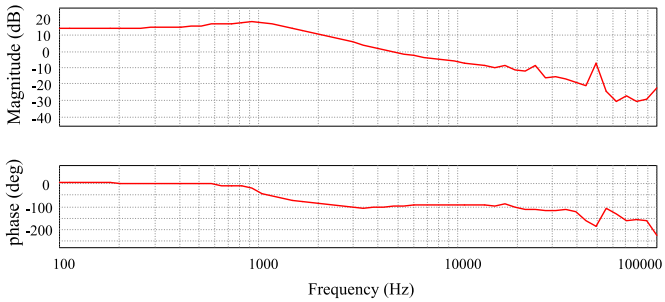

Fig. 12. Closed-loop frequency response of the proposed converter.

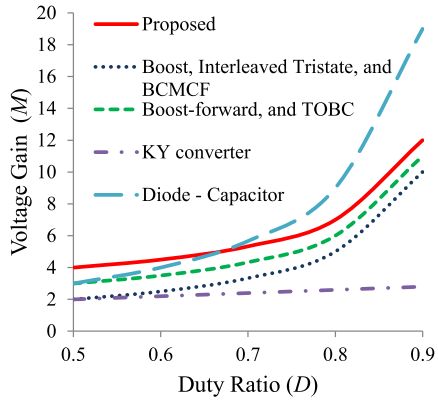

Fig. 13. Comparison curve of voltage gain versus duty cycle.

the terms of stability margin and BW is listed in Table II. It can be seen that the proposed converter has positive PM and higher BW than boost converter and boost-forward converter with $k = 0.95$. It can be seen that the proposed converter has crossover frequency more than boost-forward converter, hence higher BW for same value of k.

C. Performance Comparisons

A complete comparison between the proposed converter, and boost converter, boost-forward converter, BCMCF, two-phase interleaved tristate boost, KY converter, diode–capacitor-based boost converter, and TOBC is given in Table III. Comparison is done in terms of voltage gain, number of components, voltage stress on switching devices, ripple in input current, and minimum/nonminimum-phase characteristic. All topologies are used in high step-up gain application. The all compared typologies have minimum-phase characteristic except boost converter.

Fig. 13 shows that the proposed converter has high voltage gain in comparison to all compared topologies, and compared with diode-capacitor topology, it has higher gain for duty cycle $0 < D < 0.7$. Diode–capacitor-based boost converter has higher gain for duty cycle more than 0.7. However, it has used R–C damping network to locate zero from RHP to LHP. The proposed converter can achieve more gain than diode-capacitor for all duty cycle if designed for $n > 1$, as shown in Fig. 5(b). The proposed converter has low component count than diode–capacitor-based boost converter. The proposed converter can achieve high gain with low duty ratio in comparison to all compared converter. The voltage stress on switch in the proposed converter is less than in comparison to all compared converter. The maximum voltage stress on diode in the proposed converter is lower than boost, boost-forward, interleaved tristate boost, BCMCF, diode-capacitors converter, and TOBC. KY converter has minimum voltage stress on diode, but it has gain limited 2 with maximum number of components, as given in Table III. The proposed converter has better dynamic response in comparison to boost converter as it has minimum-phase characteristic. Tristate boost converter is independent of value of leakage inductance to remove RHP zero. However, it has voltage gain same as boost converter and complex switching control. Although the proposed converter has more components count than boost-forward, BCMCF, and TOBC, it has wide operating range to operate without RHP zero for the same value of coefficient of coupling k and low ripple in input current with low value of CI. Thus, in the proposed converter, there is reduction in the size of magnetic core, number of turns, and core and winding losses. Due to

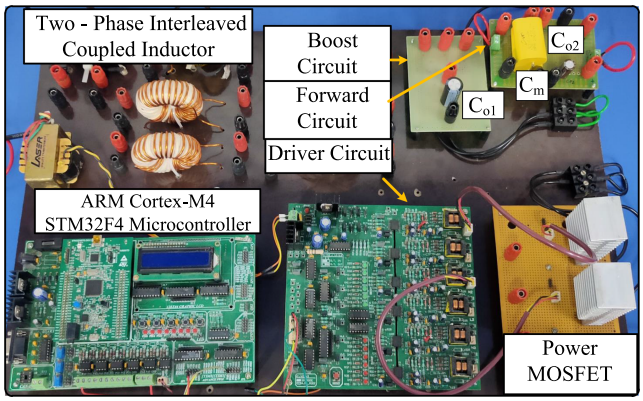

Fig. 14. Photograph of the hardware setup of the proposed converter.

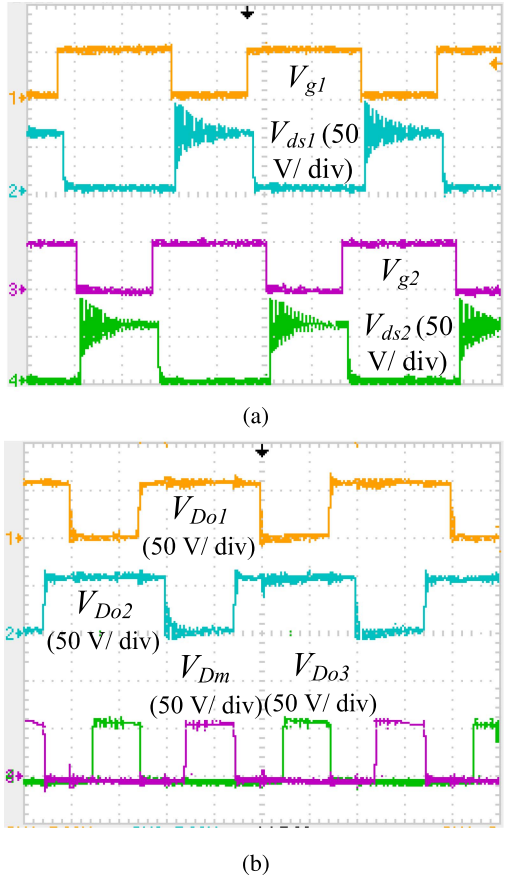

Fig. 15. Experiment results waveforms at full load. (a) Gate signal (V_{gs1}, V_{gs2}) and switch voltage (V_{ds1}, V_{ds2}). (b) Output diode voltages ($V_{Do1}, V_{Do2}, V_{Do3}$) and multiplier diode voltage (V_{Dm}).

interleaved operation at input side, the ripple in input current of the proposed converter is reduced, thus the current stress and related losses in MOSFET are reduced. In addition, low voltage and current stress on semiconductor devices allows the proposed converter to implement using low rating and high-performance semiconductor devices. Altogether, the proposed high step-up voltage gain converter can operate efficiently with faster dynamic response for a load disturbance, which makes it most suitable choice for high step-up gain and high-power conversion applications.

VI. Experimental Results

A prototype of the proposed converter with 200-W, 24-V input, and 100 V output is built in laboratory and tested to verify derived steady state and small-signal model results of the converter. The specification and components of the proposed converter are given in Table I. The converter was designed for a switching frequency of 50 kHz with an aim of experimental verification of theoretical finding. Similar to any other dc–dc converter configuration, this topology can also be designed at very high frequency. Fig. 14 shows the hardware setup picture of the prototype of the proposed converter. The experimental results are observed and measured under CCM.

The proposed converter is operated with duty cycle 0.6 in open loop to achieve 100-V output voltage from input voltage 24 V at full load 200 W. Fig. 15(a) and (b)shows gate signal voltage, voltage across both switch, and all diode at full load. Fig. 15(a) shows that steady-state blocking voltage across both the switch is 56 V. The transient voltage across the switch is 80 V due to stray inductance of long wires when the switch was OFF. Preparing a dedicated PCB with proper layout can simplify the circuit layout and the effect of stray inductance on switch can be reduced. Voltage across output diodes (D_{o1}, D_{o2}) is 59.58 V and multiplier (D_m) and output diode (D_{o3}) is 55.71 V, as shown in Fig. 15(b). Fig. 16(a) shows input current and phase current waveform at full load. The ripple of input current is 49% at 200 W. Input current is evenly shared in each phase. Fig. 16(b) shows current through multiplier diode (i_{Dm}) and all output diode (i_{Do1}, i_{Do2}, and i_{Do3}). Fig. 17 shows waveforms of input current at different duty cycle. When $D = 0.4$, input current has ripple of 57%, as shown in Fig. 17(a). When $D = 0.5$, input current has ripple of 57.28%, as shown in Fig. 17(b). When $D = 0.7$, input current has ripple of 37.78%, as shown in Fig. 17(c). It is observed that ripple in input current was decreased with increased duty cycle.

Fig. 18 shows the transient response of the open-loop control of the proposed converter for a step change in the duty cycle from 0.6 to 0.69. At the instant of step changed, an initial negative voltage dip is observed in voltage of output capacitor C_{o1}, (V_{co1}) while voltage of output capacitor C_{o2} (V_{co2}) and multiplier capacitor (V_{cm}) initially rises in voltage. Thus, the resultant output voltage has no voltage dip as it is cancelled out by output capacitor C_{o2} and output voltage reached to a steady-state value in 6 ms.

Fig. 19 shows the open-loop dynamic response of output voltage of the converter when step changed in load from half to full. The output voltage has no negative voltage dip and converter reached to steady-state value in 7.5 ms.

Fig. 20 shows the experimental open-loop frequency response of the proposed converter and boost-forward converter in CCM for same value of coefficient of coupling $k = 0.972$. The input of the sweeps is the converter duty cycle (d) and the output is the output voltage (v_o). A dc value of duty cycle (D) and a small ac sine wave ($\hat{d}\sin\ w\ t$) with amplitude of 5% of the

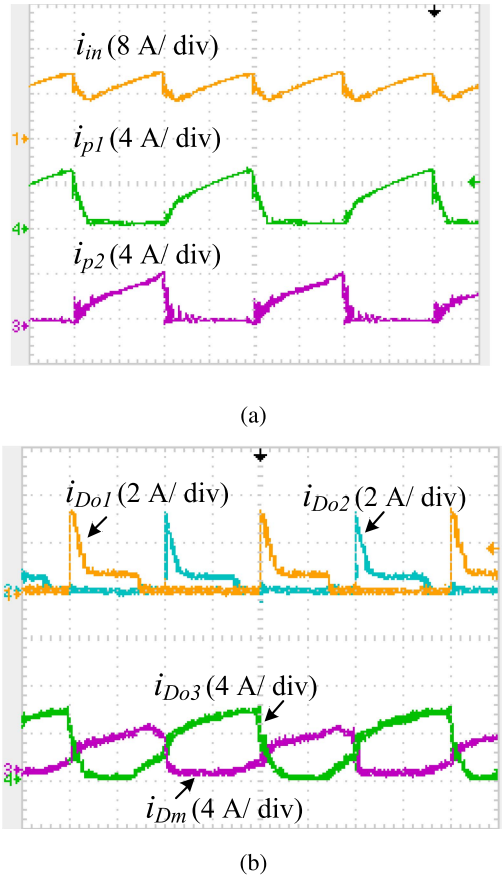

Fig. 16. Experimental results of current at full load. (a) Input current (i_{in}) and phase current (i_{p1}, i_{p2}). (b) Output diode currents ($i_{Do1}, i_{Do2}, i_{Do3}$) and multiplier diode current (i_{Dm}).

dc value to act as the small-signal perturbation is injected into the converter as input. The resulting sine wave magnitude and phase of output voltage was compared with that of the input duty cycle perturbation for frequency sweeps from 100 Hz to 15 kHz. The reading was observed up to frequency 15 kHz due to resolution error. It can be seen that frequency response of the proposed converter has PM of 55° at gain crossover frequency 8.5 kHz. The open-loop BW of the proposed converter is 14 kHz. It was observed that the proposed converter has positive stability margin and high BW, hence verified the derived small signal model result of the proposed converter in Sections IV and V. The frequency response of the boost-forward converter has PM of $-45°$, hence system has unstable operation for $k = 0.972$.

The closed-loop dynamic response of the output voltage of the proposed converter for a step-change in load from 100 to 200 W and 200 to 100 W. The output voltage was regulated to 100 V when the step changed in load using single-loop voltage control with PI controller. The ARM Cortex-M4 STM32F4 microcontroller received actual output voltage from voltage sensor. The actual and reference output voltage is compared and the generated error is compensated using a PI controller. Digital PI controller is programmed in microcontroller. The output of PI controller is compared with carrier signal and generate pulse to achieve regulated output voltage. Fig. 21 shows the frequency response of closed-loop control of the proposed converter. The gain crossover frequency of the 5.2 kHz and closed-loop BW of the proposed converter is 7.5 kHz.

It can be seen in Fig. 22 that the output voltage of the proposed converter had an initially negative 5 V voltage dip at the instant of load changed from half to full, and an initial rise in the output voltage of 6 V at the instant of load changed from full to half. In both cases, the output voltage settled to the stable output voltage of 100 V in 2.5 ms.

The calculated efficiency and losses of the proposed and boost-forward topologies at full load are given Table IV for same volume of core and implementation cost. The efficiency and losses of the both converters are calculated for specification, as given in Table I, and parasitic parameters are given in Table V. The cost and volume of core of both converters are given in Table IV. The proposed topology is operated with $D = 0.6$, whereas boost-forward converter is operated with $D = 0.7$ for same voltage gain so higher rating of POWER MOSFET was implemented in boost-forward converter. The cost of semiconductor devices and capacitor is taken from mouser website. The volume of the core is taken from the datasheet. The proposed converter has lower losses and higher efficiency compared with the boost-forward converter. The loss breakdown of the proposed converter and boost-forward converter is shown in Fig. 23. It includes losses in primary and secondary windings of CI, core loss, switching and conduction losses in switch, conduction

TABLE IV
EFFICIENCY AND LOSSES OF THE PROPOSED CONVERTER AND BOOST-FORWARD CONVERTER AT FULL LOAD AT SAME VALUE OF $K = 0.972$

Topology	Proposed converter	Boost-forward converter
Winding loss of CI	1.25 W	2.26 W
Core loss of CI	2.72 W	10 W
Conduction loss of MOSFET	0.19 W	0.50 W
Switching loss of MOSFET	0.40 W	0.38 W
Conduction loss of diode	3.8 W	3.4 W
Conduction loss of capacitor	0.43 W	1.55 W
Total losses	8.79 W	18.9 W
Calculated efficiency	95.80 %	91.70 %
Volume of the core of CI	10.9 cm^3	10.6 cm^3
Implementation cost	31.11 $	34.5 $

TABLE V
PARAMETERS VALUE OF THE PROPOSED CONVERTER AND BOOST-FORWARD CONVERTER

Topology	Proposed converter	Boost-forward converter
Drain-source on-state resistance ($R_{ds(on)}$)	5.1mΩ	9.9 mΩ
Primary winding resistance of CI (R_p)	22.7 mΩ	23.8 mΩ
Secondary winding resistance of CI (R_s)	44 mΩ	75 mΩ
ESR of C_{o1}	84 mΩ	168 mΩ
ESR of C_{o2}	50 mΩ	2.2 mΩ
ESR of C_m	4.4 mΩ	-
Diode forward voltage (V_{FD})	0.72 V	0.85 V
Fall time of MOSFET (t_f)	4.9 ns	11.1 ns
Output Capacitance of MOSFET (C_{oss})	1500 pF	533 pF

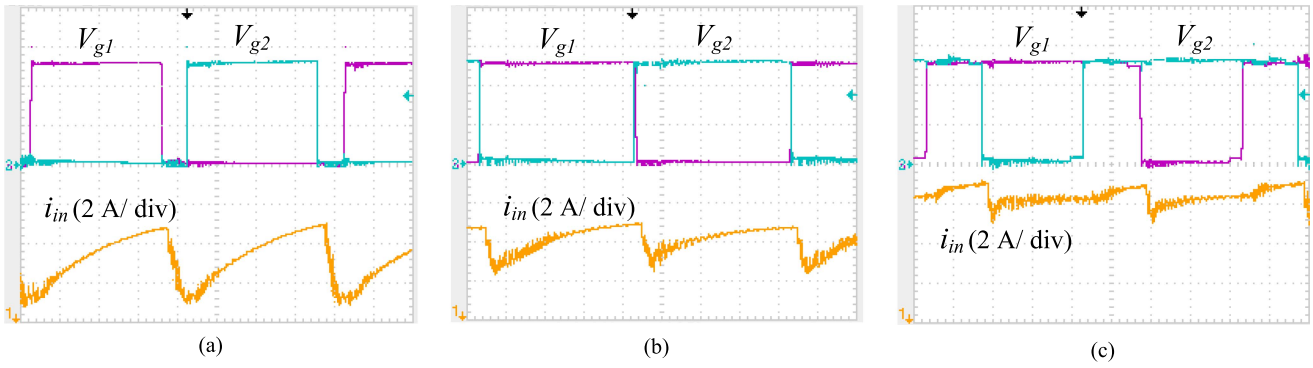

Fig. 17. Experimental waveforms of input current ($i_{\rm in}$) at different duty cycle (D). (a) $D = 0.4$. (b) $D = 0.5$. (c) $D = 0.7$.

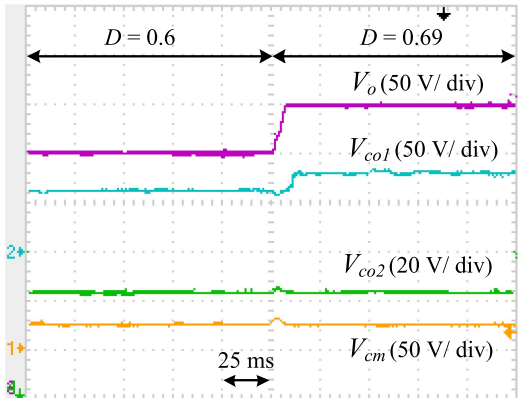

Fig. 18. Experimental waveforms of output voltage (V_o), voltage of output capacitor C_{o1} (V_{co1}), voltage of output capacitor C_{o2} (V_{co2}), and voltage of multiplier capacitor C_m (V_{cm}) when step change in duty cycle.

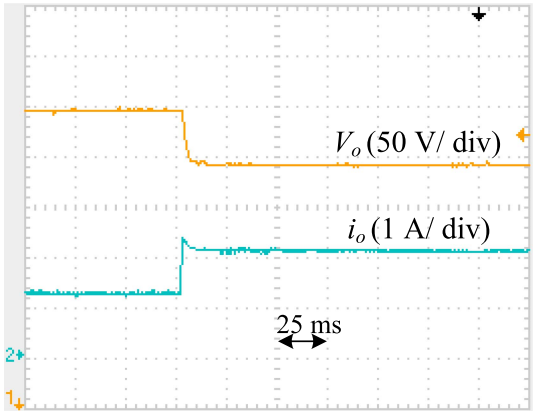

Fig. 19. Experimental waveforms of output voltage (V_o) and current (i_o) for open-loop control of the proposed converter when change in load from half to full.

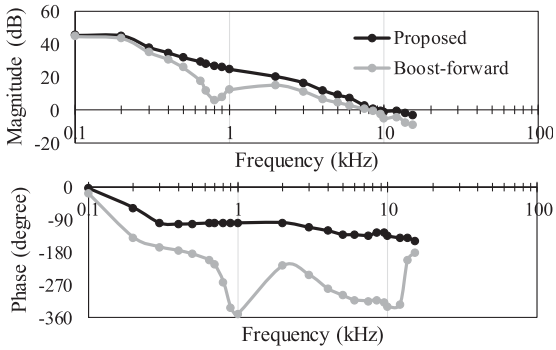

Fig. 20. Measured control to output voltage frequency response of the proposed converter and boost-forward converter for same value of coefficient of coupling $k = 0.972$.

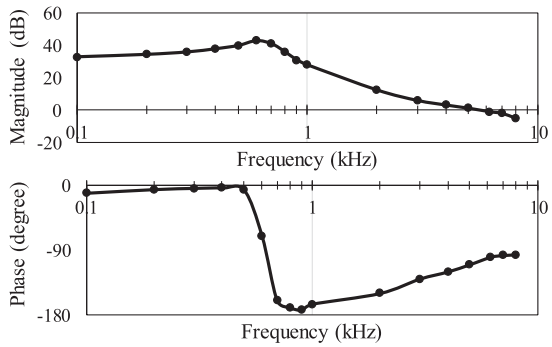

Fig. 21. Measured closed-loop control to output voltage frequency response of the proposed converter.

losses in diode, and losses in capacitor due to ESR. The core loss of both converter was approximately estimated from core loss curve of core material datasheet. Two factors are considered to calculate switching loss of MOSFET. The energy used to charge drain-source capacitance (C_{oss}) and as ZCS turn-ON of MOSFET switch is achieved by both converters due to the presence of leakage inductance of CI, and the energy loss during turn-OFF transitions was calculated. Diode reverse recovery loss is considered zero due to the presence of leakage inductance of CI in the both converters. It can be seen that major source of loss is core loss in both converters. The core loss of the proposed converter is very low compared with the boost-forward converter due to the low inductance value and low value of ripple in input current of the proposed converter. In boost-forward converter, the winding losses in CI, conduction losses in MOSFET, and capacitors are more compared with the proposed converter due to the high value of ripple in input current and high value parasitic parameters. Furthermore, boost-forward converter was operated

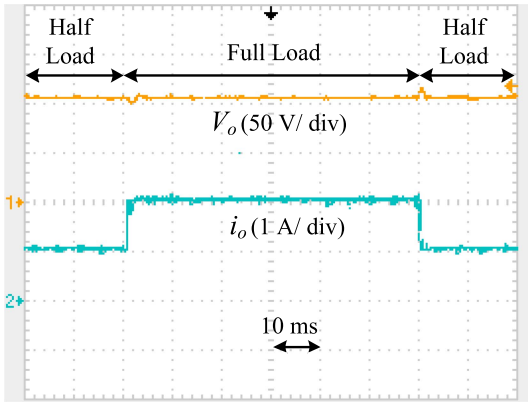

Fig. 22. Experiment results of output voltage (V_o) and current (i_o) waveforms of the proposed converter with single-loop voltage control when step changes in load from 100 to 200 W and 200 to 100 W.

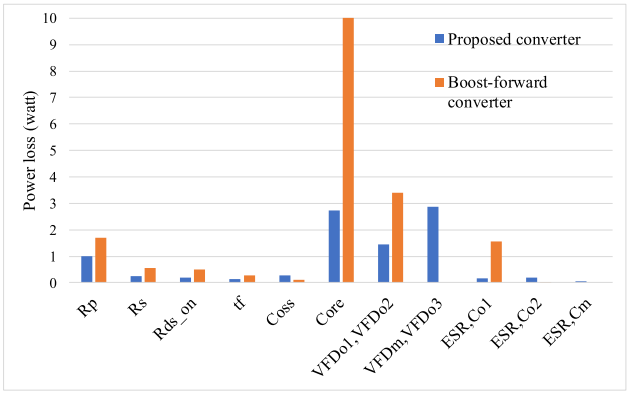

Fig. 23. Losses breakdown of the proposed converter and boost-forward converter.

with high duty cycle compared with the proposed converter to achieve same voltage gain so conduction losses of passive and active devices are more than the proposed converter. In the proposed converter, switching loss in MOSFET and conduction loss in diode are almost equal to boost-forward converter. Overall, the proposed converter has lower losses than the boost-forward converter for the same rating; hence, it can work more efficiently compared with the boost-forward converter although components are more for high step-up gain and high-power application. The measured efficiency of the proposed converter is 94.50% and boost-forward converter is 90.74% at full load.

It is verified through experimental results that the output voltage of the proposed converter had no negative dip in voltage at the instant of step changed in duty cycle from 0.6 to 0.69 with $k = 0.972$. Hence, the converter has eliminated the RHP zero over a wide operating range of duty cycle with k close to 1. In closed-loop operation, the converter achieved stable output voltage with less settling time for a load disturbance using signal-loop voltage control due to high BW and positive stability margin. The converter achieved high step-up gain with low duty cycle in comparison to boost-forward and boost converters. The maximum voltage stress on diode is 55% output voltage. As input current ripple is reduced in the proposed converter than the boost-forward converter, so related losses are reduced, hence improves the efficiency. The efficiency of the proposed converter is 2.4% higher than boost-forward converter at full load. These features of proposed high step-up gain converter allowing converter to work efficiently with good dynamic response for wide operating range.

VII. Conclusion

This article proposes a two-phase interleaved CI and voltage multiplier-based high step-up gain converter without RHP zero for wide operating range. The proposed converter used magnetic coupling to shift zero from RHP to LHP of control-to-output voltage transfer function. The operation principle, and steady-state and dynamic characteristics of the converter were analyzed in detail. Simulations and experimental results verified the results of the small-signal model of the proposed converter. The converter was operated at 200-W power for voltage conversion from 24 to 100 V. The following features are observed in the proposed converter.

1) The main significant feature of the new converter eliminated RHP zero in open-loop control-to-output voltage transfer function. As a result, the proposed converter achieved high BW with high value of stability margin than boost converter. The proposed converter achieved regulated output voltage with faster response using single-loop voltage control against load disturbances.
2) The proposed converter is operated without RHP zero for wide operating range with coefficient of coupling near to one compared to BCMCF.
3) Although the proposed converter has more components count than boost-forward converter, the operating range without RHP zeros is wide, high BW and the transient response is faster, and significant ripple reduction in input current by interleaving the two-phase input. Furthermore, it reduced the size of magnetic core, core and winding losses of CI, and current stress on MOSFET. The efficiency of the proposed converter is higher than the boost-forward converter at full load.
4) The proposed converter has high voltage gain and low voltage stress on switching devices than boost, boost-forward, and BCMCF.

   The proposed converter achieved high step-up gain and high efficiency with better dynamic response. These features make it more suitable choice for high step-up gain and high power applications in low-voltage source, PV panel, and fuel cell in dc microgrid.

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