Frequency-Domain Thermal Coupling Model of Multi-Chip Power Module

Mengqi Xu, Ke Ma, *Senior Member, IEEE*, Yuhao Qi, Xu Cai, Xinqiang Li, Aiguo Wang, and Luhai Zheng

***Abstract*—The high-power density design of the insulated gate bipolar transistor power module may lead to complicated thermal behaviors, and the thermal-coupling effect among multiple chips is a major focus in the field of thermal modeling and characterization. Unfortunately, the existing modeling methods simply describe thermal coupling effect as a superposition of temperatures caused by lateral thermal diffusion. In reality, it is not only the temperature of semiconductors which is important, but also of the heat flow characteristics in heat transfer process. In this article, the thermal coupling effect has been explained in another perspective that it is the result of the overlap between heat flow paths. Frequency domain analysis of heat flow has been first conducted by finite-element methods simulations, and a novel thermal model considering the heat flow coupling has been proposed. This approach focuses on the thermal modeling of the heat coupling effect in cooling system and greatly simplifies the thermal modeling of the heat coupling effect inside power module because it has been discovered that the coupling region is mainly contained in the section from the baseplate to the heatsink. As a result, the proposed method has the advantage of not only having some physical meaning, but also having a relatively simple modeling and characterization process when compared to existing methods. The proposed thermal coupling model is verified by both simulation and experiment, and the application for electrothermal simulation of electric machine drive complex mission profiles composed of multitimescale thermal dynamics is also provided.**

***Index Terms*—Finite-element methods (FEMs), frequency domain analysis, power module, thermal coupling, thermal network.**

I. Introduction

RECENTLY, insulated gate bipolar transistor (IGBT) power modules with multiple chips, have been widely used in reliability-critical and high-power applications, such as electric vehicle, wind turbines, smart grids, and power transmission systems [1], [2], where high cost may be paid on maintenances and failures. It is known that the thermal stress is one of the major causes of failures in power modules [3]. However, there are two main problems to derive accurate thermal behaviors of power modules. First, in order to increase power density, power semiconductor manufacturers are trying to integrate more chips into one device, leading to complexity of thermal interactions among chips inside the power module [4]. Second, the loading profile of power module is closely related to the mission profiles of the converter system [5], the correct estimation for the complex thermal dynamics of power modules under real-field mission profile, is still a challenging problem.

As a matter of fact, the thermal behaviors of a multichip power module can be represented by a simplified three-dimensional (3-D) heat diffusion equation as thermal diffusion across diverse solid regions with isotropic materials from multiple surface heat sources [6], [7]. To solve this equation, analytical methods, numerical methods, and thermal network modeling methods are the typical three approaches. Analytical methods involve various mathematical solutions, such as Fourier series solutions [8], [9], which requires extensive mathematical and physical knowledge. Numerical methods, e.g., finite-element method (FEM), are frequently used to try to find approximate solutions to the heat diffusion equation. However, large computational cost is required when using FEM to analyze transient thermal behaviors [10], [11], making it unsuitable for calculating the device temperatures in long-term mission profiles composed of multitimescale thermal dynamics.

Based on the discovery that the heat diffusion equation has almost the same form of the wave equation of a transmission line [7], thermal network modeling methods have been developed [12], [13]. Nowadays, the Foster network is widely utilized, as it appears in the datasheet, since it is independent of internal structure or material. But, the Foster network has a problem in that each internal node is crossed by the heat flow from the preceding *RC* lump which represents no physical meaning [14]. Therefore, inaccurate results will be observed when it is extended with the thermal models for the thermal grease and heatsink [12]. To deal with this issue, [15] analyzed the thermal behaviors in frequency domain and proposed a thermal model that includes a low pass filter (LPF). However, because the thermal coupling effect was not taken into account, these models cannot be applied to multichip power modules.

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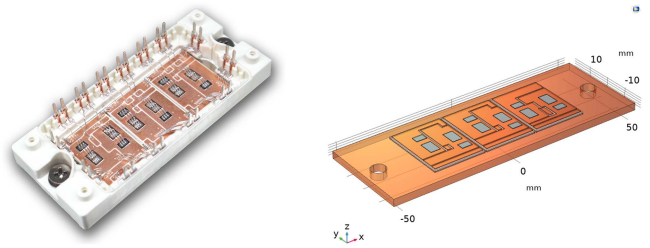
To describe the thermal coupling effect, a matrix-based thermal model developed from the 1-D thermal network has emerged [16], [17]. The simplest matrix-based thermal model is composed of pure thermal resistances with dimensions of the number of chips or heat sources as stated in [18] and [19], which is unable to predict the transient thermal behaviors of IGBT module. Afterwards, thermal impedance matrix has emerged, which replace each thermal resistance with thermal impedance in order to describe the transient thermal behaviors [4], [17], [20], [21]. The thermal coupling effect is represented by Foster-type thermal impedances in this model, so it has no physical meaning as well. Furthermore, due to its complicated structure, it could be a repeated and complex process if all the *RC* parameters in the thermal matrix are extracted [22].

Compact thermal model as stated in [23], [24], and [25] is another modeling method, which can be seen as Cauer thermal network that considers the coupling effects. However, this model contains numerous temperature nodes both inside and outside the power module, making it impossible to characterize model parameters just through experiments. Thus, a FEM model is required to be built first for assisting the modeling and characterization process of the compact thermal model, which means that the accuracy of the compact thermal model is highly dependent on the accuracy level of the built FEM model.

In this article, the thermal coupling effect has been explained in another perspective that it is the result of the overlap between heat flow paths. Frequency domain analysis of heat flow has been first conducted by FEM simulations and it has been discovered that the low-pass filtering characteristics of heat flow behaviors are only related to the distance between the junction node to case node. Additionally, the region where the thermal coupling effect occurred has been examined in this article and it turns out that the coupling region is mainly contained in the section from baseplate to the heatsink when the thermal coupling inside power module has little effect on junction temperatures. By combining these discoveries, this article proposes a novel modeling method to describe the thermal behaviors of multichip power module. The major benefit of proposed method is that the modeling and characterization process is relatively simple compared with existing methods. Furthermore, this proposed thermal model can be easily implemented in electrothermal simulation, and the calculated results are accurate in multitimescales, as verified by experiments.

II. Heat Flow Spectrum Analysis of Multichip Power Module

A 650V/50A IGBT power module, GD50FFX65C5S of Starpower, is used as study case in this article, which is composed of six IGBTs and six diodes in three-phase half-bridge configuration as shown in Fig. 1(a). For a multichip power module, the heat sources from other chips also contribute to the increase of the junction temperature, where the superposition theorem can be applied just like in electrical domain [26]. Therefore, the conventional matrix-based thermal modeling method uses the



(a) (b)

Fig. 1. Studied IGBT module. (a) Photograph of the module. (b) Schematic of the IGBT module modeled in COMSOL for FEM simulations.

following expression to consider the thermal coupling effect:

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jN} \end{bmatrix} = \begin{bmatrix} Z_{j1\text{ref@}1} & Z_{j1\text{ref@}2} & \cdots & Z_{j1\text{ref@}N} \\ Z_{j2\text{ref@}1} & Z_{j2\text{ref@}2} & \cdots & Z_{j2\text{ref@}N} \\ \vdots & \vdots & \vdots & \vdots \\ Z_{jN\text{ref@}1} & Z_{jN\text{ref@}2} & \cdots & Z_{jN\text{ref@}N} \end{bmatrix} \times \begin{bmatrix} P_{\text{in}1} \\ P_{\text{in}2} \\ \vdots \\ P_{\text{in}N} \end{bmatrix} + T_{\text{ref}}$$
$$= (\boldsymbol{Z}_{\mathbf{self}} + \boldsymbol{Z}_{\mathbf{couple}}) \cdot \boldsymbol{P}_{\mathbf{in}} + T_{\text{ref}} \quad (1)$$

where N represents the number of chips, $\boldsymbol{Z}_{\mathbf{self}}$, $\boldsymbol{Z}_{\mathbf{couple}}$, $\boldsymbol{P}_{\mathbf{in}}$, and $\boldsymbol{T}_{\mathbf{ref}}$ represent self-thermal impedance matrix, thermal-coupling impedance matrix, power loss vector, and reference point temperature, respectively. Each element in $\boldsymbol{Z}_{\mathbf{self}}$ and $\boldsymbol{Z}_{\mathbf{couple}}$ is composed of Foster-type thermal networks and the Foster-type transfer function is expressed as

$$Z_{th}^{\text{Foster}}(s) = \sum_{i=1}^{n} \frac{R_i}{R_i C_i \cdot s + 1}. \quad (2)$$

As for the reference temperature, most of the matrix-based modeling methods choose ambient/heatsink temperature as the reference for simplicity of modeling and characterization [6], [11]. Moreover, the heat flow characteristics are ignored in this matrix-based method and the thermal coupling effect is represented by a $N \times N$ thermal matrix. As a result, the testing time and number of measurements considerably rise as the number of heat sources increases [22]. A power module with 12 chips in this article, for example, requires 12 separated simulations or experiments to obtain the parameters.

A. Frequency-Domain Analysis With FEM Simulations

In order to study the heat transfer process inside the power module, the FEM model of the studied module is first constructed in software COMSOL as shown in Fig. 1(b) and the parameters for the material of each layer of the IGBT module are given in Table I. The total meshing system consists of 103 269 domain elements, 40 518 boundary elements and 4794 edge elements. As for the cooling system outside the IGBT

TABLE I
PARAMETERS FOR THE MATERIAL OF THE STUDIED IGBT MODULE

Layers	Material	Thermal conductivity λ (W/m·K)	Specific heat C_p (J/kg·K)	Density ρ (kg/m^3)
Chip	Si	148	710	2330
Chip Solder	Sn-3.5Ag-0.5Cu	33	230	7500
Copper	Copper	395	385	8700
DCB	Al_2O_3	24	896	3750
Copper	Copper	395	385	8700
Baseplate Solder	Sn-3.5Ag-0.5Cu	33	230	7500
Baseplate	Copper	395	385	8700

module, equivalent heat transfer coefficient (htc) is often used as a simplified thermal boundary condition to indicate the heat dissipation capability of the cooling system [23]. htc = 3000 W/m^2·K is picked as a reference in this article to simulate the cooling performance of water-cooled heatsink.

FEM is widely used for thermal simulations but it has two problems. 1. It is time-consuming to conduct transient simulations in time domain. 2. It is difficult to accurately simulate the heat dissipation capabilities of a complicated cooling system, which requires computational fluid dynamics simulations. As a result, the FEM model in this article is only used for model derivation and verification, and the frequency domain simulation is first conducted in this article.

The frequency domain simulation in COMSOL is composed of two steps: the first step is a Stationary study step which computes the stationary/bias solution; the second step is the frequency domain perturbation step, which computes a perturbed solution of the linearized problem around the linearization point computed in the first step [27]. Take one of the direct-copper-bonded (DCB) sections of the studied IGBT power module for analysis, there are two IGBT chips ($T1$ and $T2$) and two diode chips ($D1$ and $D2$). In order to study the heat flow characteristics of the power module, four heat flux probes at the center position of each chip and four heat flux probes on the surface of the baseplate at the same vertical position underneath each chip are set as shown in Fig. 2.

As a result, the heat gain from each chip to the case underneath the center position of the chip under frequency domain is shown in Fig. 3, proving that a low-pass filtering effect exists in the heat transfer process as stated in [15]. Furthermore, the simulation results show that the LPF characteristics of heat gain from each chip to the case point underneath are the same, which indicates that the LPF characteristics of heat gain from chip to case are purely related to the distance between two probes and not to chip size.

B. LPF Characteristics With Different Distances

Based on the discovery that the heat gain from chip to case is only related to the distance between two probes, it is worthwhile to investigate the LPF characteristics for different distances. Take the IGBT chip at the very edge of the layout as a study

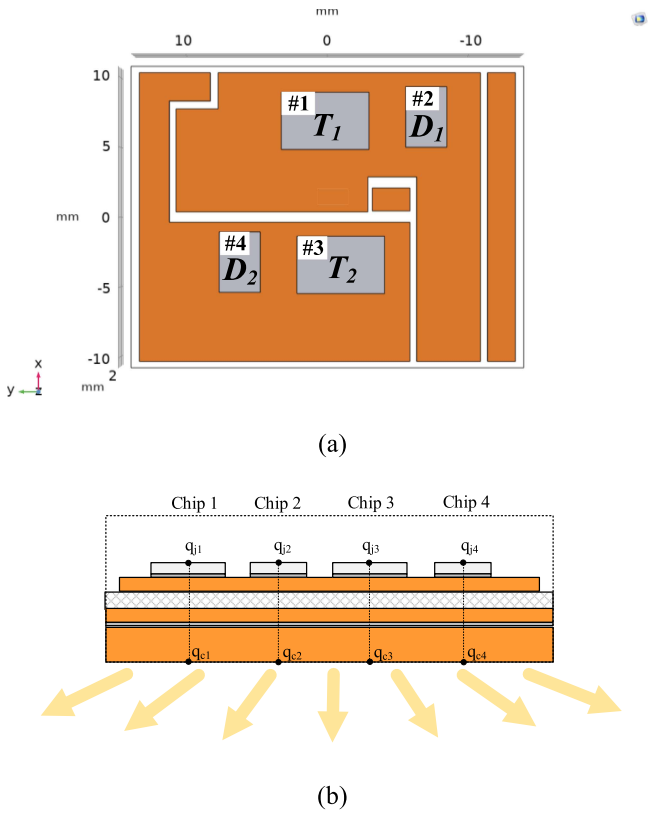


Fig. 2. One DCB section of power module. (a) Top view of four chips. (b) Cross section view with heat flux probes for obtaining LPF characteristics.

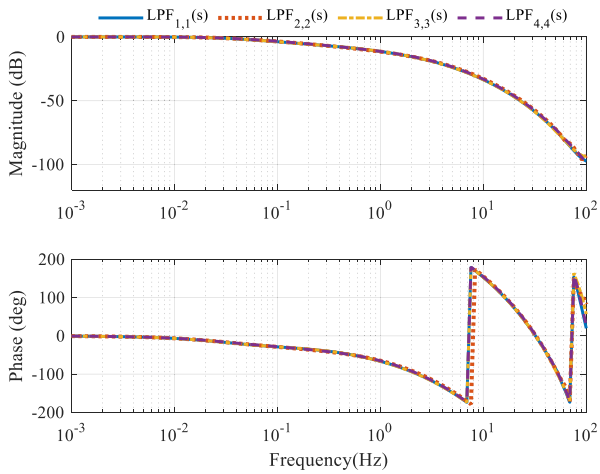


Fig. 3. LPF characteristics of heat gain from each chip to the case point underneath.

case, and select eight distances between the chip and the case, as shown in Fig. 4. After placing heat flux probes on these specified positions on the baseplate, frequency domain simulations have been conducted and the LPF characteristics for different distances are depicted in Fig. 5. It demonstrates that the LPF characteristics change regularly with the increase of distance. In other words, this changing rule can be practically applied for users to preliminarily recognize the chip layout without decapsulation of the IGBT power module in experiments. For

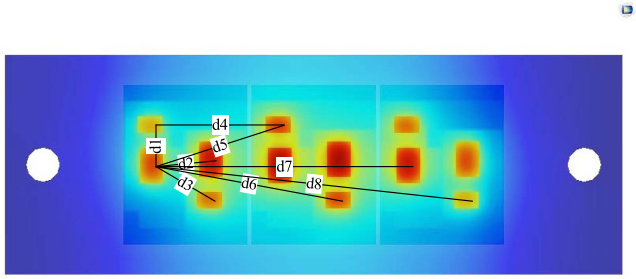


Fig. 4. Top view of distances between one probe on the chip surface to eight probes on the surface of baseplate.

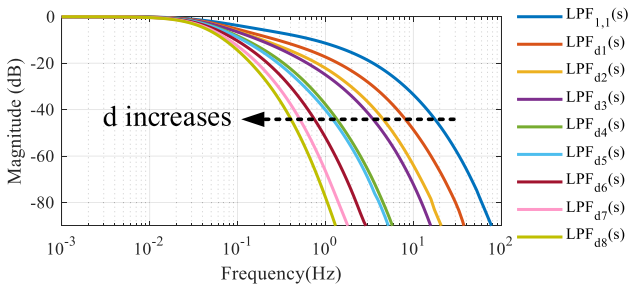


Fig. 5. LPF characteristics for different distances in Fig. 4.

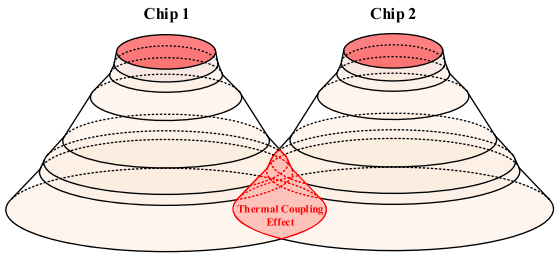


Fig. 6. Thermal coupling effect happened between two heat flow paths.

instance, if the heat flux probe on the center of baseplate surface is fixed, and the distances between different switches to case can be estimated by comparing the different LPF characteristics accordingly.

III. Heat Flow Coupling of Multichip Power Module and Proposed Model

A. Description of Thermal Coupling Effect With Heat Flow

For analysis of the heat spreading process, the conventional matrix-based thermal model as (1) can only describe the thermal behavior by overall junction temperature and the thermal coupling effect is simply represented by Foster-type thermal impedances. Thereby, it has no physical meaning, and it is also complicated to obtain all the parameters of the thermal matrix. As a matter of fact, the thermal coupling effect happened because of the overlap between heat flow paths, as shown in Fig. 6. To explain this phenomenon, one point c on the baseplate surface inside the overlap area is selected for study, and two different conditions are considered as follows.

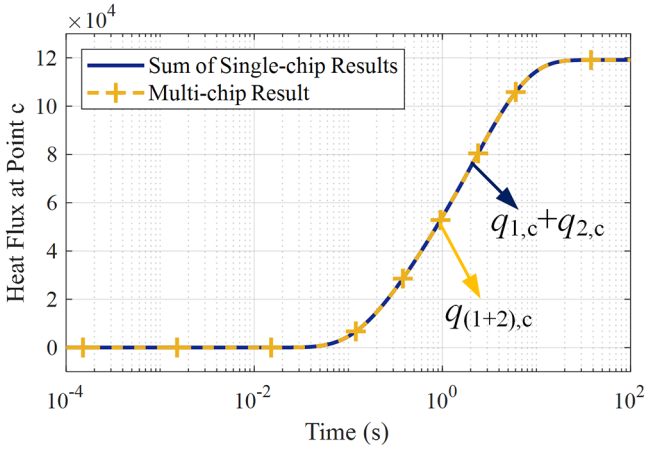


Fig. 7. Comparison of heat flux at point c with two different conditions.

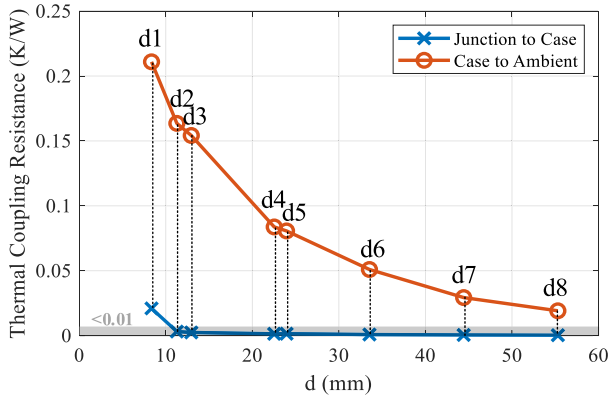


Fig. 8. Junction-to-case thermal coupling resistance compared with case-to-ambient thermal coupling resistance for different distances in Fig. 4.

1) Two chips are heated separately and the heat flux at point c is recorded, respectively, and then the sum is calculated.
2) Two chips are heated simultaneously and the heat flux at point c is recorded.

As demonstrated in Fig. 7, the multichip result is consistent with the sum of single-chip results. It indicates that the superposition theorem is also valid here for describing the heat flow characteristics, which is used in the proposed thermal modeling method in this article.

Furthermore, the region where the overlap occurs is highly dependent on the distance between two chips and the geometric dimensions of each layer. Take the eight distances shown in Fig. 4 for study, the thermal coupling resistance for the IGBT chip at the very edge of the layout measured by heating the corresponding chips are plotted in Fig. 8. Two types of thermal coupling resistance are compared here: junction-to-case thermal coupling resistance representing the thermal coupling effect inside power module, and case-to-ambient thermal coupling resistance representing the thermal coupling effect outside power module, which are calculated by

$$R_{\text{couple}-j1c1} = \frac{T_{j1} - T_{c1}}{P_{in-di}} \tag{3}$$

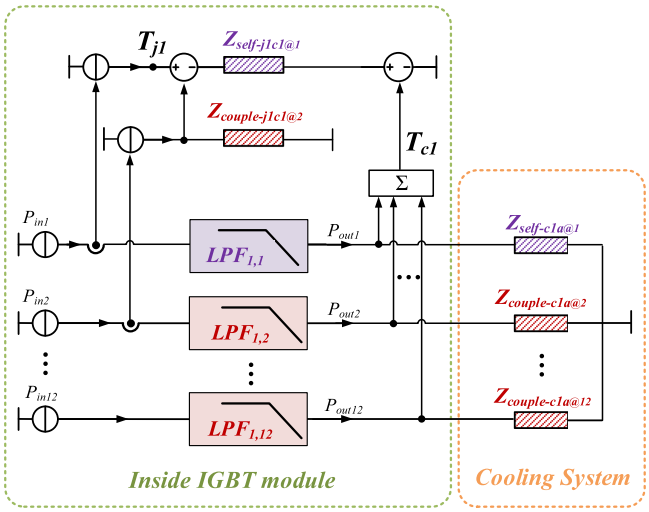


Fig. 9. Proposed modeling method considering thermal coupling effect for the studied IGBT chip in Fig. 4.

$$R_{\text{couple}-c1a} = \frac{T_{c1} - T_a}{P_{in-di}} \tag{4}$$

where i varies from 1 to 8, and it refers to the corresponding chip as marked in Fig. 4.

Obviously, the junction-to-case thermal coupling resistance is much smaller than case-to-ambient thermal coupling resistance, which indicates that the coupling region is mainly contained in the section from baseplate to the heatsink and the thermal coupling inside power module has little effect on junction temperatures. As can be seen in Fig. 8, the junction-to-case thermal coupling resistance is less than 0.01 K/W for the distance of $d2$ to $d8$. As a result, the thermal impedance matrix for describing the thermal coupling effect inside the power module can be greatly simplified based on this discovery, while the thermal coupling effect that happened from the baseplate to the heatsink should be carefully considered.

B. Proposed Frequency-Domain Model

Then, a thermal model considering thermal coupling effects for the studied IGBT chip in Fig. 4, consisting of Foster *RC* networks and LPFs, has been proposed as shown in Fig. 9. Self-heating section is highlighted in purple, while coupling section is highlighted in red. Two boxes are used to separate the junction-to-case section from the case-to-ambient section. It should be noted that the heat flux of one point is measured in this article and there are some ideal assumptions in order to construct a lumped thermal model, e.g., the heat flux distribution is assumed to be uniform, so that the characteristics of gain of heat flow can be seen as the same as heat flux. As for the structure of LPF, the characteristics of heat gain can be approximated as three cascaded LPFs as stated in [28], and the transfer function $G_{\text{LPF}}(s)$ is expressed as

$$G_{\text{LPF}}(s) = \left(\frac{2\pi f_{cr1}}{s + 2\pi f_{cr1}}\right)^a \cdot \left(\frac{2\pi f_{cr2}}{s + 2\pi f_{cr2}}\right)^b \cdot \left(\frac{2\pi f_{cr3}}{s + 2\pi f_{cr3}}\right)^c \tag{5}$$

where f_{cr1}, f_{cr2}, and f_{cr3} are the critical frequencies in LPF, a,b,c are the orders of each cascaded LPF and satisfy $a+b+c=7$. The method of determining the order of each cascaded LPF has been thoroughly described in [28] and in this article $a=1$, $b=3$, and $c=3$, respectively.

As a result, the heat flow out of power module from each heat source can be estimated as (6) after passing each LPF expressed in (5):

$$P_{\text{out}i}(s) = G_{\text{LPF1},i}(s) \cdot P_{\text{in}i}(s),\ i = 1, 2, \ldots 12. \tag{6}$$

Since the case node at baseplate is selected as the reference node in this proposed model, the thermal impedance in this model is considered to be separated into two parts: the junction-to-case thermal impedance and the thermal impedance outside power module. Furthermore, the thermal coupling impedance matrix for describing the thermal coupling effect inside the power module is greatly simplified according to Fig. 8 that only one junction-to-case thermal coupling impedance $Z_{\text{couple-}j1\,c1\,@2}$ is included in this model. The thermal coupling effect that happened from the baseplate to the heatsink is described by 11 Foster-type thermal coupling impedances. Therefore, the case temperature underneath the studied chip can calculated by applying superposition theorem:

$$T_{c1} = P_{\text{out1}} \cdot Z_{\text{self}-c1a@1} + \sum_{i=2}^{12} P_{\text{out}i} \cdot Z_{\text{couple}-c1a@i} + T_a. \tag{7}$$

C. Parameter Identification of Proposed Thermal Model

The parameter identification of components in proposed frequency-domain thermal coupling model is relatively simple.

1. Junction-to-case thermal impedance in this proposed model is composed of Foster networks, and it can be easily characterized by time-domain curve fitting [4].
2. As for the LPFs, the parameters can be characterized by utilizing the information of heat flowing out of device as stated in [29].
3. Once all of the LPFs are determined, the case-to-ambient thermal impedance can also be obtained because the input of external conditions in the proposed model is the output of LPFs, and the Foster-type network can be characterized by time-domain curve fitting of temperature difference between case and atmosphere.

To prove the effectiveness of the aforementioned LPF with the identified parameters, Fig. 10 compares the bode plot of identified $\text{LPF}_{1,1}(s)$ with FEM results as an example. It shows that the identified $\text{LPF}_{1,1}(s)$ is highly consistent with simulation results below 100 Hz. The identified parameters of all the LPFs in proposed model are given in Table II. It should be noted that the parameter identification process is simplified according to the distance-dependent characteristics mentioned above. For instance, as shown in Fig. 5, the characteristics of LPF_{d4} are similar to LPF_{d5}, so that the corresponding LPFs in this proposed model of Fig. 9 can be estimated by the same expression:

$$G_{\text{LPF1},6}(s) \approx G_{\text{LPF1},5}(s) = G_{\text{LPFd4}}(s). \tag{8}$$

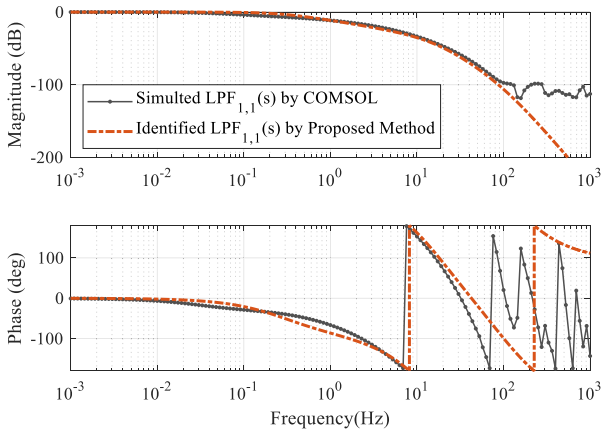


Fig. 10. Comparison of bode plots of identified $\mathrm{LPF}_{1,1}(s)$ with FEM results.

TABLE II
IDENTIFIED LPFS OF PROPOSED THERMAL MODEL

Parameter	Distance	f_{cr1}(Hz)	f_{cr2}(Hz)	f_{cr3}(Hz)
$\mathrm{LPF}_{1,1}$	-	0.2235	16.50	81.39
$\mathrm{LPF}_{1,2}$	d1	0.1061	10.23	73.68
$\mathrm{LPF}_{1,3}$	d2	0.0828	4.57	64.49
$\mathrm{LPF}_{1,4}$	d3	0.0601	1.797	50.19
$\mathrm{LPF}_{1,5}$	d4	0.0411	0.923	41.52
$\mathrm{LPF}_{1,6}$	d5	0.0411	0.923	41.52
$\mathrm{LPF}_{1,7}$	-	0.0373	0.488	30.13
$\mathrm{LPF}_{1,8}$	d6	0.0373	0.488	30.13
$\mathrm{LPF}_{1,9}$	d7	0.0288	0.269	26.65
$\mathrm{LPF}_{1,10}$	-	0.0288	0.269	26.65
$\mathrm{LPF}_{1,11}$	-	0.0259	0.216	20.06
$\mathrm{LPF}_{1,12}$	d8	0.0259	0.216	20.06

In order to validate the proposed thermal model, simulation with power loss of sinusoidal half wave is conducted because it can replace and simplify the real instantaneous power loss [23]

$$P_{\mathrm{IGBT}i}(t) = \begin{cases} 75\sin(2\pi t - \pi) & P_{\mathrm{IGBT}i}(t) \geq 0 \\ 0 & P_{\mathrm{IGBT}i}(t) < 0 \end{cases}, \mathrm{i} = 1, 2, \ldots 6 \tag{9}$$

$$P_{\mathrm{Diode}i}(t) = \begin{cases} 75\sin(2\pi t) & P_{\mathrm{Diode}i}(t) \geq 0 \\ 0 & P_{\mathrm{Diode}i}(t) < 0 \end{cases}, \mathrm{i} = 1, 2, \ldots 6. \tag{10}$$

Fig. 12(a) demonstrates that the simulated temperatures of the proposed thermal model have high consistency with FEM results that maximum error of 1.6 °C is detected. It is well known that FEM is time-consuming when analyzing transient thermal-coupling behaviors and 2 h 45 min is paid for once simulation with 1 ms of time step and 5 s of time span under the studied case in this article. But for the proposed model, only 2 s is required for once simulation with time step of 1 μs. Noted that all the simulations are executed on a workstation with AMD R9-5950X at 3.40 GHz and 128-GB RAM.

Also, it is convenient to predict temperatures of other chips because the LPF characteristics and case-to-ambient thermal coupling impedances are only related to the distances as explained in the above section. As shown in Fig. 11, only the parameters of three items in blue boxes are re-extracted for modeling of the closet diode chip ($D1$) to the studied chip ($T1$):

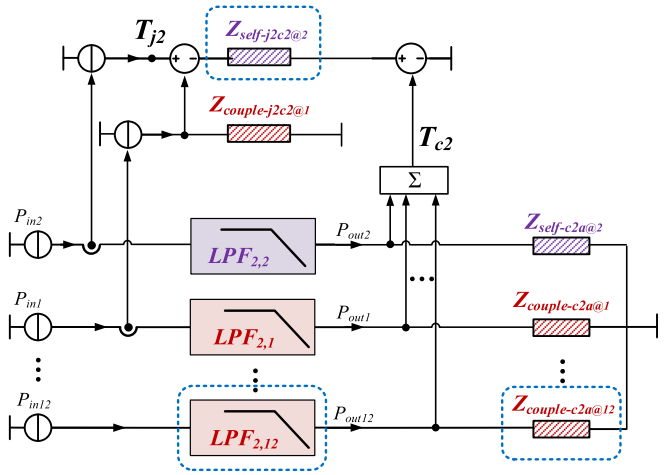


Fig. 11. Proposed modeling method for closet diode chip to the studied IGBT chip in Fig. 4.

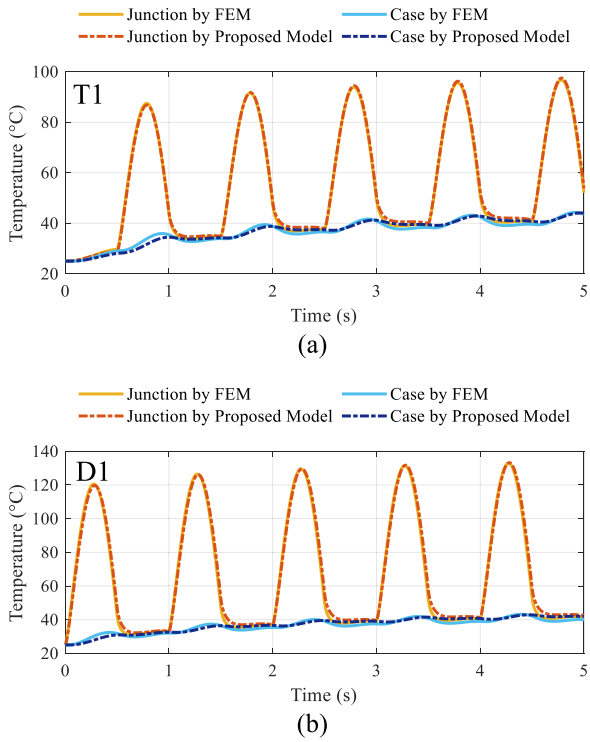


Fig. 12. Comparison of predicted temperatures by proposed thermal model with FEM results. (a) Studied IGBT chip in Fig. 4. (b) Diode chip closest to the studied IGBT chip.

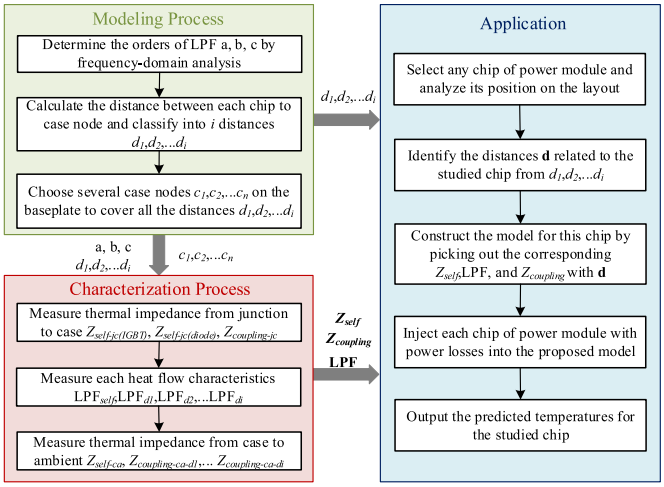


Fig. 13. Schematic of proposed method.

junction-to-case thermal impedance, the LPF with distances that are not shown in Fig. 4, and the corresponding case-to-ambient thermal coupling impedances. The parameters of rest items do not require re-extraction because they satisfy

$$G_{\mathrm{LPF1},1}(s) \approx G_{\mathrm{LPF2},2}(s) \tag{11}$$

$$G_{\mathrm{LPF1},2}(s) \approx G_{\mathrm{LPF2},1}(s) \tag{12}$$

$$Z_{\mathrm{self}-c1a@1}(s) \approx Z_{\mathrm{self}-c2a@2}(s) \tag{13}$$

$$Z_{\mathrm{couple}-j1c1@2}(s) \approx Z_{\mathrm{couple}-j2c2@1}(s) \tag{14}$$

$$Z_{\mathrm{couple}-c1a@2}(s) \approx Z_{\mathrm{couple}-c2a@1}(s). \tag{15}$$

Under this circumstance, the predicted temperatures of $D1$ are shown in Fig. 12(b), which also have a good agreement with FEM results.

This proposed modeling method only requires one IGBT chip and one diode chip of the studied power module to cover all the distances between each chip to the point underneath each chip on the baseplate. As a result, the main advantage of this method is that the number of simulations for parameter identification of proposed model is much less than existing methods and only two simulations are required here. The temperatures of other chips can be easily predicted according to their locations by using proposed method.

To conclude, the schematic of proposed method is shown in Fig. 13, it can be seen that three stages are included: modeling process; characterization process; and application. In the modeling process, the main target is to determine the structure of LPF, classify the distances between each chip to case node, and select appropriate case nodes for characterization. In the characterization process, the parameters of each component in the proposed model will be determined. In practical application, the location of interested chip should be analyzed first and then the corresponding model for this chip will be constructed by combing the distance-related components in characterization process. After injecting power losses into each chip of the power module, the temperatures will be easily calculated.

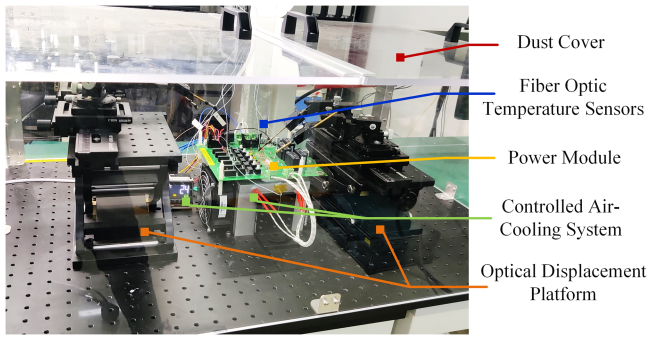


Fig. 14. Experimental setup for thermal characterization of the power module.

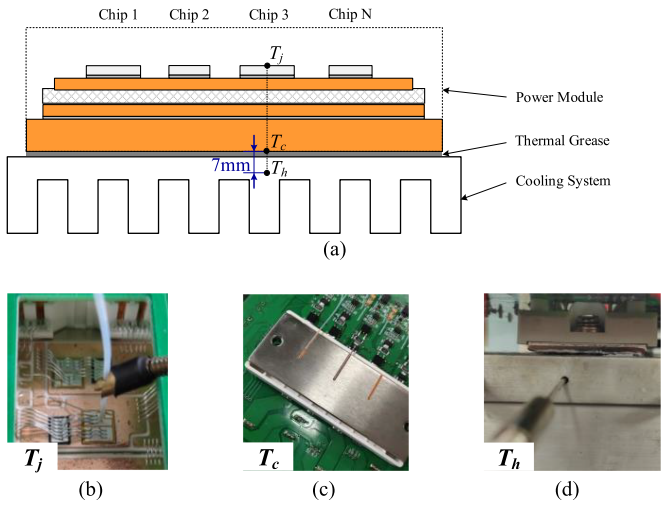


Fig. 15. Locations of three temperature sensors. (a) Cross section view of the sensros. (b) Photo of junction temperature sensor. (c) Photo of case temperature sensor. (d) Photo of heatsink temperature sensor.

IV. Experimental Validation

A. Experimental Setup and Model Verification

To verify the proposed method, the same 650 V/50 A IGBT power module is taken as an example for experimental tests. The experimental setup is shown in Fig. 14 and Opsens' OTG-F optical fiber temperature sensors with accuracy of ±0.3 to 0.8°C and response time of 5 ms are applied for temperature measurement in this article. The case node is set right underneath the IGBT chip, and the heatsink node is close to case node, which can be seen in Fig. 15(a).The photos of sensors installation for junction, case, heatsink are shown in Fig. 15(b)–(d), respectively.

During characterization process, each chip is heated with constant current of 15 A. The Foster networks for describing thermal impedances can be easily identified by using curve fitting algorithms. But, in practice, it is difficult to directly measure heat flow behaviors to identify the parameters of LPFs. As a result, the method of obtaining the heat flow out of power module $P_{\mathrm{out}}(t)$ by indirect approach through two temperature nodes is adopted as follows:

$$P_{\mathrm{out}}(t) = \frac{T_c(t) - T_h(t)}{Z_{ch}}. \tag{16}$$

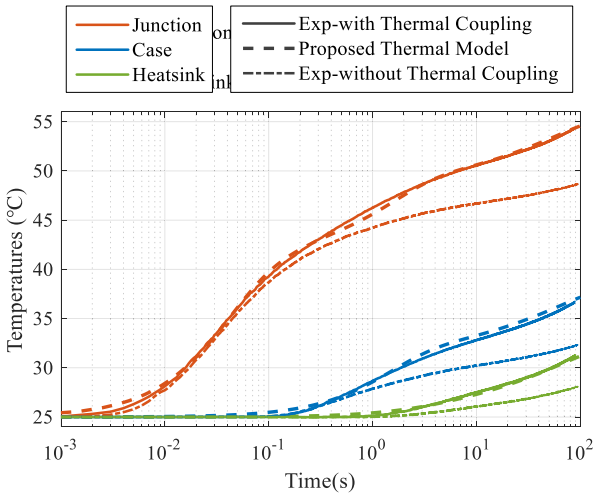


Fig. 16. Comparison of proposed thermal model with experiment with/without thermal coupling effect.

However, $Z_{ch}(t)$is impossible to define without precise measurement of $P_{\text{out}}(t)$, which creates a paradox. As a matter of fact, the thermal capacitance of thermal grease is usually smaller than 1 J/K because the thickness of thermal grease is usually less than 100 μm when module is well installed on the cooling system. Therefore, the (16) can be simplified by supposing only pure thermal resistance exists in the layer of thermal grease, if the two temperature sensors are close enough [29] and the heat flow can be calculated as

$$P_{\text{out}}(t) \approx \frac{T_c(t) - T_h(t)}{R_{ch}}. \tag{17}$$

In this experimental setup, the distance between case and heatsink measuring point is only 7 mm.

It is convenient to set probes on different locations of the baseplate surface in FEM simulations, but there is only one case node here in experiments. As a result, the characterization process for the proposed model is slightly different from that applied for simulations, and the parameters of proposed model are characterized by heating each chip separately. All the temperature curves are measured during turn-OFF process according to the JEDEC Standard [30].

For verification of the extracted parameters, an experiment by heating two IGBT chips in the same DCB section simultaneously with current of 15 A is carried out and the temperature curves are recorded. The comparison of time-domain step response of thermal behaviors with proposed model and experimental curves is plotted in Fig. 16, which directly shows that the proposed model with identified parameters has a good agreement with the experiments when two chips are heated simultaneously.

B. Electrothermal Simulation With Proposed Model

Due to its simple structure, this proposed thermal model can be easily implemented in electrothermal simulation. In this article, an electrothermal simulation with proposed thermal model is carried out by using PLECS. A drive system based on permanent magnet synchronous machine (PMSM) is chosen as the study case in this article. The target power semiconductor device under test is the drive converter. The parameters of the studied PMSM system are given in Table III, and the drive converter is operated with field oriented control. It should be noted that the designed dc-bus voltage 400 V is less than the rated voltage of power module 650 V because there will be overshoot between collector and emitter during the IGBT turn-OFF. In order to ensure safe and reliable operation of the system, a relatively larger margin is left in dc-bus voltage design.

TABLE III
PARAMETERS OF THE PMSM-DRIVE SYSTEM FOR CASE STUDY

Parameter	Value
Stator Inductance (d-axis) L_d	2.5 mH
Stator Inductance (q-axis) L_q	2.5 mH
Stator Resistance R_s	0.34 Ω
PM Flux Linkage Ψ_f	0.022 Wb
Number of Pole Pairs N_p	4
Rotational Inertia J	0.002 kg·m^2
DC Bus Voltage V_{DC}	400 V
Switching Frequency f_{sw}	20 kHz

A long-term load profile of 500 s based on drive system with the configuration as given in Table III is constructed, consisting of soft start, periodic acceleration, periodic deceleration, which is given following: The rotational speed is set as 60 r/min at first in order to simulate the soft start of the target electric machine, and the load torque is set as 2 N·m. At 2 s, the electric machine is accelerated to 1200 r/min within 3 s. At 5 s, the rotor speed is accelerated to 1800 r/min within 5 s. After 10 s, the electric machine is set to accelerate and decelerate cyclically, and the cycle of the acceleration and deceleration is 10 s. Within the first 5 s during the cycle, the electric machine is accelerated to 2400 r/min, and the load torque steps to 3.5 N·m. Within the last 5 s during the cycle, the electric machine is decelerated to 1800 r/min, and the load torque steps to 4.5 N·m.

The predicted temperature responses by proposed thermal coupling model compared with the experimental measurements of temperature responses are shown in Fig. 17. It demonstrates that the predicted junction temperature has a good agreement with measurement that the maximum junction temperature error is 1.29 °C. There are primarily two reasons for the difference between the predicted and measured junction temperature curves are as follows.

1) The response time of optical fiber is limited to 5 ms.
2) A filtering algorithm is built into the temperature measuring instrument to reduce measurement noise.

As a result, the rapid temperature fluctuations that occur on the junction cannot be detected by the temperature measuring instrument.

C. Comparison With Existing Modeling Methods

When compared to the FEM model, the key advantage of the proposed frequency-domain thermal coupling model is its

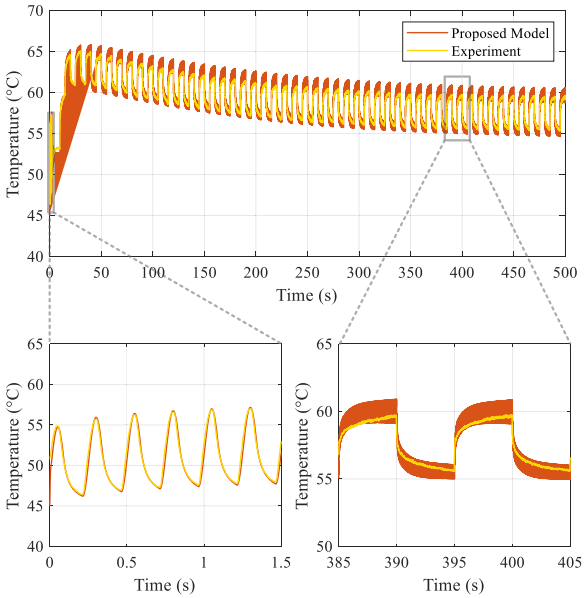


Fig. 17. Predicted temperature responses by using proposed method compared with experimental measurement under a long-term load profile.

low computational cost. It is well known that FEM is time-consuming when analyzing transient thermal-coupling behaviors and 2 h 45 min is paid for once simulation with 1 ms of time step and 5 s of time span under the studied case of Fig. 12 in this article. But for the proposed model, only 2 s is required for once simulation with time step of 1 μs. Noted that all the simulations are executed on a workstation with AMD R9-5950X at 3.40 GHz and 128-GB RAM.

Compared with conventional matrix-based modeling method, the proposed model has some physical meaning because of the uses of LPFs for representing heat flow behaviors as stated in the above sections. Another benefit of the proposed model is its comparatively simple modeling process and characterization process. Once the distances between each chip to each case node on the layout are identified, the corresponding LPF and thermal impedances can be easily characterized with limited experiments. But for conventional matrix-based modeling method, it is rather complicated to characterize the *RC* parameters when the number of chips is large.

Finally, the proposed frequency-domain thermal coupling model has two types of nodes, the junction and the case, both of which can be easily obtained by external measurement. To be specific, junction temperature can be measured by optical methods, physically contacting methods, and electrical methods, the most common of which is the use of a thermosensitive electrical parameter (TSEP) by utilizing chip itself as a sensor [31]. Because the case node is on the surface of the baseplate, TSEP cannot be applied here, so that physically contacting methods by using thermal probes can be used. But for compact thermal model with nodes inside power module, both the modeling process and characterization process requires the help of building an accurate FEM model.

In conclusion, based on literature references and the study in this article, the comparison for various models, such as the FEM model, thermal impedance matrix, compact thermal model and proposed frequency-domain thermal coupling model are given in Table IV.

TABLE IV
COMPARISON FOR DIFFERENT MODELS

Model	FEM Model	Thermal Impedance Matrix	Compact Thermal Model	Proposed Model
Computational Cost	Significant	Medium	Medium	Low
Modeling Process	Complex	Medium	Medium	Easy
Characterization Process	Medium	Complex	Medium	Easy
Physical Meaning	Yes	No	Yes	Yes
Electro-thermal Simulation	No	Yes	Yes	Yes

V. APPLICATION AND DISCUSSION

In this article, the proposed thermal model was derived based on superposition theorem as stated in Section III. But, the superposition theorem used should not be valid in case of non-linear thermal problems. As for SiC MOESFETs with much stronger temperature-dependence than Si and copper, this issue should be carefully considered [32].

Since this is not the focus of this article, a possible solution is provided here and detailed investigation will be conducted in further research. As can be seen in the proposed model in Fig. 9, the modeling of power module and the cooling system is completely separated at case node, so that the parameters of junction-to-case thermal impedances and LPFs related to the chip layer can be configured to be temperature-dependent. For example, only the f_{cr3} in LPF corresponds to high frequency band which is composed of chip layer, chip solder layer and baseplate solder layer of the studied device will be influenced as stated in [28], thereby it can be expressed as a function of temperature

$$f_{cr3} = f(T). \tag{18}$$

VI. CONCLUSION

This article proposed a frequency-domain thermal model considering thermal coupling effect, which consists of Foster *RC* networks for describing temperature behaviors and LPFs for describing heat flow behaviors. This model was derived from the discovery that LPF characteristics of heat flow in frequency domain are only related to the distance between the junction node to case node. The major benefit of proposed method is that the modeling and characterization process is relatively simple compared with existing methods. Furthermore, this proposed thermal model can be easily implemented in electrothermal simulation because of its simple structure, and the calculated results are accurate in multitimescales, as verified by experiments.

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