Fabrication Tradeoff Based Optimal Synthesis of Winding Configurations for Planar Transformer in *CLLC* DC–DC Converter

Ashwin Chandwani, *Student Member, IEEE*, and Ayan Mallik, *Senior Member, IEEE*

***Abstract*—Adhering to the objective of modeling and selecting the most optimal winding configuration for a high-frequency planar transformer (HFPT) for auxiliary charging systems for more electric aircrafts, this article elucidates numerous fabrication and design-based constraints and correlations to enable parametric modeling of various magnetic components. Instead of providing generalized solutions, this article thoroughly characterizes all possible winding configurations for HFPT employed in a bidirectional *CLLC* dc/dc converter. A detailed analytical study is presented for each component and verified using several instances of three-dimensional finite-element analysis based model to synthesize the effective field and current density distribution in the windings. Several design-based tradeoffs are graphically explained with various criteria pertaining to optimal winding selection to study the interdependence of the resultant parameters on hardware specifications, such as the printed circuit board (PCB) thickness and its fabrication layout, air gaps, and conductor thickness. The article presents a comprehensive comparison between the analytical, simulation, and experimental analysis that portrays a strong agreement between these models with an average mismatch of up to 6.2%. An experimental prototype of *CLLC* converter rated for 1 kW nominal power, operating at 500 kHz resonant frequency, is developed with the optimal HFPT characteristics that yields a peak efficiency of 98.49% with magnetics stage efficiency of 99.31%.**

***Index Terms*—Finite-element analysis (FEA), interleaved windings, planar transformer, stray capacitance.**

I. Introduction

HIGH-FREQUENCY isolated resonant converters have found widespread application in the field of electric vehicle (EV) charging and aircraft power supplies due to their higher power density and superior conversion efficiency [1]. Specific applications include auxiliary power units (APU) used in more electric aircrafts (MEA) that use fuel-cell-based system at 400–600 V dc [2] to serve battery loads at 24–28 V dc voltage levels at low load conditions. These battery loads also support the main supply during heaving loading conditions, thus raising the demand for bidirectional power flow [3]. In that context, bidirectional *CLLC* resonant converter topology has proved to provide various advantages, such as reduced losses due to soft switching in the primary bridge [4] and synchronous rectification (SR) in the secondary bridge [5], and no-load voltage regulation and wider gain range over narrow frequency modulation zone [6]. Further, in such applications, high-frequency planar transformers (HFPTs) have found wide acceptance due to their advantages pertaining to lower profile, increased reliability, and modularity [6]. However, these advantages can only be redeemed by precise design and analysis of the equivalent parameters based on the physical design of the transformer winding arrangement [7], to obtain the desired gain characteristics, yet achieving the targeted efficiency and power density.

Several articles have been published in the literature that provide detailed analysis on modeling the HFPT focusing on the aspects of reduced winding losses with interleaved arrangement [8], issues pertaining to electromagnetic interference (EMI) occurring due to stray capacitances and ways to reduce them [9], [10]. The work presented in [11] focuses on the concept of paired interleaved windings that explains its implications related to reduced stray capacitance. It explains the tradeoffs of having minimized overlapping of conductors to reduce the stray capacitance with the variation in winding resistance on account of skewed conductor placement (referred to as "alternating winding layout"), affecting the MMF distribution. Several winding configurations are proposed and tested with a target of achieving minimized winding capacitances to mitigate corresponding EMI noise. A detailed design-based tradeoff analysis is presented in [12] with elaborate justification and verification of the HFPT components. The article focuses on characterization of stray capacitances by analyzing the electric field between two consecutive layers in a printed circuit board (PCB). Based on the formulated electric field between two overlapping conductors in two consecutive layers and corresponding voltage gradient, the effective winding capacitance is calculated. However, all the abovementioned works portray a generalized model to characterize the HFPT with assumptions pertaining to uniform winding arrangements. Due to these assumptions, the correlations between the obtained equivalent parameters with the physical constraints of a PCB such as its thickness and corresponding insulation layer distribution, air gaps, and the conductor trace thickness remain unexplored.

Manuscript received 31 May 2022; revised 9 October 2022; accepted 26 January 2023. Date of publication 31 January 2023; date of current version 10 March 2023. Recommended for publication by Associate Editor O. Onar. *(Corresponding author: Ayan Mallik.)*

The authors are with the Power Electronics and Control Engineering Laboratory, Ira A. Fulton School of Engineering, Arizona State University, Mesa, AZ 85212 USA (e-mail: avchandw@asu.edu; ayan.mallik@asu.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3241135.

Digital Object Identifier 10.1109/TPEL.2023.3241135

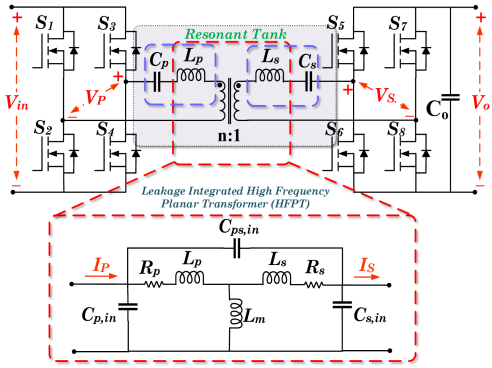

Fig. 1. *CLLC* topology with zoomed in lumped magnetic model.

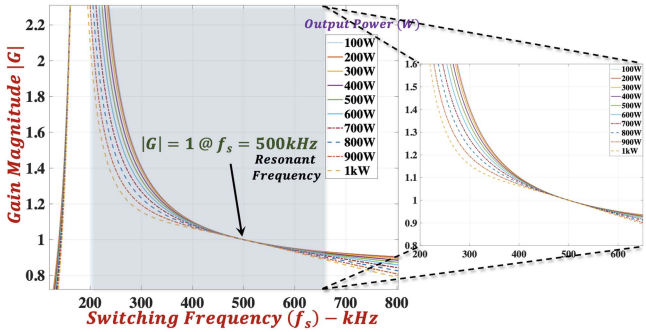

Fig. 2. Voltage gain versus frequency trend of the designed *CLLC* converter.

Considering the above limitations, the major technical contributions of this article complementing the previous article presented in [13] are as follows: 1) practical and realistic characterization of the leakage inductance, and stray capacitance of a HFPT accounting for various intricate fabrication-based nonideal considerations and their effect on the system performance, 2) graphically elucidated parametric tradeoffs and guidelines related to conductor and insulator selection employed for HFPT realization, 3) defining soft-switching-based design and implementation constraints pertaining to optimal winding structure selection criteria, and 4) thorough comparison of the analytically derived model, with three-dimensional (3-D) finite-element analysis (FEA) based simulations and experimental analysis.

The rest of this article is organized as follows: Section II introduces the lumped model for HFPT employed in a *CLLC* converter and explains the deviation in the resultant gain caused due to the stray elements. Further, a comprehensive analysis to provide parametric modeling of HFPT is presented in Section III with detailed characterization in context to the fabrication aspects of HFPT. Section IV elucidates the tradeoffs between various winding configurations and provides analysis to optimally choose the winding configuration pertaining to design and operational constraints of the *CLLC* converter. Section V provides experimental justification with relevant results to benchmark the performance of the developed experimental prototype of *CLLC* converter rated for 1 kW nominal power. Section VI points out the conclusive points with relevant discussions.

II. Comprehensive Lumped *R-L-C* Model of HFPT

Fig. 1 describes the lumped model for a leakage integrated HFPT implemented in a bidirectional *CLLC* dc/dc converter topology. As observed, L_m signifies the magnetizing inductance of the HFPT, while the leakage inductances obtained in the primary and secondary windings (L_p and L_s, respectively) are coupled with resonant capacitors (C_p and C_s) with a resonant frequency f_r. Additionally, as the topology is intended to run at high switching frequency (f_s), there exist significant components of winding resistances R_p and R_s corresponding to the primary and secondary side, respectively. Further, due to potential difference between the winding layers and various turns, stray inter and intrawinding capacitances are formed, that appear as shunt elements. $C_{P\text{in}}$ and $C_{S\text{in}}$ represent the equivalent intrawinding capacitances appearing in the primary and secondary windings, respectively, while $C_{PS\text{in}}$ corresponds to the equivalent interwinding capacitance between the two sets of windings. Due to the stray components appearing in the equivalent HFPT model, the converter tends to shift from its normal operating gain curve obtained using the generalized harmonic approximation (GHA) based model [5]. Thus, to minimize the deviation from the predicted gain curve and effectively reduce the losses in the transformer, it is important to analyze and model each component and study its dependence on the fabrication aspects of the transformer.

III. Mathematical Modeling and Analysis of HFPT Parameters

Referring to the APU-based application of (400–600 V) to (24–28 V) conversion, a turns ratio (n) of 22:1 is selected based on the tradeoffs between the core loss and winding loss to adhere to the unity nominal gain requirement of the *CLLC* converter resulting in efficient voltage regulation [14]. Fig. 2 shows the voltage gain magnitude versus the switching frequency (f_s) trend of the designed *CLLC* converter for the design specifications mentioned in Table VII. As observed, for a design gain range from $G = 0.88$ (for $600 - 24$ V conversion) to $G = 1.54$ (for $400 - 28$ V conversion) corresponding to the corner operating conditions, with the selected turns ratio and resonant tank parameter selection, the gain modulation is seamlessly achieved by varying the operational frequency between 200 and 650 kHz.

Corresponding to the selected n, the number of turns selected in each multilayer PCB are selected as per interconnecting and packaging electronic circuits (IPC) 2221 standard [15] that provides the minimum copper conductor width required to ensure the desired current flow for a defined copper conductor thickness adhering to a maximum temperature rise limit in the winding. The empirical formula to corelate the conductor width required with respect to temperature rise is shown as follows:

$$A_c = \frac{I_c}{(k \times \Delta T^b)^{\frac{1}{c}}}. \tag{1}$$

Using the area of the conductor calculated by (1), the width of the conductor is obtained as follows:

$$w_c = \frac{A_c}{h_t \times 1.378} \tag{2}$$

where A_c is the area of the conductor in $mils^2$, w_c is the conductor width in *mils*, I_c is the current in the conductor in amperes, ΔT is the temperature rise in °C, and h_t is the thickness of the conductor used in ounces (oz.) of copper. The empirical constants k, b, and c are obtained from curve fitting to the IPC 2221 current carrying standard curves and the numerical values are shown as follows: For external layers: $k = 0.048$, $b = 0.44$, and $c = 0.725$, while for the internal layers: $k = 0.024$, $b = 0.44$, and $c = 0.725$. Further, the spacing between the windings are decided by the voltage gradient between the two windings to ensure desired creepage to prevent any potential turn-to-turn short circuit.

To elucidate further, an analytical formulation for primary winding configuration is shown that depicts the maximum and minimum number of windings in the external and internal layers adhering to the specifications shown as follows:

1) Magnetic core—FR45810EC planar ferrite core.
2) Window width $(b_t) - 21.4\,\text{mm} \rightarrow 20\,\text{mm}$ (clearance from the core edges 0.7 mm each side).
3) $I_p\,(\text{max}) = 10\,\text{A}$.
4) Selected conductor thickness $(h_t) - 2\,oz.$ copper.
5) Temperature rise (ΔT) limited to 40 °C.

With h_t defined as 2 oz., the minimum conductor width (w_{ce}) for external layers is 1.76 mm (selected to be 2 mm for safety margin) and that for internal layers (w_{ci}) is 3.49 mm (selected to be 3.75 mm for safety margin). Additionally, corresponding to per-turn voltage gradient ($\frac{V_p}{N} = \frac{600}{22} = 27$ V), the safe creepage between the windings is selected to be 0.5 mm for external layers (c_e) and 0.25 mm for internal layers (c_i).

Using the specifications for the winding thicknesses, the maximum number of turns in external layers $(N_{e,\max})$ can be derived as follows:

$$b_t = N_{e,\max} \times w_{c_e} + (N_{e,\max} - 1) \times c_e \tag{3}$$

$$20\text{mm} = N_{e,\max} \times 2\text{mm} + (N_{e,\max} - 1) \times 0.5\text{mm} \tag{4}$$

$$N_{e,\max} = 8.2 \sim 8. \tag{5}$$

As seen in (5), the maximum number of turns in external layer $(N_{e,\max})$ is limited to 8.

Similarly, for internal layers, the maximum number of turns in internal layers $(N_{i,\max})$ can be derived as follows:

$$b_t = N_{i,\max} \times w_{c_i} + (N_{e,\max} - 1) \times c_i \tag{6}$$

$$20\text{mm} = N_{i,\max} \times 3.75\text{mm} + (N_{i,\max} - 1) \times 0.25\text{mm} \tag{7}$$

$$N_{i,\max} = 5.06 \sim 5. \tag{8}$$

As seen in (8), the maximum number of turns in internal layer $(N_{i,\max})$ is limited to 5.

Using the abovementioned information, three noninterleaved winding configurations are studied in this article (explained in Table I). In addition to that, to explain the *R-L-C* modeling of an interleaved structure, one example of eight layers {7P-1S*-1S*-4P-4P-1S*-1S*-7P}configuration is also explained.

TABLE I
WINDING CONFIGURATIONS UNDER STUDY

No.	No. of Layers per winding	Primary Winding (series)	Secondary Winding (*Layers are connected in parallel)	Turns Ratio
1	4 layers	8P-3P-3P-8P	1S*-1S*-1S*-1S*	22:1
2	4 layers	7P-4P-4P-7P	1S*-1S*-1S*-1S*	
3	4 layers	6P-5P-5P-6P	1S*-1S*-1S*-1S*	
4	8 layers	Interleaved: 7P-1S*-1S*-4P-4P-1S*-1S*-7P (*Layers 2,3,6,7 are connected in parallel)		

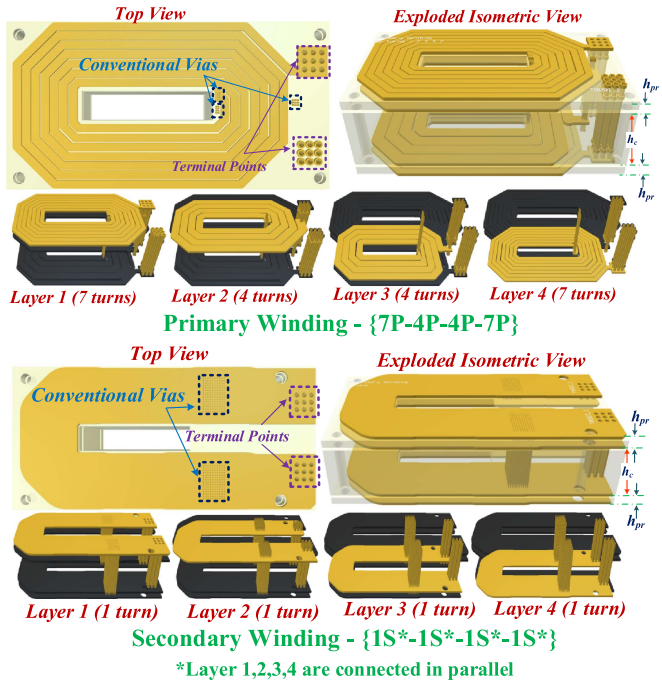

Fig. 3. PCB winding arrangement for noninterleaved {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} configuration.

As observed in Table I, for the noninterleaved winding configurations, the 4-layer primary winding consisting of 22 turns is realized using different number of turns in each layer. The winding structure and its PCB layout design for one such noninterleaved configuration {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} is shown in Fig. 3. As observed, the nomenclature of the primary winding: 7P-4P-4P-7P denotes that seven turns of primary (P) winding are placed in the first layer, followed by four in the second layer, four in the third layer, and the rest seven turns in the fourth layer. The insulation between the copper layers is enabled by the prepreg and core layer of thicknesses h_{pr} and h_c, respectively. Further, the transition from one layer to the next one is realized using conventional vias in the PCB, with their hole dimensions matching the current carrying requirements of the windings as per IPC 2221. Similarly, arrangement is observed for the other two noninterleaved winding configurations with different number of turns in each of the PCB layer. The secondary winding in the noninterleaved configurations is designed to portray a single

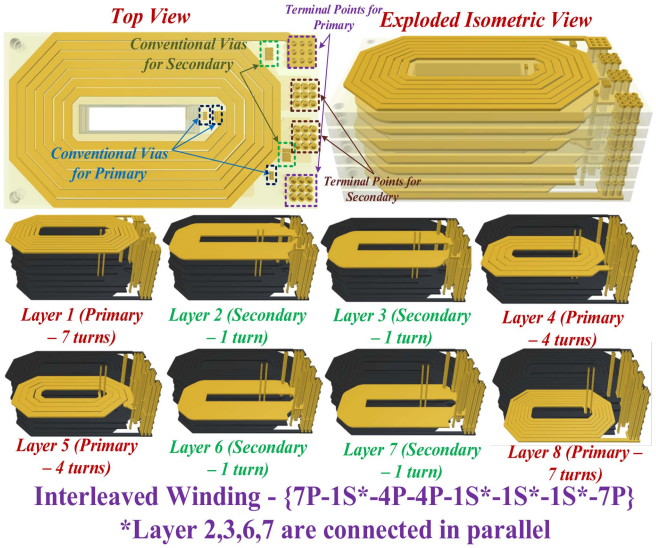

Fig. 4. PCB winding arrangement for interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) configuration.

turn, which is realized using one turn in each of the four layers and using vias at the winding terminals to effectively connect them in parallel. The nomenclature 1S*-1S*-1S*-1S* (*layers are connected in parallel) is used to highlight the parallel connection of the four layers, thus only extracting a single equivalent turn from a four-layer PCB. In addition to that, Fig. 4 shows the winding configuration of the interleaved winding structure. As observed, the notation for interleaved winding configuration (as seen in Table I) corresponds to an eight-layer PCB denoted as 7P-1S*-1S*-4P-4P-1S*-1S*-7P. In this case, the PCB winding assembly is realized using seven turns of primary winding in the first layer, followed by four turns of primary winding in the fourth layer, four turns in the fifth layer, and finally seven turns in the eighth layer, all connected through conventional vias. The secondary winding is realized using single turn in second, third, sixth, and seventh layer, all connected in parallel through vias at their terminal points to realize one turn in the secondary winding.

The respective 2-D (front view) illustrations of the winding configurations mentioned in Table I are shown in Fig. 5. Corresponding to the winding configurations as shown in Fig. 5, this section characterizes the transformer components in detail and provides detailed tradeoffs pertaining to design and fabrication-based aspects by analyzing the model through 3-D FEA simulations and analysis.

A. Modeling and Controllable Synthesis of Leakage Inductance

Several studies have emphasized on the modeling and controllable reduction of leakage inductance focusing on the winding arrangement and interleaved structure [11], [12]. However, with an objective to attain minimized switching losses (through zero-voltage switching (ZVS)) and yet achieve the required gain, this subsection focusses on the fabrication-based tradeoffs and elucidates the dependencies on various factors pertaining to the orientation of the winding structures.

The configurations mentioned in Table I are assembled using EE type of ferrite core, as observed in Fig. 6. To implement a leakage integrated HFPT design, an air gap (h_g) (as seen in Fig. 6) is introduced between the cores, intentionally leading to flux leakage from the core with the return path through the gap, winding layers, and the insulation layers. Based on this structure, as explained in [13], the magnetic energy (E_k) associated with the leakage flux is used to analytically formulate the leakage inductance, highlighting its dependency on the conductor thickness and insulator between them as follows:

$$E_k = \frac{\mu_o}{2} \sum \int_0^{h_t} H^2 l_t b_t dl = \frac{1}{2} L_k I_k^2;\ k \in \{P, S\} \tag{9}$$

where μ_o represents the permeability of the core, H denotes the field strength, which is formulated by the ampere turns linked, l_t is the length of each winding, b_t is the window width of the core, and h_t is the thickness of the conductor. Further, dl is the incremental thickness situated at a distance of l from the inner surface of the conductor, as observed in Fig. 5. Referring to (9), (10)–(12) elucidate the formulation of the magnetic energy corresponding to the primary winding, secondary winding, and the air gap, respectively, for a noninterleaved {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} winding configuration

$$\begin{aligned} E_P = \frac{\mu_o}{2} l_t b_t \Bigg[& 22 \int_0^{h_t} \left(\frac{I_P l}{b_t h_t}\right)^2 dl + \left(\frac{7 I_P}{b_t}\right)^2 \\ & \times (h_t + h_{pr} + h_\Delta) + \left(\frac{11 I_P}{b_t}\right)^2 (h_t + h_c + h_\Delta) \\ & + \left(\frac{15 I_P}{b_t}\right)^2 (h_t + h_{pr} + h_\Delta) \\ & + \left(\frac{22 I_P}{b_t}\right)^2 (h_t + h_\Delta) \Bigg] \end{aligned} \tag{10}$$

$$\begin{aligned} E_S = \frac{\mu_o}{2} \frac{l_t b_t}{n^2} \Bigg[& 22 \int_0^{h_t} \left(\frac{I_P l}{b_t h_t}\right)^2 dl + \left(\frac{22 I_P}{b_t}\right)^2 (h_t + h_\Delta) \\ & + \left(\frac{\frac{33}{2} I_P}{b_t}\right)^2 (h_t + h_{pr} + h_\Delta) + \left(\frac{11 I_P}{b_t}\right)^2 \\ & \times (h_t + h_c + h_\Delta) + \left(\frac{\frac{11}{2} I_P}{b_t}\right)^2 (h_t + h_{pr} + h_\Delta) \Bigg] \end{aligned} \tag{11}$$

$$E_{\text{lk,air}} = \frac{\mu_o}{2} l_t b_t \left[\left(\frac{22 I_P}{b_t}\right)^2 (h_\Delta) \right]. \tag{12}$$

Further, analytical expressions corelating the leakage inductances for the four winding structures with the conductor and PCB insulator thickness (h_{pr} : prepreg layer and h_c : core layer) are shown in Table II.

Referring to the interdependency of the leakage inductances on the structural arrangement and related hardware specifications of the windings, the designer has the flexibility to obtain the

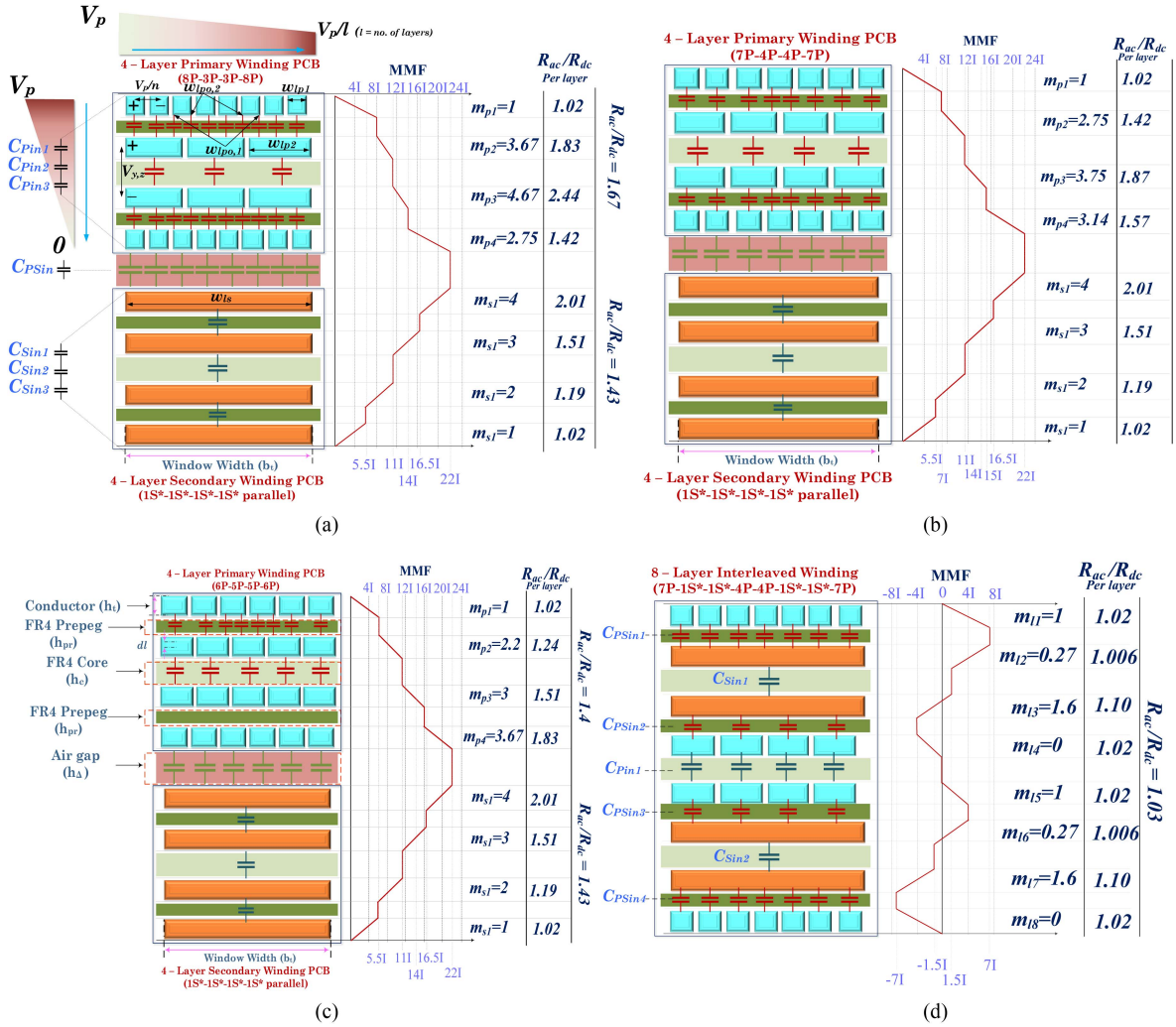

Fig. 5. Structural winding configurations with respective MMF distributions for (a) primary: 8P-3P-3P-8P (series); secondary: 1S*-1S*-1S*-1S*(parallel); (b) primary: 7P-4P-4P-7P (series); secondary: 1S*-1S*-1S*-1S*(parallel); (c) primary: 6P-5P-5P-6P (series); secondary: 1S*-1S*-1S*-1S*(parallel) configurations with 4-layer PCB; and (d) interleaved winding configuration: 7P-1S*-1S*-4P-4P-1S*-1S*-7P with eight-layer PCB.

TABLE II
LEAKAGE INDUCTANCE ANALYTICAL MODEL FOR WINDING CONFIGURATIONS UNDER STUDY

Winding Configuration	Primary Leakage Inductance (L_p) =	Secondary Leakage Inductance (L_s) =	Leakage in the air gap between the windings =
{8P-3P-3P-8P}, {1S*-1S*-1S*-1S*}	$\frac{\mu_o l_t}{b_t}\left[\frac{2617}{3}h_1 + 260h_{pr} + 121h_c + 865h_\Delta\right]$	$\frac{\mu_o l_t}{n^2 b_t}\left[\frac{2745}{3}h_1 + \frac{605}{2}h_{pr} + 121h_c + \frac{1815}{2}h_\Delta\right]$	$\frac{\mu_o l_t}{b_t}\left[484h_\Delta\right]$
{7P-4P-4P-4P}, {1S*-1S*-1S*-1S*}	$\frac{\mu_o l_t}{b_t}\left[\frac{2659}{3}h_1 + 274h_{pr} + 121h_c + 879h_\Delta\right]$		
{6P-5P-5P-6P}, {1S*-1S*-1S*-1S*}	$\frac{\mu_o l_t}{b_t}\left[\frac{2713}{3}h_1 + 292h_{pr} + 121h_c + 897h_\Delta\right]$		
Interleaved {7P-1S*-1S*-4P-4P-1S*-1S*-7P}	$\frac{\mu_o l_t}{b_t}\left[\frac{217}{3}h_1 + 65h_{pr}\right]$	$\frac{\mu_o l_t}{b_t}\left[\frac{461}{6}h_1 + 65h_{pr} + \frac{18}{4}h_c\right]$	N/A

required leakage varying the air gap (h_Δ). Further, the leakage inductances also depend on the thickness of the conductor (h_1) used for the PCB fabrication that typically ranges between 35 to 140 μm corresponding to 1 to 4 oz. of copper. To elucidate this dependency, Fig. 7 portrays a plot of different values of leakage inductances obtained from 3-D FEA simulations for the abovementioned four winding configurations. As observed, due to increased flux leakage with increasing values of air gap between the winding, the resultant leakage inductances also see a linear rise. In case of interleaved winding structure, due to absence of airgap between the two windings, the leakage inductance depends only the conductor thickness, which results

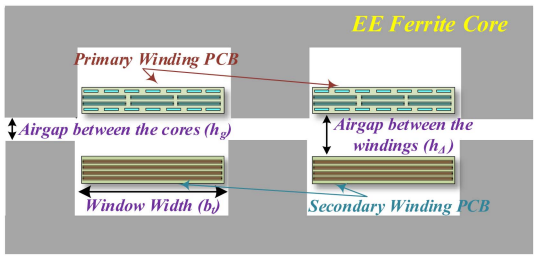

Fig. 6. Arrangement of transformer windings in EE ferrite core assembly.

in a linearly increasing trend—matching well with the derived analytical expressions (as shown in Table II).

Furthermore, as observed in Table II, the effective value of leakage inductance also depends on the arrangement, width, and thickness of the insulators used for PCB fabrication. This aspect generally depends on the PCB manufacturing capabilities and is defined according to the thickness of the fabricated PCBs [16]. The variation of the obtained leakage inductances with {[8P-3P-3P-8P],[1S*-1S*-1S*-1S*]}configuration fabricated using various PCB thicknesses (t) and corresponding thickness of insulation layers (h_{pr} and h_c) for a typical four-layer PCB is illustrated in Fig. 8. Please note that the solid lines show the trend of L_P and $L_S$with respect to variation in h_{pr}, while the dotted lines show the variation with respect to h_c. Further, it is worthwhile to point out that the flexibility provided due to the variation in h_{pr}, h_c, and h_t is limited to the design phase of the PCB windings. Once the PCBs are fabricated, the control parameter to tightly modulate the leakage inductances is limited to h_Δ only.

As seen in the above analysis, the leakage inductance obtained using interleaved winding is considerably smaller than that with noninterleaved winding. This is because the magnetic energy linked to leakage flux is significantly lesser due to absence of interwinding air gap, leading to better flux linkage between the windings and the core. In that context, Fig. 9 compares the MMF distribution and field linkage of each layer of noninterleaved {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} and interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) winding structures, obtained through 3-D FEA simulations. Relating these results to the MMF distribution shown in Fig. 9, the resultant magnitude of H (A/m) is found to be increasing while moving from the primary layer-1 toward the air gap, reaching its peak for primary layer-4 and secondary layer-1, and consequently reducing at secondary layer-4. With all the abovementioned considerations, the optimal selection of fabrication parameters depends on the ZVS criteria and the application specific voltage gain requirement, which are covered in Section IV.

B. Stray Capacitance Modeling

As explained in Section II, the switching performance of the *CLLC* resonant converter majorly degrades due to presence of inter and intrawinding capacitances in the HFPT. Several techniques have been discussed in the literature that focus on modeling these stray capacitances to enhance the EMI performance and voltage regulation of the converters under various loading conditions [11]. However, all the works have presented a generalized analysis to model these capacitors, with several assumptions pertaining to nonuniformity in the PCB insulation layers and winding configurations. For example, Saket et al. [11] considered the overlapping area for all the capacitors to be equal with equal spacing between the two layers. However, as observed in Fig. 5, generally the winding arrangement dictates the resultant stray capacitance with varying winding widths adhering to PCB fabrication standards. Thus, with an intent to provide intricate modeling while accounting for the winding arrangement, insulation thickness, overlapping area, and voltage gradient between the conductors, this section provides a detailed model to formulate the stray capacitances appearing in the primary and secondary windings.

Fig. 5(a) shows the voltage distribution of primary winding of {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} winding configuration. The potential across the winding is assumed to vary linearly with the turns. Thus, the potential at each turn of the winding (V_y) can be written as

$$V_y = \frac{(n+1)-y}{n} V_p; y \in \{1, 2, 3, \ldots, n\} \tag{13}$$

where n is the number of turns in the winding and V_p is the primary voltage excitation. Thus, a voltage gradient ($V_{y,z}$) exists between the two adjacent windings and the windings in two adjacent layers, which essentially leads to formation of virtual capacitors. This capacitance ($C_{y,z}$) can be formulated by analyzing the overlapping conductor area and the distance between the two subsequent conductors as follows:

$$C_{y,z} = \frac{\varepsilon_o \varepsilon_r S_{y,z}}{d} \tag{14}$$

where ε_o and ε_r denote the permittivity of air and relative permittivity of the dielectric material, respectively, $S_{y,z}$ is the overlapping area between turns y and z as observed in (14), and d denotes the spacing between the two conductors

$$S_{y,z} = \int_0^{l_t} w_o dl \tag{15}$$

where w_o is the overlapping conductor width and dl_t represents an infinitesimally small sectional length of a turn, which is integrated over the entire circumference to form a complete turn of length l_t.

Referring to Fig. 10, since the overlap area ($\int_0^{l_t} h_1 dl$) between the two turns is very small with air (distance between the conductors: h_{is}) being the dielectric medium between them, the turn-to-turn capacitance is negligible, and thus, its effect can be ignored. On the other hand, the capacitance between adjacent layers can be formulated by analyzing the total energy associated with the electric field between the two layers

$$E_l = \sum_{l=1}^{l_n} \frac{1}{2} [C_{y,z} V_{y,z}^2]_{\text{layer}} \tag{16}$$

$$E_{l_t} = \sum_{l=1}^{l_n} E_l \tag{17}$$

where $V_{y,z}$ is the potential difference between two conductor surfaces and E_l denotes the total energy in a layer l.

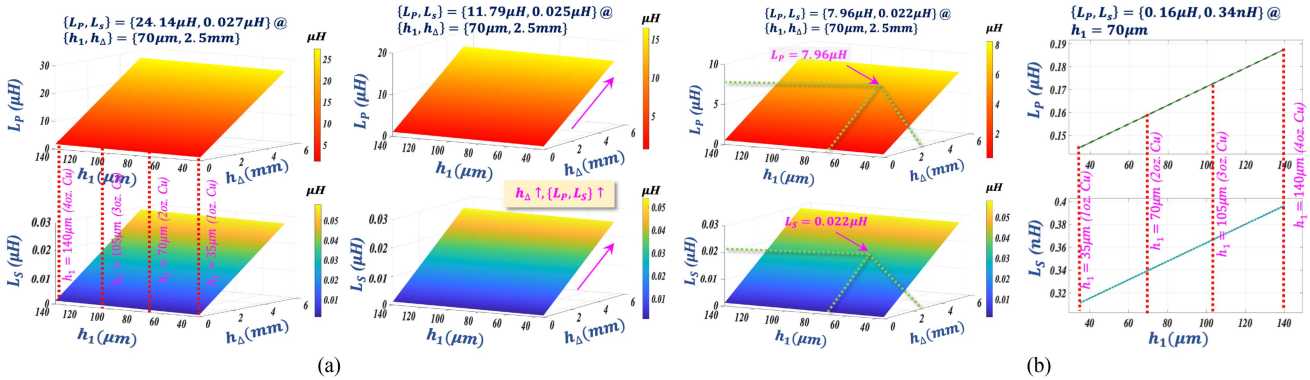

Fig. 7. (a) 3-D plot comparing resultant leakage inductances for different h_1 and h_Δ for noninterleaved winding configurations. (b) Plot corelating leakage inductances for different h_1 for interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P} configuration.

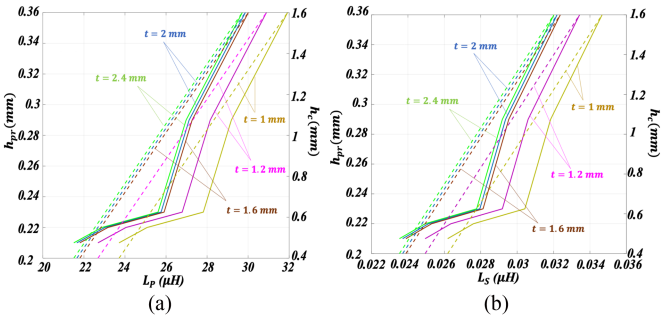

Fig. 8. Plots explaining the relation between (a) $L_P$and (b) L_S for different h_{pr} and h_c corresponding to different PCB thicknesses for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} winding configuration.

Thus, using (16)–(17), the effective inter or intrawinding capacitance can be formulated as

$$C_{in} = \sum_{t=1}^{l_t(\text{no. of layers})} \frac{2E_{l,t}}{V_{y,z}^2}. \tag{18}$$

Referring to Fig. 5(a), the intrawinding capacitance between first and second layer ($C_{P\text{in},1}$) is similar to that of between third and fourth layer ($C_{P\text{in},3}$) and can be formulated as

$$C_{p\text{in},1} = \frac{\varepsilon_o \varepsilon_r}{h_{pr}} \left[6w_{w_{l_{p1}}} + 2w_{l_{Po,1}} + 2w_{l_{Po,2}}\right] \int_0^l dl = C_{p\text{in},3}. \tag{19}$$

Similarly, the intrawinding capacitance between second and third layer of primary PCB is formulated as

$$C_{p\text{in},2} = \frac{\varepsilon_o \varepsilon_r}{h_c} \left[3w_{l_{p2}}\right] \int_0^l dl. \tag{20}$$

All three capacitances are in parallel and thus can be added to formulate the overall primary intrawinding capacitance

$$C_{P\text{in}} = C_{p1} + C_{p2} + C_{p3}. \tag{21}$$

Similarly, the intrawinding capacitance for the secondary winding can be formulated as

$$C_{\text{sin},1} = C_{\text{sin},3} = \frac{\varepsilon_o \varepsilon_r}{h_{pr}} w_{l_s} \int_0^l dl \tag{22}$$

$$C_{\text{sin},2} = \frac{\varepsilon_o \varepsilon_r}{h_c} w_{l_s} \int_0^l dl \tag{23}$$

$$C_{\text{sin}} = C_{s1} + C_{s2} + C_{s3}. \tag{24}$$

Following the same method, the interwinding capacitance between primary and secondary board can be calculated as

$$C_{P\text{Sin}} = \frac{\varepsilon_o \varepsilon_r}{h_\Delta} \left[8w_{l_{p1}}\right] \int_0^l dl. \tag{25}$$

A comprehensive comparison of the analytical formulation to determine the inter and intrawinding capacitances for the four mentioned winding configurations referring to Fig. 5 is presented in Table III.

As observed in Table III, the capacitances depend majorly on the overlapping area of the windings, airgap between the windings, thickness of the insulation between the layers, and the length of a conductor turn. Out of the abovementioned factors, the overlapping area is dependent on the winding configuration and relevant works [9] have provided methods to reduce it by modifying the arrangement of turns. Further, the length of the conductor also depends on the core geometry, which solely depends on the application specifications. To elucidate the dependency of the inter and intrawinding capacitances on the insulator layer thicknesses, Fig. 11 shows the variation of intrawinding capacitances ($C_{P\text{in}}$ and $C_{S\text{in}}$) for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]}configuration, fabricated using various PCB thicknesses (t) with respect to change in h_{pr} and h_c, obtained through 3-D FEA simulations. Further, Fig. 12 shows the variation of interwinding capacitance for with respect to change in h_Δ for all the winding configurations. As observed, as the airgap increases, the interwinding capacitance observes a steep descent, and the trend becomes more flatter for higher values of airgap, which matches the analytical formulations presented in this section. Referring to the presented plots and analytical formulations shown in Table III, it can be deduced that reduction in the intrawinding capacitance can be achieved either by increasing the insulator thicknesses or by reducing the overlap area of the conductors in two consecutive layers, as demonstrated in [10]. Both of these aspects of stray capacitance reduction can

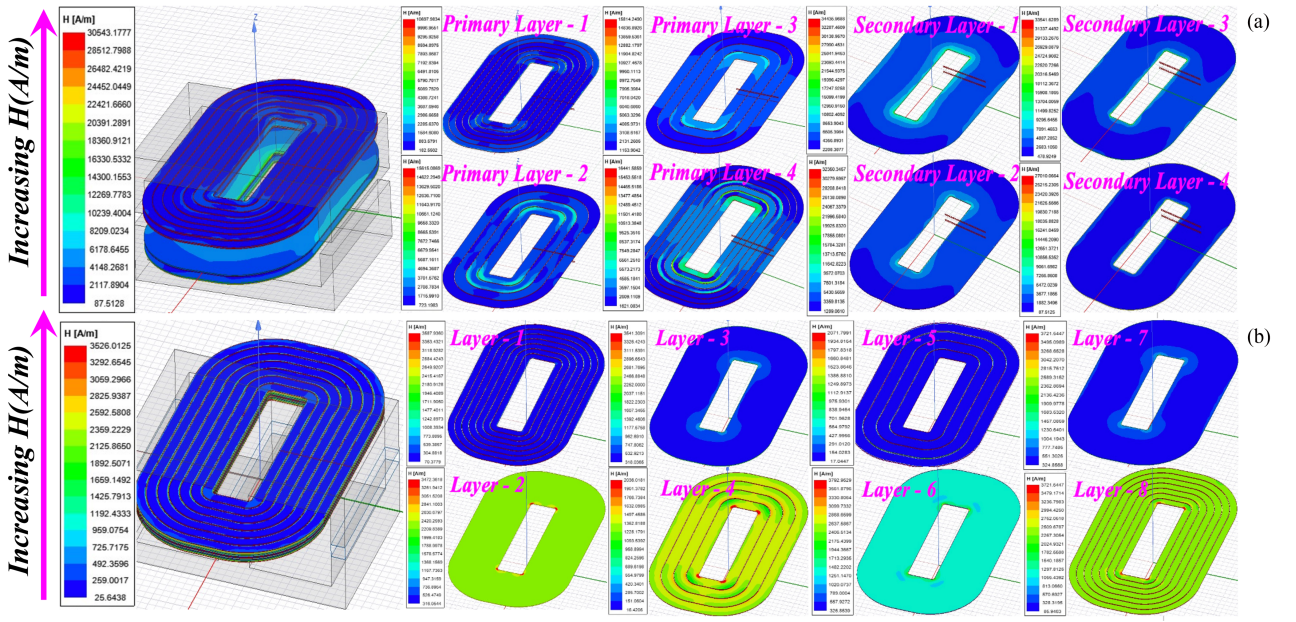

Fig. 9. MMF distributions obtained from 3-D FEA sim. for (a) {[8P-3P-3P-8P],[1S*-1S*-1S*-1S*]}winding configuration and (b) interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) configuration.

TABLE III
STRAY CAPACITANCE ANALYTICAL MODEL FOR WINDING CONFIGURATIONS UNDER STUDY

Winding Configuration	Primary Intra-winding Capacitance ($C_{P_{in}}$) =	Secondary Intra-winding Capacitance ($C_{P_{in}}$) =	Inter-winding Capacitance ($C_{PS_{in}}$) =
{8P-3P-3P-8P}, {1S*-1S*-1S*-1S*}	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[6w_{l_{p1}}+2w_{l_{po,1}}+2w_{l_{po,2}}\right]+\frac{\varepsilon_o\varepsilon_r}{h_c}\left[3w_{l_{p2}}\right]\right]\int_0^{l_t}dl$	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}w_{l_S}+\frac{\varepsilon_o\varepsilon_r}{h_c}w_{l_S}\right]\int_0^{l_t}dl$	$\frac{\varepsilon_o\varepsilon_r}{h_\Delta}[8w_{l_{p1}}]\int_0^{l_t}dl$
{7P-4P-4P-4P}, {1S*-1S*-1S*-1S*}	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[6w_{l_{p1}}+2w_{l_{po,1}}\right]+\frac{\varepsilon_o\varepsilon_r}{h_c}\left[4w_{l_{p2}}\right]\right]\int_0^{l_t}dl$		$\frac{\varepsilon_o\varepsilon_r}{h_\Delta}[7w_{l_{p1}}]\int_0^{l_t}dl$
{6P-5P-5P-6P}, {1S*-1S*-1S*-1S*}	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[4w_{l_{p1}}+2w_{l_{po,1}}+2w_{l_{po,2}}\right]+\frac{\varepsilon_o\varepsilon_r}{h_c}\left[5w_{l_{p2}}\right]\right]\int_0^{l_t}dl$		$\frac{\varepsilon_o\varepsilon_r}{h_\Delta}[6w_{l_{p1}}]\int_0^{l_t}dl$
Interleaved {7P-1S*-1S*-4P-4P-1S*-1S*-7P}	$\frac{\varepsilon_o\varepsilon_r}{h_c}[4w_{l_{p2}}]\int_0^{l_t}dl$	$\frac{2\varepsilon_o\varepsilon_r}{h_c}[w_{l_S}]\int_0^{l_t}dl$	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[4w_{l_{p1}}\right]+\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[4w_{l_{p2}}\right]\right]\int_0^{l_t}dl$

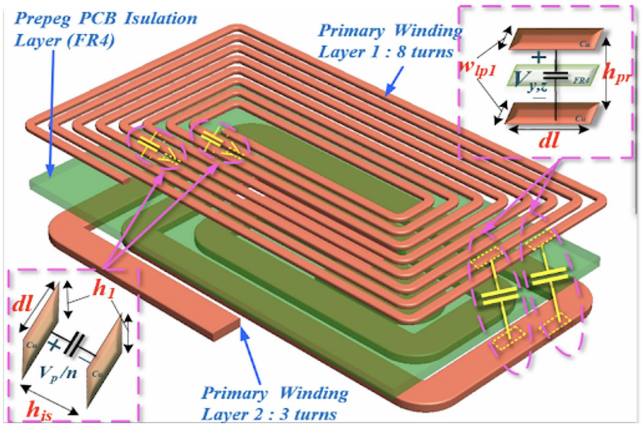

Fig. 10. Intrawinding capacitance model for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} winding configuration.

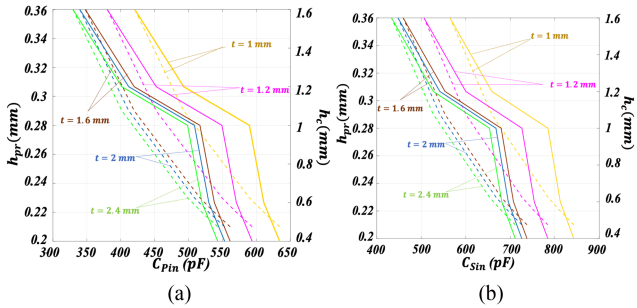

Fig. 11. Plots explaining the relation between (a) $C_{P_{\text{in}}}$ and (b) $C_{S_{\text{in}}}$ for different h_{pr} and h_c corresponding to different PCB thicknesses for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} winding configuration.

be exercised in the PCB design phase only. However, the interwinding capacitance can be reduced externally by increasing the airgap (h_Δ) between the windings in the postfabrication phase, adhering to the core dimensions.

IV. SELECTION OF OPTIMAL WINDING CONFIGURATION

As presented in the previous sections, the resultant values of leakage inductance and stray capacitances depend on the

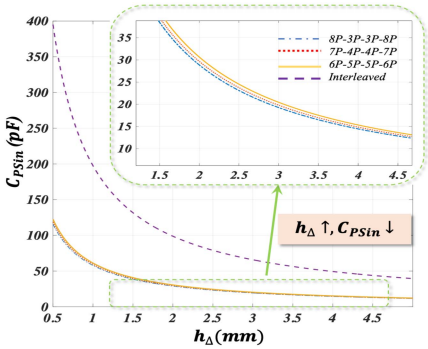

Fig. 12. Plots explaining the relation between $C_{PS_{\text{in}}}$ and air gap h_Δ.

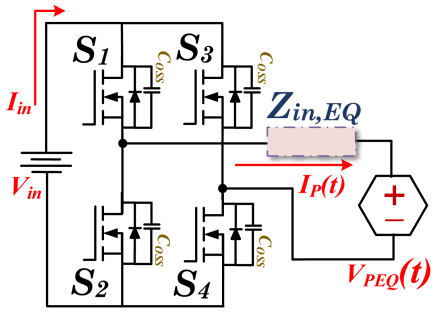

Fig. 13. Equivalent circuit for ZVS investigation.

winding orientation and corresponding PCB fabrication-based specifications. However, it is important to understand the implication of each configuration on the performance of the *CLLC* converter and understand the specifics behind choosing the most optimal one for enhanced efficiency and gain modulation. In that context, factors like ZVS criteria, winding losses, and its frequency dependency, resultant gain, and physical constraints play a major role, as described in this section.

Unlike a conventional *CLLC* converter model, where a lagging phase of primary current along with sufficient dead-time intervals is sufficient to ensure ZVS [17], [18], [19], the inclusion of nonidealistic components in the *CLLC* converter model requires detailed investigation for understanding the conditions for achieving ZVS. Here, the drain-to-source capacitance of the MOSFET (C_{oss}) necessitates constraints in the form of minimum equivalent impedance required to facilitate ZVS commutation. In that context, an equivalent model is developed to comprehensively analyze the ZVS constraints for different conditions for each switch of the primary bridge as shown in Fig. 13.

As observed in Fig. 13, $Z_{\text{in,EQ}}$ represents the equivalent input impedance of the *CLLC* converter, whereas $V_{\text{PEQ}}(t)$ represents the equivalent voltage source, both referred to the primary side. The equivalent topological structure of the *CLLC* converter with the inclusion of parasitics is shown in Fig. 14 obtained by reconfiguring the stray capacitance as a single lumped capacitance referred to the primary side [11], [20]. The equivalent

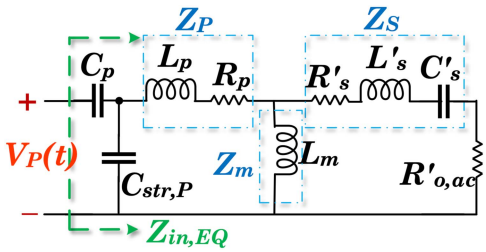

Fig. 14. Equivalent circuit with reconfigured stray capacitors.

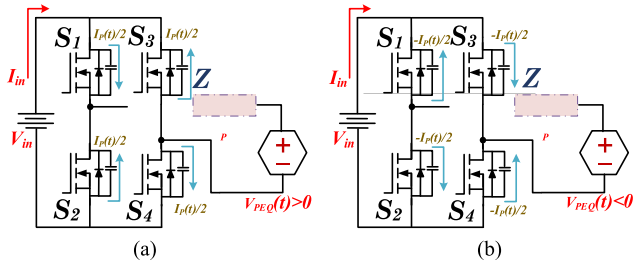

Fig. 15. ZVS turn ON cases (a) for switch S_2 and S_3 and (b) for switch S_1 and S_4.

value of $C_{\text{str,P}}$ can be formulated as follows:

$$C_{\text{str,P}} = C_{\text{pstr}} + C_{\text{sstr}}$$
$$= C_{\text{p,in}} + (1-n)\,C_{\text{ps,in}} + n^2 C_{\text{s,in}} - n\,(n-1)\,C_{\text{ps,in}}. \quad (26)$$

Utilizing the equivalent circuit shown in Fig. 14, the analytical formulation of $Z_{\text{in,EQ}}$ (27) shown at the bottom of this page, where $f = \frac{\omega}{\omega_r}$, $\omega_r = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}}$, $k_1 = \frac{L_m}{L_p}$, $k_2 = \frac{L_m}{L'_s}$, $m_1 = \frac{L_p}{R_p}$, $m_2 = \frac{L'_s}{R_{\text{seq}}}$, $m_3 = \frac{L_p}{R_T}$, $n_1 = \frac{C_{\text{str,P}}}{C_p}$, $R_{\text{seq}} = R'_{o,\text{ac}} + R'_s$, $R_T = R_p + R_{\text{seq}}$.

Further, following the derived equivalent circuit, the equivalent voltage $V_{\text{PEQ}}(t)$ can be derived as follows:

$$V_{\text{PEQ}}(t) = V_s(t)\left[\frac{Z_m\left(Z_{C_{\text{str,P}}} + Z_{C_P}\right)}{\left(Z_P + Z_{C_{\text{str,P}}}\right)\left(Z_m + Z_S\right)}\right]. \quad (28)$$

Referring to the equivalent circuit shown in Fig. 13, two commutation cases can be studied to examine the constraint for the value of L_p required to achieve ZVS as follows:

1) When switch S_2 and S_3 turn ON ($I_P(t) > 0$); as shown in Fig. 15(a).
2) When switch S_1 and S_4 turn ON ($I_P(t) < 0$); as shown in Fig. 15(b).

As the equivalent port voltage follows half wave symmetry, the condition $V_{\text{PEQ}}(t) = -V_{\text{PEQ}}(\pi + t)$ is implied. Thus, the analysis for both the cases proves to be similar for formulating the necessary constraint for ZVS. Focusing on the formulation for case (a) (for S_2 and S_3), the energy sunk by the sources can

$$Z_{\text{in,EQ}} = \frac{\left\{(1-f^2-f^2k_2)(1-f^2C-f^2)+f^2k_1(1+C)\left(\frac{f^2}{\omega}-1\right)-\frac{f^4}{m_2}(1+C)\left(\frac{1}{m_1}+\frac{1}{\omega}\right)\right\}+j\left\{f^2(1-f^2)\frac{(1+n_1)}{\omega m_1}-f^4k_2\frac{(1+n_1)}{\omega m_3}-\frac{f^2}{\omega m_2}\right\}}{\left\{\frac{f^6n_1}{\omega^2L_p}\left(\frac{1}{m_1}+\frac{k_2}{m_3}\right)-\frac{f^4}{\omega^2L_p}\left(\frac{n_1}{m_1}+\frac{1}{m_2}\right)\right\}-j\left\{\frac{f^6n_1}{\omega m_2L_p}\left(\frac{1}{m_1}+\frac{1}{\omega}\right)-\frac{f^4}{L_p}\left(1-\frac{n_1k_1}{\omega}\right)-\frac{f^2}{\omega L_p}(1-f^2-f^2k_2)(1-f^2n_1)\right\}} \quad (27)$$

TABLE IV
MINIMUM VALUE OF PRIMARY LEAKAGE INDUCTANCE REQUIRED TO ENSURE ZVS

No.	Winding Configuration	Minimum L_P required
	{8P-3P-3P-8P},{1S*-1S*-1S*-1S*}	22.15μH
	{7P-4P-4P-7P },{1S*-1S*-1S*-1S*}	11.08μH
	{6P-5P-5P-6P },{1S*-1S*-1S*-1S*}	9.72μH

be formulated as follows:

$$E_{\text{sunk}} = \int_0^{\tau_d} \left(V_{\text{PEQ}} I_P(\zeta) - V_{\text{in}} i_{\text{in}}(\zeta)\right) dt = \int_0^{\tau_d} \left(V_{\text{PEQ}} \left(-2C_{\text{oss}} \frac{dV_{\text{in}}}{dt}\right)\right) dt = 2C_{\text{oss}} V_{\text{in}} V_{\text{PEQ}}(\zeta) \tag{29}$$

where τ_d is the dead time provided to the switches. Further, the total energy in the switch remains constant during the commutation interval, which helps formulate the necessary constraint for ZVS for this case, as follows:

$$E_{\text{sourced}} \geq E_{\text{sunk}} = \frac{1}{2} |Z_{\text{in,EQ}}| I_P^2(\zeta) \geq 2C_{\text{oss}} V_{\text{in}} V_{\text{PEQ}}(\zeta). \tag{30}$$

Thus, using (30), the minimum impedance for $V_{\text{PEQ}}(\zeta) > 0$ can be analyzed as

$$|Z_{\text{in,EQ}}| \geq \left| \frac{4C_{\text{oss}} V_{\text{in}} V_{\text{PEQ}}(\zeta)}{I_{\text{P}}^2(\zeta)} \right| \tag{31}$$

where ζ is the turn ON instant of switch S_2 and S_3.

Solving the constraint in MATLAB for finding the constraints for L_P with respect to the magnitude of $Z_{\text{in,EQ}}$ for known values of other resonant tank parameters yields the minimum requirement of L_P for different winding configurations. To provide an instance of this evaluation, Table IV shows the formulated values of minimum L_p required to ensure ZVS for all noninterleaved winding configurations at 1 kW rated load.

In addition to that, for applications targeting high switching frequency similar to the proposed *CLLC* dc/dc converter topology, winding losses pertaining to the effective ac winding resistance are found to be significantly high due to eddy current and skin effects [11]. Further, the HFPTs used for resonant converters experience nonuniform current density due to variable switching frequencies leading to winding losses due to proximity effect. Conventionally, Dowell's equation [13], [21], [22], [23] is used to characterize the ratio of effective ac resistance with respect to dc resistance, adhering to the current density distortion due to skin and proximity effects. Additionally, as studied in [13], the effective winding resistance depends on the MMF distribution factor (m), skin depth (δ), and thickness of the conductor (h_t), all of which are decided during the design process of PCB without any scope of external modification following the PCB fabrication. It is also widely established in the literature [13] that the interleaved winding configuration results in significantly reduced effective winding resistances. As observed in Fig. 5, the effective ratio ($\left[\frac{R_{\text{ac}}}{R_{\text{dc}}}\right]_{\text{eff}}$) is 38.3% (avg.) lower than for the interleaved structure as compared to the other three winding arrangements resulting in minimum ac resistance. This concept is also verified by visualizing and comparing the current density distribution of {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} and interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) winding structures through 3-D FEA analysis, as shown in Fig. 16. As observed, the current density is higher near the edges for noninterleaved winding arrangements due to skin and proximity effects, which tend to distort the current distribution even further at higher frequencies, leading to higher winding losses.

Further, to adhere to the cost-effectiveness for fabrication, power density constraints, and the current carry capabilities, the conductor thickness is selected to be 2 oz. copper ($h_1 = 70\,\mu\text{m}$). Moreover, the air gap between the cores is selected to be 1.9 mm to obtain the required magnetizing inductance (L_m). Adhering to the supplementary ZVS criteria [17], [18], [19] of L_m with respect to the dead band time duration and maximum switching frequency for achieving the desired gain, the maximum value of L_m is formulated to be 76.26 μH.

With the mentioned design criteria, the GHA [24] based gain curves achieved for all four winding configurations are shown in Fig. 17(a). To adhere to the gain requirements, the relative variation of gain with frequency should follow: $\left[\frac{dG}{df}\right]_{\text{min}} \leq \frac{dG}{df} \leq \left[\frac{dG}{df}\right]_{\text{max}}$. The factor $\left[\frac{dG}{df}\right]_{\text{min}}$ is decided based on the gain range requirement, which depends on the Q factor selection for *CLLC* converter and its tradeoffs [25]. Lower $\left[\frac{dG}{df}\right]_{\text{min}}$ will lead to an operating range with higher switching frequencies, thus resulting in higher switching losses. On the other hand, higher $\left[\frac{dG}{df}\right]_{\text{max}}$ will lead to steeper gain curve, which might not be realizable by the frequency resolution (or least count) of the controller (TMS320F28379D) used for this application. To validate the accuracy and applicability of the analytical model, the resultant impedances for the primary (Z_P) and secondary (Z_S) side corresponding to all four fabricated windings structures are compared in Fig. 17(b).

Further, a detailed comparison of the resultant parameters obtained by simulation models and developed windings measured experimentally are shown in Table V. For measuring the *R-L-C* parameters, GWINSTEK LCR8101G impedance analyzer is employed that has a frequency sweep range of 20 Hz to 1 MHz with a measurement accuracy of 0.1% and a resolution of six digital measurement units. The procedure follows several iterations of a standard open-circuit/short-circuit test implemented at the terminals of the HFPT, as follows:

1) *Open-circuit test with primary probing*: The HFPT equivalent circuit for open-circuit test by probing the primary winding, while keeping the secondary side open is shown in Fig. 18(a). Please note, $C_{\text{str},P}$ represents the lumped intra and interwinding capacitance referred to the primary side [as seen in (26)]. Selecting the resistance mode measurement, for an excitation frequency of 500 kHz (matching the resonant frequency), the value of R_p is obtained. Next, changing the mode to inductance mode calculation, the lumped value of inductance at the primary side is obtained as follows:

$$L_{\text{eq},P} = L_P + L_m. \tag{32}$$

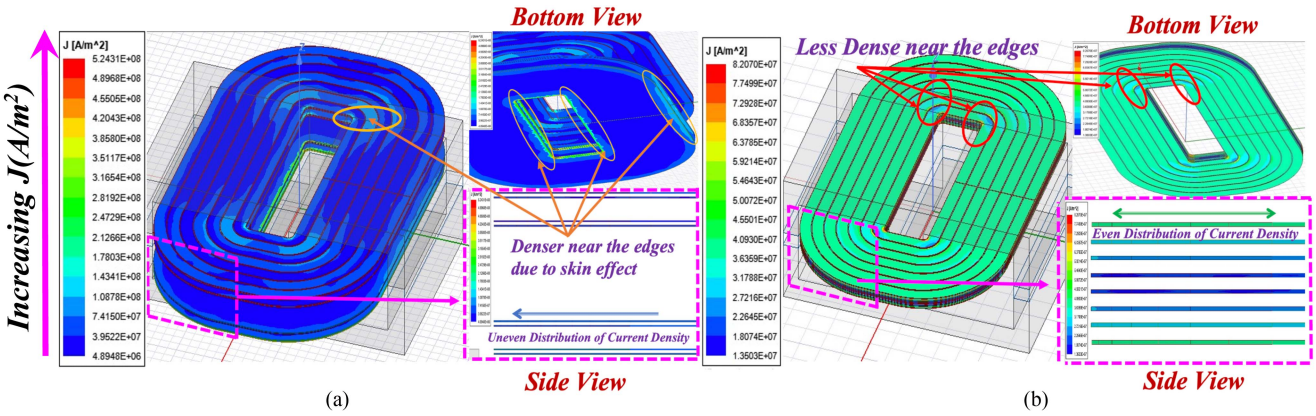

Fig. 16. Current density distribution obtained from 3-D FEA simulations for (a) ({[7P-4P-4P-7P], [1S*-1S*-1S*-1S*]}) and (b) interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) winding distribution.

TABLE V
COMPARISON OF ANALYTICAL, SIMULATION, AND EXPERIMENTAL RESULTS FOR DIFFERENT WINDING CONFIGURATIONS

Winding Configuration	Primary Leakage Inductance (μH) L_P			Secondary Leakage Inductance (nH) L_S			Effective Primary Winding Resistance ($m\Omega$) R_P			Effective Secondary Winding Resistance ($m\Omega$) R_S			Primary Intra-winding Capacitance (nF) C_{Pin}			Secondary Intra-winding Capacitance (nF) C_{Sin}			Inter-winding Capacitance (pF) $C_{PS_{in}}$		
	Anly.	Sim.	Exp.	Anly.	Sim.	Exp.	Anly.	Sim.	Exp.	Anly.	Sim.	Exp.	Anly.	Sim.	Exp.	Anly.	Sim.	Exp.	Anly.	Sim.	Exp.
{8P-3P-3P-8P}, {1S*-1S*-1S*-1S*}	25.887	24.142	25.845	17.63	19.58	14.55	102.683	91.776	121.866	0.819	0.814	1.144	0.509	0.582	0.526	0.668	0.701	0.712	23.102	23.985	25.195
{7P-4P-4P-7P}, {1S*-1S*-1S*-1S*}	12.113	11.794	11.828	17.63	19.94	18.32	82.59	87.254	92.735	0.819	0.843	1.022	0.555	0.618	0.558	0.668	0.673	0.702	23.747	24.553	25.577
{6P-5P-5P-6P}, {1S*-1S*-1S*-1S*}	8.524	7.961	7.825	17.63	19.11	17.62	72.634	82.534	93.216	0.819	0.827	0.981	0.552	0.592	0.561	0.668	0.686	0.698	24.527	25.553	26.731
Interleaved {7P-1S*-1S*-4P-4P-1S*-1S*-7P}	0.109	0.157	0.211	0.239	0.218	0.324	46.438	49.583	44.356	0.312	0.227	0.236	0.544	0.591	0.561	0.117	0.121	0.121	790.081	791.252	812.252

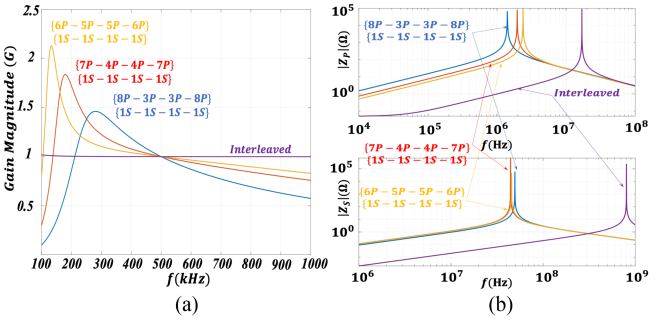

Fig. 17. (a) Gain plots for all winding configurations. (b) Plot of equivalent primary and secondary impedance versus operational frequency.

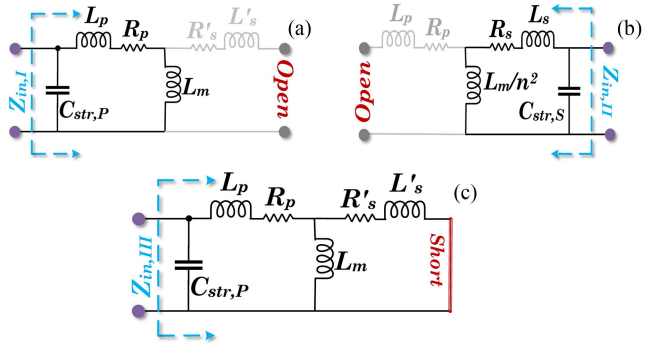

Fig. 18. Open-circuit/short-circuit tests on HFPT to experimentally measure the *R-L-C* parameters. (a) Open-circuit test with primary probing. (b) Open-circuit test with secondary probing. (c) Short-circuit test with primary probing.

Further, selecting the impedance measurement mode, the magnitude of $Z_{\text{in},I}$ is measured, the analytical equivalent magnitude of which is formulated as follows:

$$|Z_{\text{in},I}| = \text{mag} \times \left(\frac{R_p + j\omega \left\{ L_{\text{eq},P} - \omega^2 C_{\text{str},P} L_{\text{eq},P}^2 - C_{\text{str},P} R_p^2 \right\}}{1 - \omega^2 \left(2C_{\text{str},P} L_{\text{eq},P} - C_{\text{str},P}^2 R_p^2 \right) + \omega^4 C_{\text{str},P}^2 L_{\text{eq},P}^2} \right). \tag{33}$$

2) *Open-circuit test with secondary probing:* Similar procedure of measurement is implemented referred to the secondary side, by keeping the primary side winding open [as seen in Fig. 18(b)]. With an excitation frequency of 500 kHz, the value of R_s is obtained with the resistance mode measurement. The inductance mode measurement provides the value of lumped inductance referred to the secondary side as follows:

$$L_{\text{eq},S} = L_S + \frac{L_m}{n^2}. \tag{34}$$

Following the same procedure of impedance measurement, the magnitude of $Z_{\text{in,II}}$ is measured and recorded

$$|Z_{\text{in,II}}| = \text{mag} \times \left(\frac{R_s + j\omega \left\{ L_{\text{eq},S} - \omega^2 C_{\text{str},S} L_{\text{eq},S}^2 - C_{\text{str},S} R_s^2 \right\}}{1 - \omega^2 \left(2C_{\text{str},S} L_{\text{eq},S} - C_{\text{str},S}^2 R_s^2 \right) + \omega^4 C_{\text{str},S}^2 L_{\text{eq},S}^2} \right) \tag{35}$$

where $C_{\text{str},S} = \frac{C_{\text{str},P}}{n^2}$ is the lumped stray capacitance referred to the secondary side.

3) *Short-circuit test with primary probing:* In this step, the secondary side winding terminals are shorted, resulting in the equivalent circuit shown in Fig. 18(c). In this case, with the inductance mode measurement, the lumped inductance obtained is formulated as

$$L_{\text{eq,SC}} = L_P + (L_m || \left(n^2 L_S \right)). \tag{36}$$

Further, the impedance measured at the primary winding terminal has a magnitude of $Z_{\text{in,III}}$ formulated in (37), shown at the bottom of this page, where $C_{\text{str,SC}}$ represents the lumped stray capacitance excluding the value of $C_{s_{\text{in}}} (= C_{p_{\text{in}}} + (1 - n^2) C_{ps_{\text{in}}})$.

Once the measurements are recorded, (32), (34), and (36) are solved as simultaneous set of equations in MATLAB using *vpasolve* [26], to obtain the values of L_P, L_S, and L_m. Further, substituting the obtained value of inductances and winding resistances in (33), (35), and (37), the set of equations are solved in MATLAB to obtain the values of $C_{\text{str},P}$, $C_{\text{str},S}$, and $C_{\text{str,SC}}$. Finally, using the values of stray capacitances obtained, the experimental values of $C_{p_{\text{in}}}$, $C_{s_{\text{in}}}$, and $C_{ps_{\text{in}}}$ are obtained by solving for three equations with three variables using *vpasolve*. To further validate the accuracy of the obtained parameters, the excitation frequencies are varied, and the same set of steps are repeated, thus establishing the repeatability (with a mismatch threshold of 5%) of the experimental procedure to obtain the *R-L-C* parameters of HFPT. As observed in Table V, the FEA simulation and experimental results match the analytically calculated values with an average mismatch of 6.2% and 5.5% respectively, thus validating the model developed and analyses. Further, the experimentally measured values of winding resistance show a larger mismatch with the analytically calculated values due to the inconsistency introduced by the assumptions employed in Dowell's equation. As suggested in [12], there are several assumptions pertaining to the Dowell's equation that are ignored for reduced analytical complexity. These factors include the porosity factor [27] (included when the conductor width is comparable to its thickness leading to proximity effect in horizontal direction), distance considerations between multiple conductors turns in a single layer, distance of conductor surface from the core, and sinusoidal excitation provided to the windings. Thus, to accurately characterize the winding resistance and to observe the losses due to skin and proximity effects, the

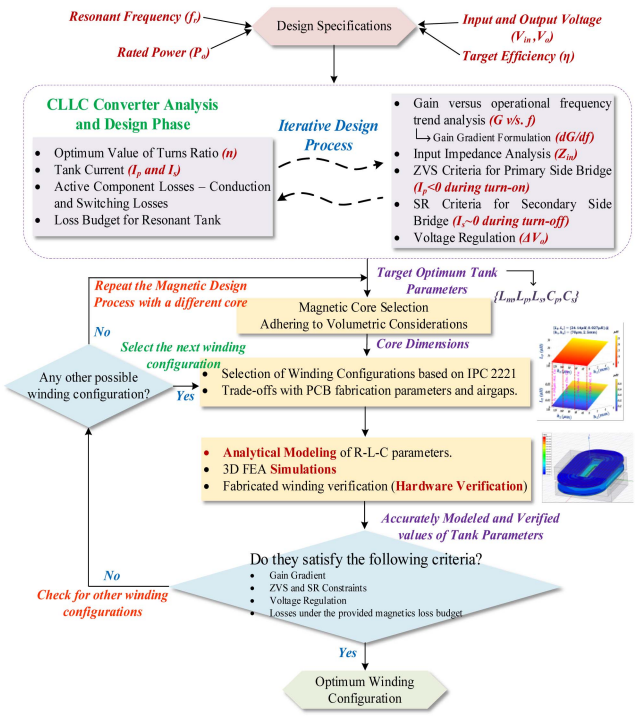

Fig. 19. Flowchart depicting the process to obtain the most optimum winding configuration.

3-D FEA simulation proves to be more reliable as presented in this article. However, it is important to highlight the accuracy of the analytical calculations to obtain the values of leakage inductances and stray capacitance, as seen in Table V. The accuracy obtained thereof essentially helps reduce the number of time and memory intensive iterations of FEA simulations for characterizing L_p, L_s, $C_{p_{\text{in}}}$, $C_{s_{\text{in}}}$, and $C_{ps_{\text{in}}}$ for different winding configurations.

Corelating the constraints for the optimum winding selection, Fig. 19 elucidates a detailed flowchart depicting the iterative process of finding the most optimum winding configuration. As observed, based on the design specifications, the converter analysis and design phase include an iterative process of finding the optimum values of tank parameters based on factors like resultant gain dependencies, loss budget for resonant tank by enabling ZVS and SR, input impedance function, and corresponding tank currents. Following the design phase, as per the target tank parameters, a compatible magnetic core is selected, adhering to the requirements pertaining to rated power and the required magnetizing inductance (L_m).

The core selection follows a volumetric minimization based comparative analysis, where the following considerations pertaining to the gain-frequency trend, soft-switching criteria, and dimensional constraints of the core are imposed for the design specifications mentioned in Table VII:

1) The turns ratio needs to be $n = 22:1$, adhering to the near unity gain requirement at maximum operating voltages

$$Z_{\text{in.III}} = \text{mag} \left(\frac{R_p R'_s - \omega^2 \left(L_P L_{\text{eq},S} + L_m L'_S \right) + j\omega \left\{ L_m R'_s + L_{\text{eq},S} R_p + L_P R'_S \right\}}{\left(R'_s + j\omega L_{\text{eq},S} \right) \left(R_s - \omega^2 C_{\text{str,SC}} \left(L_m R'_s + L_{\text{eq},S} R_p + L_P R'_S \right) + j\omega \left\{ C_{\text{str,SC}} \left(R_p R'_s - \omega^2 \left(L_P L_{\text{eq},S} + L_m L'_s \right) \right) + L_{\text{eq},S} \right\} \right)} \right). \tag{37}$$

TABLE VI
COMPARISON OF PLANAR CORES FOR VOLUMETRIC MINIMIZATION

Relevant Ferrite Magnetic Planar Cores	Window Width (b_t)	Area of the core (A_e)	Volume of the core (V_e)	Air gap (h_g) for $L_m = 76\mu H$ and n = 22:1	B_{max} for excitation voltage = 400V, and n = 22:1	Analytically calculated core loss [29]
FR43808EC	11.43mm	194mm^2	10200mm^3	1.5mm	46.8mT	5.287W
FR44310EC	13.2mm	229mm^2	13900mm^3	1.8mm	39.6mT	5.876W
FR45810EC	21.4mm	310mm^2	24600mm^3	1.9mm	29.5mT	5.221W
FR46410EC	21.8mm	516mm^2	41400mm^3	4.1mm	17.6mT	6.242W
0R49928EC	36mm	540mm^2	79800mm^3	4.25mm	16.8mT	8.385W

(for 600–28 V conversion). Corresponding to the current carrying capacity of a 2 oz. copper trace for a four-layer PCB, the window width should be at least 20 mm with $N_{e,\max} = 8$ and $N_{i,\max} = 5$.

2) Corresponding to the gain trend and ZVS requirements, the magnetizing inductance is calculated to be less than 76.26 μH. The airgap between the cores should be <2.5 mm to prevent excessive leakage of flux from the cores.
3) The $B_{\max}$ obtained corresponding to the turns ratio (n), area of the core (A_e), and excitation voltage should be less than the saturation flux density (B_{sat} value) of the core.

With the abovementioned considerations, Table VI compares five different planar cores [28] and analyzes the dimensions of the core, the airgap requirement to obtain the required L_m with $n = 22{:}1$, corresponding $B_{\max}$ values, and the core losses.

As observed in Table VI, the selected core FR45810EC proves to be the most ideal selection, adhering to the requirements corresponding to the window width and airgap to achieve the required L_m with $n = 22{:}1$. Further, the selected core also provides an optimal tradeoff corresponding to the dimensions (the area and volume) of the core with respect to the $B_{\max}$ obtained thereof, resulting in the least amount of analytically calculated core losses**.** Please note that the comparison shown above is only targeted for the converter specifications for the presented work. However, as Fig. 14 provides a generic flowchart for optimum HFPT design, the magnetic core selection is also included in the iterative design process.

Further, as observed in (1)–(8), based on the core selection and the available window area, different winding configurations are formulated along with their tradeoffs pertaining to the airgaps and PCB fabrication parameters. This process is followed by analytical modeling, FEA simulations, and hardware verification to accurately characterize the obtained tank parameters. The optimal winding selection process is successful if the obtained tank parameters satisfy the constraints pertaining to gain gradients, soft-switching, and core losses. In addition to that, ideally for obtaining minimized winding losses, interleaved winding configurations proves to be the most feasible option. However, it is worthwhile to point out at the limitation of implementing an interleaved structure in a leakage integrated design of HFPT. As observed in the analytical calculations in Table II, with verified resultant parameters shown in Table V and corresponding gain graphs in Fig. 17(a), although the interleaved winding structure provides reduced effective winding resistance, due to negligible value of leakage inductances obtained thereof, the required gain is not achieved as required by the application. Thus, an additional inductor is required to meet the requirements of voltage gain and ZVS soft switching, which degrades the power density of the developed converter. This necessitates the criteria of checking the winding losses and ensuring them to be under the defined magnetic loss budget as seen in Fig. 19.

If none of the possible winding structures satisfy the performance constraints, then the same process of *R-L-C* modeling is carried out for all possible winding configurations with different compatible magnetic cores. This iterative process facilitates the most optimum HFPT design for a given set of design specification pertaining to a selected converter topology.

TABLE VII
DESIGN SPECIFICATIONS FOR BIDIRECTIONAL *CLLC*

Parameters	Values
Primary input voltage range (V_{in})	400-600V
Secondary output voltage range (V_o)	24-28V
Rated Power (P_o)	1kW
Transformer Turns Ratio (n)	22:1
Tank Leakage Inductances (L_P,L_S)	11.8μH, 0.022μH
Magnetizing Inductance (L_m)	72μH
Tank Capacitors (C_P,C_S)	8.58nF, 5.06μF
Resonant frequency (f_r)	500 kHz

V. EXPERIMENTAL VERIFICATION AND BENCHMARKING

Following the tradeoffs-based optimal selection presented in the previous section, an experimental setup is built to test and verify the transformer characteristics and to analyze the performance of the *CLLC* converter with the selected transformer winding configuration. By following the design considerations pertaining to the gain requirement, ZVS criteria, and frequency of operation, Table VII shows the design specifications for the developed *CLLC* converter.

To realize these specifications, a 22:1 HFPT, as shown in Fig. 20 with {[7P-4P-4P-7P], [1S*-1S*-1S*-1S*]} winding arrangement using two four-layer 1.6 mm PCBs with a copper conductor thickness of 70 μm is employed. Further, FR45810EC core from Magnetics Inc. is selected for this application. Referring to the trends shown in the previous sections for the PCB fabrication details, to obtain the required leakage inductance with a {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} arrangement, the following insulation thickness values are selected: $h_{pr} = 0.23$ mm and $h_c = 1.19$ mm. Correspondingly, the air gap between the

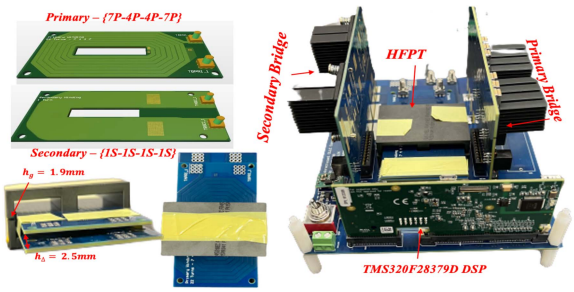

Fig. 20. Experimental setup for developed CLLC converter.

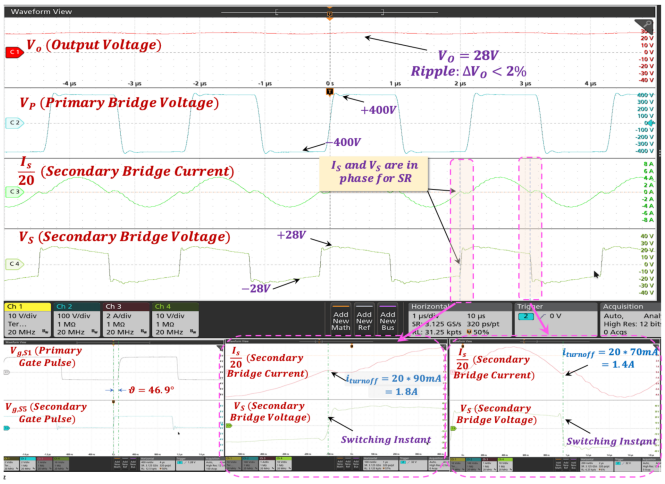

Fig. 21. Experimental waveforms for V_O, V_P, I_S, and V_S [Y-axis: V_O –10 V/div V_P – 100 V/div, $\frac{I_S}{20}$ – 2 A/div, V_S – 10 V/div; X-axis: time - 1 μs/div].

primary and secondary winding is selected to be $h_\Delta = 2.5$ mm, while that between the cores is selected to be $h_g = 1.9$ mm.

Figs. 21 and 22 show the experimental results obtained at the rated input voltage at 462.9 kHz switching frequency to obtain the required voltage gain. As observed, the primary current lags the primary bridge voltage thus achieving ZVS operation, which matches the presented analysis and justifies the winding selection based on the gain conditions and physical constraints. The output voltage is settled at 28 V with a peak-to-peak ripple of <2%. The secondary bridge is switched at a phase angle ($\varphi = 46.9°$) with respect to the primary bridge gate pulse to achieve SR at the secondary bridge, which enables it to be soft switched, thus enhancing the overall efficiency.

In order to validate the selection of optimal winding configuration and its relevance for obtaining ZVS at the primary side (switch S_2), Fig. 23 shows the experimentally obtained waveforms of the drain to source voltage, gate to source voltage, and the drain current at the switching instant. As observed, V_{DS,S_2} falls down to 0 V prior to the V_{GS,S_2} reaching its threshold value of the switch. Further, the drain current I_{D,S_2} observes a negative magnitude at the turn ON instant with a lagging phase. Both these occurrences highlight the ZVS-based soft switching of switch S_2.

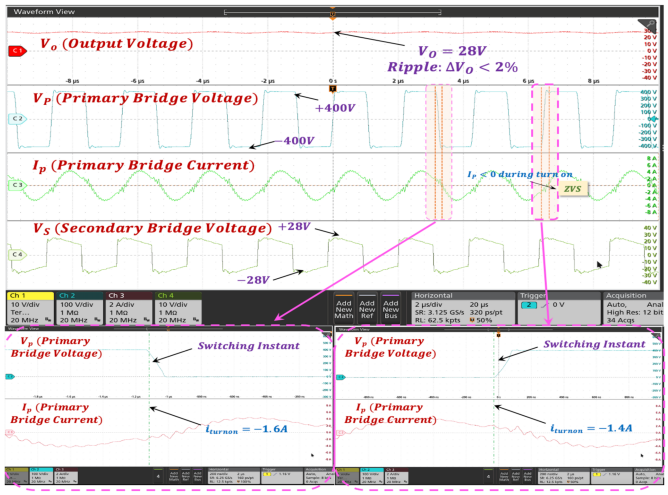

Fig. 22. Experimental waveforms for V_O, V_P, I_P, and V_S [Y-axis: V_O – 10 V/div, V_P – 100 V/div, I_P – 2 A/div, V_S – 10 V/div; X-axis: time—2 μs/div].

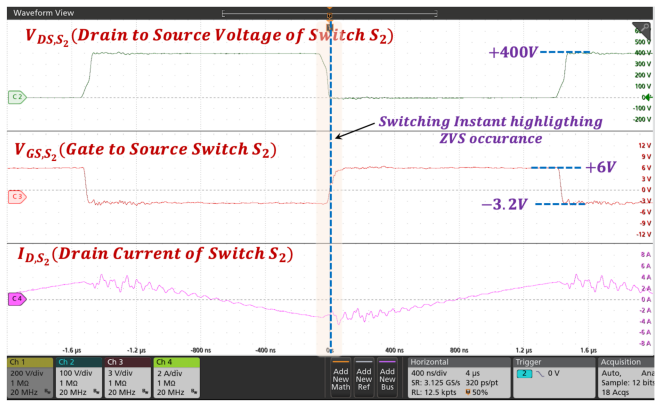

Fig. 23. Experimental waveforms elucidating the ZVS based soft switching at switch S_2.

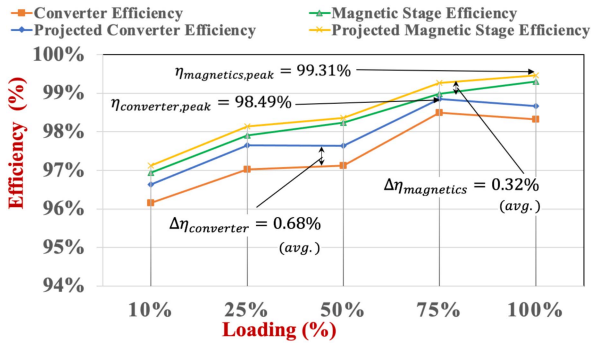

Fig. 24. Converter and magnetic stage component efficiency at different loading conditions.

Further, the efficiency curve for the developed converter at different loading conditions is presented in Fig. 24, which indicates a peak converter efficiency of 98.49% and magnetic stage efficiency of 99.31%. Additionally, the actual converter and magnetic stage efficiency matches with its projected value with

TABLE VIII
PERFORMANCE COMPARISON OF THE DEVELOPED HARDWARE WITH THE STATE-OF-THE-ART WORKS

Comparison Metrics ---------- SOA Works	Topology	Power Level	Voltage Conversion Range	Power Density	Peak Converter Efficiency	Operational /Resonant Frequency
[7]	Resonant LLC	500W	$V_{in} = 400V;\ V_o = 100V$	-	~90%	200kHz
[9]	Resonant LLC	1.2kW	$V_{in} = 200V;\ V_o = 96V$	-	96.3%	200kHz
[12]	Dual Active Bridge (DAB)	1.2kW	$V_{in} = 50V;\ V_o = 50 - 100V$	-	~96.5%	50kHz
[30]	Resonant LLC	20W	$V_{in} = 80V;\ V_o = 10V$	6.1W/inch^3	90.9%	1MHz
[31]	Dual Bridge Series Resonant (DBSR)	200W	$V_{in} = 110V;\ V_o = 100V$	-	95%	100kHz
[32]	Resonant LLC	1kW	$V_{in} = 360V;\ V_o = 40V$	-	96.5%	1MHz
[33]	Resonant LLC	800W	$V_{in} = 380V;\ V_o = 12V$	900W/inch^3	97.6%	1MHz
[34]	Three Phase Interleaved Resonant LLC	3kW	$V_{in} = 400V;\ V_o = 48V$	600W/inch^3	97.7%	1MHz
[35]	Resonant CLLC	400W	$V_{in} = 400V;\ V_o = 20 - 25V$	53W/inch^3	94.3%	1MHz
[36]	Resonant LLC	350W	$V_{in} = 320 - 390V;\ V_o = 19.5V$	137.16W/inch^3	95.26%	800kHz
[37]	Half Bridge Resonant CLCL	25W	$V_{in} = 80V;\ V_o = 15V$	5.43W/inch^3	88.7%	1MHz
[38]	Resonant CLLC	6.6kW	$V_{in} = 400V;\ V_o = 250 - 400V$	130W/inch^3	97.8%	500kHz
This work	Resonant CLLC	1kW	$V_{in} = 400 - 600V;$ $V_o = 24 - 28V$	106W/inch^3 (scalable up to 350W/inch^3)	98.49%	500kHz

a mismatch of 0.68% and 0.32%, respectively, thus affirming the accuracy of presented analysis.

A detailed comparison of several published works (that employ HFPTs in their power conversion topologies) in terms of the overall efficiency, power levels, nominal voltage conversion levels, power densities, and operational frequencies is presented in Table VIII. As observed, due to intricate modeling and parameterization of the parasitic components along with the most optimal HFPT selection, the developed *CLLC* results in an improved efficiency as compared to the state-of-the-art works [7], [9], [12], [30], [31], [32], [33], [34], [35], [36], [37], [38]. Please note that that although the proof-of-concept has been tested only up to 1 kW for concept verification, its power rating can be further scaled up to 3.3 kW with utilization of higher current-rated switching devices while retaining the same footprint areas, with the existing control and gate drive system, which would elevate the power density to 350 W/inch^3.

VI. CONCLUSION

Based on realistic considerations to fabricate an HFPT for a bidirectional *CLLC* dc/dc converter, this article emphases comprehensive analytical modeling to formulate the leakage inductance, winding resistance, and stray capacitance by elaborating on their structural dependencies on PCB specifications. The characterization of four different winding structures is carried out comprehensively and corresponding results are verified using various 3-D FEA models and experimental analysis, portraying an average mismatch of 6.2% and 5.5%, respectively. Further, optimal selection tradeoffs are presented pertaining to ZVS constraints, gain requirements, and frequency dependencies referring to experimentally developed 1.6 mm (2 oz. copper) four-layer PCBs for noninterleaved configurations and 1.6 mm (2 oz. copper) eight-layer for interleaved structure. To validate and benchmark the model with the most suitable winding structure selected for the application pertaining to APUs used in MEA, an experimental proof-of-concept is developed and tested. The results show a peak converter efficiency of 98.49% with magnetics stage efficiency of 99.31% at 1 kW rated load, thus supporting, and validating the presented analysis. This design approach and analysis can be further extended to any winding configuration used for different HFPT applications.

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Ashwin Chandwani (Student Member, IEEE) received the Ph.D. degree in electrical engineering from the Arizona State University, Tempe, AZ, USA, in 2022.

He has authored/coauthored more than 28 journal/conference papers. His research interests include advanced power electronics and its applications in fields like renewable energy sources, datacenters, electric vehicle charging infrastructure, point of load applications, microgrids, and power quality compensators. He is currently working as a Senior Power Management Systems Engineer with the Qualcomm Technologies Inc., San Diego, CA, USA.

Dr. Chandwani was the recipient of various awards and recognitions, including the Fulton Engineering Graduate Fellowship Award (2021), Fulton Graduate College Travel Award (2021), and Outstanding Young Researcher Award (2021).

Ayan Mallik (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Maryland, College Park, MD, USA, in 2019.

He joined the Arizona State University, Tempe, AZ, USA, as an Assistant Professor, in August 2019. He has authored/coauthored/coinvented more than 80 peer-reviewed publications and 4 issued/pending U.S. Patents. His research interests include the design, control, and multiobjective optimization of power electronic converters, highly efficient and high-density power conversion solutions in the applications of more-electric-aircrafts, electric vehicles, grid-tied renewables, space, avionics, and data centers.

Dr. Mallik serves as an Associate Editor of IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY and IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS. He is the recipient of various awards and recognitions, including first place in Dean's Doctoral Dissertation award competition at UMD (2019), ECE distinguished dissertation award at UMD (2019), University of Maryland's (UMD) Invention of the Year award (2018), Jimmy H.C. Lin invention award (2018), and third place in Allegheny Region Cleantech University Prize Collegiate Competition (2017) sponsored by the U.S. Department of Energy, among many others.