Computationally-Efficient Model Predictive Control of Dual-Output Multilevel Converter in Hybrid Microgrid

Vijesh Jayan, *Member, IEEE*, and Amer Mohammad Yusuf Mohammad Ghias, *Senior Member, IEEE*

***Abstract*—This article presents a hybrid microgrid configuration with a flying capacitor dual-output (FCDO) converter. The output ports of the FCDO converter can directly interface ac sources/loads operating at different amplitudes and frequencies without additional ac/dc/ac converter units. Compared to the conventional configuration, the hybrid microgrid with the FCDO converter operates at multilevel voltages, reduced power conversion stages, less power switch count, and fewer control loops. The article also presents a cascaded model predictive control (CMPC) algorithm for such configuration to control the variables, namely three-phase dual-output currents, ac/dc bus and FC voltages, and active/reactive power. The proposed CMPC sequentially executes multiple single-objective MPC units with adaptive dynamic reference (ADR) models to control the multivariable. The controller first obtains the optimum voltage vector for each output port by minimizing the output current errors, where the ADR model generates the appropriate references. Finally, the controller identifies the optimum state from the determined voltage vector pair by minimizing the FC voltage errors. Unlike conventional MPC, the CMPC algorithm reduces the computational burden of the controller and attains multivariable control without additional control loops and weighting factors. Furthermore, the converter's performance with the CMPC algorithm is validated experimentally on a low-power hybrid microgrid.**

***Index Terms*—Hybrid microgrid, independent dual-output multilevel converter, model predictive control.**

I. Introduction

HYBRID microgrid has proven to be a promising technology to integrate different types of energy sources and loads with a reduced number of power converters, enhanced system stability, and efficiency [1], [2]. The hybrid microgrid consists of an ac and dc bus, where the renewable energy sources, grid, and loads are connected. The ac and dc bus is interconnected by an ac/dc converter, which is commonly referred as the bidirectional interlinking converter (BIC). The hybrid microgrid generally operates in two modes, namely grid-connected mode [3] and islanded mode [4]. The control objective of each converter in the hybrid microgrid is dependent on its operation mode and is defined by a dedicated supervisory control [5]. The schematic diagram of a typical hybrid microgrid in grid-connected mode is shown in Fig. 1. Due to the direct integration of the grid, the ac bus of the hybrid microgrid operates at voltage e and frequency f_g. As a result, interfacing ac sources and loads operating at varying amplitudes and frequencies, namely wind energy, motor drive, etc., to the ac bus requires an ac/dc/ac converter (see Fig. 1). Such a conventional approach not only increases the total number of power components but also increases the power conversion stages, power losses, and control complexities [6]. The number of power conversion stages and primary control loops required to realize the conventional hybrid microgrid configuration with two ac systems are summarized in Table I.

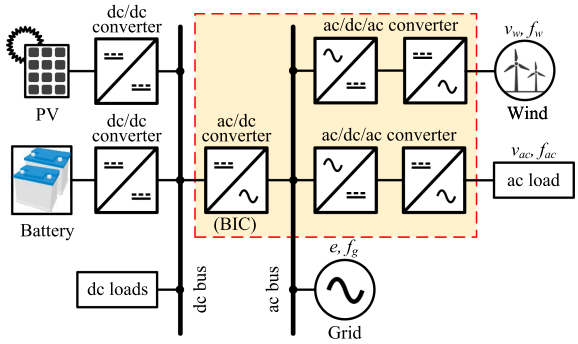


Fig. 1. Schematic diagram of the conventional hybrid microgrid in grid-connected mode.

Observe that the conventional configuration interfacing two ac systems to the dc bus has three power conversion stages and five control variables. This suggests that to interface every additional ac system, the conventional configuration requires two more power conversion stages and three additional variables to control, thus increasing the system complexities and power losses. One of the ways to sort out the complexity is to use a dual-output converter, which can integrate two ac systems operating at different amplitudes (DAs) and different frequencies (DFs) through its output ports, as shown in Table I. Observe that a dual-output converter simplifies the hybrid microgrid by blending the BIC and ac/dc/ac converters. In doing so, the configuration has only one power conversion stage and three control variables.

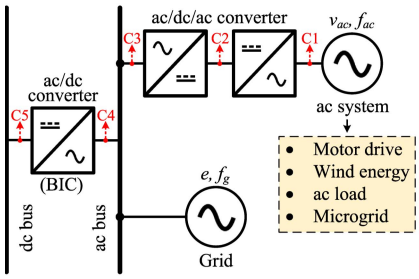
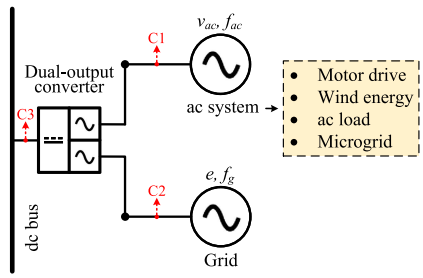
Manuscript received 1 June 2022; revised 7 September 2022, 2 November 2022, and 3 January 2023; accepted 20 January 2023. Date of publication 24 January 2023; date of current version 10 March 2023. This work was supported by the School of Electrical and Electronic Engineering at Nanyang Technological University, Ministry of Education, Singapore, under Grant RG 50/21. Recommended for publication by Associate Editor Mei Su. *(Corresponding authors: Vijesh Jayan; Amer Mohammad Yusuf Mohammad Ghias.)*

The authors are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: vijeshja001@e.ntu.edu.sg; amer.ghias@ntu.edu.sg).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3239437.

Digital Object Identifier 10.1109/TPEL.2023.3239437

TABLE I
QUANTITATIVE COMPARISON BETWEEN CONVENTIONAL AND PROPOSED HYBRID MICROGRID CONFIGURATIONS WITH DIFFERENT CONVERTER TOPOLOGIES

Hybrid microgrid configuration	**Conventional** 							
Power conversion stages	Three				One			
Primary control variables	Five – Three-phase ac currents at C1, C3, C4 – dc voltages at C2, C5				Three – Three-phase ac currents at C1, C2 – dc voltage at C3			
Converter topology	Two-level [39]	NPC [7]	NPP [8]	FC [9]	NSDO [10]	NPCDO [31]	NPPDO [32]	FCDO [38]
Number of power switches	18	36	54	36	9	15	21	21
Number of diodes	0	18	0	0	0	6	0	0
Number of inductors	9	9	9	9	6	6	6	6
Number of capacitors	1	4	4	10	0	2	2	3
Total number of components	28	67	67	55	15	29	29	30
Voltage levels	Two	Three	Three	Three	Two	Three	Three	Three
Independent operation	Yes				Restricted			Yes

Note: Total number of components for the conventional configuration are calculated by considering the same topology for both ac/dc and ac/dc/ac converter.

Another notable feature is that the proposed configuration with dual-output converter topologies offers multilevel voltages at a reduced number of components compared to the conventional converter topologies (see Table I). This difference in the number of components gets significantly higher with the number of ac systems. Hence, the proposed configuration with a multioutput converter has reduced bulkiness and control complexities.

The first dual-output converter topology was developed by eliminating three power switches from a conventional two-level ac/dc/ac converter having 12 power switches. Since the resulting topology had only nine power switches, the converter was named the nine switch dual-output (NSDO) converter [10]. Due to power switch reduction, the output ports of the NSDO converter share a common current path. As a result, a modified pulsewidth modulation (PWM) technique was developed for the NSDO converter to realize an independent control of its output ports [11]. Such enhancement made the NSDO converter a suitable choice for various microgrid applications. In [12], a grid-connected photovoltaic (PV) system using the NSDO converter with self-supported dynamic voltage restorer functionality was presented. The dc side of the NSDO converter was connected to the PV system while one of its output ports was connected in parallel and other in series to the point of common coupling (PCC). The output port shunted across the PCC injected the PV power to the grid while the other output port provided voltage compensation in an event of fault. Thus, three linear controllers were required to realize the configuration. A similar application of the NSDO converter as a power quality conditioner was reported in [13]. In [14], a unified expandable converter (UEC) was proposed to integrate renewable energy sources into the grid. The UEC was essentially an NSDO converter with three output ports, which were interfaced to the grid, ac, and dc sources. The authors developed sequential space vector modulation (SSVM) to obtain switching signals for the independent operation of the three output ports. In [15] and [16], the UEC utilized the SSVM technique to integrate multiple wind energy systems into the grid. Even though the above-mentioned methods offered independent output port operation, traditional linear controllers were used to control the NSDO converter. Note that the gain parameters for these controllers were obtained for a specific operating point in the microgrid. In practice, the operating point varies abruptly with changes in renewable penetrations and load in the microgrid. Thus, the designed linear controllers do not exhibit the desired dynamic response during a sudden transition in the operating point. In addition, the developed SSVM for UEC lacks experimental validation and is expected to burden the controller's computation process during real-time implementation. Thus, a robust controller is required for dual-output converter that ensures a dynamic regulation of its variables to the desired references.

A significant increase in the use of the finite control set model predictive control (FCS-MPC) for various power electronic applications is observed [17]. Unlike the conventional linear controller, the FCS-MPC utilizes a discrete-time model of the converter variables to identify the optimum switching action, thereby guaranteeing a dynamic performance. Another notable feature of the FCS-MPC is its ability to realize multiple control objectives by simply incorporating the control variables in its cost function through weighting factors [18], thus making FCS-MPC a right choice to control dual-output converter in

microgrid application. The FCS-MPC implementation of the NSDO converter as a power quality conditioner was reported in [19]. Both the output ports were connected to the PCC, where one of the output ports provided shunt compensation and the other regulated the dc bus voltage. To realize such a configuration, the FCS-MPC utilized a cost function that consisted of weighted quadratic error terms of the shunted output port current and dc bus voltage. In [20], one of the output ports of the NSDO converter was connected to the grid and another to the ac load. The authors defined a weighting factor-less cost function with absolute error terms of grid active, reactive power, and ac load current. In [21], the FCS-MPC implementation of the NSDO converter driving two ac loads with an output filter was presented. The FCS-MPC utilized a quadratic cost function based on the capacitor voltage error to regulate the output ac load voltages to their desired references. In [22], the NSDO converter integrated two islanded microgrids through its output ports. A cost function with quadratic error terms of active and reactive power of both the output ports was used to realize an independent bidirectional power transfer between the microgrids. A similar integration of two different ac sources was performed using a cascaded dual-output multilevel (CDOM) converter [23]. Unlike the NSDO converter, the CDOM converter operates its output ports at multilevel voltages [24]. The CDOM converter interfaced multiple dc sources and ac sources operating at different frequencies to the grid. The authors utilized a cost function with quadratic error terms of both the output currents. Observe that in all the above-mentioned FCS-MPC implementation, the error in the control variables of the two output ports is incorporated in a single cost function. To ensure equal priority in controlling the output ports, these error terms are required to be normalized by using appropriate weighting factors [25]. Note that estimating these factors is a nontrivial optimization problem and requires the development of complex numerical models for their estimation [26]. Such FCS-MPC implementation also burdens the controller's computation process and introduces a delay in the application of the optimum state to the converter. This is because the controller identifies the optimum state to control the output ports by evaluating a finite set of all possible states in a sampling period. Note that these complexities are bound to increase further for dual-output multilevel converter topologies because of having a huge finite set of states and additional control variables. A simplified FCS-MPC algorithm was reported for a three-level neutral-point clamped (NPC) converter in [27]. At first, the algorithm identified an optimum hexagon consisting of 12 switching states in a 2-D space vector by utilizing the reference voltage vector. The algorithm then obtained the optimum switching signals by minimizing a cost function based on the output and neutral-point (NP) voltage prediction model using 12 switching states of the hexagon. Adopting such a strategy reduced the computation burden significantly, as the algorithm need not search through a finite set of 27 switching states to identify the optimum switching signals. However, the algorithm required a weighting factor to incorporate the secondary control objective of NP voltage regulation in the cost function. In [28], a computationally-efficient MPC algorithm free from weighting factors was reported for a five-level active NPC converter. The algorithm utilized cost functions based on the voltage prediction model to not only select the optimum sector but also determine the small triangle formed by three voltage vectors within the selected sector. The secondary control objective of capacitor voltage regulation was accomplished by exploiting the redundant states through if-else comparative logic. As a result, the need for weighting factors was eliminated. Even though the algorithm effectively controlled the multivariable, its implementation on a dual-output converter increases computational complexity. Since each output port has an individual space vector, a combination of two such algorithms are required to generate the optimum switching signals for a dual-output converter. Also, developing if-else comparative logic for a dual-output converter is challenging as four combinations of output current directions must be evaluated to determine the appropriate state from the redundancies. Hence, a computationally-efficient FCS-MPC is required to be developed for dual-output converters that regulate the multivariable to their desired references without the need for weighting factors.

A dual predictive current control (PCC-D) for the NSDO converter was reported in [29]. One of the output ports of the NSDO converter was connected to the grid while the other was connected to a squirrel cage induction generator. The authors defined separate cost functions for each output port, which were evaluated alternatively. When the cost function for an output port was being evaluated from seven active voltage vectors, a null vector was applied to the other output port. As a result, a finite set of only seven states were required to be evaluated in a sampling period instead of 27. In doing so, controller's computational burden was reduced and the need for weighting factor estimation was eliminated. A similar approach using PCC-D with duty cycle optimization for NSDO converter was reported in [30]. Note that the PCC-D neglected 12 active voltage vector pairs and always forced the null vector to either of the output ports during the operation. In doing so, n output ports of the converter would always operate at null vector for $n-1$ consecutive sampling period. This would distort the output currents and increase their total harmonic distortion (THD). Other dual-output converter topologies reported in the literature were the NPC dual-output (NPCDO) [31], NP piloted dual-output (NPPDO) [32], T-type dual-output (TDO) [33], nested NPC dual-output (NNPCDO) [34], and active NPC dual-output (ANPCDO) [35]. Unlike the NSDO converter, the CDOM, NPCDO, NPPDO, TDO, NNPCDO, and ANPCDO topologies generate multilevel voltages across their dual-output ports. Note that the above-mentioned converter topologies are derived by eliminating power switches from their conventional ac/dc/ac configuration. As a result, the converter output ports share a common path that restricts them from operating independently under certain operating conditions, such as DA, DF, and different phase angle (DP) modes [36]. These restrictions are quantified by the converter's operating region, which is defined in terms of attainable voltage amplitude range across the output ports [37]. The output ports lose their independent operation and cause distortions when the converter operates beyond its operating region, thus making the above-mentioned converter topologies an infeasible choice for microgrid applications, where a fully

independent operation of the ac systems is required. In [38], a flying capacitor dual-output (FCDO) converter was proposed. Compared to other dual-output topologies, the FCDO converter provides independent multilevel voltages across its dual-output ports, thereby becoming a suitable candidate to interface multiple ac sources and loads operating at DA and DF to the hybrid microgrid. However, the FCDO converter in a hybrid microgrid demands a multiobjective controller that regulates the multivariable to their desired references throughout the operation. None of the above-mentioned controllers can accomplish these multiple control objectives at the reduced computational burden and minimal control loop complexities.

Therefore, the objective of the article is as follows.

1) Propose a hybrid microgrid configuration with an FCDO converter, where its independent output ports integrate two ac systems operating at DAs, DFs, and DPs. Compared to conventional configuration with multiple two-level converters, the proposed hybrid microgrid has reduced power conversion stages, less power components, and fewer control loops (see Table I).
2) Develop a cascaded model predictive control (CMPC) algorithm for the FCDO converter that regulates its two three-phase output currents and three FC voltages to their desired references. The proposed CMPC algorithm is free from weighting factors and operates at least computational burden compared to the FCS-MPC algorithms mentioned in the literature.
3) Replace outer-loop linear controllers with adaptive dynamic reference (ADR) models to generate appropriate output current references for the microgrid voltage regulations. Unlike linear controllers, the control parameters of the ADR model are easier to design and independent of the microgrid's operating conditions. As a result, the ADR model guarantees the desired dynamic response during step-transition in the operating point.

The remainder of the article is organized as follows: Section II presents the mathematical model and the control variables of the three-phase FCDO converter. Section III discusses the implementation of a conventional FCS-MPC algorithm and its limitations. Section IV presents the implementation of the proposed CMPC algorithm for the FCDO converter. Section V presents the experimental results of the FCDO converter in a hybrid microgrid under different modes. Finally, Section VI concludes this article.

II. Three-Phase FCDO Converter

A. Topology and Operation

The circuit configuration of a three-phase FCDO converter is shown in Fig. 2. Each phase x ($x \in \{a, b, c\}$) of the converter consists of two output ports (v_{1x}, v_{2x}), seven power switches ($S_{1x} - S_{7x}$), and a flying capacitor ($C_{\text{fc}x}$), whose voltage $v_{\text{fc}x}$ is regulated as

$$v_{\text{fc}x} = \frac{v_{\text{dc}}}{2} \tag{1}$$

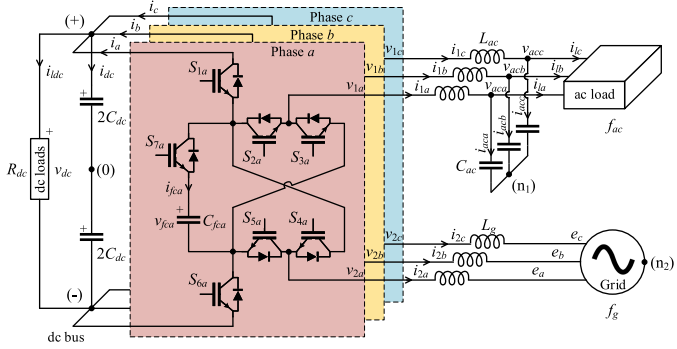


Fig. 2. Three-phase FCDO converter in a hybrid microgrid.

TABLE II
Switching States of Single-Phase FCDO Converter With Output Voltages and FC Current

s_{1x}	s_{2x}	s_{4x}	s_{6x}	s_{7x}	v_{1x0}	v_{2x0}	i_{fcx}
1	1	1	0	0	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	0
1	1	0	0	1	$\frac{v_{dc}}{2}$	0	i_{2x}
1	1	0	1	0	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	0
1	0	1	0	1	0	$\frac{v_{dc}}{2}$	i_{1x}
0	1	1	1	1	0	0	$-i_{1x} - i_{2x}$
1	0	0	0	1	0	0	$i_{1x} + i_{2x}$
0	1	0	1	1	0	$-\frac{v_{dc}}{2}$	$-i_{1x}$
1	0	1	1	0	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	0
0	0	1	1	1	$-\frac{v_{dc}}{2}$	0	$-i_{2x}$
0	0	0	1	0	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	0

where v_{dc} is the dc bus voltage. The binary switching signal of the ith power switch ($i \in \{1, 2, 3, 4, 5, 6, 7\}$) in xth phase is denoted as s_{ix}. Thus, the switching signals for each phase can be represented as $\mathbf{s}_x = [s_{1x}, s_{2x}, s_{3x}, s_{4x}, s_{5x}, s_{6x}, s_{7x}]$. On performing circuit analysis, each phase of the FCDO converter is found to operate under 10 possible switching states, as shown in Table II. Note that the switching signals for power switch S_{3x} and S_{5x} are obtained as

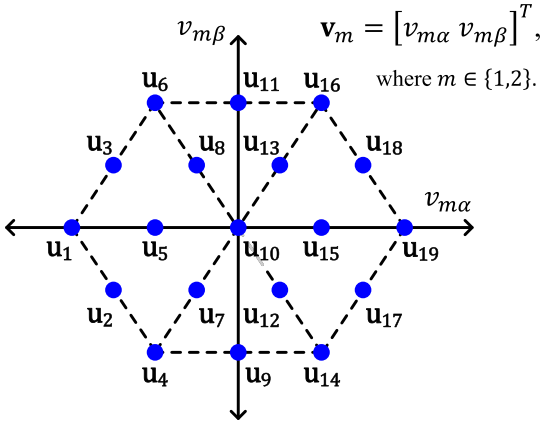
$$s_{3x} = \overline{s}_{2x} \text{ and} \tag{2}$$

$$s_{5x} = \overline{s}_{4x}. \tag{3}$$

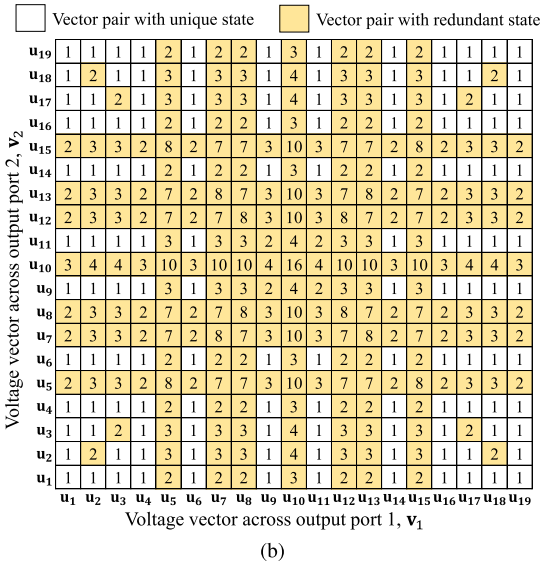
The output phase voltage of the FCDO converter referred across its NP 0 can be expressed in terms of v_{dc}, $v_{\text{fc}x}$, and switching signals as

$$v_{mx0} = \left(s_{1x}s_{7x} - s_{6x} + \overline{s}_{7x}(s_{1x} + s_{6x})s_{2mx}\right)\frac{v_{\text{dc}}}{2} - s_{7x}(s_{1x} - (s_{1x} + s_{6x})s_{2mx})v_{\text{fc}x}, \text{ where } m \in \{1, 2\}. \tag{4}$$

Observe that v_{1x0} and v_{2x0} of the FCDO converter can generate three voltage levels: $-\frac{v_{\text{dc}}}{2}$, 0, $\frac{v_{\text{dc}}}{2}$ independent of each other (see Table II), thus allowing the FCDO converter to drive its three-phase output ports independently compared to the existing dual-output converters. Furthermore, the FC current $i_{\text{fc}x}$ can be expressed in terms of the output phase currents i_{1x}, i_{2x} and



(a)



(b)

Fig. 3. (a) Voltage vectors across the output port m. (b) Number of states for different output voltage vector pairs $[\mathbf{v}_1, \mathbf{v}_2]$.

switching signals as

$$i_{\mathrm{fc}x} = s_{7x}\left((s_{1x} - s_{2x})\, i_{1x} + (s_{1x} - s_{4x})\, i_{2x}\right). \tag{5}$$

The voltage regulation of $C_{\mathrm{fc}x}$ is dependent on the sign of $i_{\mathrm{fc}x}$. $v_{\mathrm{fc}x}$ increases when $i_{\mathrm{fc}x} > 0$ and reduces when $i_{\mathrm{fc}x} < 0$. Similarly, the phase currents i_x across the dc bus side can be expressed as

$$i_x = -s_{1x}\left(s_{2x} + \overline{s}_{2x}s_{7x}\right) i_{1x} - s_{1x}\left(s_{4x} + \overline{s}_{4x}s_{7x}\right) i_{2x}. \tag{6}$$

From Table II, a three-phase FCDO converter is observed to operate under 1000 possible states ($10\times10\times10$). On transforming 1000 values of $v_{ma0}, v_{mb0}, v_{mc0}$ (4) to $\mathbf{v}_m = [v_{m\alpha}\ v_{m\beta}]^T$ using Clarke transformation, each three-phase output port of the FCDO converter is observed to generate 19 distinct voltage vectors: $\mathbf{u_1}, \mathbf{u_2}, \ldots, \mathbf{u_{19}}$ as shown in Fig. 3(a). Thus, the three-phase FCDO converter generates a total of $19 \times 19 = 361$ distinct voltage vector pairs $[\mathbf{v}_1, \mathbf{v}_2]$. The number of states for different $[\mathbf{v}_1, \mathbf{v}_2]$ pairs is shown in Fig. 3(b). Among the 361 pairs, 132 $[\mathbf{v}_1, \mathbf{v}_2]$ pairs can be generated by only one state. Such states are classified as the unique state. The rest 229 $[\mathbf{v}_1, \mathbf{v}_2]$ pairs can be generated by more than one state and are regarded as the redundant state [see the shaded region in Fig. 3(b)]. Consider that the FCDO converter is operating its output ports 1 and 2 at voltage vectors $\mathbf{u_5}$ and $\mathbf{u_{10}}$, respectively. From Fig. 3(b), the corresponding voltage vector pair $[\mathbf{u_5}, \mathbf{u_{10}}]$ is observed to have ten possible states. Even though these 10 states generate the same voltage vector across their three-phase output ports, their effects on the $v_{\mathrm{fc}x}$ are different. Through the selection of an appropriate state from the redundancies, $v_{\mathrm{fc}x}$ can be controlled.

B. Control Variables and Objectives

The FCDO converter in a hybrid microgrid comprising of grid, ac, and dc loads is shown in Fig. 2. The lower output port integrates the grid that operates at phase voltage amplitude E and frequency f_g while the upper output port interfaces the ac load that operates at phase voltage amplitude V_{ac} and frequency f_{ac}. The dc side of the converter is connected to the dc bus that consists of dc loads R_{dc} operating at voltage v_{dc}. Thus, the objectives of the controller are as follows:

1) Control two three-phase output currents;
2) Regulate dc bus voltage to V^*_{dc};
3) Regulate three-phase ac load voltage to $\mathbf{V}^*_{\mathrm{ac}}$ and f^*_{ac};
4) Regulate three FC voltages to $\frac{V^*_{\mathrm{dc}}}{2}$;
5) Ensure unity power factor (UPF) operation of the grid.

C. Continuous-Time Model

From Fig. 2, the continuous-time equation of the converter's output currents $\mathbf{i}_1 = [i_{1\alpha}\ i_{1\beta}]^T$ and $\mathbf{i}_2 = [i_{2\alpha}\ i_{2\beta}]^T$ can be expressed in terms of $\mathbf{v}_1$ and $\mathbf{v}_2$ as

$$L_{\mathrm{ac}}\frac{d\mathbf{i}_1}{dt} = \mathbf{v}_1 - \mathbf{v}_{\mathrm{ac}} \text{ and} \tag{7}$$

$$L_g\frac{d\mathbf{i}_2}{dt} = \mathbf{v}_2 - \mathbf{e} \tag{8}$$

where L_{ac} and L_g are the inductance of the filter connected to output ports 1 and 2, respectively. The grid voltage and ac load voltage in $\alpha\beta$ coordinate are referred as vector $\mathbf{e} = [e_\alpha\ e_\beta]^T$ and $\mathbf{v}_{\mathrm{ac}} = [v_{\mathrm{ac}\alpha}\ v_{\mathrm{ac}\beta}]^T$, respectively. Similarly, the continuous-time equation for $v_{\mathrm{fc}x}$, v_{dc}, and $\mathbf{v}_{\mathrm{ac}}$ can be expressed as

$$C_{\mathrm{fc}x}\frac{dv_{\mathrm{fc}x}}{dt} = i_{\mathrm{fc}x}, \text{ where } x \in \{a,b,c\} \tag{9}$$

$$C_{\mathrm{dc}}\frac{dv_{\mathrm{dc}}}{dt} = -\frac{v_{\mathrm{dc}}}{R_{\mathrm{dc}}} + \sum_{x=a,b,c} i_x, \text{ and} \tag{10}$$

$$C_{\mathrm{ac}}\frac{d\mathbf{v}_{\mathrm{ac}}}{dt} = \mathbf{i}_1 - \mathbf{i}_l \tag{11}$$

where the vector $\mathbf{i}_l = [i_{l\alpha}\ i_{l\beta}]^T$ is the ac load current in $\alpha\beta$ coordinate. From the mathematical model (7)–(11), a three-phase FCDO converter in a hybrid microgrid is observed to be a multivariable system with $\mathbf{i}_1, \mathbf{i}_2, v_{\mathrm{fc}a}, v_{\mathrm{fc}b}, v_{\mathrm{fc}c}$, v_{dc}, and $\mathbf{v}_{\mathrm{ac}}$ as the control variables. Thus, a multiobjective controller is required to control these variables to their desired references.

D. Prediction Model

Since the hybrid microgrid is in a grid-connected configuration (see Fig. 2), the objective of the FCDO converter is to regulate $v_{\rm dc}$ and $\mathbf{v}_{\rm ac}$ to their desired references by processing the power from the grid at UPF. This is accomplished by controlling the output currents of the FCDO converter. Thus, the continuous-time equations of $\mathbf{i}_1$ and $\mathbf{i}_2$ are transformed into discrete-time equations by using a forward Euler method. From (7) and (8), the output current predictions $\mathbf{i}_1^{k+1}$ and $\mathbf{i}_2^{k+1}$ for time instant $k+1$ can be expressed as

$$\mathbf{i}_1^{k+1} = \mathbf{i}_1^k + \frac{T_s}{L_{\rm ac}}\left(\mathbf{v}_1^k - \mathbf{v}_{\rm ac}^k\right) \text{ and} \tag{12}$$

$$\mathbf{i}_2^{k+1} = \mathbf{i}_2^k + \frac{T_s}{L_g}\left(\mathbf{v}_2^k - \mathbf{e}^k\right) \tag{13}$$

where T_s is the controller sampling period and $\mathbf{i}_1^k$, $\mathbf{i}_2^k$, $\mathbf{e}^k$, $\mathbf{v}_{\rm ac}^k$ are the variables measured by the sensors at time instant k. The terms $\mathbf{v}_1^k$, $\mathbf{v}_2^k$ are the output voltage vectors applied by the controller at time instant k, which can be expressed as

$$\mathbf{v}_m^k = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{ma0}^k \\ v_{mb0}^k \\ v_{mc0}^k \end{bmatrix}, \text{ where } m \in \{1,2\}. \tag{14}$$

Apart from the control of dual-output currents, the converter also requires regulation of its FC voltages to the desired reference as defined in (1). From (5) and (9), the prediction of the FC voltages $v_{{\rm fc}x}^{k+1}$ can be expressed as

$$v_{{\rm fc}x}^{k+1} = v_{{\rm fc}x}^k + \frac{T_s}{C_{{\rm fc}x}} s_{7x}^k \left(s_{1x}^k - s_{2x}^k\right) i_{1x}^k + \frac{T_s}{C_{{\rm fc}x}} s_{7x}^k \left(s_{1x}^k - s_{4x}^k\right) i_{2x}^k, \text{ where } x \in \{a,b,c\}. \tag{15}$$

Note that the terms s_{1x}^k, s_{2x}^k, s_{4x}^k, and s_{7x}^k are the switching signals applied by the controller at time instant k. The prediction model defined in (12), (13), and (15) are used in the multiobjective MPC formulation to control the variables.

E. Cost Function Design

Since the two three-phase output currents and three FC voltages are the control objectives, separate quadratic cost functions are defined to control these variables. The cost function based on the current error for each output port can be expressed as

$$J_m^k = (\mathbf{i}_m^{*k+1} - \mathbf{i}_m^{k+1})^2, \text{ where } m \in \{1,2\}. \tag{16}$$

Note that $\mathbf{i}_m^{*k+1} = [i_{m\alpha}^{*k+1}\ i_{m\beta}^{*k+1}]^T$ is the current reference for the output port m at time instant $k+1$. The details on the generation of $\mathbf{i}_m^*$ is explained in the following section. Similarly, $v_{{\rm fc}a}$, $v_{{\rm fc}b}$, and $v_{{\rm fc}c}$ are controlled by considering a quadratic cost function $J_{\rm FC}$ that is expressed as

$$J_{\rm FC}^k = \sum_{x=a,b,c} \left(V_{{\rm fc}x}^{*k+1} - v_{{\rm fc}x}^{k+1}\right)^2 \tag{17}$$

where $V_{{\rm fc}x}^{*k+1}$ is the voltage reference for the FC voltage at time instant $k+1$. $V_{{\rm fc}x}^*$ is dependent on the magnitude of the dc bus voltage reference as described in (1).

F. Reference Generation

$\mathbf{i}_1^*$ and $\mathbf{i}_2^*$ are generated based on their desired objective. $\mathbf{i}_1^*$ is generated to regulate the three-phase ac voltage across $C_{\rm ac}$ to $\mathbf{V}_{\rm ac}^* = [V_{{\rm ac}d}^*\ V_{{\rm ac}q}^*]^T$ and frequency $f_{\rm ac}^*$ while $\mathbf{i}_2^*$ is generated to regulate the voltage across $C_{\rm dc}$ to its nominal reference $V_{\rm dc}^*$ and ensure a UPF operation of the grid. Instead of using a constant reference, the ADR model [39] is used to generate $\mathbf{i}_1^*$ and $\mathbf{i}_2^*$. Through the use of the ADR model, appropriate $\mathbf{i}_1^*$ and $\mathbf{i}_2^*$ can be generated without introducing any undesirable oscillation, overshoot, and steady-state error in $\mathbf{v}_{\rm ac}$ and $v_{\rm dc}$, respectively. The ADR model comprises three control parameters N_R, N_L, and V_e, where N_R determines the dynamics of voltage reference generation, N_L governs the elimination of steady-state error, and V_e quenches the overshoot in the dynamic voltage reference. Thus, the N_R, N_L pair are selected such that the condition $\frac{\sqrt{N_L}}{2N_R} > 1$ is satisfied and V_e is chosen depending on the permissible percentage overshoot (PO) in the dynamic voltage reference. The detailed theoretical analysis on the derivation of the continuous-time equations, stepwise procedure to design its parameters: N_R, N_L, V_e and performance comparison with a traditional PI controller are given in [39].

1) $\mathbf{i}_1^*$ Generation: The dynamic voltage reference for the ac load $\mathbf{v}_{\rm ac}^*$ is expressed as

$$\mathbf{v}_{\rm ac}^{*k+1} = T_{\alpha\beta/dq}\mathbf{v}_{\rm ac}^k + \frac{\Delta\mathbf{v}_{\rm ac}^k}{N_R^{\rm ac}} + \frac{\mathbf{A}_{\rm ac}^k}{N_L^{\rm ac}}, \text{ where}$$

$$\mathbf{A}_{\rm ac}^k = \begin{cases} 0, & \text{if } V_e^{\rm ac} < |\Delta\mathbf{v}_{\rm ac}^k| \\ \mathbf{A}_{\rm ac}^{k-1} + \Delta\mathbf{v}_{\rm ac}^k, & \text{otherwise} \end{cases}, \text{ and}$$

$$\Delta\mathbf{v}_{\rm ac}^k = \mathbf{V}_{\rm ac}^* - T_{\alpha\beta/dq}\mathbf{v}_{\rm ac}^k. \tag{18}$$

Since $\mathbf{V}_{\rm ac}^*$ is in dq coordinate, park transformation matrix $T_{\alpha\beta/dq}$ is used to transform $\mathbf{v}_{\rm ac}^k$ to dq coordinate. $T_{\alpha\beta/dq}$ is defined as

$$T_{\alpha\beta/dq} = \begin{bmatrix} \cos\theta_{\rm ac}^* & \sin\theta_{\rm ac}^* \\ -\sin\theta_{\rm ac}^* & \cos\theta_{\rm ac}^* \end{bmatrix}, \text{ where } \theta_{\rm ac}^* = 2\pi f_{\rm ac}^* t. \tag{19}$$

Thus, the capacitance current reference $\mathbf{i}_{\rm ac}^* = [i_{{\rm ac}d}^*\ i_{{\rm ac}q}^*]^T$ required to regulate $C_{\rm ac}$ to $\mathbf{v}_{\rm ac}^*$ and $f_{\rm ac}^*$ can be obtained as

$$\mathbf{i}_{\rm ac}^{*k+1} = \frac{C_{\rm ac}}{T_s}\left(\mathbf{v}_{\rm ac}^{*k+1} - T_{\alpha\beta/dq}\mathbf{v}_{\rm ac}^k\right). \tag{20}$$

Since the objective of output port 1 is to regulate the $C_{\rm ac}$ to $\mathbf{v}_{\rm ac}^*$ and $f_{\rm ac}^*$, the appropriate $\mathbf{i}_1^*$ in $\alpha\beta$ coordinate can be obtained by applying inverse parks transformation on (20). The resulting expression is given as

$$\mathbf{i}_1^{*k+1} = \frac{C_{\rm ac}}{T_s}\left(T_{\alpha\beta/dq}^{-1}\mathbf{v}_{\rm ac}^{*k+1} - \mathbf{v}_{\rm ac}^k\right). \tag{21}$$

Thus, (21) generates appropriate $\mathbf{i}_1^*$ to regulate the three-phase ac load voltage to $\mathbf{V}_{\rm ac}^*$ and $f_{\rm ac}^*$.

2) $\mathbf{i}_2^*$ Generation: The dynamic voltage reference for the dc bus $v_{\rm dc}^*$ is expressed as

$$v_{\rm dc}^{*k+1} = v_{\rm dc}^k + \frac{\Delta v_{\rm dc}^k}{N_R^{\rm dc}} + \frac{A_{\rm dc}^k}{N_L^{\rm dc}},$$

where

$$A_{\rm dc}^k = \begin{cases} 0, & \text{if } V_e^{\rm dc} < |\Delta v_{\rm dc}^k| \\ A_{\rm dc}^{k-1} + \Delta v_{\rm dc}^k, & \text{otherwise} \end{cases},$$

and

$$\Delta v_{\rm dc}^k = V_{\rm dc}^* - v_{\rm dc}^k. \tag{22}$$

The instantaneous power reference $p_{\rm dc}^*$ required to regulate the $C_{\rm dc}$ to $v_{\rm dc}^*$ can be obtained as

$$p_{\rm dc}^{*k+1} = v_{\rm dc}^{*k+1} i_{\rm dc}^{k+1}, \text{ where } i_{\rm dc}^{k+1} = \frac{C_{\rm dc}}{T_s}\left(v_{\rm dc}^{*k+1} - v_{\rm dc}^k\right). \tag{23}$$

Note that $p_{\rm dc}^*$ generated by (23) can be huge during the transient. Thus, to ensure operational safety, a hard constraint is imposed on the generated $p_{\rm dc}^*$ as

$$p_g^{*k+1} = \begin{cases} P_{\rm lim}, & \text{if } p_{\rm dc}^{*k+1} > P_{\rm lim} \\ p_{\rm dc}^{*k+1}, & \text{if } -P_{\rm lim} \le p_{\rm dc}^{*k+1} \le P_{\rm lim} \\ -P_{\rm lim}, & \text{if } p_{\rm dc}^{*k+1} < -P_{\rm lim} \end{cases} \tag{24}$$

where $P_{\rm lim}$ is set based on the maximum permissible grid current. On applying the instantaneous power theory, the appropriate $\mathbf{i}_2^*$ to supply p_g^* from the grid can be obtained as

$$\mathbf{i}_2^* = \frac{1}{(e_\alpha)^2 + (e_\beta)^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} -p_g^{*k+1} \\ q^* \end{bmatrix}. \tag{25}$$

Note that q^* is the reactive power to be supplied/absorbed by the grid. q^* is set zero to ensure UPF operation of the grid.

III. Conventional FCS-MPC Implementation

The conventional FCS-MPC utilizes a single cost function $J_{\text{FCS-MPC}}$ with appropriate weighting factors to incorporate the errors of $\mathbf{i}_1$, $\mathbf{i}_2$, $v_{\text{fc}a}$, $v_{\text{fc}b}$, and $v_{\text{fc}c}$. $J_{\text{FCS-MPC}}$ is defined as

$$J_{\text{FCS-MPC}}^k(\mathbf{s}^k) = \lambda_{\text{FC}} J_{\text{FC}}^k(\mathbf{s}^k) + \sum_{m=1}^{2} \lambda_m J_m^k(\mathbf{s}^k) \tag{26}$$

where λ_1, λ_2, and λ_{FC} are the weighting factors that allow us to set priority to accomplish certain control objectives. Note that the converter's switching signals applied at time instant k are denoted as $\mathbf{s}^k = [\mathbf{s}_a^k, \mathbf{s}_b^k, \mathbf{s}_c^k]$. The FCS-MPC identifies the optimum switching signals $\mathbf{s}_{\text{opt}}^k$ by minimizing $J_{\text{FCS-MPC}}^k$ every T_s. The mathematical definition to minimize $J_{\text{FCS-MPC}}^k$ is expressed as

$$\underset{\mathbf{s}^k \in \mathbb{S}}{\text{argmin}}\, J_{\text{FCS-MPC}}^k(\mathbf{s}^k) \tag{27}$$

where $\mathbb{S}$ is the finite set of 1000 possible states of a three-phase FCDO converter.

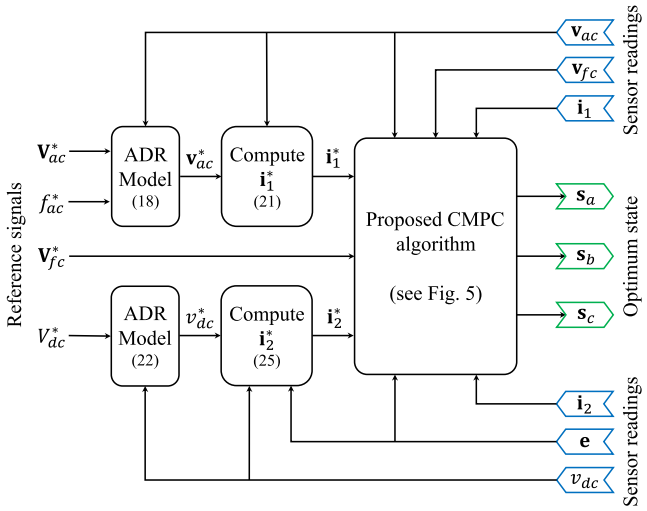


Fig. 4. Block diagram of the proposed control implementation.

A. Limitations of Conventional FCS-MPC Algorithm

1) Computational Burden: Observe from (27) that the conventional FCS-MPC identifies $\mathbf{s}_{\text{opt}}^k$ by evaluating 1000 values of $J_{\text{FCS-MPC}}^k$ in T_s. As a result, the controller experiences a computational burden that delays the application of $\mathbf{s}_{\text{opt}}^k$ during real-time implementation. Let us consider T_e as the time taken by the controller to obtain $\mathbf{s}_{\text{opt}}^k$ in T_s. If T_e takes a significant part of T_s, the application of $\mathbf{s}_{\text{opt}}$ is delayed and undesirable ripples are introduced in the system variables. These ripples can be eliminated through the implementation of delay compensation [40], where the $k+2$th prediction of the control variables is evaluated instead of $k+1$. Even though the ripple in the variables is reduced, such an approach remains computationally intensive as it has to evaluate 1000 values of $J_{\text{FCS-MPC}}^k$ to obtain $\mathbf{s}_{\text{opt}}^k$.

2) Weighting Factors: Observe from (26) that the cost function of a conventional FCS-MPC requires the estimation of three weighting factors. Weighting factor estimation is nontrivial and one of the ongoing research challenges. Numerous work for the weighting factor estimations are found in the literature [41], [42]. All these methods develop a complex numerical model by running numerous experimental and simulations on a predefined model. The developed numerical model estimates appropriate values of weighting factors for a desired converter operation. However, such an approach does not guarantee the desired converter performance when the model parameters deviates from its predefined values. Therefore, such a multivariable system requires an online weighting factor estimator that adjusts the weighting factor values. However, such an approach makes the overall implementation complex and challenging.

IV. Proposed CMPC Implementation

The block diagram of the proposed CMPC implementation for the FCDO converter in a hybrid microgrid is shown in Fig. 4. The procedure begins with output current reference generation ($\mathbf{i}_1^*$ and $\mathbf{i}_2^*$) by the ADR models and capacitor dynamics as discussed

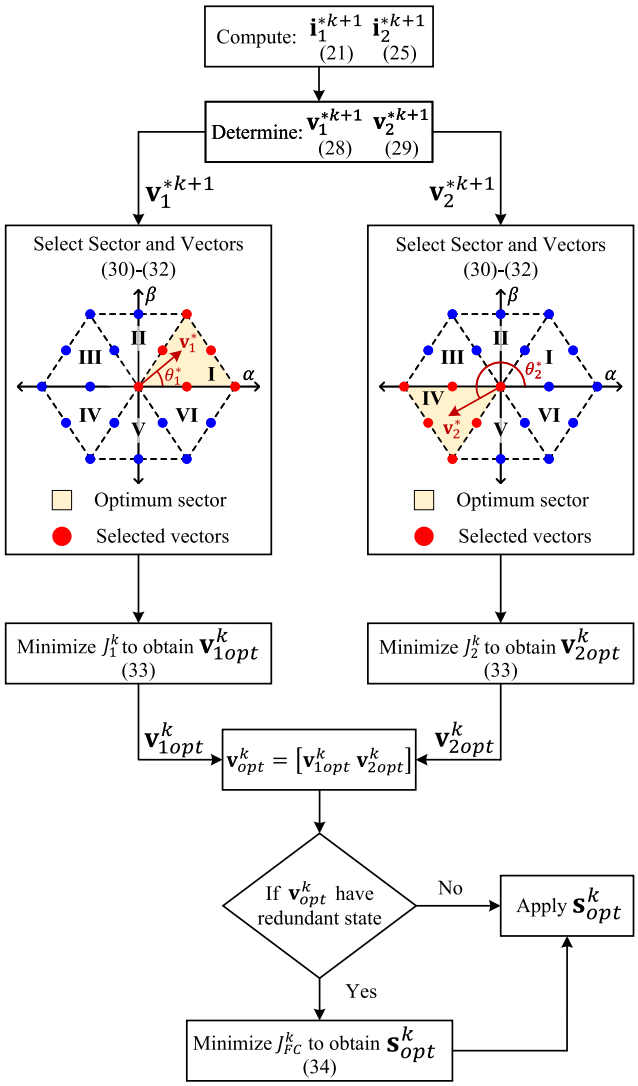


Fig. 5. Flowchart of the proposed CMPC algorithm.

in Section II-F. $\mathbf{i}_1^*$ and $\mathbf{i}_2^*$ are generated to regulate the ac load and dc bus voltages, respectively. Finally, the proposed CMPC algorithm applies optimum switching signals to the converter by minimizing the two output currents and FC voltage errors. The flowchart summarizing the implementation of the proposed CMPC algorithm is shown in Fig. 5. The algorithm operates at a sampling period of T_s. At first, the algorithm reads the system variables and current references $\mathbf{i}_1^*$ and $\mathbf{i}_2^*$. The output voltage vector reference $\mathbf{v}_1^*$ and $\mathbf{v}_2^*$ are then determined from the computed $\mathbf{i}_1^*$ and $\mathbf{i}_2^*$, respectively. Observe that the 2-D space vector of each output port consists of 6 sectors and 19 voltage vectors, where a group of 6 voltage vectors forms a sector [see Fig. 3(a)]. The computed $\mathbf{v}_1^*$ and $\mathbf{v}_2^*$ localize the search for the optimum voltage vectors ($\mathbf{v}_{1\text{opt}}$ and $\mathbf{v}_{2\text{opt}}$) to a sector. This suggests that $\mathbf{v}_{1\text{opt}}$ and $\mathbf{v}_{2\text{opt}}$ can be determined by searching through a finite set of only six voltage vectors. As a result, the CMPC algorithm becomes computationally less intensive when compared to the conventional FCS-MPC approach. Finally, the optimum voltage vector pair $\mathbf{v}_{\text{opt}} = [\mathbf{v}_{1\text{opt}}\ \mathbf{v}_{2\text{opt}}]$ is translated to $\mathbf{s}_{\text{opt}}$ based on the FC voltage regulation. If $\mathbf{v}_{\text{opt}}$ has redundant states, $\mathbf{s}_{\text{opt}}$ that minimizes the FC voltage errors is selected. In case $\mathbf{v}_{\text{opt}}$ is a unique state, the FC minimization is by-passed and $\mathbf{s}_{\text{opt}}$ is applied. Adopting such a strategy not only eliminates the need for weighting factors but also introduces a significant reduction in the controller's computational burden. The stepwise procedure for the implementation of the CMPC algorithm is explained in the following section.

A. Calculating Output Voltage Vector References

The output voltage vector references $\mathbf{v}_1^{*k+1}$ and $\mathbf{v}_2^{*k+1}$ for time instant $k+1$ are determined from the computed $\mathbf{i}_1^{*k+1}$ and $\mathbf{i}_2^{*k+1}$. On setting $\mathbf{i}_1^{k+1} = \mathbf{i}_1^{*k+1}$, and $\mathbf{i}_2^{k+1} = \mathbf{i}_2^{*k+1}$, (12) and (13) can be rewritten as

$$\mathbf{v}_1^{*k+1} = \mathbf{v}_{\text{ac}}^k + \frac{L_{\text{ac}}}{T_s}\left(\mathbf{i}_1^{*k+1} - \mathbf{i}_1^k\right) \text{ and} \tag{28}$$

$$\mathbf{v}_2^{*k+1} = \mathbf{e}^k + \frac{L_g}{T_s}\left(\mathbf{i}_2^{*k+1} - \mathbf{i}_2^k\right). \tag{29}$$

Note that the determined $\mathbf{v}_1^{*k+1}$ and $\mathbf{v}_2^{*k+1}$ need not necessarily belong to the finite set of 19 distinct voltage vectors, as presented in Fig. 3(a).

B. Identifying Optimum Sectors

Observe from the 2-D space vector that each sector is spaced $\frac{\pi}{3}$ rad apart [see Fig. 3(a)]. Thus, the angle between the α and β coordinates of the computed $\mathbf{v}_1^{*k+1}$ and $\mathbf{v}_2^{*k+1}$ provides the information on the optimum sector for the output ports. The angle between the $v_{m\alpha}^{*k+1}$ and $v_{m\beta}^{*k+1}$ can be obtained as

$$\theta_m^{*k+1} = n\pi + \tan^{-1}\left(\frac{v_{m\beta}^{*k+1}}{v_{m\alpha}^{*k+1}}\right), \text{ where} \tag{30}$$

$$n = \begin{cases} 1, & \text{if } v_{m\alpha}^{*k+1} < 0 \\ 2, & \text{if } v_{m\alpha}^{*k+1} > 0\ \&\ v_{m\beta}^{*k+1} < 0 \\ 0, & \text{otherwise.} \end{cases}, \text{ and } m \in \{1,2\}. \tag{31}$$

The resulting θ_m^k determines the optimum sector for the output ports as

$$\text{sector} = \begin{cases} \mathbf{I}, & \text{if } 0 \le \theta_m^{*k+1} < \frac{\pi}{3} \\ \mathbf{II}, & \text{if } \frac{\pi}{3} \le \theta_m^{*k+1} < \frac{2\pi}{3} \\ \mathbf{III}, & \text{if } \frac{2\pi}{3} \le \theta_m^{*k+1} < \pi \\ \mathbf{IV}, & \text{if } \pi \le \theta_m^{*k+1} < \frac{4\pi}{3} \\ \mathbf{V}, & \text{if } \frac{4\pi}{3} \le \theta_m^{*k+1} < \frac{5\pi}{3} \\ \mathbf{VI}, & \text{if } \frac{5\pi}{3} \le \theta_m^{*k+1} < 2\pi \end{cases}, \text{ where } m \in \{1,2\}. \tag{32}$$

Note that the optimum sector selection allows localizing the search for the $\mathbf{v}_{m\text{opt}}^k$ from a set of only six voltage vectors. Fig. 5 demonstrates the optimum sector (shaded region) and the corresponding six voltage vectors (highlighted red) based on the determined $\mathbf{v}_1^{*k+1}$ and $\mathbf{v}_2^{*k+1}$.

C. Computing Optimum Output Voltage Vectors

The optimum output voltage vectors $\mathbf{v}_{1\text{opt}}^k$ and $\mathbf{v}_{2\text{opt}}^k$ are obtained by minimizing J_1^k and J_2^k, respectively. The mathematical definition of minimization is expressed as

$$\underset{\mathbf{v}_m^k \in \mathbb{U}_s^k}{\text{argmin}}\, J_m^k(\mathbf{v}_m^k), \text{ where } m \in \{1, 2\}. \tag{33}$$

Note that $\mathbb{U}_s^k$ is the finite set of six voltage vectors that is dependent on the optimum sector selection, as discussed in Section IV-B. For instance, if sector $\mathbf{I}$ is determined as optimum for output port 1 at time instant k, the proposed approach identifies the $\mathbf{v}_{1\text{opt}}^k$ from the finite set $\mathbb{U}_s^k = \{\mathbf{u_{10}}, \mathbf{u_{13}}, \mathbf{u_{15}}, \mathbf{u_{16}}, \mathbf{u_{18}}, \mathbf{u_{19}}\}$. Thus, the entries of $\mathbb{U}_s$ changes with respect to the optimum sector selection.

D. Obtaining Optimum Switching Signals

The optimum switching signal $\mathbf{s}_{\text{opt}}^k$ is determined based on the obtained $\mathbf{v}_{\text{opt}}^k = [\mathbf{v}_{1opt}^k\ \mathbf{v}_{2opt}^k]$ and the FC voltage regulation. If $\mathbf{v}_{\text{opt}}^k$ has redundant states, $\mathbf{s}_{\text{opt}}^k$ is selected from its redundancies by minimizing J_{FC}^k. The mathematical definition of minimization is expressed as

$$\underset{\mathbf{s}^k \in \mathbb{S}_s^k}{\text{argmin}}\, J_{\text{FC}}^k(\mathbf{s}^k) \tag{34}$$

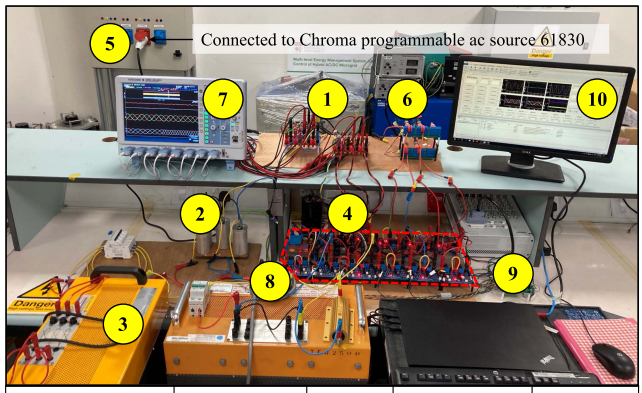
where $\mathbb{S}_s^k$ is the finite set of redundant states, whose size varies from 2 to 16 depending on the obtained $\mathbf{v}_{\text{opt}}^k$ [see Fig. 3(b)]. Thus, the determined $\mathbf{s}_{\text{opt}}^k$ from (34) not only applies the desired $\mathbf{v}_{1\text{opt}}^k$ and $\mathbf{v}_{2\text{opt}}^k$ across the output ports but also ensures that v_{fca}^k, v_{fcb}^k, and v_{fcc}^k are regulated to their references (1). Note that the minimization of J_{FC}^k is by-passed and the corresponding $\mathbf{s}_{\text{opt}}^k$ is applied to the converter when the obtained $\mathbf{v}_{\text{opt}}^k$ is a unique state.

V. Experimental Results

Experimental tests are performed on a low-power FCDO converter in a hybrid microgrid as demonstrated in Fig. 2. The proposed CMPC algorithm is programmed in a dSPACE MicroLabBox 1202 using a MATLAB function block with a sampling time of 80 μs. The experimental setup is shown in Fig. 6. The grid was emulated by a Chroma programmable ac source 61830. The system and control parameters considered are given in Table III. The case studies demonstrating the performance of a three-phase FCDO converter with the proposed CMPC algorithm in a hybrid microgrid during mode transitions and step-load change are elaborated in the following sections.

A. Case Study 1: Precharging C_{dc}, C_{fca}, C_{fcb}, and C_{fcc}

The performance of a three-phase FCDO converter with the proposed CMPC algorithm while precharging its capacitors C_{dc}, C_{fca}, C_{fcb}, and C_{fcc} to their desired references during start-up operation is shown in Fig. 7. Note that the output port 1 is considered nonoperational in this analysis. Until $t = 2$ s, all the variables of the system are zero. At $t = 2$ s, the grid is connected to the output port 2 and CMPC is activated with $V_{\text{dc}}^* = 150$V.



1. Voltage sensors [e_a, e_b, v_{aca}, v_{acb}, v_{dc}, v_{fca}, v_{fcb}, v_{fcc}]	2. ac capacitors [C_{aca}, C_{acb}, C_{acc}]	3. ac load	4. Three-phase FCDO converter	5. Grid
6. Current sensors [i_{1a}, i_{1b}, i_{2a}, i_{2b}]	7. Oscilloscope	8. dc load	9. dSPACE MicroLabBox	10. Host PC

Fig. 6. Experimental prototype of a three-phase FCDO converter in a hybrid microgrid.

TABLE III
Parameters for Experimental Test

System parameters						
E (V)	f_g (Hz)	L_g (mH)	L_{ac} (mH)	C_{ac} (μF)	C_{fcx} (μF)	C_{dc} (mF)
$45\sqrt{2}$	50	6.3	6	50	470	2.2
Control parameters						
N_R^{dc}	N_L^{dc}	V_e^{dc} (V)	N_R^{ac}	N_L^{ac}	V_e^{ac} (V)	T_s (μs)
400	10^6	$0.1V_{dc}^*$	5	200	V_{acd}^*	80
Reference and loading parameters						
Case study	t (s)	V_{dc}^* (V)	R_{dc} (Ω)	V_{acd}^* (V)	f_{ac}^* (Hz)	R_l:L_l (Ω:mH)
1	$2-6$ $6-10$	150 200	250	–	–	–
2	$0-1.5$ $1.5-3.5$ $3.5-5$	200	400	20 30 30	50 50 100	10:0
3	$0-3$ $3-7$ $7-10$	200	400 400 285	30	100	10:0 10:10 10:10

Note: The values for N_R^{dc}, N_L^{dc}, V_e^{dc} and N_R^{ac}, N_L^{ac}, V_e^{ac} are designed based on the procedure presented in [39].

Observe that v_{dc} smoothly converges to the desired reference in less than 500 ms without introducing undesirable oscillations/overshoot. v_{fca}, v_{fcb}, and v_{fcc} are observed to converge to the desired reference of 75 V in less than 200 ms. Thus, the proposed CMPC can smoothly precharge the capacitors to the desired value without any additional control circuitry. The steady-state waveform of the grid voltage and output port 2 current are demonstrated in a zoomed view of Fig. 7. Since the setting $q^* = 0$VAR, e_a, e_b, e_c and i_{2a}, i_{2b}, i_{2c} are observed to be in-phase, thus ensuring UPF operation of the grid.

At $t = 6$s, V_{dc}^* is stepped to 200 V. v_{dc} is observed to converge to 200 V in 500 ms. The v_{fca}, v_{fcb}, and v_{fcc} are also observed

TABLE IV
AVERAGE SWITCHING FREQUENCY OF POWER SWITCHES IN THREE-PHASE FCDO CONVERTER FOR DIFFERENT CASE STUDIES

Case study	t (s)	Average switching frequency (kHz)															
		S_{1a}	S_{2a}	S_{4a}	S_{6a}	S_{7a}	S_{1b}	S_{2b}	S_{4b}	S_{6b}	S_{7b}	S_{1c}	S_{2c}	S_{4c}	S_{6c}	S_{7c}	Converter
1	$2-6$	2.9	2.4	3.2	2.8	2.5	2.9	2.5	3.3	2.9	2.6	2.9	2.6	3.1	2.9	2.6	3.5
	$6-10$	3.5	3.1	3.7	3.6	1.5	3.6	3.1	3.7	3.6	1.5	3.7	3.3	3.8	3.7	1.5	3.9
2	$0-1.5$	3.7	2.8	3.7	3.7	2.6	3.6	2.7	3.7	3.7	2.7	3.7	2.8	3.7	3.7	2.6	4.1
	$1.5-3.5$	3.5	2.6	3.4	3.5	2.8	3.5	2.5	3.3	3.5	2.8	3.5	2.5	3.4	3.5	2.8	3.9
	$3.5-5$	3.5	2.7	3.4	3.3	2.6	3.2	2.5	3.5	3.4	2.6	3.3	2.5	3.5	3.4	2.7	3.8
3	$0-3$	3.5	2.7	3.4	3.3	2.6	3.2	2.5	3.5	3.4	2.6	3.3	2.5	3.5	3.4	2.7	3.8
	$3-7$	3.3	2.8	3.3	3.3	2.6	3.3	2.6	3.4	3.5	2.7	3.3	2.7	3.4	3.4	2.7	3.9
	$7-10$	3.4	2.9	3.4	3.3	2.6	3.5	2.8	3.4	3.4	2.6	3.4	2.8	3.3	3.5	2.6	3.9

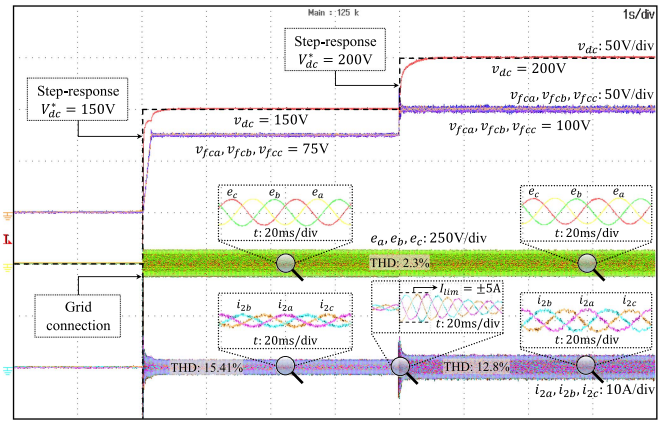
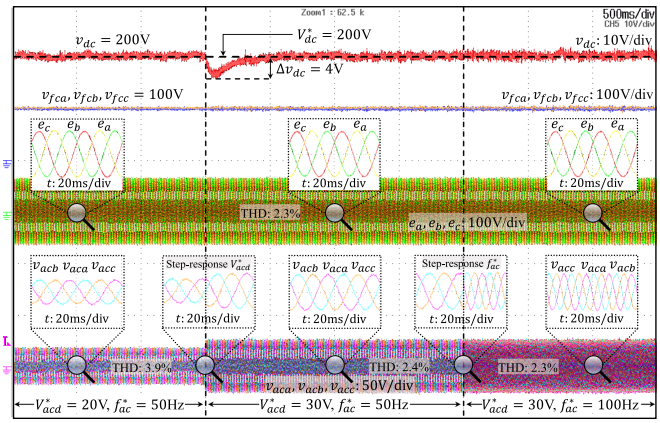
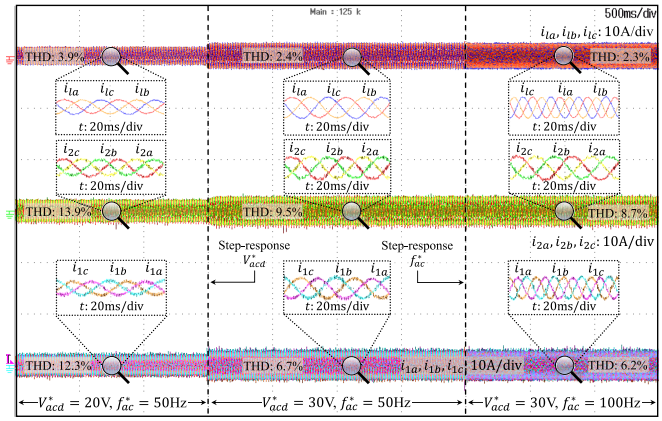


Fig. 7. Experimental results on the performance of a three-phase FCDO converter with the proposed CMPC algorithm in a hybrid microgrid during a step-response of $V_{\rm dc}^{*}$: Operating waveforms $v_{\rm dc}$, $v_{\rm fca}$, $v_{\rm fcb}$, $v_{\rm fcc}$, e_a, e_b, e_c, i_{2a}, i_{2b}, i_{2c}.



(a)



(b)

Fig. 8. Experimental results on the performance of a three-phase FCDO converter with the proposed CMPC algorithm in a hybrid microgrid during a step-response of $\mathbf{V}_{\rm ac}^{*}$ and $f_{\rm ac}^{*}$: (a) Operating voltage waveforms $v_{\rm dc}$, $v_{\rm fca}$, $v_{\rm fcb}$, $v_{\rm fcc}$, e_a, e_b, e_c, $v_{\rm aca}$, $v_{\rm acb}$, $v_{\rm acc}$. (b) Operating current waveforms i_{la}, i_{lb}, i_{lc}, i_{1a}, i_{1b}, i_{1c}, i_{2a}, i_{2b}, i_{2c}.

to attain its desired reference of 100 V during the operation. The dynamics of i_{2a}, i_{2b}, i_{2c} during the step-response in $v_{\rm dc}$ is shown in a zoomed view of Fig. 7. Due to a huge dc bus voltage error $|V_{\rm dc}^{*} - v_{\rm dc}^{k}|$ during the instant of step-response, the ADR model generates large $\mathbf{i}_2^{*}$. The large value of $\mathbf{i}_2^{*}$ can exceed the safe operating conditions of the converter and is required to be clamped to a safer value. This is accomplished by $P_{\rm lim}$ as defined in (24). Hence, the peaks of i_{2a}, i_{2b}, and i_{2c} are limited to $\pm$5A during the transient. As the $|V_{\rm dc}^{*} - v_{\rm dc}^{k}|$ approaches zero, i_{2a}, i_{2b}, and i_{2c} are observed to settle to a steady-state value (see Fig. 7). Since $dv_{\rm fcx}$ is proportional to the magnitude of $\mathbf{i}_2$ (9), the ripple in FC voltage $dv_{\rm fcx}$ is observed to increase when $v_{\rm dc} = 200$ V. The average switching frequency of the converter and its power switches during step-response of $V_{\rm dc}^{*} = 150$ V and $V_{\rm dc}^{*} = 200$ V is shown in Table IV. Due to complementary logic [see (2) and (3)], the power switches S_{3x} and S_{5x} toggles at the same frequency as S_{2x} and S_{4x}, respectively.

B. Case Study 2: Step-Response of AC Load Voltage and Frequency

The performance a three-phase FCDO converter with the proposed CMPC algorithm during a step-response in $\mathbf{V}_{\rm ac}^{*}$ and $f_{\rm ac}^{*}$ is shown in Fig. 8. Until $t = 1.5$ s, the CMPC algorithm operates with references $V_{\rm dc}^{*} = 200$ V, $V_{acd}^{*} = 20$ V, and $f_{\rm ac}^{*} =$ 50 Hz. Note that V_{acq}^{*} is set to zero throughout the operation. The operating voltage and current waveforms are shown in Fig. 8(a) and (b), respectively. The three-phase FCDO converter is observed to operate its dual-output ports at desired references. At $t = 1.5$ s, V_{acd}^{*} is stepped to 30 V. $v_{\rm ac}$ instantly attains the desired reference, as shown in the zoomed view of Fig. 8(a). However, a dip of $\Delta v_{\rm dc} = 4$V is observed in $v_{\rm dc}$ during the transient. The CMPC algorithm corrects $\Delta v_{\rm dc}$ by supplying the necessary power from the grid. This correction can be visualized

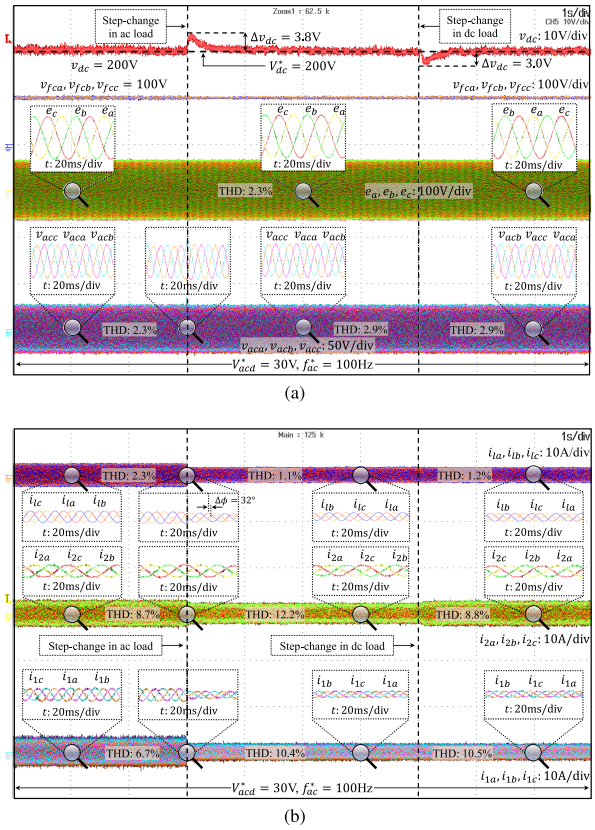


Fig. 9. Experimental results on the performance of a three-phase FCDO converter with the proposed CMPC algorithm in a hybrid microgrid during a step-change in ac and dc loads: (a) Operating voltage waveforms $v_{\rm dc}$, $v_{{\rm fc}a}$, $v_{{\rm fc}b}$, $v_{\rm fcc}$, e_a, e_b, e_c, $v_{{\rm ac}a}$, $v_{{\rm ac}b}$, $v_{\rm acc}$. (b) Operating current waveforms i_{1a}, i_{1b}, i_{1c}, i_{1a}, i_{1b}, i_{1c}, i_{2a}, i_{2b}, i_{2c}.

by the change in current waveforms, as shown in Fig. 8(b). As a result, $v_{\rm dc}$ converges back to its desired reference of 200 V.

At $t = 3.5$s, $f^*_{\rm ac}$ is stepped to 100 Hz. Observe that the converter instantly operates its output port 1 at 100 Hz. Since no additional power is required, a dip is not observed in $v_{\rm dc}$ during the step-response of $f_{\rm ac}$. Observe from Fig. 8 that the three-phase output ports of the FCDO converter operate independently at DAs, DFs, and DPs. Such a feature allows the converter to be a suitable choice to integrate source/loads into a hybrid microgrid without an additional conversion stage. The average switching frequency of the converter and its power switches during step-response in $\mathbf{V}^*_{\rm ac}$ and $f^*_{\rm ac}$ is shown in Table IV.

C. Case Study 3: Step-Change in AC and DC Loads

The performance of a three-phase FCDO converter with the proposed CMPC algorithm during a step-change in ac load and dc load is shown in Fig. 9. In this study, the dc bus and ac load voltage references are set as $V^*_{\rm dc} = 200$ V, and $V^*_{{\rm ac}d} = 30$ V, $V^*_{{\rm ac}q} = 0$ V, $f^*_{\rm ac} = 100$ Hz, respectively. Until $t = 3$ s, the ac load of $R_l = 10\,\Omega$ and the dc load of $R_{\rm dc} = 400\,\Omega$ are considered. Observe that the CMPC algorithm enables the FCDO converter to attain its control objectives during the operation. At $t = 3$ s, the ac load is step-changed by adding $L_l = 10$ mH in series with $R_l = 10\,\Omega$. Due to the sudden increase in ac load impedance Z_l, $v_{\rm dc}$, and $\mathbf{v}_{\rm ac}$ are observed to increase. The CMPC algorithm identifies the change and enables the FCDO converter to correct $v_{\rm dc}$ and $\mathbf{v}_{\rm ac}$ to their desired references, as shown in the zoomed view of Fig. 9(a). The corresponding dual-output currents and ac load current are shown in Fig. 9(b). Since the ac load is $Z_l = 10 + j6.28\,\Omega$, a phase angle difference of 32° is introduced between $\mathbf{v}_{\rm ac}$ and $\mathbf{i}_l$ [see the zoomed view of Fig. 9(b)].

At $t = 7$s, $R_{\rm dc}$ is stepped to $285\,\Omega$. Due to the reduction in $R_{\rm dc}$, a dip of $\Delta v_{\rm dc} = 3$V is observed in $v_{\rm dc}$. The CMPC algorithm corrects $\Delta v_{\rm dc}$ by supplying the necessary power from the grid. Finally, $v_{\rm dc}$ converges back to 200 V in less than 1 s. Observe that the ac load continues to operate at the desired reference and is not affected during the step-change in $R_{\rm dc}$. Hence, the CMPC algorithm effectively realizes its control objectives and ensures an independent operation of the converter's dual-output ports. The average switching frequency of the converter and its power switches during step-change in ac load and dc load is shown in Table IV.

TABLE V
COMPUTATIONAL BURDEN OF ALGORITHMS

Algorithm	T_e (μs)	Computation time plot
FCS-MPC	99.6	T_s, T_e; k, $k+1$; $T_e > T_s$: Task overrun
Proposed CMPC	8	T_s, T_e, T_e; k, $k+1$; $T_e << T_s$

D. Case Study 4: Comparison With FCS-MPC Algorithm

1) Computational Burden: The computational burden of the conventional FCS-MPC and proposed CMPC algorithms is evaluated using a dSPACE MicroLabBox controller. Both the algorithms are programmed in the controller and its execution time T_e is recorded, as shown in Table V. T_e is the time taken by the controller to obtain $\mathbf{s}_{\rm opt}$ in T_s. The controller with the conventional FCS-MPC algorithm takes $T_e = 99.6$ μs to identify $\mathbf{s}_{\rm opt}$. Since $T_e > T_s$, the controller undergoes task overrun and real-time implementation of the conventional FCS-MPC algorithm becomes impossible for $T_s = 80$ μs. This suggests that the conventional FCS-MPC should operate at a higher T_s and incorporate a two-step prediction model to compensate the delay caused by T_e [40]. However, operating FCS-MPC at higher T_s can deteriorate the converter's performance by increasing the THD of the waveform. Another alternative is to use a high-speed controller that can identify $\mathbf{s}_{\rm opt}$ in lesser T_e. However, such an approach introduces additional system cost. On the other hand, the controller with the proposed CMPC algorithm takes only $T_e = 8$ μs to identify the $\mathbf{s}_{\rm opt}$. Note that T_e is only 10% of $T_s = 80$ μs. This is because the proposed CMPC do not search

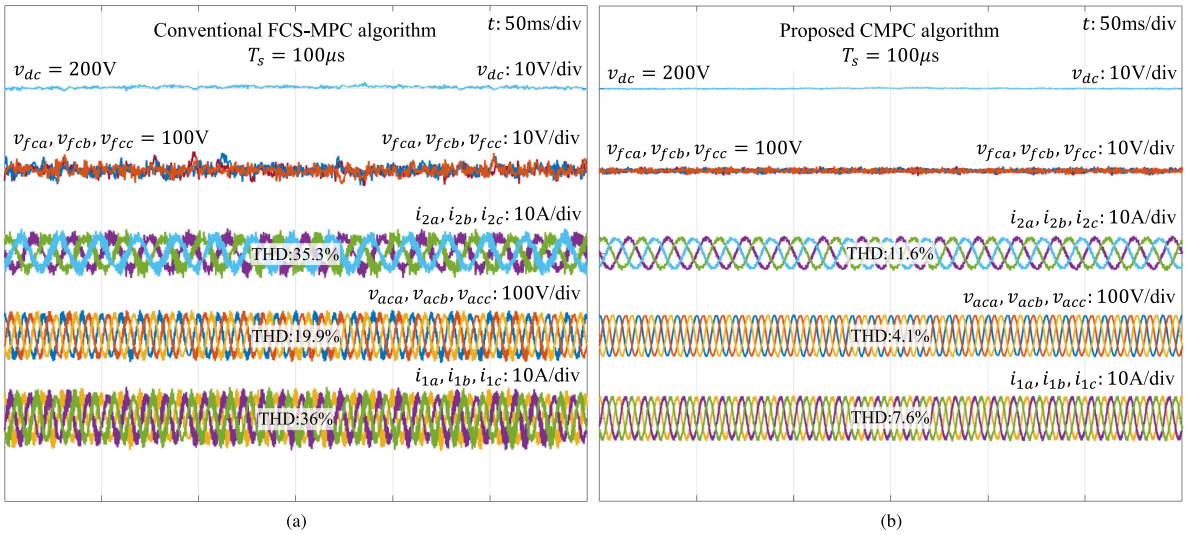


Fig. 10. Performance of a three-phase FCDO converter in a hybrid microgrid using (a) conventional FCS-MPC algorithm with $T_s = 100$ μs and (b) proposed CMPC algorithm with $T_s = 100$ μs.

through the entire set of 1000 states to identify the $\mathbf{s}_{\rm opt}$ in T_s. The CMPC algorithm first identifies $\mathbf{v}_{1\rm opt}$ and $\mathbf{v}_{2\rm opt}$ by searching through a finite set of six voltage vectors and then identifies $\mathbf{s}_{\rm opt}$ by searching through the finite set of redundant states, whose entries vary from 2 to 16 depending on the [$\mathbf{v}_{1\rm opt}$ $\mathbf{v}_{2\rm opt}$] pair [see Fig. 3(b)]. Adopting such a strategy reduces the computational burden of the controller by 91.9%.

2) Performance Metrics: The performance of a three-phase FCDO converter with FCS-MPC and proposed CMPC algorithms is shown in Fig. 10(a) and (b), respectively. Note that a sampling period $T_s = 100$ μs is considered to avoid task overrun of the FCS-MPC algorithm and ensure a fair comparison with the proposed CMPC algorithm. Even though the FCS-MPC and CMPC algorithms effectively regulate the variables to their desired references, their effect on the converter's performance metrics, such as THD and ripples, differ significantly. The differences in the performance metrics arise due to the effect of computational delay caused by the controller, as discussed in Section V-D1. Since $T_e = 99.6$ μs for the FCS-MPC algorithm is significant compared to $T_s = 100$ μs, there will be a huge delay between the instant when variables are measured and instant when the optimum state is applied [40]. Thus, converter's performance is deteriorated and large ripples are introduced on its variables. As a result, the converter with the FCS-MPC algorithm exhibits a deteriorated current and voltage waveform compared to the proposed CMPC algorithm.

VI. Conclusion

This article proposed a CMPC algorithm for a three-phase FCDO converter in a hybrid microgrid. The FCDO converter integrated grid and ac load operating at different voltage magnitudes and frequencies through its output ports. Adopting FCDO converter in a hybrid microgrid eliminated the need for multiple conversion stages in the ac side, thereby reducing the total power component count and control complexities. The CMPC algorithm was developed to control the multiple variables of the FCDO converter in a hybrid microgrid. Unlike conventional FCS-MPC, the CMPC algorithm fulfilled the multiple control objectives at a reduced computational burden and eliminated the need for weighting factors in the cost function. This was accomplished by the sequential execution of multiple single-objective MPC units. At first, the dual-output voltage vector pair $\mathbf{v}_{1\rm opt}$, $\mathbf{v}_{2\rm opt}$ was obtained by minimizing the output current errors individually. The obtained $\mathbf{v}_{1\rm opt}$, $\mathbf{v}_{2\rm opt}$ was translated to $\mathbf{s}_{\rm opt}$ by minimizing the FC voltage error. The appropriate $\mathbf{i}_1^*$ for $v_{\rm dc}$ regulation and appropriate $\mathbf{i}_2^*$ for $\mathbf{v}_{\rm ac}$ regulation was generated by the ADR model. Finally, the effectiveness of the proposed CMPC algorithm was demonstrated experimentally on a low-power FCDO converter in a hybrid microgrid under various conditions.

References

[1] X. Liu, P. Wang, and P. C. Loh, "A hybrid AC/DC micro-grid," in *Proc. IEEE Int. Power Electron. Conf.*, 2010, pp. 746–751.

[2] R. A. Kaushik and N. M. Pindoriya, "A hybrid AC-DC microgrid: Opportunities and key issues in implementation," in *Proc. Int. Conf. Green Comput. Commun. Elect. Eng.*, 2014, pp. 1–6.

[3] Y. Shan, J. Hu, K. W. Chan, Q. Fu, and J. M. Guerrero, "Model predictive control of bidirectional DC–DC converters and AC/DC interlinking converters—A new control method for PV-wind-battery microgrids," *IEEE Trans. Sustain. Energy*, vol. 10, no. 4, pp. 1823–1833, Oct. 2019.

[4] Y. Shan, J. Hu, M. Liu, J. Zhu, and J. M. Guerrero, "Model predictive voltage and power control of islanded PV-battery microgrids with washout-filter-based power sharing strategy," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1227–1238, Feb. 2020.

[5] M. Najafzadeh, R. Ahmadiahangar, O. Husev, I. Roasto, T. Jalakas, and A. Blinov, "Recent contributions, future prospects and limitations of interlinking converter control in hybrid AC/DC microgrids," *IEEE Access*, vol. 9, pp. 7960–7984, 2021.

[6] Bo Zhang and D. Qiu, "Multiple-input multiple-output high-voltage AC–AC converters," in *Multi-Terminal High-Voltage Converter*. Hoboken, NJ, USA: Wiley, 2019, pp. 113–133.

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[8] Z. Kehl and T. Glasberger, "Analysis of three-level neutral point piloted power converter topology," in *Proc. IEEE Int. Conf. Appl. Electron.*, 2018, pp. 1–4.
[9] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.
[10] T. Kominami and Y. Fujimoto, "A novel nine-switch inverter for independent control of two three-phase loads," in *Proc. IEEE Ind. Appl. Annu. Meeting*, 2007, pp. 2346–2350.
[11] T. Kominami and Y. Fujimoto, "Inverter with reduced switching-device count for independent AC motor control," in *Proc. 33rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2007, pp. 1559–1564.
[12] A. M. Rauf and V. Khadkikar, "Integrated photovoltaic and dynamic voltage restorer system configuration," *IEEE Trans. Sustain. Energy*, vol. 6, no. 2, pp. 400–410, Apr. 2015.
[13] L. Zhang, P. C. Loh, and F. Gao, "An integrated nine-switch power conditioner for power quality enhancement and voltage sag mitigation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1177–1190, Mar. 2012.
[14] H. Bizhani et al., "Current stress and switching loss evaluation of a unified expandable power converter used for grid-integration of renewable energy sources," *IET Renewable Power Gener.*, vol. 15, no. 12, pp. 2561–2570, May 2021.
[15] H. Bizhani, S. M. Muyeen, F. R. Tatari, K. Techato, L. Ben-Brahim, and F. Blaabjerg, "Current rating analysis of a nine-switch based unified expandable power converter considering different configurations," in *Proc. IEEE Int. Conf. Smart Power Internet Energy Syst.*, 2020, pp. 426–430.
[16] H. Bizhani, R. Noroozian, S. M. Muyeen, and F. Blaabjerg, "Wind farm grid integration architecture using unified expandable power converter," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3407–3417, Apr. 2019.
[17] S. Vazquez et al., "Model predictive control: A review of its applications in power electronics," *IEEE Ind. Electron. Mag.*, vol. 8, no. 1, pp. 16–31, Mar. 2014.
[18] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control—A simple and powerful method to control power converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1826–1838, Jun. 2009.
[19] V. Jayan and A. Ghias, "Finite control set model predictive control of a nine switch dual output converter as a power quality conditioner," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2019, pp. 1241–1246.
[20] S. S. Lee, Y. E. Heng, and M. A. Roslan, "Finite control set model predictive control of nine-switch AC/DC/AC converter," in *Proc. IEEE Int. Conf. Power Energy*, 2016, pp. 746–751.
[21] O. Gulbudak and E. Santi, "Model predictive control of dual-output nine-switch inverter with output filter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1582–1589.
[22] S. S. Lee and Y. E. Heng, "Predictive control of power flow between two islanded microgrids using nine-switch converter," *J. Renewable Sust. Energy*, vol. 8, no. 5, Sep. 2016, Art. no. 055502.
[23] V. Jayan and A. Ghias, "Cascaded dual output multilevel converter to enhance power delivery and quality," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 2910–2915.
[24] V. Jayan, A. S. Hussein, and A. Ghias, "Model predictive control of cascaded multi-output multilevel converter," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2019, pp. 1247–1251.
[25] P. Cortes et al., "Guidelines for weighting factors design in model predictive control of power converters and drives," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2009, pp. 1–7.
[26] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, Feb. 2017.
[27] C. Xia, T. Liu, T. Shi, and Z. Song, "A simplified finite-control-set model-predictive control for power converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 2, pp. 991–1002, May 2014.
[28] Y. Yang et al., "Computationally efficient model predictive control with fixed switching frequency of five-level ANPC converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 11903–11914, Dec. 2022.
[29] P. R. U. Guazzelli et al., "Dual predictive current control of grid connected nine-switch converter applied to induction generator," in *Proc. IEEE Int. Conf. Ind. Appl.*, 2018, pp. 1038–1044.
[30] P. R. U. Guazzelli et al., "Decoupled predictive current control with duty-cycle optimization of a grid-tied nine-switch converter applied to an induction generator," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2778–2789, Mar. 2022.
[31] L. Pan, J. Zhang, J. Zhang, K. Wang, Y. Pang, and B. Wang, "A new three-level neutral-point-clamped fifteen-switch inverter for independent control of two three-phase loads," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2870–2885, Sep. 2020.
[32] A. S. Hussein, V. Jayan, and A. Ghias, "Modeling and control of a three-level dual output voltage converter," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2019, pp. 1215–1219.
[33] A. S. Hussein and A. Ghias, "Reduced switch count dual-output T-type multilevel converter," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc.*, 2020, pp. 1437–1442.
[34] R. Wang, L. Ai, and C. Liu, "A novel three-phase dual-output neutral-point-clamped three-level inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7576–7586, Jul. 2021.
[35] J. Haruna and N. Hoshi, "A novel three-level inverter which can drive two PMSMs," in *Proc. 7th IET Int. Conf. Power Electron, Mach., Drives*, 2014, pp. 1–6.
[36] F. Gao, L. Zhang, D. Li, P. C. Loh, Y. Tang, and H. Gao, "Optimal pulsewidth modulation of nine-switch converter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2331–2343, Sep. 2010.
[37] V. Jayan and A. M. Y. M. Ghias, "Operational limits of a cascaded dual-output multilevel converter using model predictive control," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7026–7037, Jun. 2021.
[38] S. Yousofi-Darmian and S. M. Barakati, "Compact dual-output inverter based on flying-capacitor: Modelling, control, and prototypevalidation," *IET Power Electron.*, vol. 12, no. 7, pp. 1825–1832, Jun. 2019.
[39] V. Jayan, A. M. Y. M. Ghias, J. M. Guerrero, and A. Merabet, "An adaptive dynamic reference control for power converters in a microgrid," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9164–9174, Aug. 2022.
[40] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 1323–1325, Feb. 2012.
[41] T. Dragičević and M. Novak, "Weighting factor design in model predictive control of power electronic converters: An artificial neural network approach," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8870–8880, Nov. 2019.
[42] M. Babaie, M. Mehrasa, M. Sharifzadeh, and K. Al-Haddad, "Floating weighting factors ANN-MPC based on Lyapunov stability for seven-level modified PUC active rectifier," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 387–398, Jan. 2022.

Vijesh Jayan (Member, IEEE) received the Ph.D. degree in power engineering from Nanyang Technological University, Singapore, in 2022, and the B.Tech. degree in electrical and electronics engineering from the National Institute of Technology Puducherry, Puducherry, India, in 2016.

He is currently a Research Scientist for Power Electronics with Hitachi Energy Research Centre, Sweden. From 2016 to 2018, he was a Technical Trainee under Nuclear Power Division, Lloyd's Register Energy Pvt., Ltd., Mumbai, India. His research interests include power converter topologies, model predictive control, renewable energy systems, and power quality.

Amer Mohammad Yusuf Mohammad Ghias (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from Saint Cloud State University, St Cloud, MN, USA, in 2001, the M.Eng. degree in telecommunications from the University of Limerick, Limerick, Ireland, in 2006, and the Ph.D. degree in electrical engineering from the University of New South Wales (UNSW), Sydney, NSW, Australia, in 2014.

From February 2002 to July 2009, he had held various positions, such as Electrical Engineer, Project Engineer, and Project Manager while working with the top companies in Kuwait. He was with UNSW during 2014–2015, and the University of Sharjah, United Arab Emirates, during 2015–2018. In 2018, he joined the Nanyang Technological University as an Assistant Professor. He is also a Cluster Director (Power Electronics and the Energy Management) for Energy Research Institute @ NTU (ERI@N), Singapore. His research interests include model predictive control, hybrid energy storage, renewable energy sources, multiphase drives, new multilevel converters, and advanced modulations for the multilevel converter.

Dr. Amer is an Editor for *IET Power Electronics*.