Burst Mode Control of Active-Power-Decoupling Integrated Active Clamp Flyback PFC Rectifiers

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***Abstract*—To mitigate the bulky and heavy twice-line frequency power buffer in single-phase power-factor-correction (PFC) rectifiers while maintaining a lower cost, active-power-decoupling integrated active clamp flyback (iACF) PFC rectifier is recently proposed in the literature. The solution inherits all the benefits of conventional ACF converters such as low component count, leakage energy recycling, and soft-switching while being able to reduce the size of the power buffer in the system without hardware modifications. However, existing modulation and control strategies, based on continuous-conduction-mode (CCM), can only achieve a high efficiency at heavy load but not at light load. This article proposes a new modulation to improve the light-load efficiency of iACF PFC rectifiers. By combining CCM and burst mode of operation, this new modulation method can maintain all good features of CCM while effectively reducing the operating frequency, thus reducing the switching losses of the system at light load. This article, first, reviews the existing light-load modulation methods for ACF converters and limitations of applying these methods to iACF are highlighted. The detailed operating principles of the proposed modulation method are explained, and controller implementation that supports simultaneous full-load, medium load and ultralight load operation is developed. A 100-W laboratory iACF prototype is developed to verify the feasibility of the proposal, showcasing a 4-point average efficiency 91.9%, superior to the conventional two-stage solutions.**

***Index Terms*—Ac–dc converters, active power decoupling, burst, efficiency, light load, power factor, soft switching.**

I. Introduction

SINGLE-PHASE ac–dc converters are extensively utilized in applications such as consumer electronics and LED lighting. In these applications, it is highly desirable to achieve a high efficiency and a high density at a low cost.

When power level exceeds 75 W, power factor correction (PFC) is mandatory [1]. A two-stage power-conversion architecture [2], consisting of a PFC converter and an isolated dc–dc converter, is generally the de-facto solution in this power range. One key limitation of the two-stage solution is its relatively higher component count and thus a higher cost. To reduce the bill of materials, many single-stage schemes have been proposed. The idea is to integrate the function of PFC and isolated output voltage regulation in a single power-conversion stage [3], [4], [5], [6]. Most reported single-stage PFC converters, however, cannot outperform their two-stage counterpart in terms of efficiency and power density. One key reason is that these single-stage solutions can only buffer the double-line frequency ripple power (inherent with single-phase systems) at the dc output instead of at the dc bus as the two-stage solutions do. Power buffering at the dc output [see Fig. 1(a)] will lead to two challenges: 1) bulky buffer capacitor. The reason is that the dc output is directly connected to the load, typically with stringent voltage ripple requirements, leading to increased energy storage requirements in the output capacitors [7]. 2) High secondary-side conduction losses. The reason is that the instantaneous power passing on to secondary side of these single-stage PFC solutions can be twice as high as that of the two-stage PFC converters, leading to significantly increased secondary-side current, conduction losses, and low efficiency [4].

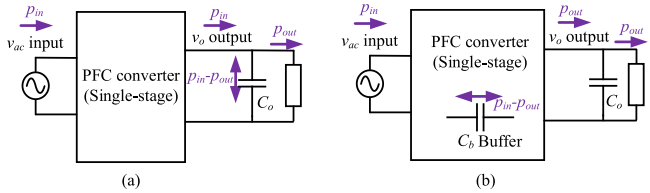

Fig. 1. Single-stage PFC converter. (a) Power buffering at the dc output. (b) Integrated active power decoupling.

To tackle the abovementioned challenges, a recent trend is to integrate active power decoupling (APD) function [8] into these single-stage topologies, allowing power buffering at locations rather than the dc output without hardware modifications. The basic principle of APD integration is to leverage the energy storage capability of some internal capacitors (instead of the output capacitor) in those circuits to perform power buffering [see Fig. 1(b)]. The APD integration concepts have been successfully demonstrated in many single-stage PFC topologies, e.g., bridgeless Cuk rectifier [9], three-level buck rectifier [10], and active-clamp flyback (ACF) converter [11]. Among them, APD-integrated ACF converter (iACF herein), which has the same topology as ACF converter (see Fig. 2) has huge potential to outperform both conventional single-stage [4] and two-stage PFC solutions [12] in terms of efficiency, density, and cost. Particularly, iACF inherits all the benefits of ACF converter such

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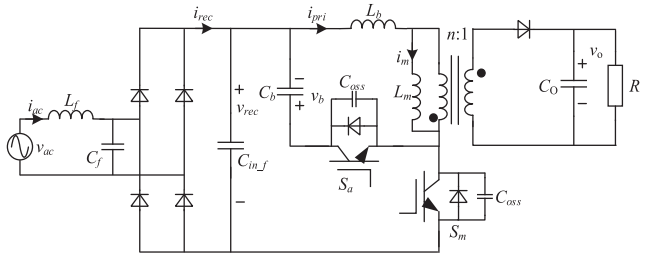

Fig. 2. Circuit topology of iACF converter.

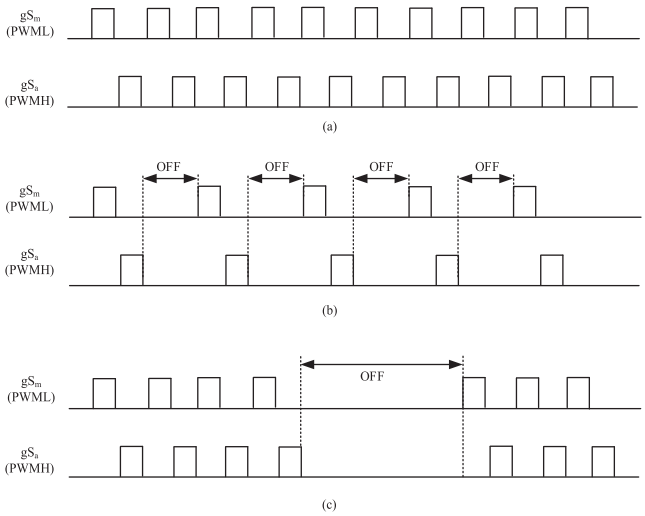

Fig. 3. Operating mode. (a) Normal (CCM). (b) DCM. (c) burst mode.

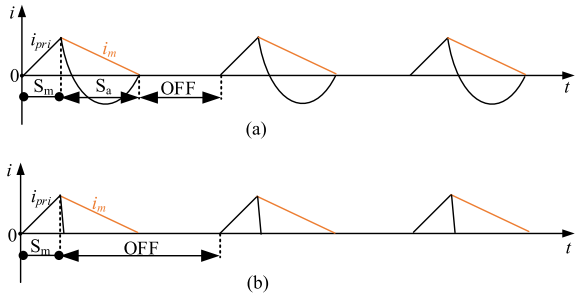

Fig. 4. Modulation pattern in DCM of ACF. (a) S_m and S_a. (b) S_m.

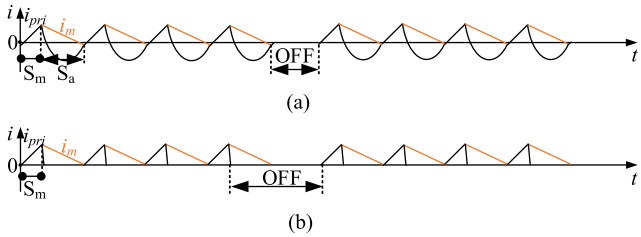

Fig. 5. Modulation pattern in burst mode of ACF. (a) S_m and S_a. (b) S_m.

as simple structure, leakage energy recycling and soft-switching while being able to substantially reduce the energy storage requirement in the system.

Some early investigations have been made into the iACF converter [11]. It is shown that the efficiency of the iACF converter is high at full load but can be substantially reduced at light load with the existing circuit modulation method (i.e., continuous conduction mode, or CCM), see Fig. 3(a). The reason for the reduced efficiency at light load is that the operating frequency of iACF with CCM modulation increases sharply with the decrease of the load, leading to greater switching losses. In many applications, such as external power supply, the average efficiency plays a more important role than the full-load efficiency for the sake of energy saving [13]. Thus, improving the light-load efficiency is critical for iACF.

Conventionally, DCM/Burst mode operation can be adopted to improve the system's light load efficiency [see Fig. 3(b) and (c), respectively]. However, we show (see Section II) that most existing control and DCM/Burst modulation methods [14], [15], [16], [17], [18], [19], [20], including the light load control strategies of ACF converters [21], [22], [23], cannot be directly applied to iACF converter. In particular, we show that existing light-load control and modulation methods can lead to loss of APD function and increased switching losses. In this article, new light-load modulation patterns and control methods are proposed for iACF converter. Different from existing modulation patterns of ACF, the proposed modulation pattern hybrids the CCM and burst mode, achieving reduced current stress, switching losses while maintaining the functions of APD, PFC, and output voltage regulation. The light-load efficiency is improved and can be implemented with simplicity.

The rest of this article is organized as follows. Section II discusses existing switching patterns of ACF. Section III proposes new modulations patterns. Section IV puts forward control strategies to realize the control mode based on proposed modulation patterns. Section V discusses the practical parameters design. Section VI reports the experimental validation. Finally, Section VII concludes this article.

II. Existing Modulation Patterns of Burst Mode and DCM

To appreciate the fact that existing light-load modulation methods for ACF converters cannot be directly applied to iACF converters, a critical review of these methods and issues related to applying these methods to iACF converters are discussed in this section. Both gate driving signals and inductor currents (including primary current $i_{\rm pri}$ and magnetizing current $i_{\rm m}$ annotated in Fig. 2) are highlighted to differentiate these modulation methods.

A. Existing Light-Load Modulation Patterns of ACF Converters

In general, light-load modulation methods for ACF converters can be classified into two categories 1) the DCM modulation patterns (see Fig. 4), and 2) burst mode modulation patterns (see Fig. 5). Among the state-of-the-art ACF commercial ICs,

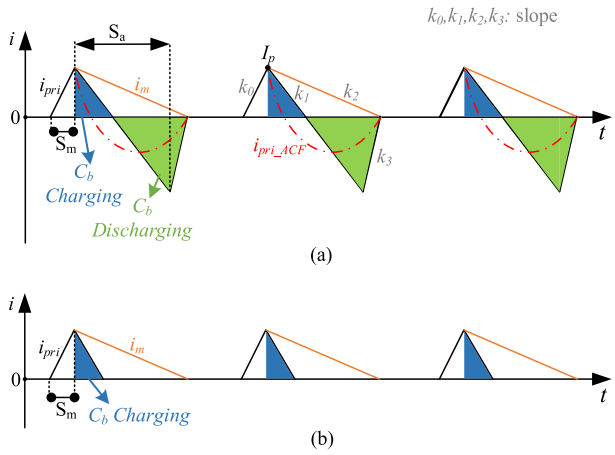

Fig. 6. Modulation patterns in DCM of iACF. (a) Based on Fig. 4(a). (b) Based on Fig. 4(b).

NCP1568 (Onsemi) [21] adopts the modulation patterns in Fig. 4, while UCC28780 (TI) [22] and UCC28782 (TI) [23] adopt the modulation patterns in Fig. 5.

Both modulation patterns of DCM and burst mode involve a converter active phase and a converter inactive phase. During the active phase, S_m or S_a is turned ON; during the inactive phase, all switches are turned OFF. To maximize efficiency, S_m and S_a are often controlled in a way such that i_m and i_{pri} roughly intersect at 0 A. The main difference between DCM operations and burst mode operations is that there is only a single pulse of switching signal pair (i.e., gS_m and gS_a) between OFF intervals with DCM operations, while there are multiple consecutive pulses of switching signal pair between OFF intervals with burst mode operations. The multiple consecutive pulses under burst mode effectively make ACF work as critical conduction mode (CRM) between OFF intervals.

The difference between Figs. 4(a), 5(a) and Figs. 4(b), 5(b) is that S_a is periodically turned ON and OFF in Figs. 4(a) and 5(a) while constantly OFF in Figs. 4(b) and 5(b) to improve efficiency, through the reduction of the gate-driving and switching losses of S_a.

B. Limitations of Existing Modulation Patterns

Although having identical circuit topology to ACF converter, iACF converter cannot leverage the abovementioned modulation patterns of ACF to improve its light load performance. Specifically, the following conditions hold.

1) *Modulation pattern in* Fig. 4(a)*:* Directly applying this modulation pattern to iACF will lead to two issues: a) incapable of simultaneous APD and active PFC functions and b) high switching losses.
   a) Incapable of simultaneous APD and active PFC: To show this, we first present Fig. 6(a), which shows the operating waveforms of an iACF converter (highlighted in solid lines), in comparison to those of conventional ACF converters (highlighted in red dotted lines). As an iACF converter demands a much greater C_b (which is used to buffer the double-line frequency pulsating power) than ACF converter does, the resonant period of the equivalent circuit of iACF while S_a is ON (formulated by L_b and C_b) becomes excessively longer, leading to an almost linearly decreasing i_{pri} current profile. Particularly, the decreasing slope k_1 can be approximated by

$$k_1 = \frac{v_{Lm} - v_b}{L_b} \tag{1}$$

which is constant, where $v_{Lm} = nV_o$ is the voltage applied to L_m. Here, both v_b and v_{Lm} can be assumed constant within one switching cycle T_{sw} since the switching frequency f_{sw} in iACF is much faster than dynamics of V_o and v_b. In contrast, a typical ACF converter features a resonant process with a gradually curved up i_{pri} current profile while S_a is ON. Suppose that T_{sm} is the ON time of S_m, and T_{sa} is the ON time of S_a, and k_0, k_1, k_2, k_3 are the current slopes annotated in Fig. 6(a). Then, the positive peak of i_{pri} of iACF is

$$I_p = k_0 T_{Sm}. \tag{2}$$

Meanwhile, since i_m and i_{pri} roughly intersect at 0 A, we have

$$I_p + k_1 T_{Sa} + k_3 \left(\frac{I_p}{k_2} - T_{Sa} \right) = 0. \tag{3}$$

Combining (2) and (3) gives

$$T_{Sm} = \frac{(k_3 - k_1)k_2}{(k_2 + k_3)k_0} T_{Sa}. \tag{4}$$

Eq. (4) suggests that there is only one control freedom in the system, i.e., either T_{Sm} or T_{Sa} can be independently controlled but not both. With only one control freedom, the PFC system cannot realize simultaneous APD and active PFC [24]. For example, if T_{Sm} is used to perform PFC function (i.e., regulating i_{ac}), T_{Sa} will then be determined by (4) and cannot be flexibly varied, losing the active discharging capability of C_b. Unfortunately, APD function relies on the capabilities of both active charging and discharging of C_b.
   b) High switching losses: The turn-ON of S_m can only achieve ZCS but not ZVS, leading to increased switching losses at high switching frequency.
2) *Modulation pattern in Fig. 4(b):* Directly applying this modulation pattern to iACF will also lose APD capability. As shown in Fig. 6(b), the charging current of C_b with such a modulation pattern will always be positive, meaning that only active charging of C_b is possible. Additionally, the problem of ZVS switching of S_m inherent with DCM operation is not solved.
3) *Modulation pattern in Fig. 5(a):* This modulation pattern consists of N consecutive CRM switching pulses before one OFF interval per burst period. However, similar to that shown in Fig. 6(a), the same issues will occur except that S_m can realize N-1 ZVS turn-ON per N switching pulses.

TABLE I
LIMITATIONS OF EXISTING PATTERNS FROM ACF

Modulation Patterns	Type	Main Limitations
Fig. 4(a)	DCM	Loss of APD function and high switching losses
Fig. 4(b)	DCM	Loss of APD function and high switching losses
Fig. 5(a)	Burst mode	Loss of APD function
Fig. 5(b)	Burst mode	Loss of APD function and high switching losses

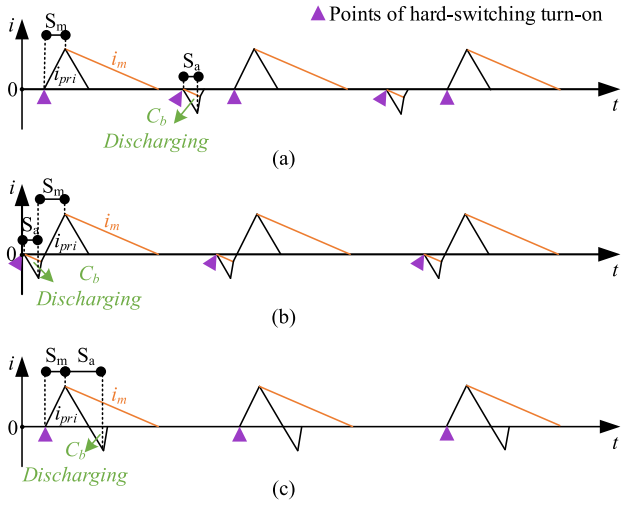

Fig. 7. Improved switching patterns. (a) Solution I. (b) Solution II. (c) Solution III.

4) *Modulation pattern in* Fig. 5(b)*:* Similar to Fig. 6(b), this modulation pattern will result in the same issues of losing APD function and increased switching losses.

Table I summarizes the issues of applying the existing modulation patterns of ACF converter to iACF converter.

C. Other Improved Modulation Patterns

To solve the problems in Table I, other advanced modulation patterns proposed for the control of ACF converter [13] are discussed here. The idea is to provide a flexible $C_{\rm b}$ discharging interval by turning on S_a before or after the turn-ON or turn-OFF of $S_{\rm m}$ (see Fig. 7). This modulation method differs from that shown in Figs. 4(a) and 5(a) in that the ON time of S_a is flexible, as there is no need to ensure $i_{\rm m}$ and $i_{\rm pri}$ to intersect at 0 A. As the result of the flexibility, i) the ON time of $S_{\rm a}$ can be used as an active control variable, and thus, the modulation patterns of Fig. 7 can provide both active charging and discharging of $C_{\rm b}$, thereby allowing iACF converter to achieve APD function, ii) the ON time of $S_{\rm a}$ can be reduced as compared to the modulation pattern in Fig. 6(a), leading to lower current stress, which is proportional to the ON time of $S_{\rm a}$. However, these modulation patterns will lead to at least one hard-switching turn-ON per DCM cycle [i.e., twice for Fig. 7(a) and once for Fig. 7(b) and (c)], resulting in increased switching losses.

The improved DCM modulation patterns in Fig. 7 can be further extended to burst modulation patterns. However, the frequent hard-switching turn-ON problem is not solved, i.e., at least one hard-switching turn-ON per burst period, thus, cannot be applied to iACF converters for light load efficiency improvement.

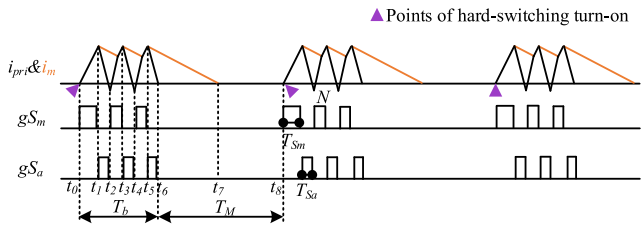

Fig. 8. Proposed modulation pattern (pattern I).

III. PROPOSED MODULATION PATTERNS

A. Novel Modulation Pattern

Fig. 8 illustrates the proposed modulation pattern, which essentially combines the CCM and burst mode of operation. Particularly, the new modulation pattern is comprised of N pairs of consecutive complementary gate-driving pulses ($gS_{\rm m}$ and $gS_{\rm a}$), followed by one OFF interval $T_{\rm M}$, per burst period. Compared to Figs. 4 and 5, the ON time of both $S_{\rm m}$ and $S_{\rm a}$ can be independently controlled, thereby offering similar benefits as the modulation patterns of Fig. 7 do, including the APD function and reduced current stress. Different from Fig. 7, however, the system operates similarly to CCM operation before $T_{\rm M}$. Therefore, the turn-ON of $S_{\rm m}$ for all the N pulse signals can realize ZVS, except for the first one, which can only realize ZCS. As a result, the occurrences of hard-switching turn-ON of S_m can be decreased to once per N pairs of driving pulses. In summary, the proposed modulation pattern can realize simultaneous APD function, low current stress, and low switching losses.

B. Operating States

Assuming each burst period consists of $N = 3$ complimentary gate-driving pulses and one $T_{\rm M}$, and neglecting the dead time, there are eight operating states associated with the proposed modulation pattern for iACF converter.

State I [t_0-t_1]: At t_0, $S_{\rm m}$ is turned ON under ZCS. Both $i_{\rm pri}$ and $i_{\rm m}$ increase linearly at a rate of

$$\frac{di_{pri}}{dt} = \frac{di_m}{dt} = \frac{v_{rec}}{L_m + L_b} \tag{5}$$

where $v_{\rm rec}$ is the rectified input voltage, as defined in Fig. 2.

State II [t_1-t_2]: At t_1, $S_{\rm m}$ is turned OFF, and $S_{\rm a}$ is turned ON under ZVS. As the output diode on the secondary side is forward biased, then $v_{\rm Lm} = -nv_{\rm o}$, and $i_{\rm pri}$ and $i_{\rm m}$ decrease at different rates shown in (6) and (7), respectively. During this state, $C_{\rm b}$ is first charged when $i_{pri} > 0$, and discharged once the polarity of $i_{\rm pri}$ reverses

$$\frac{di_{pri}}{dt} = -\frac{v_b - nv_o}{L_b} \tag{6}$$

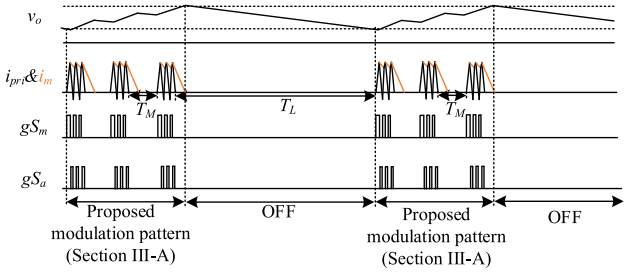

Fig. 9. Extended modulation pattern.

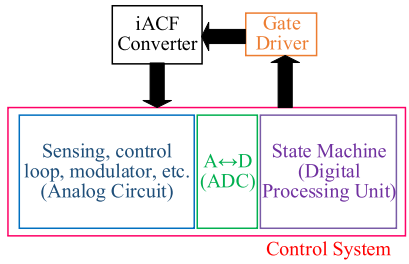

Fig. 10. Simplified control blocks with the mixed ICs' structure.

$$\frac{di_m}{dt} = -\frac{nv_o}{L_m}. \tag{7}$$

State III [t_2-t_3]: At t_2, S_a is turned OFF, and S_m is turned ON under ZVS as $i_\mathrm{pri} < 0$. i_m first decreases at the same rate as (7) in State II, but i_pri increases at rate of

$$\frac{di_{pri}}{dt} = \frac{v_{rec} + nv_o}{L_b}. \tag{8}$$

When i_pri equals i_m, both i_pri and i_m increase at a rate of (5).

State IV [t_3-t_4]: Identical to State II.

State V [t_4-t_5]: Identical to State III.

State VI [t_5-t_6]: At t_5, S_m is turned OFF. S_a is turned ON under ZVS as $i_\mathrm{pri} > 0$, and i_pri decreases at a rate of (6), and i_m decreases at a rate of (7). At t_6, when i_pri decreases to 0, S_a is turned OFF under ZCS. Here, the driving pulse of S_a during this state serves the function of the synchronous rectifier. This gate driving pulse of S_a can be disabled to simplify the control without influencing the circuit operation.

State VII [t_6-t_7]: i_m keeps decreasing at the same rate as (7) until $i_\mathrm{m} = 0$.

State VIII [t_7-t_8]: All switches are disabled.

C. Extended Modulation Pattern for Ultralight Load and No Load

When the load is further decreased, we further propose an extended modulation pattern, which adopts the concept of skip mode operation to avoid the audible noise [21]. As shown in Fig. 9, the extended modulation pattern consists of multiple Section III-A's modulation gate driving pulses and another OFF interval T_L. T_L is typically long to drive the frequency of skip mode far below the audible range. In the skip mode, T_L will be actively controlled to ensure v_o's ripple to stay within specifications, and T_M will be fixed to simplify the control. The extended modulation pattern still retains the key features of the proposed modulation pattern of Fig. 8, including APD function, low current stress, and low switching losses.

To differentiate the two proposed modulation patterns, Figs. 8 and 9 are, respectively, named Mburst mode and Lburst mode hereafter, targeting medium load operation, and ultralight load/no load operation, respectively.

IV. Control Realization

A. Overview of Control System

Based on the design specifications of mixed ICs, Fig. 10 illustrates the hardware architecture of the control system to realize the proposed Mburst and Lburst mode modulation patterns. The control system consists of an analog circuit, an analog-to-digital converter (ADC), and a digital processing unit (DPU). The analog circuit is to dynamically determine the ON-time of S_a and S_m based on the sensed system's state variables to regulate system's operation; the ADC is to discretize several key intermediate variables from the analog circuit; and the DPU is to implement a state machine based on the ADC signals and output signals of analog circuit to facilitate modulation patterns (i.e., CCM, Mburst, and Lburst mode).

B. Control Variables Selection

The control system aims to support three modulation patterns, including CCM, Mburst, and Lburst and their smooth transitions. Therefore, it will be more convenient to select control variables, which are common to all three modes of modulation. As per the operating principles of each modulation pattern, the respective control variables are as follows:

CCM: T_Sa and T_Sm;
Mburst: T_Sa, T_Sm, N, and T_M;
Lburst: T_Sa, T_Sm, N, T_M, and T_L.

Therefore, T_Sa and T_Sm, which are common to all modulation patterns can be selected as the control variables of iACF. Other variables can be auxiliary control variables or dependent variables or constant: Since N is a discrete value, it cannot be utilized as a control variable but can be set constant or dynamically varying to further optimize system performance. T_M should be set as a variable to optimize the efficiency in Mburst, but it can be fixed in Lburst to simplify control while T_L can be used as a control variable to maintain the output voltage ripple Δv_o below specifications during Lburst mode.

C. Control Loop

To further simplify the control system implementation and improve the stability of mode transition, it is convenient for all three modes to share the same control architecture in Fig. 11. Below we propose three types of controller candidates, which can all meet these design objectives.

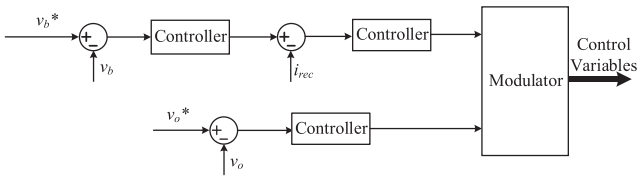

Fig. 11. General control architecture.

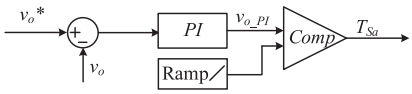

Fig. 12. v_o control loop.

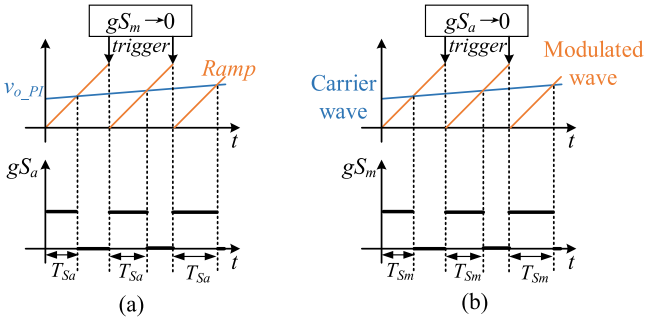

Fig. 13. Comparing/Modulation process. (a) T_{Sa}. (b) T_{Sm}.

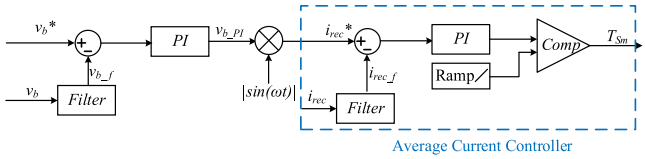

Fig. 14. Control diagram of average current control.

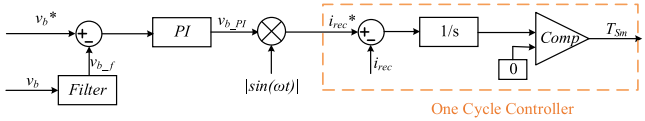

Fig. 15. Control diagram of one cycle control.

v_o control loop: Identical to the conventional ACF controller, a single PI controller is sufficient to ensure the reference tracking performance, see Fig. 12. Here, v_o controller determines the switching action of T_{Sa} by comparing the output of the PI controller, v_{o_PI}, with a ramp signal. The comparing process is shown in Fig. 13(a). A similar process can be adopted for T_{Sm}, shown in Fig. 13(b), with the modulation wave and the carrier wave to be determined by the input of Comp part in the input current (i.e., i_{rec}) control loop.

i_{rec} control loop: To realize PFC function, the input current to the rectifier, i_{rec} needs to be actively regulated. Figs. 14–16 show several potential solutions, including the conventional average current controller (ACC), one cycle controller (OCC), and a novel peak current controller (PCC), respectively. The new PCC consists of an average current controller (based on PI controller) as the first stage, and a conventional peak current controller as the second stage. Due to the structure of controller, we can expect the ACC to regulate the averaged input current i_{rec_f} (through the use of a filter) to follow its reference i_{rec}^*; the OCC to regulate the instantaneous i_{rec} to follow i_{rec}^* within one switching cycle; the new PCC to regulate i_{rec_f} to follow i_{rec}^* while maintaining a relatively constant peak current per cycle. The detailed operating waveforms in Mburst mode with ACC, OCC and the proposed PCC controller are shown in Fig. 17(with an irregular peak current) and Fig. 8(with a constant peak current), respectively. To differentiate Figs. 8 and 17, the Mburst modulation pattern in Figs. 8 and 17 are named pattern I and pattern II, respectively. The output of all three types of controllers is T_{Sm}, and the input i_{rec}^* is generated as per an outer v_b control loop based on a PI controller. The v_b controller is expected to regulate the dc voltage of v_b at v_b^*.

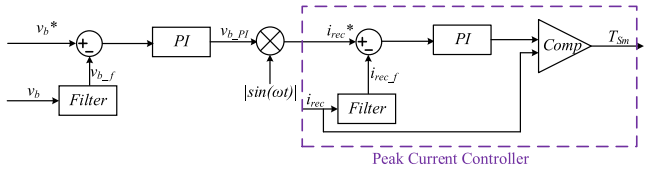

Fig. 16. Control diagram of proposed peak current control.

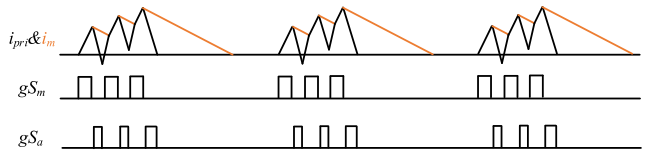

Fig. 17. Modulation pattern with irregular current shapes (pattern II).

In general, there are three sorts of i_{rec} control loops, i.e., ACC, OCC, and PCC. ACC and OCC contribute to the modulation pattern II in Fig. 17, while PCC contributes to the modulation pattern I in Fig. 8. Since modulation pattern I has a regular peak current, making its efficiency higher than that of modulation pattern II with an irregular peak current.

D. System State Machine

Fig. 18 illustrates a simplified state machine diagram of the proposed control system, supporting the transition of different modulation modes throughout the full load range. Particularly, the innermost state loop (highlighted in black) in Fig. 18 represents the switch operating sequences in CCM, i.e., turn ON and turn OFF S_m and S_a complementarily and periodically. When the load becomes lighter, the system enters the Mburst mode. The controller will first count N CCM pulses and then augment one OFF interval T_M afterward. When the load is further reduced, the system enters the Lburst mode, a longer OFF interval

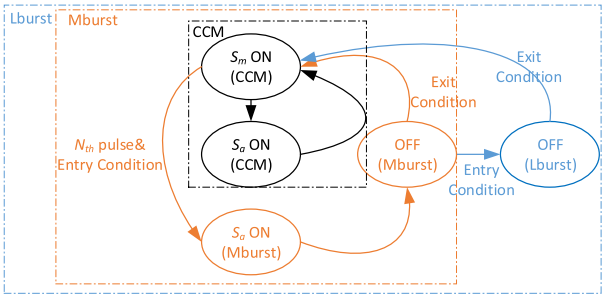

Fig. 18. Simplified state machine diagram.

$T_{\rm L}$ will be further augmented after N Mburst pulses. Fig. 18 also highlights the entry conditions and exit conditions of each modulation pattern, which will be detailed in Section V-E.

V. Design Considerations

The design of circuit parameters of iACF can refer to [11] with similar design procedures, including buffer capacitor, and magnetizing inductance. In addition, the minimum output capacitance is mainly constrained by the maximum transient voltage deviation for transient response, because the double-line frequency ripple has been absorbed by the buffer capacitor. This section is dedicated to the design of control parameters to achieve high efficiency and low output ripple.

A. Design of T_M

The goal of $T_{\rm M}$ design is mainly to i) ensure ZVS operation of all active switches (except for the first turn-ON pulse of $S_{\rm m}$) throughout the light load range and ii) reduce switching losses, which basically dominate the overall system's power losses at a lighter load. As per the operating principles of iACF, ZVS turn-ON of $S_{\rm m}$ can be achieved except for the first turn-ON of $S_{\rm m}$ for proposed light-mode control, provided that $I_p > 0$ and

$$\frac{1}{2}(L_m + L_b)I_p^2 \geq C_{oss}(v_{rec} + v_b)^2 \tag{9}$$

is satisfied, where $C_{\rm oss}$ is the output capacitance of $S_{\rm m}$ and $S_{\rm a}$, and I_p is the positive-peak current of $i_{\rm pri}$. Generally, (9) can always be satisfied throughout the load range as $L_{\rm m}$ is typically large. On the other hand, ZVS turn ON of $S_{\rm m}$ demands that $I_{\rm n} < 0$ and that

$$\frac{1}{2}L_b I_n^2 \geq C_{\rm oss}(v_{rec} + v_b)^2 \tag{10}$$

is satisfied, where $I_{\rm n}$ is the negative peak of $i_{\rm pri}$. The worst-case scenario of $I_{\rm n}$, i.e., the minimum $|I_n|$, happens at the peak of $v_{\rm ac}$. The reason is mainly twofold (see Fig. 19): First, at the peak of $v_{\rm ac}$, i.e., $v_{\rm ac\_p}$, $I_{\rm p}$ is maximized; Second, at $v_{\rm ac\_p}$, the $C_{\rm b}$ charging power is maximum, leading to minimal $C_{\rm b}$ discharging interval. Such two factors make $I_{\rm n}$ be maximized at this particular operating point. Therefore, we need to ensure this worst-case scenario of I_n meet (10).

The proposed modulation patterns at light load can be regarded as a transformation that turns the constantly light load $R_{\rm L}$ into a periodically heavy load $R_{\rm eq}$. The relationship between

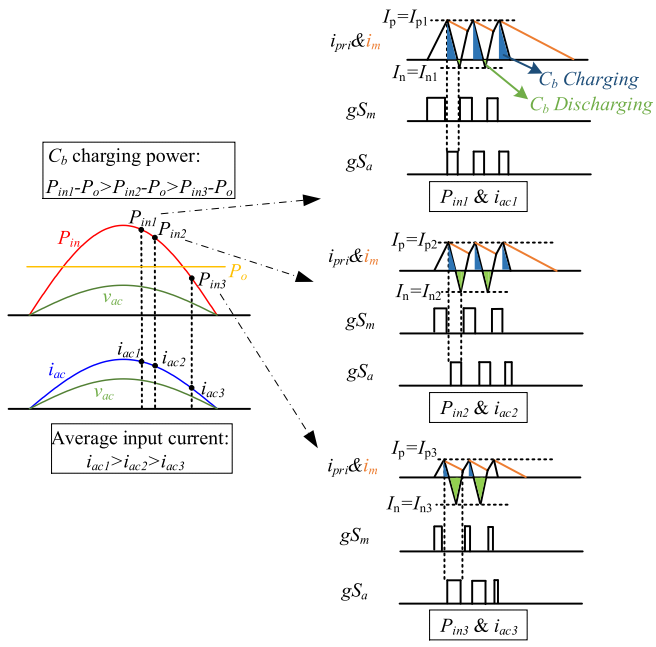

Fig. 19. Modulation patterns at different time.

equivalent heavy load $R_{\rm eq}$ and the true output load $R_{\rm L}$ can be approximately expressed as

$$R_{eq} \approx R_L \frac{T_b}{T_M + T_b} \tag{11}$$

where $T_{\rm b}$ is the active-switching time (see Fig. 8). Therefore, combining (10), (11), and (32) in Appendix, we have the following ZVS condition of $S_{\rm m}$:

$$T_M \geq \sqrt{\frac{2C_{\rm oss}(V_{\rm ac\_p} + V_b)^2 T_b^2 R_L^2}{L_b f^2} - T_b^2}. \tag{12}$$

Meanwhile, to maximize the efficiency, $T_{\rm M}$ needs to be increased to lower f_{sw} until the voltage ripple constraint Δv_o (13) is violated

$$\Delta v_o = \frac{1}{C_b}\frac{V_o}{R_o}T_M. \tag{13}$$

In the final design, taking (12), (13) into consideration, $T_{\rm M}$ is selected as 13 μs at half load, and $T_{\rm M}$ will increase with $R_{\rm L}$ according to (12).

B. Design of N

The goal of N design is to seek optimal tradeoff between switching losses, THD, and $v_{\rm o}$'s ripple. Fig. 20 shows the impact of N on the current waveforms of iACF during Mburst mode of operation. All other circuit parameters remain the same. We can define an equivalent switching frequency $f_{\rm eq}$ as

$$f_{eq} = \frac{N}{T_P} \tag{14}$$

where $T_{\rm p}$ is the Mburst cycle, as shown in Fig. 20. To make a fair comparison with different N, both f_{sw} and f_{eq} should keep

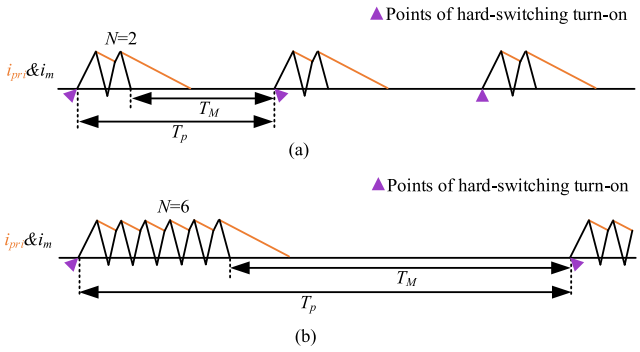

Fig. 20. Current waveforms of Mburst mode. (a) $N = 2$. (b) $N = 6$.

TABLE II
CONVERTER PARAMETERS

Parameters/Components	Value
Input voltage (v_{in})	110V, 60Hz
Output voltage (v_o)	20V
Average buffer voltage (v_b)	170V
Input filter inductance (L_f)	150uH
Input filter capacitance (C_f)	470nF
High-frequency filter capacitance (C_{in_f})	27nF
Magnetizing inductance (L_m)	250uH
Primary inductance (L_b)	55uH
Turns ratio (n)	5:1
Buffer capacitor (C_b)	47uF-250V-2454mm^3
Output capacitor (C_o)	2*680uF-25V-940mm^3
Primary side main switch (S_m, S_a)	IPL60R285P7AUMA1I

same. Then, we can get

$$T_M = \frac{N}{\left(\frac{1}{f_{eq}} - \frac{1}{f_{sw}}\right)} = \frac{N f_{eq} f_{sw}}{f_{sw} - f_{eq}}. \tag{15}$$

As per Fig. 20, v_o's ripple Δv_o during T_M is approximately

$$\Delta v_o = \frac{1}{C_b}\frac{V_o}{R_o} T_M = \frac{N f_{eq} f_{sw} V_o}{(f_{sw} - f_{eq}) C_b R_o}. \tag{16}$$

Equation (16) shows that Δv_o increases linearly with N. On the other hand, the power losses associated with the hard-switching turn-ON of S_m in Mburst can be determined as

$$P_h = \frac{E_h}{N f_{eq}} \tag{17}$$

where E_h is the energy loss per hard-switching turn-ON of S_m. (17) predicts that the switching losses associated with the hard-switching turn-ON of first pulse will be decreased with the increase of N. However, from (15), we know that T_M increases with N, resulting in a higher THD. In this article with converter parameters in Table II, we choose $N = 3$ for both Mburst and Lburst modes with consideration of (16), (17), and practical experimental results.

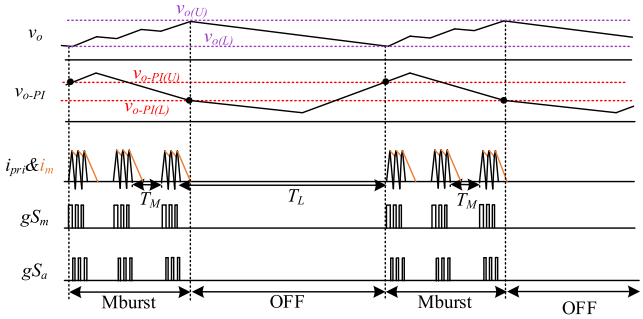

Fig. 21. Updated waveforms for Lburst mode.

C. Design of T_L Controller in Lburst Mode

As per Fig. 9, T_L is introduced in Lburst mode as a control variable to regulate v_o within a given voltage band while T_M is fixed. Ideally, T_L can be determined through bang-bang control, i.e., when v_o reaches its upper bound, T_L begins; when v_o reaches its lower bound, T_L ends. However, a bang–bang control based on the feedback signal of v_o requires a precise voltage detector with high resolution, increasing the costs and complexity. Therefore, we propose to use an alternative variable as an agent for v_o. Here, we choose the variables from the v_o control loop (see Fig. 12), i.e., T_{Sa} and v_{o_PI}, as v_o's agents, where v_{o_PI} is the output of the PI controller. Since v_{o_PI} is a continuous signal whereas T_{sa} is a pulsed signal, $v_{o\text{-}PI}$ is selected as the final agent of v_o. Therefore, T_L will be directly controlled by $v_{o\text{-}PI}$ in a bang–bang fashion. The updated Lburst mode with v_{o_PI} as feedback signal is shown in Fig. 21. As shown, T_L begins (or ends) when v_{o_PI} reaches its lower threshold, $v_{o\_PI(L)}$ (or upper threshold $v_{o\_PI(U)}$). The relationship between $v_{o\_PI(U)}$-$v_{o\_PI(L)}$ (i.e., Δv_{o_PI}) and $v_{o(U)}$- $v_{o(L)}$ (i.e., Δv_o) is shown in (40) of Appendix, which demonstrates v_{o_PI} can be used as the agent, because Δv_{o_PI} is positively correlated with output voltage ripple.

D. Parameters Design for Mode Transition

There are three working modes: CCM, Mburst mode, and Lburst mode. As the entry and exit conditions into different working modes mainly depend on the loading condition, variables proportional to output power p_o can be selected to determine the working modes. Here, p_o is not directly used as the mode-selection variable as the measurement of p_o demands an extra current sensor at the load side, leading to an increase in the system's complexity and cost.

As per Fig. 16, the output of the PI controller from the v_b control loop, $v_{b\text{-}PI}$, can be selected as the agent of p_o, as $v_{b\text{-}PI}$ determines the amplitude of the input current. Mathematically

$$v_{b-PI} = kP_{in} \tag{18}$$

where k is a constant coefficient. Assuming 100% power conversion efficiency, we have $\overline{p_o} = P_o = P_{in}$, and $v_{b\text{-}PI}{}^*$ corresponds to full power $P_o{}^*$. Thus, we can perform mode transition from CCM mode to Mburst mode once P_o (or $v_{b\text{-}PI}$) decreases to $\alpha P_o{}^*$ (or $\alpha v_{b\text{-}PI}{}^*$), and Mburst mode to Lburst mode once P_o

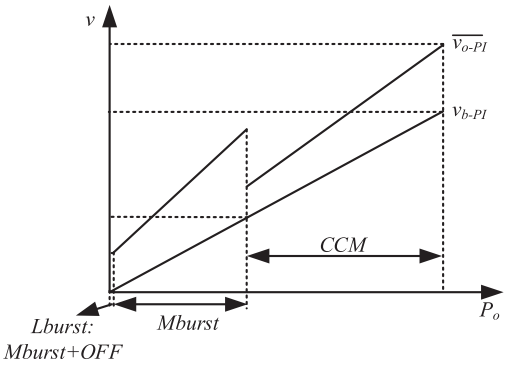

Fig. 22. Mode switching characteristics.

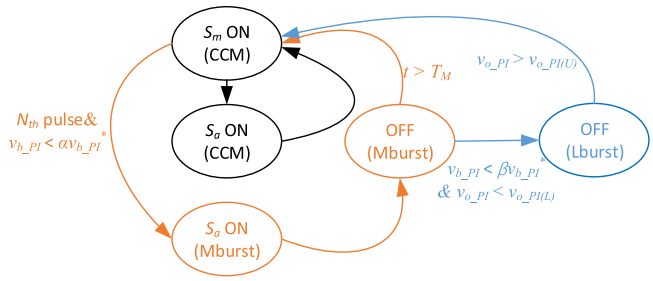

Fig. 23. State machine diagram.

(or $v_{\text{b-PI}}$) decreases to $\beta P_{\text{o}}{}^*$ (or $\beta v_{\text{b-PI}}{}^*$). Here, α and β can be determined by the crossing points of efficiency curves in different modes, either through theoretical calculations or experimental measurements. In our case, we obtain the efficiency curves experimentally. In particular

$$v_{b\_\text{PI(CCM To Mburst)}} = \alpha v_{b\_\text{PI}}^* \ (P_o = \alpha P_o^*) \tag{19}$$

$$v_{b\_\text{PI(Mburst To Lburst)}} = \beta v_{b\_\text{PI}}^* \ (P_o = \beta P_0^*). \tag{20}$$

It should be emphasized that $v_{\text{b-PI}}$ can be quite small in Lburst mode. For instance, if $\beta = 0.01$, the resultant $0.01 v_{\text{b-PI}}{}^*$ can be so small that may bring difficulties to detect $v_{\text{b-PI}}{}^*$ accurately in analog circuit, of which maximum voltage constrains the maximum output of PI controller. To solve this problem, we propose to use $v_{\text{o-PI}}$ as an alternative agent of p_{o}, as i) $v_{\text{o-PI}}$ (i.e., a filtered version of T_{sa}) is proportional to p_{o}, according to the operating principles of iACF, and ii) when the long OFF intervals is inserted, p_o will increase to maintain same average output power, then correspondingly $v_{\text{o-PI}}$ will increase. Therefore, $v_{\text{o-PI}}$ could be the complementary index of $v_{\text{b-PI}}$ to determine mode transition from Mburst mode to Lburst mode if a more accurate mode transition is required.

Based on the analysis abovementioned, the mode transition characteristics are presented in Fig. 22, where $\overline{v_{o-\text{PI}}}$ represents its average value over a line period and the values of the axis depend on the actual hardware and control parameters used in the system.

E. Control System With Designed Parameters

Based on the parameters designed in this section and control loop in Section IV, the entry and exit conditions in Fig. 18 can be completed accordingly, which is shown in Fig. 23. First, when $v_{\text{b-PI}} < \alpha v_{\text{b-PI}}{}^*$, CCM is switched to Mburst mode. Then, when $v_{\text{b-PI}} < \beta v_{\text{b-PI}}{}^*$ and $v_{\text{o-PI}} < v_{\text{o-PI(L)}}$, Mburst mode is switched to Lburst mode, but once $v_{\text{o-PI}} > v_{\text{o-PI(U)}}$, system is back to Mburst mode.

At the same time, the simplified control blocks can be further extended from Figs. 10–24, where the control loops (see Fig. 12 and Figs. 14–16) are implemented in the analog circuit, and the state machine diagram (see Fig. 23) is implemented in the digital circuit (FPGA). The state machine implemented in FPGA will be the control core, which is triggered by both pulses of analog control loop and sensing signals of ADC, and output driving signals through gate drivers to control S_{m} and S_{a}.

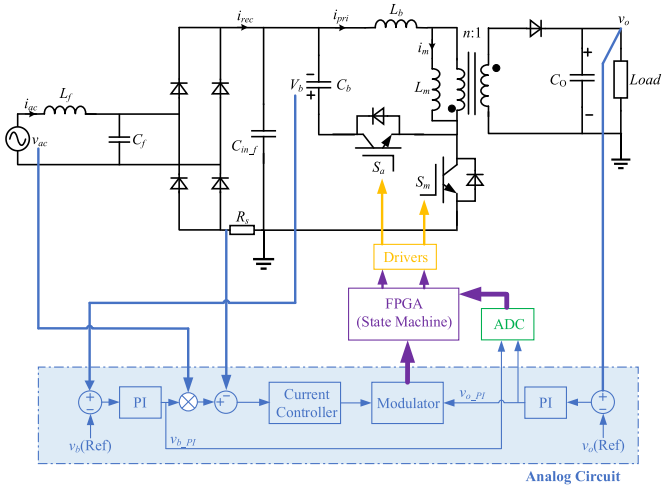

Fig. 24. Simplified control blocks of proposed control strategies.

VI. Experimental Results

To demonstrate the superiority of the proposed control modes, a 100-W prototype is constructed, and its control part follows the design blocks in Fig. 24, where the digital circuit is implemented via the FPGA (Cyclone IV EP4CE6). The key circuit parameters are shown in Table II, where the superiority of the active power decoupling in iACF is shown through the key point that only a small buffer capacitor with low capacitance and low voltage rating is required. The power board of the prototype is shown in Fig. 25, while the control board is shown in Fig. 26.

The proposed burst modes implemented through PCC and ACC are investigated experimentally, as examples of modulation pattern I and modulation pattern II, respectively.

A. Experimental Verification

Figs. 27 and 28, respectively, show the operating waveforms of Mburst mode based on modulation pattern I (see Fig. 8, realized through PCC) and modulation pattern II (see Fig. 17, realized through ACC) at 50% of full power. In both cases, high power factors at the input terminal and constant voltage at the output terminal are obtained. Meanwhile, the output voltage is

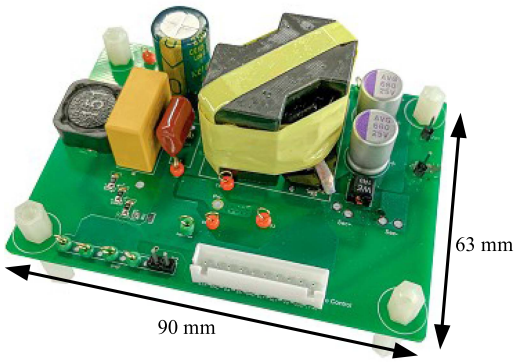

Fig. 25. Prototype of main converter (iACF).

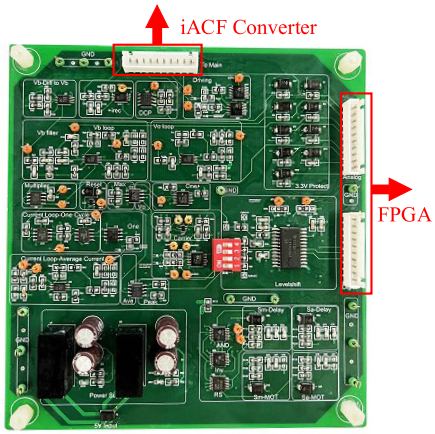

Fig. 26. Prototype of control part.

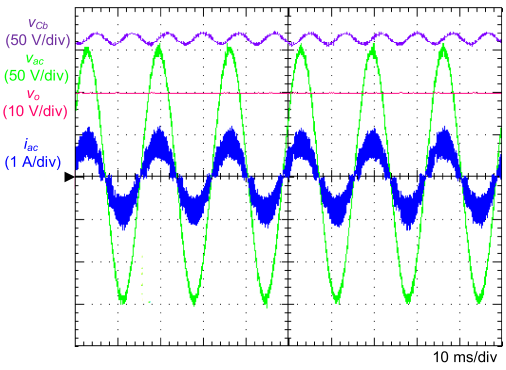

Fig. 27. Waveforms of Mburst mode based on pattern I (realized by PCC) at 50 W (50% load).

stably constant, and the buffer capacitor C_b takes the double-line frequency ripple. These waveforms confirm the feasibility of applying the proposed control and modulation patterns to perform ac current shaping and output voltage regulation and active power decoupling function.

Fig. 29 further shows the operating waveforms of CCM (realized through PCC) at 50% of full power. Generally, the operating waveforms are almost identical to the proposed Mburst modes, except that i_{ac} features reduced current harmonics. This is an

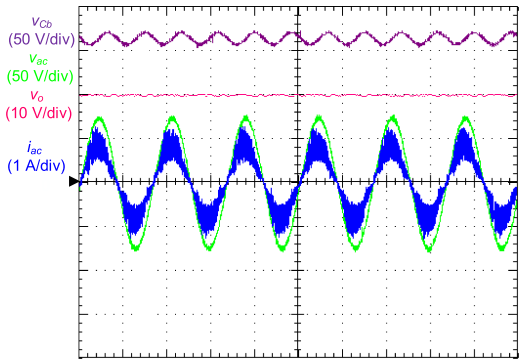

Fig. 28. Waveforms of Mburst mode based on pattern II (realized by ACC) at 50 W (50% load).

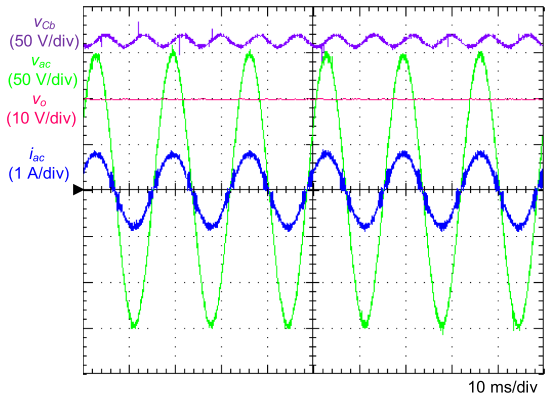

Fig. 29. Waveforms of CCM (realized by PCC) at 50 W (50% load).

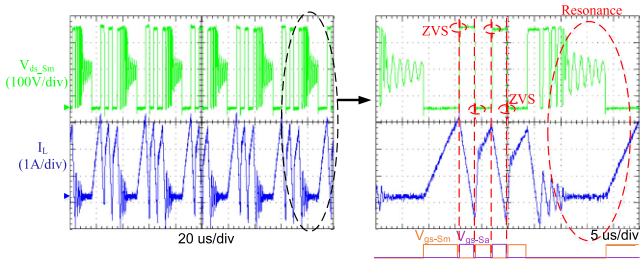

Fig. 30. Switching waveforms of Mburst mode based on pattern I (realized by PCC) at 50% load.

expected result as the equivalent switching frequency of Mburst mode is lower than that of CCM due to the deliberately inserted OFF intervals. In particular, the equivalent switching frequency f_{eq} [defined in (14)] of Mburst at half-load are measured at 75–85 kHz (see Fig. 27) and 75–120 kHz (see Fig. 28), respectively, much lower than the f_{sw} of CCM at half-load, which is measured at 130–250 kHz (see Fig. 29). The THD of i_{ac} in Figs. 27–29 are 6.72%, 4.18%, and 3.5%, respectively.

The zoom-in switching waveforms of the iACF based on modulation pattern I (realized through PCC) are shown in Fig. 30. The waveforms confirm that ZVS turn-ON of S_m for the last two gate pulses is realized. Due to the reverse recovery current of the body diode of S_a, and the relatively greater inductance L_b (amounting to more energy stored in L_b), a resonant process can

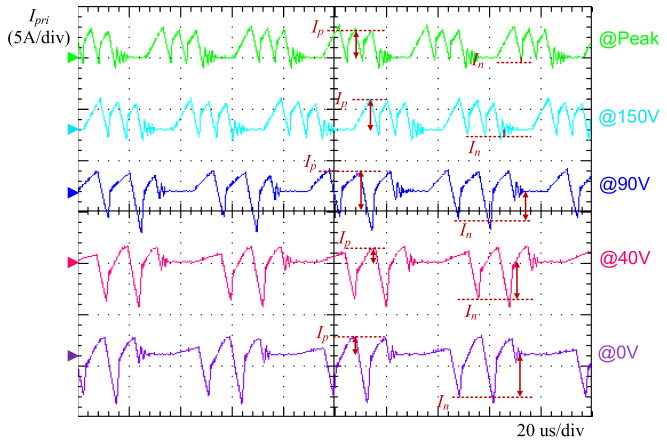

Fig. 31. Current waveforms of Mburst mode based on pattern I (realized by PCC) at 50% load.

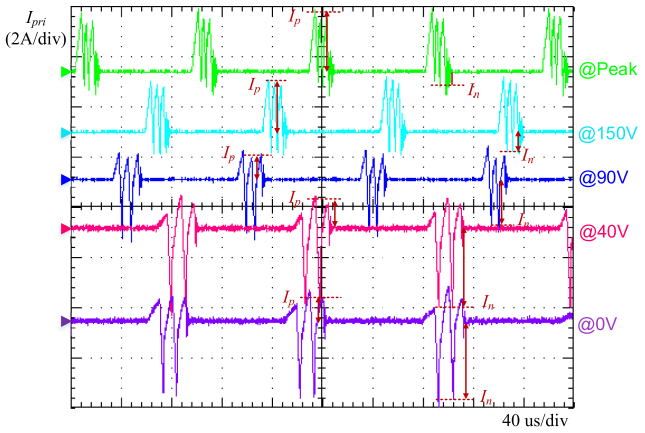

Fig. 32. Current waveforms of Mburst mode based on pattern I (realized by PCC) at 25% load.

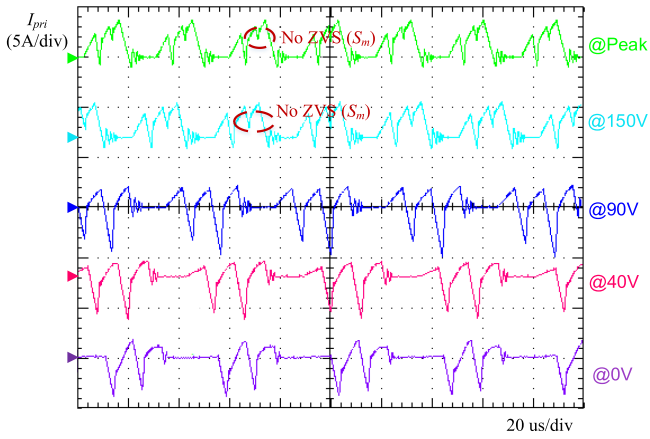

Fig. 33. Current waveforms of Mburst mode with pattern II (realized by ACC) at 25% load.

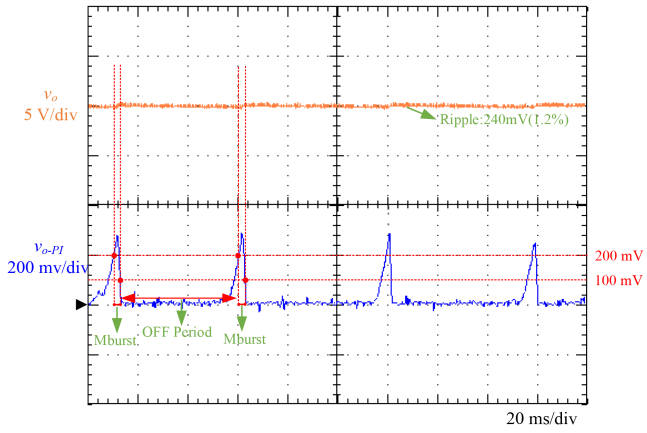

Fig. 34. Waveforms of Lburst with pattern I at 0.2% load.

be observed during the OFF interval, which leads to increased switching losses. Wide bandgap devices such as SiC and GaN can be used to further improve efficiency by attenuating the resonant process.

To further verify the ZVS turn-ON of active switches, the waveforms of $I_{\rm pri}$ at different $v_{\rm ac}$ phases are shown in Fig. 31 and Fig. 32, respectively, at 50% and 25% of full load, based on modulation pattern I. The ZVS turn-ON of $S_{\rm a}$ can be realized in the whole line period, because there is enough positive current. Meanwhile, the peak $v_{\rm ac}$ is confirmed to be the worst case to realize ZVS of $S_{\rm m}$, corresponding to the minimal $|I_{\rm n}|$. The $I_{\rm n}$ at the peak $v_{\rm ac}$ is measured as 0.2 and 0.5 A, respectively, in Figs. 31 and 32, which are sufficient to realize ZVS turn-ON of $S_{\rm m}$. In contrast, Mburst based on modulation pattern II cannot realize ZVS at high $v_{\rm ac}$, as shown in Fig. 33, because $I_{\rm n}$ turns to be positive on the second turn-ON gate pulse of $S_{\rm m}$.

Fig. 34 shows the working waveforms of iACF in Lburst mode, which is consistent with those in Fig. 21. Here, the threshold of $v_{\rm o\text{-}PI}$ to enable $T_{\rm L}$ period and Mburst mode are 100 and 200 mV, respectively. From Fig. 34, the voltage ripple of $v_{\rm o}$ is 240 mV (1.2%).

B. System Performance

Efficiency is the key index to evaluate the performance of proposed control strategies. Fig. 35 shows the system's efficiency based on i) CCM (realized by PCC), ii) CCM (realized by ACC), iii) Mburst mode based on modulation pattern I (realized by PCC), and iv) Mburst mode based on modulation pattern II (realized by ACC). It can be observed that as follows:

1) Mburst based on modulation pattern I can achieve higher efficiency than that based on modulation pattern II, a conclusion in line with the analysis abovementioned;
2) CCM based on both PCC and ACC achieves almost identical efficiency performance.

In addition, compared with TI's two-stage solution [boost PFC + ACF, PFC IC: UCC28056 (TI), ACF IC: UCC28780 (TI)] [12], iACF with proposed Mburst mode based on the proposed modulation patterns can increase the efficiency performance by up to 10% for $P_{\rm o} < 50$ W (by comparing the efficiency curve of "Mburst (Pattern I & PCC)" and that of "Boost PFC + ACF" in Fig. 35), showcasing the superiority of proposed modulation patterns and control methods.

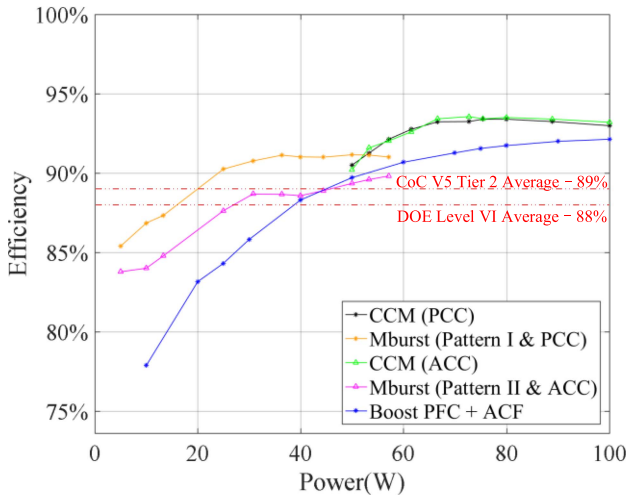

Fig. 35. Comparison of efficiency performance with different solutions.

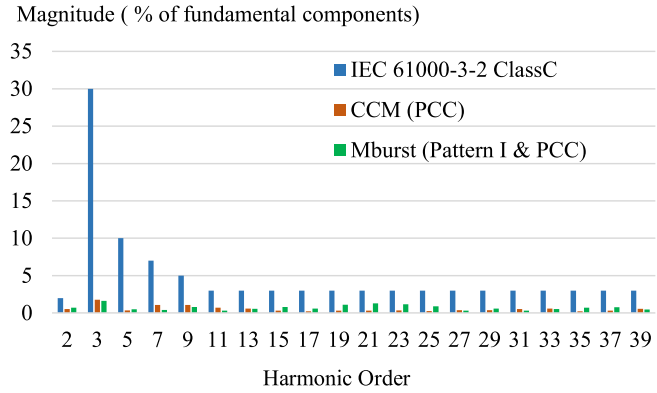

Fig. 36. THD of CCM and Mburst mode.

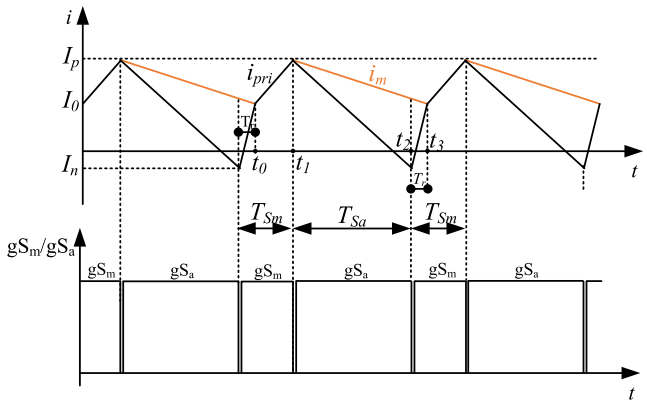

Fig. 37. Current waveforms in CCM.

To sum up, Fig. 35 shows that iACF can achieve a higher efficiency than the conventional two-stage ac–dc solution (boost PFC+ACF) throughout the load range.

On the other hand, consumer electronics need to comply with stringent global efficiency standards such as DoE Level VI and EU CoC V5 Tier-2, which specify the minimum average efficiency at 25%, 50%, 75%, and 100% of full rated output power. The four-point average efficiency of iACF is 91.90%, which meets the requirements of 88% of DoE Level VI and 89% of CoC V5 Tier-2, as shown in Fig. 35. These results are also greater than that of the conventional two-stage solution from TI, which is 89.43%.

Power quality is another key performance index. Taking the performance at 50% of full power as an example, Mburst mode based on modulation pattern I (realized through PCC) and CCM (realized through PCC) are compared with IEC 61000-3-2 Class standard, as shown in Fig. 36. The results show that, the power quality of Mburst mode is comparable to that of CCM, both meeting the requirements of Class C of IEC 61000-3-2. Furthermore, the power quality of both CCM and Mburst mode also complies with the requirements of Class A, Class B, and Class D of IEC 61000-3-2.

VII. Conclusion

In this article, a novel burst mode control is proposed for a new single-stage ac–dc topology that APD iACF, to achieve high performance at light load, including high efficiency, low THD, and small output voltage ripple. The novel control mainly consists of proposed modulation patterns and dedicated control strategies including a novel peak current controller, which could also be alternatively adopted by other APD integrated topologies. The experimental results demonstrate the superiority of iACF converter at light load besides heavy load, which not only fully complies with mandatory standards of industry but also outperforms the conventional two-stage solution in efficiency.

Appendix

The parameters and variables used during the following derivation process have been mostly noted in Fig. 2. In addition, dead time is neglected in the derivation.

A. Derivation of v_b

Assuming the peak value of ac input voltage and ac input current are $V_{\mathrm{ac\_p}}$ and $I_{\mathrm{ac\_p}}$, the instantaneous input power

$$p_{in} = V_{\mathrm{ac\_p}} I_{\mathrm{ac\_p}} \sin\omega t \sin\omega t = P_o + v_b \frac{C_b dv_b}{dt} \tag{21}$$

where P_{o} is output power. Then, we can get

$$\begin{cases} \frac{1}{2} V_{\mathrm{ac\_p}} I_{\mathrm{ac\_p}} \\ = P_o - \frac{1}{2} V_{\mathrm{ac\_p}} I_{\mathrm{ac\_p}} \cos 2\omega t = v_b \frac{C_b dv_b}{dt} \end{cases}. \tag{22}$$

Equation (22) can be rearranged as

$$-P_o \cos 2\omega t = v_b \frac{C_b dv_b}{dt}. \tag{23}$$

Solving (23)

$$v_b = \sqrt{V_b^2 - \frac{P_o \sin 2\omega t}{\omega C_b}} = \sqrt{V_b^2 - \frac{V_o^2 \sin 2\omega t}{\omega C_b R_o}} \tag{24}$$

where $V_{\rm b}$ is the value of dc component of $v_{\rm b}$. While ac input voltage is right at the peak value, we can get (25) from (24)

$$v_b = V_b \ \left(\omega t = \frac{\pi}{2}\right). \tag{25}$$

B. Derivation of I_n

The current waveforms in CCM are shown in Fig. 37. Assuming the output voltage is constant with the value of $V_{\rm o}$, then the peak value of ac input current

$$I_{\rm ac\_p} = \frac{2V_o^2}{V_{\rm ac\_p}R_o}. \tag{26}$$

Since the inductor current $i_{\rm pri}$ at t_0 and t_3 is almost same, then

$$\frac{V_{\rm ac\_p}}{L_m + L_r}(T_{Sm} - T_{Sa}) = \frac{nV_o}{L_m}(T_{Sa} + T_r). \tag{27}$$

The magnetizing current $i_{\rm m}$ and the inductor current $i_{\rm pri}$ diverge at t_1 and merge at t_3, we have

$$\frac{nV_o}{L_m}(T_{Sa} + T_r) = \frac{(v_b - nV_o)}{L_r}T_{Sa} - \frac{(nV_o + V_{\rm ac\_p})}{L_r}T_r. \tag{28}$$

The average value of current flowing from primary side to secondary side of transformer is the same, so

$$\left[\left(\frac{-nV_o}{L_m} - \frac{nV_o - v_b}{L_r}\right)T_{Sa}\right](T_{Sa} + T_r)\frac{1}{2} = \frac{1}{n}\frac{V_o}{R_o}(T_{sa}+T_{sm}). \tag{29}$$

The average value of current during ($T_{\rm sm}$ - $T_{\rm r}$) should be roughly the same as the value of ac input current, we have

$$\begin{aligned}\tfrac{1}{2}(T_{Sm} - T_r)(I_0 + I_0 + \tfrac{V_{\rm ac\_p}}{L_m+L_r}(T_{Sm} - T_r)) \\ = I_{\rm ac\_p}(T_{Sm} + T_{Sa}).\end{aligned} \tag{30}$$

The negative-peak current

$$I_n = I_0 - \frac{nV_o + V_{\rm ac\_p}}{L_r}T_r. \tag{31}$$

Combining (25)–(31), the negative-peak current can be further expressed as

$$I_n = -\frac{f(V_{\rm ac\_p}, V_o, V_b, L_b, L_m, n, C_b)}{R_o} \tag{32}$$

where f represents a function

$$\begin{aligned} f &= \frac{a_1 + a_2 + a_3 + a_4 + a_5}{a_6 + a_7 + a_8 + a_9 + a_{10}} \\ a_1 &= L_r^2 V_{\rm ac\_p} V_o^2 n,\ a_2 = -L_r^2 V_b V_o^2 n \\ a_3 &= -L_m L_r V_b V_o^2 n,\ a_4 = L_m L_r V_{\rm ac\_p} V_o^2 n \\ a_5 &= -2L_m L_r V_b V_{\rm ac\_p} V_o,\ a_6 = V_{\rm ac\_p} V_o L_m^2 n^2 \\ a_7 &= -V_b V_{\rm ac\_p} L_m^2 n,\ a_8 = 2V_{\rm ac\_p} V_o L_m L_r n^2 \\ a_9 &= -V_b V_{\rm ac\_p} L_m L_r n,\ a_{10} = V_{\rm ac\_p} V_o L_r^2 n^2. \end{aligned} \tag{33}$$

C. Derivation of Δv_o of Lburst Mode

Suppose that the PI parameters of $v_{\rm o}$ controller are $K_{\rm p}$ and $K_{\rm i}$ separately. It is apparent that

$$v_o^* = \frac{v_{o(U)} + v_{o(L)}}{2}. \tag{34}$$

Then, the upper and lower value of $v_{\rm o}$ can be expressed as

$$v_{o(U)} = v_o^* + \frac{1}{2}\Delta v_o,\ v_{o(L)} = v_o^* - \frac{1}{2}\Delta v_o. \tag{35}$$

Based on the energy balance of the output capacitor, we can get

$$P_o T_L = \frac{1}{2}C_o v_{o(U)}^2 - \frac{1}{2}C_o v_{o(L)}^2. \tag{36}$$

Combine (35) and (36)

$$P_o T_L = C_o v_o^* \Delta v_o. \tag{37}$$

Then,

$$\begin{aligned} v_{o-{\rm PI}(U)} - v_{o-{\rm PI}(L)} &= K_i \int_{T_L} (v_o^* - v_o)dt + K_p(v_o^* - v_{o(L)}) \\ &= K_i(v_o^* T_L - \frac{1}{2}\Delta v_o T_L) + K_p\frac{1}{2}\Delta v_o \\ &= K_i(v_o^* - \frac{1}{2}\Delta v_o)T_L + \frac{1}{2}K_p\Delta v_o. \end{aligned} \tag{38}$$

Combine (37) and (38)

$$\begin{aligned} v_{o-{\rm PI}(U)} - v_{o-{\rm PI}(L)} &= K_i(v_o^* - \tfrac{1}{2}\Delta v_o)\tfrac{C_o v_o^* \Delta v_o}{P_o} + \tfrac{1}{2}K_p\Delta v_o \\ &= -\tfrac{K_i C_o v_o^*}{2P_o}(\Delta v_o)^2 + (\tfrac{1}{2}K_p + \tfrac{K_i C_o (v_o^*)^2}{P_o})\Delta v_o. \end{aligned} \tag{39}$$

The voltage ripple Δv_o can be solved from (39)

$$\begin{aligned} \Delta v_o &= \frac{K_p P_o + 2C_o K_i (v_o^*)^2 - \sqrt{b_1 + b_2}}{2C_o K_i v_o^*} \\ b_1 &= (2C_o K_i (v_o^*)^2)^2 + (K_p P_o)^2 + 4C_o K_i K_p P_o (v_o^*)^2 \\ b_2 &= -8(v_{o-{\rm PI}(U)} - v_{o-{\rm PI}(L)})C_o K_i P_o v_o^* \\ &= -8\Delta v_{o-{\rm PI}} C_o K_i P_o v_o^*. \end{aligned} \tag{40}$$

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