Letters

An Ultralow-Loss Fault-Current-Limiting Z-Source LVDC Circuit Breaker Using Cryogenic Power Electronics

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***Abstract*—Room-temperature power electronics based dc circuit breakers and fault current limiters face two major challenges: high conduction loss and time-delayed response. This letter presents a novel circuitry, for the first time (based on literature studies), to combine cryogenic power electronics (CPE), together with the superconducting Z-source dc circuit breaker technology. The design, fabrication, and tests of the new device were carried out, and three advantages were proved. First, the actual overall system loss (including cryogenic issues) reduced by 62.1% in the 2 kW case study. Second, the no-delay automatic fault current limiting technology provided a sudden protective resistor ∼0.1 Ω to suppress the fault below 200 A, and meanwhile stabilized the bus voltage. Third, the CPE-based breaker achieved both the active device isolation and passive fault isolation within 60 μs.**

***Index Terms*—Cryogenic power electronics (CPE), dc circuit breaker, dc fault current limiter, superconducting resistor/inductor.**

I. Introduction

When interfacing with renewable energy sources, energy storage devices, and sensitive loads, LVDC technologies can simplify power conversion procedures [1], and provide much higher reliability and efficiency over conventional ac systems. However, there are still two major issues to be addressed. The first issue is the absence of zero-current crossing point to trigger the active isolation for an arbitrary dc line from the dc bus during normal operation, or the passive isolation during fault transients. The second issue is the extremely high/sharp fault currents due to the small impedance in dc lines.

Particularly, when a serious line-to-ground accident occurs, the fault over-current can rise up to hundreds of times larger than the normal current within microseconds (μs). For the converters interconnected the dc buses and sources/loads, experimental results have proved that most of commercial MOSFETs can only withstand a maximum faulty time of 5-20 μs [2]. This means one short-time disturbance may destroy a whole power electronic device, and eventually cause further damage on adjacent dc lines as well as the entire dc microgrid. Therefore, prior to circuit breaking, it is crucial to add an extra fault current limiter to suppress the initial fault current in an early stage.

At present, some literatures have studied the integration of current-limiting resistors and/or inductors into LVDC systems by using power-electronics-based fault current limiters (solid-state bridge [3], saturated iron core [4], flux-coupling inductance [5], etc.). For the dc breaking, a classical solid-state circuit breaker structure can be applied using a power electronic switch in parallel with a metal oxide varistor (MOV). However, the connection leads of a MOV to power electronic switch introduce a stray inductance, which would cause serious switch-off voltage spikes and even destroy the whole device [6]. To address this voltage spike issue, two typical solutions are used: applying an additional snubber circuit module for a residual current device [7], and adding a zero-current switching (ZCS) circuit module to minimize transient switch-off currents [8], [9]. However, these two methods still suffer from relatively complex circuit topologies and software controls. Recently, an emerging solid-state circuit breaker topology, called Z-source circuit breaker, has been widely studied and verified by experiments [10], [11], [12], [13]. Compared with classical solid-state circuit breakers, most Z-source circuit breakers (cross structure [10], parallel structure [11], series structure [12], [13], etc.) have the advantages of fewer components, simpler control, lower conduction loss, and higher system reliability. During transients and faults, they can artificially create a zero-crossing point to realize the zero-current dc line interruption, without the risk of causing switch-off voltage spikes. In addition, there are three typical methods to embed current limiting functions into dc circuit breakers [14]: adding inductors or resistors, operating in the chopper mode with freewheeling diodes, and utilizing the saturation region of switches.

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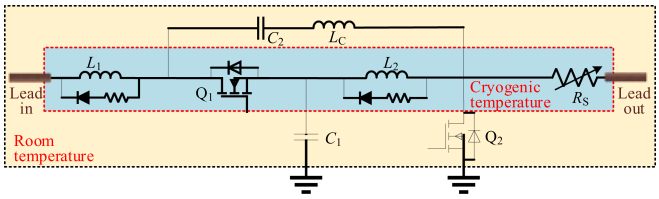

Fig. 1. Configuration of the CPE-based Z-source LVDC circuit breaker.

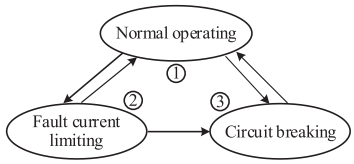

Fig. 2. Transitions among the three main modes.

In order to effectively implement the dc current-limiting and/or circuit-breaking operation, a series of semiconductor-based power electronic devices and copper-based impedance circuits are generally adopted [15], [16]. For the uses in LVDC networks with high-power loads (e.g., data centers and EV charging stations), existing dc fault current limiters and dc circuit breakers have three major drawbacks.

1) During normal operation, most power electronic switches/diodes and fault-current-limiting resistors/inductors inevitably have huge conduction power losses, which reduce the overall efficiency and even cause over-heat problems.
2) During long-time/permanent faults, most hardware and/or software eventually rely on the time-delayed fault diagnosis and the corresponding treatments with additional delays, which inevitably slow down the transient response for suppressing dc fault currents [17], [18].
3) During short-time/transient disturbances, conventional breakers suffer the problem of "over sensitive," which will wrongly identify dc lines having "permanent" faults and unnecessarily cut off the loads. These "over sensitive" actions may affect the reliability of the entire dc microgrid [11].

To overcome the time-delayed/over-sensitive fault handling issues above, an emerging solution of using superconducting fault current limiter (SFCL) has been proposed and experimentally verified [19], [20]. The SFCL (also called superconducting resistor) is a self-acting over-current limiter based on the nature of superconductivity. It manifests itself as an ideal 0 Ω resistor under normal-current conditions, and has ultrahigh resistance under over-current conditions.

The conduction power losses mainly come from the inductors and switches in most Z-source circuit breakers. Benefited from the advantages of zero loss and compact size, a superconducting inductor can be a reasonable substitute for a copper inductor [21]. Moreover, the complimentary cryogenic environment also offers a favorably low temperature operation condition for the power electronic switches. Experimental results proved the advantages that the cryogenic operations of power MOSFETs have much lower conduction losses than the losses in room temperature operations [22], [23].

Therefore, we designed and fabricated a novel ultralow-loss fault-current-limiting Z-source dc circuit breaker using cryogenic power electronics (CPE), which merged multiple benefits of ultralow loss, fault-current limiting, and ZCS into one device. As shown in Fig. 1, the proposed CPE-based breaker can be divided into two parts. The first part is the cryogenic-temperature main module which can supply the dc power directly from the source to the load during normal operation. The main elements include two superconducting inductors (L_1, L_2), a superconducting resistor R_s, and a power MOSFET Q_1. The second part is the room-temperature auxiliary module which can implement the ZCS operation when required. The auxiliary module elements include two nonpolarized thin-film capacitors (C_1, C_2), a copper inductor L_C and a power MOSFET Q_2.

The main novelties and contributions of this letter are as follows.

1) For the first time (based on literature studies), a novel circuitry has been designed and fabricated, which combines CPE together with the superconducting Z-source dc circuit breaker technology.
2) The new device presents much lower total loss than conventional circuit breakers. The actual system total loss (including cryogenic issues) has been reduced by 62.1% in the 2 kW case study.
3) In addition to coupling the ZCS advantage, this new device also includes a superconducting resistor to suppress all kinds of fault currents caused by short-time/transient disturbances and/or long-time/permanent faults. This advantage is based on the ultrafast auto-triggered fault protection, which does not need extra fault detection modules, and can effectively avoid time-delayed responses and unnecessary breaking actions.

II. Circuit Fundamentals

As shown in Fig. 2, the CPE-based circuit breaker has three main operating modes: ① normal operating, ② fault current limiting, and ③ circuit breaking. Thanks to the unique self-triggering and self-healing characteristics of the superconducting resistor R_S, the breaker can be automatically converted between modes ① and② when encountering any short-time over-current disturbances. If a permanent circuit fault occurs, mode ② can be converted to mode ③ by triggering a short-circuit command using the auxiliary MOSFET Q_2. In addition, the breaker can also be manually converted between modes ② and③, depending on the actual demand from the LVDC load. Fig. 3 presents characteristic waveforms of the three operating modes above. The circuit conversion processes include four transient-states and three steady-states, which are described as follows.

Normal operating mode ①. steady state, $[-\infty, t_0]$, $[t_6, +\infty]$: In mode ①, the breaker connects the load R_{load} to the dc source V_{dc} through two inductors (L_1, L_2), a MOSFET Q_1, and a resistor R_S, as shown in Fig. 4(a). The normal steady-state

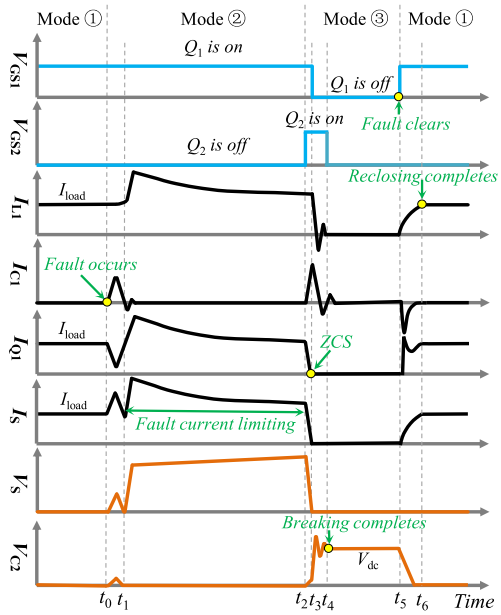

Fig. 3. Characteristic waveforms when changing modes to ①, ②, and ③.

current flowing through these circuit elements is

$$I_{\text{load}} = I_{\text{L1}} = I_{\text{Q1}} = I_{\text{L2}} = I_{\text{S}} = \frac{V_{\text{dc}}}{2R_{\text{L}} + R_{\text{Q}} + R_{\text{S}} + R_{\text{load}}} \tag{1}$$

where R_{Q} is the on-state resistance of the MOSFET, which is in milliohm level; R_{L} and R_{S} are the resistances of the superconducting inductor and resistor. These two resistances can be neglected in mode ①. In addition, the voltage across the C_1 is almost same as the V_{dc}, and the currents flowing through the two capacitors (C_1, C_2) are zero.

Although a superconductor can transport current without resistance, its current-carrying ability is limited. It loses its superconducting behavior if the operating current I_{S} exceeds a certain value (the critical current I_{c}). The instantaneous surge of resistance under such an over-current condition is triggered by the nature of superconductivity. The instantaneous voltage drop V_{S} and its equivalent resistance R_{S} approximately satisfy the power-law model [19], [20]

$$V_{\text{S}} = E_{\text{c}} S_{\text{tape}} \left(\frac{I_{\text{S}}}{I_{\text{c}}} \right)^{n} = I_{\text{S}} R_{\text{S}} \tag{2}$$

where E_{c} represents the critical electric field; n is the material-based index; S_{tape} is the total length of the superconducting tape used.

Current limiting mode ②. oscillating transient, [t_0, t_1]: In mode ②, the entire process can be divided into two sub-processes: temporal triggering process, and steady current-limiting process. In the initial stage after fault occurrence, the two inductors (L_1, L_2) can maintain their initial currents, and the capacitor C_1 can maintain its initial voltage almost unchanged. There is an obvious voltage difference between C_1 and fault point, and then C_1 starts to discharge an ever-increasing current I_{C1} to the fault point through Q_1, C_2, L_{C} and R_{S}. According to Kirchoff's Voltage Law (KVL), the oscillating current I_{C1} in Fig. 4(b) can be expressed by

$$I_{\text{C1}}(t) = \frac{U_{\text{dc}} \sin(\omega t) e^{(-\delta t)}}{\omega L_{\text{C}}} \tag{3}$$

where the damped angular frequency $\omega = \sqrt{\omega_0^2 - \delta^2}$, the undamped angular frequency $\omega_0 = \sqrt{1/(L_{\text{C}} C_1)}$, and the damping coefficient $\delta = (2R_{\text{Q}} + R_{\text{S}})/(2L_{\text{C}})$. The I_{C2} is exactly the same as the I_{C1} during the temporal triggering process, and its peak value must be lower than the I_{L1}. This implies that the I_{Q1} (I_{L1}-I_{C1}) can be always above zero to avoid incorrect breaking operations in mode ②.

Current limiting mode ②. steady state, [t_1, t_2]: After a couple of cycles of oscillations, the transient I_{C1} goes to zero, and the steady-state fault current [Fig. 4(c)] flowing through the R_{S} can be calculated in (1). For the V_{S} and R_{S} in (2), both of them increase exponentially with the increasing ratio of the $I_{\text{S}}/I_{\text{c}}$. This sudden resistance surge during the transition from the superconducting state to quench state limits the fault current automatically. Once the ratio is less than one again, the superconducting state recovers immediately (nature of superconductivity). This is the inherent mechanism to describe the self-acting conversion between mode ① and ②.

Circuit breaking mode ③. transient before ZCS, [t_2, t_3]: If the lasting time of this disturbance is relatively long, the faulty line must be disconnected from the dc bus. Mode ② can be forced to convert to mode ③ by triggering the auxiliary MOSFET Q_2. As shown in Fig. 4(d), C_1 discharges an ever-increasing current I_{C1} to the artificial fault point through Q_1, C_2, and L_{C}. Ignoring the short-circuit impedance, I_{C1} can be considered as an undamped oscillating current

$$I_{\text{C1}}(t) = \frac{U_{\text{dc}} \sin(\omega t)}{\omega L_{\text{C}}}. \tag{4}$$

When the I_{C1} increases to the same value as the real-time I_{L}, the corresponding I_{Q1} drops down to zero at the same time. At this zero-current-crossing time point, the MOSFET Q_1 can be fully turned off to trigger the ZCS operation.

Circuit breaking mode ③. transient after ZCS, [t_3, t_4]: After triggering this ZCS operation, the residual energies stored in the inductive and capacitive components gradually dissipate to zero, as shown in Fig. 4(e).

Circuit breaking mode ③. steady state, [t_4, t_5]: Finally, the voltage across C_2 gradually increases to the same value as V_{dc}, and there is no current flowing through the faulty line, as shown in Fig. 4(f).

Normal operating mode ①. reclosing transient, [t_5, t_6]: When the fault is removed, the breaker can be reclosed, and dc power can be supplied to the load. The current can be ramped to the rated value I_{load}, and the voltage across C_1 gradually increases to the same value as the V_{dc} again.

III. Experimental Results and Analyses

A. Experimental Set-Up

We established an experimental platform for the 24 V/85 A/2 kW CPE-based Z-source LVDC breaker, as shown

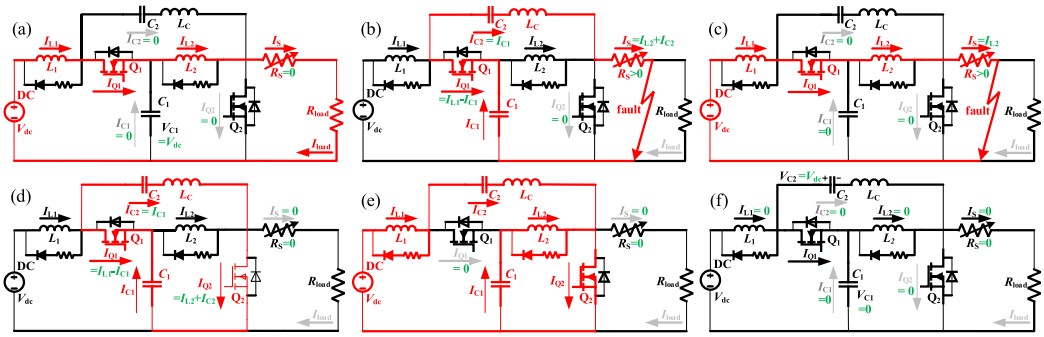

Fig. 4. (a) Normal operating mode ①. (b) Current limiting mode ②: oscillating transient. (c) Current limiting mode ②: steady state. (d) Circuit breaking mode ③: transient before ZCS. (e) Circuit breaking mode ③: transient after ZCS. (f) Circuit breaking mode ③: steady state.

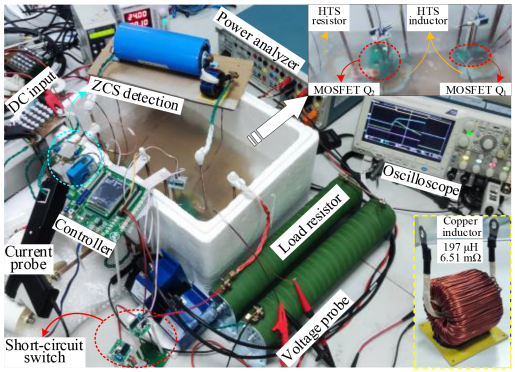

Fig. 5. Experimental set-up for the CPE-based LVDC circuit breaker.

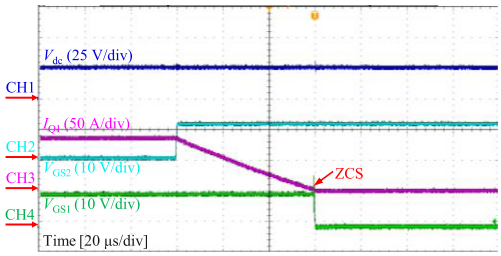

Fig. 6. Waveforms of $V_{\rm dc}$, $I_{\rm Q1}$, $V_{\rm GS1}$, and $V_{\rm GS2}$ during a direct transition from the normal operating mode ① to the circuit breaking mode ③.

in Fig. 5. Two power MOSFETs IPT007N06N were used as the semiconductor-based CPE elements (Q_1, Q_2). Two types of 90-A-class and 200-A-class high-temperature superconducting (HTS) wires were used to make the resistor R_S and the inductors (L_1, L_2). These three superconductor-based CPE elements were wound using a compact pancake coil structure, and were assembled together on the printed circuit board integrated with various small-size power electronic elements. The main parameters as follows: $L_1 = L_2 = 197.8$ μH, $C_1 = 607.4$ μF, $C_2 = 1505.6$ μF, $L_C = 10.2$ μH.

It should be noted that the parameter settings above were mainly based on the detailed circuit analysis described in Section II. When implementing a dc line breaking, the instant discharging current from the capacitor C_1 needed to quickly balance out the initial current passing through the main switch Q_1. In order to further smooth the current fluctuations from both the power source and load, two large-capacity inductors (L_1, L_2) were installed before and after the main switch Q_1. A circuit model was built based on MATLAB/Simulink, and the results showed that with an inductance value (~200 μH), the current drop could be less than 10% during transients and faults. This phenomenon also well matched the CPE-based breaker experiments and other reported results. Based on recent literatures, for the circuit voltage level in tens of volts, inductors rated at 100 μH or above were normally used, e.g., 200 μH inductors for a 35 V/14 A/490 W case [24], and 500 μH inductors for a 20 V/10 A/200 W case [25]. Fortunately, the benefit of high current density in HTS wires makes it available to wind a small-size inductor without any magnetic cores. In theory, these two HTS inductors (L_1, L_2) can be considered as ideal inductors without copper loss and magnetic loss.

B. Direct DC Line Breaking and Dual-Function Experiments

To verify the technical feasibility of the CPE-based Z-source breaker, two experiments were carried out. The first experiment was the direct dc line breaking to trigger the ZCS operation. This scheme can be used when the load needs to be disconnected from the dc line during normal operations, or encounters some high-impedance short-circuit faults. In this experiment, Q_2 was first turned on to trigger an artificial short-circuit event, and then I_{Q1} decreased quickly to zero within 60 μs. At this zero-current point, Q_1 was turned off immediately to trigger the ZCS, as shown in Fig. 6.

The second experiment was the enhanced dual-function scheme, which combined the dc line breaking with the fault current limiting process. This scheme can be used when the dc line encounters some serious disturbances such as the short-time over-load fault and line-to-ground fault. In this experiment, a short-circuit switch connected in parallel with the load was first turned on to create a line-to-ground fault. I_S increased quickly to exceed the critical current of the superconducting resistor, and then an instantaneous surge of resistance was triggered automatically to limit the fault peak.

Fig. 7 shows an entire transition from the normal operating mode ① to the current limiting mode ②, and finally to the circuit breaking mode ③. During the oscillating transient at the

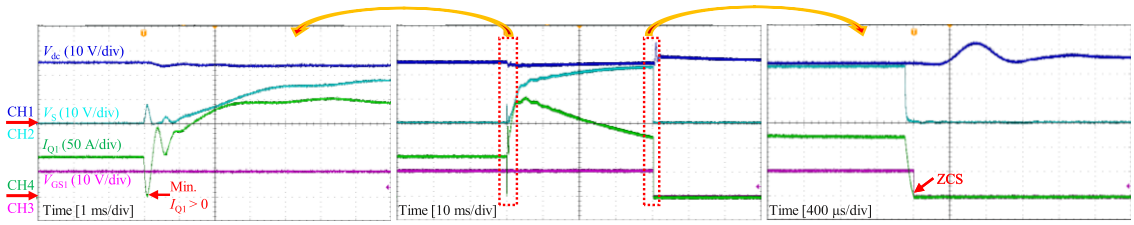

Fig. 7. Waveforms of V_{dc}, V_S, I_{Q1}, and V_{GS1} during an entire transition from the normal operating mode ① to the current limiting mode ②, and finally to the circuit breaking mode ③.

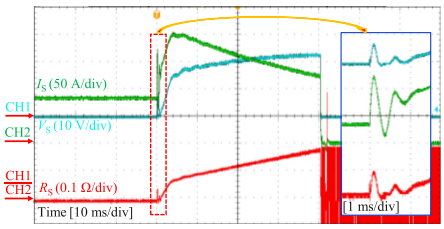

Fig. 8. Waveforms of V_S, I_S, and R_S corresponding to Fig. 7.

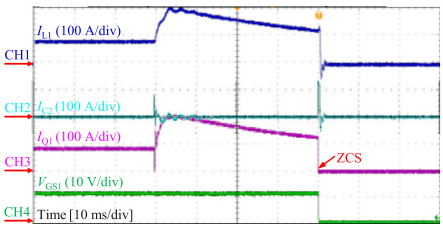

Fig. 9. Waveforms of I_{L1}, I_{C2}, I_{Q1}, and V_{GS1} corresponding to Fig. 7.

beginning of mode ②, a "small" fault current peak ($\approx I_{L1} + I_{C2}$) was first suppressed. As shown in Fig. 8, within 100 μs after the fault occurred, I_S (current flowing through superconducting resistor) quickly reached a peak of 175 A, and the instantaneous R_S (auto-triggered superconducting resistance when encountering faults) reached about 0.05 Ω. The corresponding I_{Q1} decreased quickly from the nominal value 85 A to its minimum value 5 A. Afterward, the whole circuit entered into the steady mode ②. Both Figs. 8 and 9 show that after entering the steady-state, the variation trends of the I_{Q1}, I_{L1}, and I_S were almost the same. Steady-state results show within 5 ms after the fault occurred, a high fault current peak ($I_S = 204$ A) was safely suppressed.

More importantly, the input voltage V_{dc} from the dc bus almost remained unchanged during the whole fault period. This means that the proposed CPE-based breaker device can suppress the over-current in the faulty line, but also can stabilize the dc bus voltage to supply normal power to other loads sharing the same bus in an actual dc microgrid.

It should be noted that the heat accumulation inside the superconducting resistor further increased the fault-limiting resistance. During the steady state in mode ②, this increasing resistance continuously inhibited the fault current. However, if the lasting time is too long, this event can be identified as an actual fault rather than a transient disturbance, and thus the faulty line must be disconnected from the dc bus.

In the experiment, the maximum duration was set as 40 ms, to judge whether it was a "real" fault to trigger the dc breaking. If the line current returned to normal within 40 ms, the proposed CPE-based breaker could automatically convert from modes ② to ①. The dc bus continued to supply power to the load, and the superconducting resistor also automatically went back to zero-resistance.

C. *Performance Comparisons: CPE-Based Breaker Versus Conventional Room-Temperature Breakers*

For a conventional room-temperature dc breaker without the superconducting resistor, when a short-circuit fault occurred, although two inductors (L_1, L_2) were able to slow down the fault surging, they could not keep suppressing the current for a long time. For a 40-ms transient disturbance, the estimated fault peak would reach 2.4 kA, which would directly destroy the whole breaker. By contrast, in the proposed CPE-based breaker system, the fault current in Fig. 8 was merely 125 A at 40 ms. At this moment, the superconductor-based current-limiting resistance was around 0.2 Ω, which well protected the breaker from being damaged.

To avoid the risk of destroying devices, most conventional breakers are designed to implement the breaking operation immediately whenever a short-time/transient disturbance or a long-time/permanent fault occurs [26]. However, for those very short-time disturbances in dc microgrids [27], relatively large transient over-currents could happen in dc lines. For example, the sudden connection or disconnection of a high-power electric vehicle (EV) into an EV charging station [28], or some auto-recovered ground faults could cause large surge currents. However, these surge currents are transient, and will attenuate down to normal values in a very short time. For these situations, conventional breakers suffer the problem of "over sensitive," which will wrongly identify dc lines having "permanent" short-circuit faults and unnecessarily cut off the loads. These "over sensitive" actions will largely affect the reliability of the power supply to loads, and meanwhile, frequent switching actions of dc circuit breakers will also possibly induce extra undesired surge currents to further threaten the stability of the entire dc microgrid.

Even worse, for the faults with less severity and slower dynamics, the fault current may not be sufficiently large to

naturally trigger the conventional breakers [24]. Specifically, if a high-impedance fault or an attenuating short-circuit fault occurs in the load side, the amplitude differences between the fault current and normal current might be very small. The instant discharging current from the capacitor C_1 cannot fully balance out the initial current passing through the main switch Q_1, which means the ZCS operation cannot be realized using conventional breaking methods. In the proposed CPE-based breaker system, an artificial short-circuit switch Q_2 has been added. Once those slight faults happen, Q_2 can be quickly switched on, to produce an artificial ZCS condition, and then the corresponding faulty line can be cut off immediately.

It should be noted that, as conventional breakers cannot quickly cut off those slight faults above, those fault currents will progress steeply. Although an additional power-electronics-based fault current limiter can suppress the current, it also raised two extra issues [3], [4], [5]: (i) Time-delayed fault detection slows down the current limiting response during fault transients; and (ii) Power electronics and impedance elements causes additional loss during normal operations.

By contrast, in the proposed CPE-based breaker system, the superconducting resistor can suppress all kinds of fault currents. No matter the fault currents are caused by short-time/transient disturbances or long-time/permanent faults, the superconducting resistor can speedily response and induce a high impedance to effectively suppress the fault current, by the nature of superconducting materials [20]. Therefore, this newly added superconducting resistor can avoid those unnecessary/wrong breaking actions by conventional circuit breakers, and can substantially protect the entire system with improved stability and fault-tolerance. Moreover, as the superconducting resistor can be instantly self-triggered to suppress the fault peaks in a very early stage, and this unique advantage can also help other conventional protection schemes to have more time to response, and collaboratively protect the entire dc microgrid.

IV. Discussions: Energy Efficiency and Applications

A. Cryogenic COP Analysis

For an ideal reversible cryogenic device, the coefficient of performance *COP* is defined as follows:

$$COP = \frac{Q_{\mathrm{C}}}{W_{\mathrm{in}}} = \frac{T_{\mathrm{C}}}{T_{\mathrm{H}} - T_{\mathrm{C}}} \tag{5}$$

where Q_{C} is the heat energy removed to build up the cryogenic environment from a high temperature T_{H} to a low temperature T_{C}, and W_{in} is the actual electric energy used for the cooling work. For the LN_2 environment in this work, the T_{C} and T_{H} are 77 and 300 K, and the *COP* can be optimized up to 0.35. However, a real cooling process is always less efficient than the ideal reversible process. For most commercial cryogenic devices, the *COP* can achieve a reasonable value of 0.2 [29]. Therefore, the actual power consumption (i.e., cryogenic conduction loss + equivalent cooling loss) is up to 6 W, in order to realize 1 W cooling power (77 K, LN_2 environment).

TABLE I
Operating Losses Measured in the 2 and 20 kW Case Studies

Loss elements	24 V/85 A/2 kW		240 V/85 A/20 kW	
	77 K (New)	300 K (Conventional)	77 K (New)	300 K (Conventional)
Switch loss	2.38 W	6.30 W	11.57 W	118.76 W
Inductor loss	≈ 0	94.07 W	≈ 0	94.07 W
Resistor loss	≈ 0	N/A	≈ 0	N/A
Lead loss	3.96 W	N/A	3.96 W	N/A
Total loss (excluding cryogenic system)	6.34 W	100.37 W	15.53 W	212.83 W
Total loss (whole system)	**38.04 W**	**100.37 W**	**93.18 W**	**212.83 W**

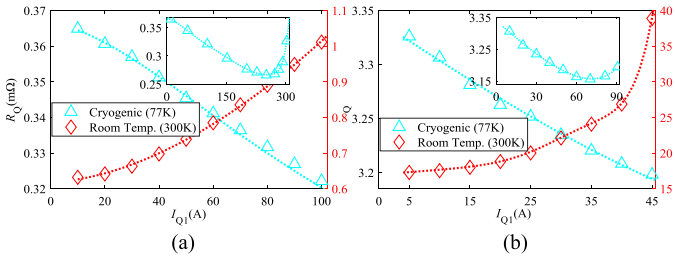

Fig. 10. Measured and fitted on-state resistance behaviors at 77 and 300 K. (a) IPT007N06N. (b) IXTX120N65X2.

B. Loss Comparisons: CPE-Based Breaker Versus Conventional Room-Temperature Breakers

To clarify the overall energy efficiency of the CPE-based breaker, the operating losses of the main circuit components were measured, and listed in Table I. Two types of 60-V-class and 650-V-class MOSFETs were tested in the experiments: i) IPT007N06N from Infineon Technologies; ii) IXTX120N65X2 from IXYS Corporation. For the 2 and 20 kW case studies, one unit of 60-V-class MOSFET and two parallel units of 650-V-class MOSFETs were used as the dc breaking switch Q_1. Their rated currents were the same (85 A), and the measurements of the on-state resistances of these MOSFETs (Fig. 10) were used to estimate switch losses.

1) *Switch loss:* In the cryogenic environment (77 K), the switch losses were about 2.38 and 11.57 W in the 60-V-class and 650-V-class MOSFETs. By contrast, they increased to 6.30 and 118.76 W, at the room temperature (300 K).
2) *Inductor loss:* These two superconducting inductors (L_1, L_2) had zero loss with a normal current (85 A). However, those two copper inductors (rated at ∼100 A) had a total loss of 94.07 W with a dc resistance of 6.51 mΩ [21].
3) *Resistor loss:* Similarly, the superconducting resistor R_{s} also had zero loss when the normal operating current was below its critical value.
4) *Lead loss:* Due to the temperature difference between the cryogenic and room-temperature environments, two current leads had inevitable heat leakage. For an optimized heat leakage of 23.3 W/kA for each lead terminal [30], 85 A current caused 3.96 W heat leakage.

To summarize, the total loss measured at 77 K was 6.34 W in the 2 kW case study, and was 15.53 W in the 20 kW case study. By using a realistic *COP* (0.2), the total loss of the whole system was 38.04 W (2 kW case study), and was 93.18 W (20 kW case study). By contrast, the corresponding loss measured at 300 K was up to 100.37 W for the 2 kW case study), and was up to 212.83 W for the 20 kW case study. Therefore, the total loss reduced by 62.10% (2 kW case study), and reduced by 56.22% (20 kW case study). Results proved that the CPE-based breaker had much higher energy efficiency over conventional room-temperature breakers.

C. Benefits for Potential Large-Scale Applications

With the rapid global development of digital economy, the high-efficiency high-reliability dc power distribution technology is becoming urgently essential for data centers, which contain large amounts of information-technology (IT) equipments. In order to protect these dc sensitive loads, the proposed CPE-based breaker device is favored by its unique advantages of ultralow power loss and automatic fault current limiting. Replacing the conventional room-temperature breakers by the proposed CPE-based breaker can improve the power supply reliability of IT equipments whenever they encounter a transient disturbance or a permanent fault, but also improve the energy efficiency of the entire system. For a 10 MW data center application scenario in [31], 500 units of 20-kW-class CPE-based breaker units can be directly installed to interconnect the 240 V dc bus to a series of IT cabinets. Compared with conventional breaker assemblies, the total power loss can be reduced by 59825 W. For long-time operation, the total electricity saving can be up to 524067 kWh every year.

V. Conclusion

A novel CPE based Z-source LVDC circuit breaker has been designed, fabricated, and tested, for the first time (based on literature studies). The new circuitry can integrate three advantages of ultralow loss, automatic fault-current limiting, and ZCS, into an all-in-one power device.

1) *Ultralow power loss:* Replacing copper inductors by superconducting inductors realized zero conduction loss. The cryogenic operation of power MOSFETs only had $<10\%$ on-state resistance of that in room temperature. Even measuring the actual overall system loss (including cryogenic issues), the total system loss reduced by 62.10% in the 2 kW case study, and reduced by 56.22% in the 20 kW case study.
2) *No-delay automatic fault current limiting:* The superconducting resistor was a self-acting fault current limiter based on the nature of superconductivity. For the 2 kW case study, it manifested itself as an ideal 0 Ω resistor with an operating current 85 A, and provided a sudden protective 0.1 Ω resistor to suppress the fault current below 200 A, and it also stabilized the dc bus voltage to normally supply power.
3) *Zero-current circuit breaking:* With the cooperation of the superconducting inductors/resistors and the artificial short-circuit switch, the improved Z-source breaker realized both the active device isolation and passive fault isolation within 60 μs.

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