An Interleaved High Step-Up DC/DC Converter-Based Three-Winding Coupled Inductors With Symmetrical Structure

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***Abstract*—This article proposes an interleaved high step-up converter based on three-winding coupled inductor (TW-CI) with symmetrical structure. By utilizing the TW-CI along with a voltage multiplier cell, the proposed converter achieves high power transfer ability as well as minimized voltage stress across power switches and diodes. The converter has significantly improved the voltage gain by integrating two TW-CIs with the passive clamp circuit. The leakage inductor energy of the TW-CI is recycled to improve the voltage gain and efficiency while facilitating the soft switching condition for the power switches. Additionally, the voltage stress across the power switches is decreased with the help of the clamping capacitors. Therefore, low-voltage-rated semiconductors with small on-resistance can be chosen which reduce conduction losses and improve the overall performance. Moreover, two series-connected capacitors of the primary side are introduced, which effectively balance the voltage between the power switches and the capacitors during steady and dynamic states. Finally, a 400 W experimental prototype with 24–400 V is built to verify the accuracy of the proposed converter.**

***Index Terms*—Dc–dc converter, high step-up, low voltage stress, three-winding coupled inductor (TW-CI), zero-current switching.**

I. Introduction

TO ACHIEVE the global carbon neutrality target, the global energy system structure has been adjusted on a regular basis, and the proportion of new energy sources connected to the power grid has continued to increase. However, the renewable energy sources, such as photovoltaic, fuel cells, offer a low voltage level (12∼48 V), which provide insufficient voltage for the inverter. Therefore, a high step-up and high-performance dc–dc converter is required. The high step-up and high-performance dc–dc converter is directly connected to the renewable energy sources and contributes to raising the voltage to a higher level (200∼400 V).

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In recent years, scholars have proposed a series of high step-up schemes such as cascade, switched inductor, switched capacitor (SC), interleaved technology, isolated voltage boosting, voltage multiplier cell (VMC), coupled inductor (CI), and other voltage boosting techniques [1], [2], [3]. The CI is a straightforward, efficient, and convenient approach to achieve a high voltage conversion ratio when compared to other voltage boosting techniques. The CI converters have the flexibility to adjust the turns-ratio to control the necessary voltage gain.

In various boosting techniques, CI is widely used because of its simplicity and convenience. A series of high step-up converters with the CI were proposed in [2]. However, the leakage inductor of CI would result in voltage spikes, which leads to more voltage stress on semiconductors. In [4] and [5], the impact of the leakage inductor was eliminated by integrating the SC technology into the converters. By utilizing the VMCs with SC, the energy of the leakage inductor is recovered in [6] and [7]. In this way, the voltage gain had improved and a group of expandable CI high step-up converters with clamping were given.

In high-power applications, the interleaved high step-up converters were used as an efficient solution to increase the conversion efficiency, reduce the current ripple, etc. Therefore, a series of high step-up converters with interleaved structure were proposed. The interleaved structure applied to high step-up converters were presented in [8], [9], and [10]. A high step-up active-switched-inductor converter with CI was proposed in [11]. The interleaved technique is employed into the Sepic in [12]. By integrating different fundamental converters, a novel high step-up converter with interleaved structure was proposed in [13]. The aforementioned interleaved converters can improve the transmission power capability. However, the above converters are asymmetrical, which makes it challenging to select the components. And those converters demand a lot of passive components, which raises the cost. Therefore, a double switch converter with symmetric structure was proposed in [14], which has achieved the voltage balance of power switches and capacitors in steady and dynamic state.

An interleaved structure with double CI structure was proposed in [15] and [16]. A series of high step-up dc–dc converters with three-winding coupled inductor (TW-CI) were proposed in [17], [18], [19], [20], [21], and [22], which effectively improved the voltage gain of the converters. The interleaved converter with TW-CI was presented in [23], which has improved the voltage

gain and power transfer capability. By integrating TW-CIs with a VMC, the voltage gain of the interleaved converter was improved in [24].

Inspired by the mentioned papers, the symmetrical interleaved dc–dc converter with TW-CI is presented in this article. By using two capacitors at the input, the voltage balance of the power switches and capacitors are realized in a steady and dynamic states. The diode-capacitor cells are used as a passive clamp to absorb the energy of the leakage inductor, which eliminates voltage stress across the power switches. In this way, the current peak and voltage stress of the power switches is effectively suppressed, and the zero current switching (ZCS) of power switches are realized.

In this article, an interleaved high step-up converter-based TW-CI was proposed. The main benefits of the proposed converter can be regarded as follows:

1) Ultrahigh step-up is obtained by integrating two group of TW-CI.
2) The proposed converter is a symmetrical structure, and the stresses in the circuit are distributed.
3) The interleaved structure results in shared thermal stress across the phases and low input current ripple.
4) The ZCS of the power switches are implemented to decrease the switching losses, the efficiency has significantly increased.
5) The voltage stress on the semiconductors is significantly lower than the output voltage.
6) The current falling rate of the diodes is controlled by the leakage inductor of the TW-CI.
7) The symmetric construction is used instead of asymmetric high step-up converters, which is beneficial for reducing the electromagnetic interference (EMI) of system.

The rest of this article is as follows. The topology of the proposed converter is presented, and the operating principles are analyzed in Section II. Section III is devoted to the steady-state analysis of the proposed converter. The efficiency and loss analysis of the proposed converter are presented in Section IV. The design of the proposed converter is presented in Section V. Section VI is devoted to the comparative analysis and the experimental results analysis of the proposed converter. Finally, the conclusion of this article is presented in Section VII.

II. Proposition and Modal Analysis of Converters

A. Structure of the Proposed Converter

The TW-CI is employed to the basic high step-up converter with CI. The high step-up converter with TW-CI is shown in Fig. 1(a). To improve the power transfer ability, the two phase of the high step-up converter with TW-CI is interleaved, and the new topology is shown in Fig. 1(b). As seen in Fig. 1(c), the input of the high step-up converter is divided into two capacitors, which can realize the voltage balance of the power switches under steady and dynamic states. The voltage gain of the proposed converter is further enhanced, and its circuitry is symmetrical. The energy of leakage inductor is recycled with the help of the clamping capacitors to reduce the voltage spikes of the semiconductors.

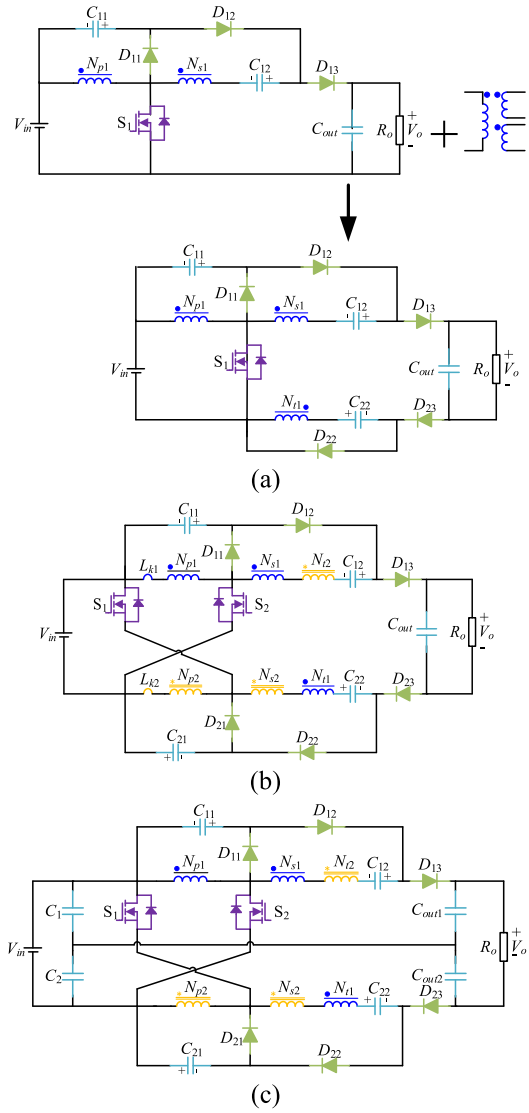

Fig. 1. Evolution of topology. (a) High step-up converter with TW-CI. (b) Symmetrical high step-up converter with TW-CI. (c) Proposed converter.

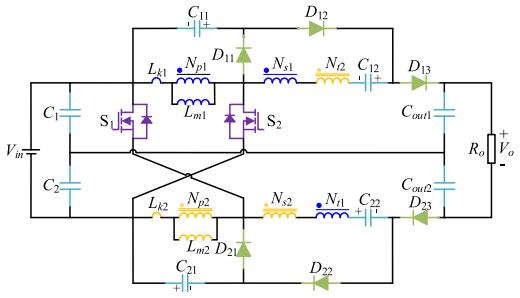

Fig. 2. Equivalent circuit of the proposed converter.

B. Modal Analysis of the Proposed Converter

The equivalent circuit of the converter is shown in Fig. 2. The TW-CI consists of magnetizing inductor L_m, leakage inductor L_k, secondary-tertiary wingdings. The turns-ratio of TW-CI are n_{s1}, n_{s2}, n_{t1}, and n_{t2}. The main working waveform in one cycle is shown in Fig. 3.

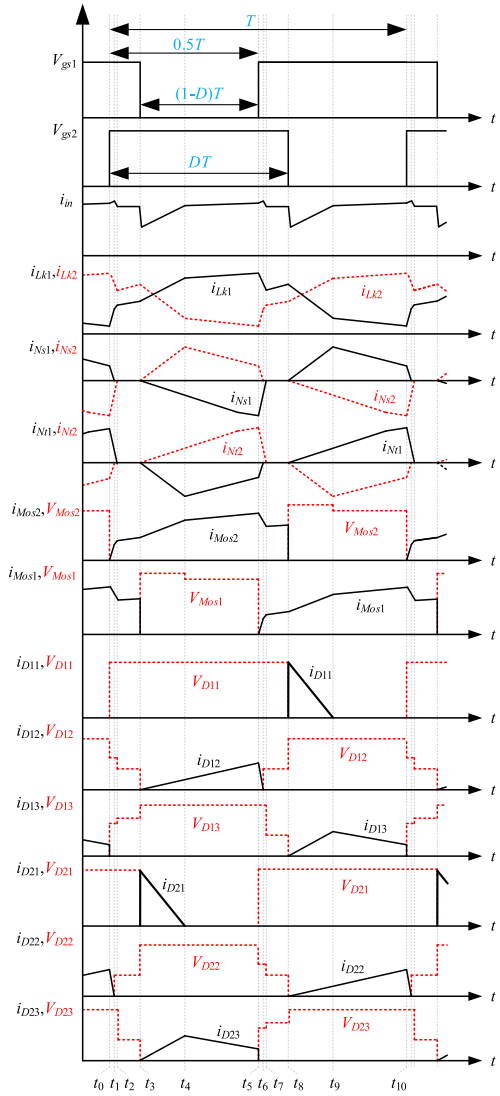

Fig. 3. Key waveform of the proposed converter.

Mode 1 ($t_0 \le t \le t_1$): At $t = t_0$, the magnetizing inductor L_{m1} and leakage inductor L_{k1} are charged by the source V_{in} and capacitor C_1, which result the current i_{Lm1} and i_{Lk1} to increase linearly. The energy of C_{12} and the secondary-tertiary windings N_{s1}, N_{t2} are delivered to the load via the diode D_{13}. The secondary-tertiary windings N_{s1} and N_{t2} charge the C_{22} via the D_{22}. Since the power switch S_2 is just turned ON, the input current i_{in} will quickly increase. The current flow is shown in Fig. 4(a).

Mode 2 ($t_1 \le t \le t_2$): During this mode, the power switches S_1 and S_2 remain ON-state, the D_{22} is forward biased. The magnetizing inductor L_{m1} and the leakage inductor L_{k1} are charged by the power supply V_{in}, which result the currents i_{Lm1} and i_{Lk1} to increase linearly. The capacitor C_{22} is charged by the secondary-tertiary windings N_{s2} and N_{t1} via the D_{22}. Because the diodes D_{13} and D_{23} are reverse biased, the load is charged by C_{out1} and C_{out2}. The current flow in this mode is shown in Fig. 4(b).

Mode 3 ($t_2 \le t \le t_3$): In this mode, all of the diodes are reverse biased and the power switches S_1 and S_2 are kept in the ON-state. The magnetizing inductors L_{m1}, L_{m2} and the leakage inductors L_{k1}, L_{k2} are charged by the power supply V_{in}. The current of the magnetizing inductors, i_{Lm1} and i_{Lm2}, increase linearly. The load is supplied by the capacitors C_{out1} and C_{out2}. Because the rise speed of the current of leakage inductor i_{Lk1} coincides with the drop speed of the current of leakage inductor i_{Lk2}, the input current i_{in} is almost unchanged in this mode. The current flow in the circuit is shown in Fig. 4(c).

$$i_{Lk1} = i_{Lm1} = i_{Lm1}(t_2) + \frac{V_{in}}{L_{m1}}(t - t_2) \tag{1}$$

$$i_{Lk2} = i_{Lm2} = i_{Lm2}(t_2) + \frac{V_{in}}{L_{m2}}(t - t_2). \tag{2}$$

Mode 4 ($t_3 \le t \le t_4$): In this mode, the power switch S_1 turns OFF, and the diodes D_{12}, D_{21}, and D_{23} are forward biased. Since the magnetizing and leakage inductors are charged by power supply V_{in}, the currents i_{Lm1} and i_{Lk1} grow linearly. The C_{12} is charged by the power supply V_{in} and C_{11} via the D_{12}. And the C_{21} is charged by the leakage inductor L_{k2} via the D_{21}. During this mode, the input current is determined by adding the currents of the power switch S_2 and diode D_{23}. The current flow is shown in Fig. 4(d).

$$V_{in} = V_{C12} - V_{C11} - V_{Ns1} - V_{Nt2}. \tag{3}$$

Mode 5 ($t_4 \le t \le t_5$): In this mode, the energy of the leakage inductor L_{k2} has been released. The rest of this mode is similar to mode 4. The current flow is shown in Fig. 4(e).

Mode 6 ($t_5 \le t \le t_6$): In this mode, the power switch S_1 is turned ON, and the D_{12} and D_{23} are forward biased. The magnetizing inductor L_{m2} and the leakage inductor L_{k2} are charged by the power supply V_{in} and C_1, which causes the current i_{Lm2} and i_{Lk2} to grow linearly. Though the D_{23}, the load absorbs the energy of secondary-tertiary windings N_{s2}, N_{t1}, and C_{12}. Due to the conduction of S_1, the C_{12} is charge by the N_{s1} and N_{t2} via D_{22}. The current flow is shown in Fig. 4(f).

Mode 7 ($t_6 \le t \le t_7$): In this mode, the power switches S_1 and S_2 are ON-state, and the D_{12} is forward biased. The power supply V_{in} charges the magnetizing inductor L_{m2} and the leakage inductor L_{k2}, which causes the current i_{Lm2} and i_{Lk2} to increase linearly. Due to the D_{13} and D_{23} are reverse biased, the load is supplied by the C_{out1} and C_{out2}. The current flow is shown in Fig. 4(g).

Mode 8 ($t_7 \le t \le t_8$): In this mode, all of the diodes are reverse biased and the power switch S_1 and S_2 are kept in the ON-state. The magnetizing inductors L_{m1} and L_{m2}, and the leakage inductors L_{k1} and L_{k2} are linearly charged by the power supply V_{in}. During this mode, the current flow in the circuit is shown in Fig. 4(h). The following relationship can be derived from the current of leakage and magnetizing inductor:

$$i_{Lk1} = i_{Lm1} = i_{Lm1}(t_7) + \frac{V_{in}}{L_{m1}}(t - t_7). \tag{4}$$

Mode 9 ($t_8 \le t \le t_9$): In this mode, the power switch S_2 remains OFF-state, and the D_{11}, D_{13}, and D_{22} are forward biased. The magnetizing inductor L_{m2} and the leakage inductor L_{k2} are charged by the source V_{in}, the current of i_{Lm2} and i_{Lk2} increases linearly. The power supply V_{in} and the C_{21} are charged C_{22} via the D_{22}. The leakage inductor L_{k1} is charged C_{11} via the D_{11}.

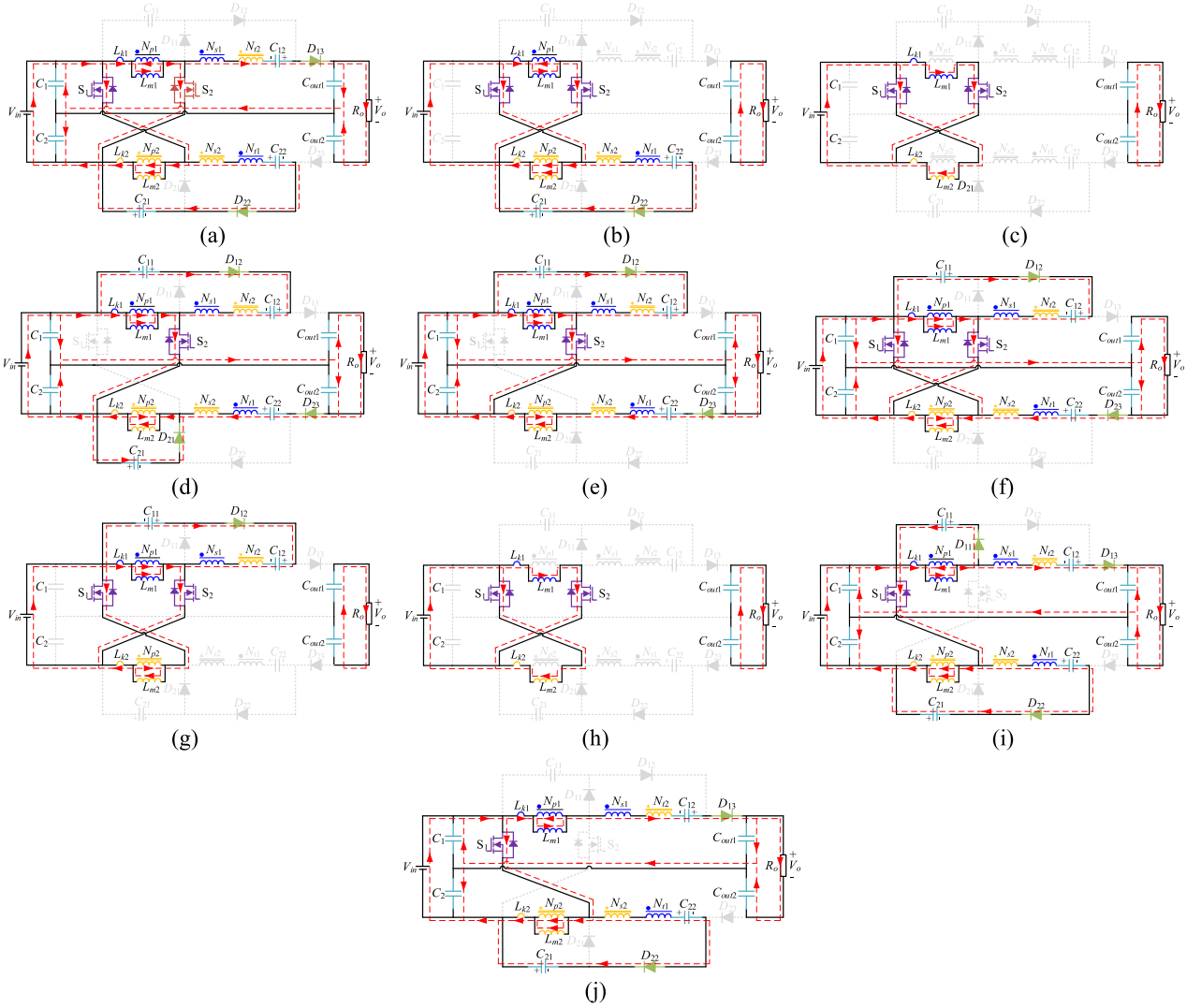

Fig. 4. Operation modes in one period. (a) Mode 1 [t_0~t_1]. (b) Mode 2 [t_1~t_2]. (c) Mode 3 [t_2~t_3]. (d) Mode 4 [t_3~t_4]. (e) Mode 5 [t_4~t_5]. (f) Mode 6 [t_5~t_6]. (g) Mode 7 [t_6~t_7]. (h) Mode 8 [t_7~t_8]. (i) Mode 9 [t_8~t_9]. (j) Mode 10 [t_9~t_{10}].

Through the D_{13}, the load is charged by C_2 and C_{out2}. The current flow is shown in Fig. 4(i). The following equations can be achieved for this mode.

$$V_{in} = V_{C22} - V_{C21} - V_{Ns2} - V_{Nt1} \tag{5}$$

$$i_{Lk2} = i_{Lm2} = i_{Lm2}(t_7) + \frac{V_{in}}{L_{m2}}(t - t_7). \tag{6}$$

Mode 10 ($t_9 \le t \le t_{10}$): In this mode, the power switch S_2 is forward biased, and the D_{11} is forward biased. Since the energy of the leakage inductor L_{k1} has been discharged. The rest of this mode is similar to mode 9. The current flow is shown in Fig. 4(j).

III. Steady-State Analysis of Proposed Converter

For convenience in analysis, the following assumptions are made:

1) All of the switching components are an ideal component.
2) The parasitic parameters of the inductive and capacitive components are ignored.
3) The capacitance is infinite, and the voltage ripple is ignored.
4) The turn ratios of the TW-CI are: $n_{s1} = N_{s1}/N_{p1}$, $n_{s2} = N_{s2}/N_{p2}$, $n_{t1} = N_{t1}/N_{p1}$, $n_{t2} = N_{t2}/N_{p2}$.

A. Voltage Gain of the Proposed Converter

The coupled coefficient of TW-CI is presumed as follows:

$$k = \frac{L_{m1}}{L_{m1} + L_{k1}} = \frac{L_{m2}}{L_{m2} + L_{k2}}. \tag{7}$$

The secondary-tertiary windings voltage of the TW-CI is expressed as follows:

$$\begin{cases} V_{Ns1} = n_{s1} V_{Lm1} \\ V_{Ns2} = n_{s2} V_{Lm2} \\ V_{Nt1} = n_{t1} V_{Lm1} \\ V_{Nt2} = n_{t2} V_{Lm2} \end{cases}. \tag{8}$$

To facilitate steady-state analysis, the four short-time transition modes of modes 1, 2, 6, and 7 are ignored. By applying

Kirchhoff's voltage law (KVL) to the loops shown in Fig. 4(c), the following equation can be derived.

$$V_{Lm1}^{(3)} = V_{Lm2}^{(3)} = kV_{in}. \tag{9}$$

By applying KVL to the loops shown in Fig. 4(d), the following equations can be obtained.

$$V_{Lm1}^{(4)} = kV_{in} \tag{10}$$

$$V_{in} = V_{C12} - V_{C11} - V_{Ns1}^{(4)} - V_{Nt2}^{(4)} \tag{11}$$

$$V_{Lm2}^{(4)} = kV_{C21}. \tag{12}$$

By applying KVL to the loops shown in Fig. 4(h), the following equation can be derived.

$$V_{Lm1}^{(8)} = V_{Lm2}^{(8)} = kV_{in}. \tag{13}$$

By applying KVL to the loops shown in Fig. 4(i), the following equations can be obtained.

$$V_{Lm2}^{(9)} = kV_{in} \tag{14}$$

$$V_{in} = V_{C22} + V_{Ns2}^{(9)} + V_{Nt1}^{(9)} - V_{C21} \tag{15}$$

$$\mathrm{V}_{Lm1}^{(9)} = kV_{C11}. \tag{16}$$

According to the voltage-second balance of the magnetizing inductor L_{m1} and L_{m2}, the voltage of C_{11}, C_{12}, and C_{22} can be solved by using (8)–(16):

$$V_{C11} = V_{C21} = \frac{D}{1-D}V_{in} \tag{17}$$

$$V_{C12} = \left(k\left(n_{s1} - n_{t2}\right) + \frac{1+kn_{t2}}{1-D}\right)V_{in} \tag{18}$$

$$V_{C22} = \left(k\left(n_{s2} - n_{t1}\right) + \frac{1+kn_{t1}}{1-D}\right)V_{in}. \tag{19}$$

The voltage gain of the converter is deduced as follows:

$$G = \frac{V_o}{V_{in}} = \frac{3 + k\left(n_{s1} + n_{s2} + n_{t1} + n_{t2}\right) + D}{1-D}. \tag{20}$$

From (20), the voltage gain of the converter is related to the coupling coefficient k, turns-ratio n, and duty D. The voltage gain ratio is shown as a function of k, n, and D in Fig. 5.

When the turns ratio is $n = n_{s1} = n_{s2} = n_{t1} = n_{t2}$. The voltage gain is determined as follows:

$$G = \frac{V_o}{V_{in}} = \frac{3 + 4kn + D}{1-D}. \tag{21}$$

B. Voltage Stress of the Proposed Converter

According to (8)–(19) and (21), the voltage stress of capacitors C_1, C_2, C_{11}, C_{12}, C_{21}, and C_{22} are derived as follows:

$$V_{VpsC1} = V_{VpsC2} = \frac{1-D}{2\left(3+4n+D\right)}V_o \tag{22}$$

$$V_{VpsC11} = V_{VpsC21} = \frac{D}{3+4n+D}V_o \tag{23}$$

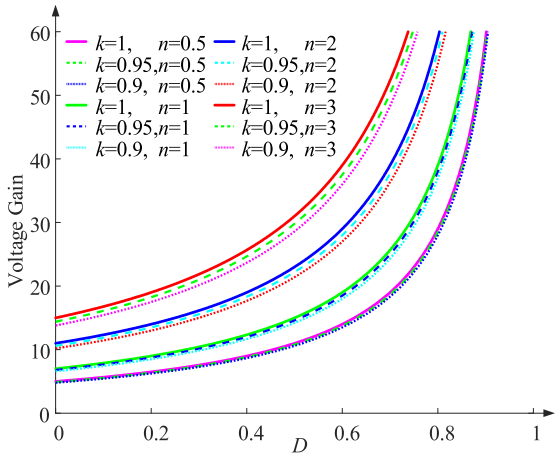

Fig. 5. Relationship between k, n, D, and voltage gain.

$$V_{VpsC12} = \frac{1+kn_{t2}+k\left(n_{s1}-n_{t2}\right)\left(1-D\right)}{3+4n+D}V_o \tag{24}$$

$$V_{VpsC22} = \frac{1+kn_{t1}+k\left(n_{s2}-n_{t1}\right)\left(1-D\right)}{3+4n+D}V_o \tag{25}$$

$$V_{VpsCout1} = V_{VpsCout2} = \frac{1}{2}V_o. \tag{26}$$

According to (22)–(26), the voltage stress of the capacitors is related to duty and output voltage. The voltage stress of the capacitors is lower than the output voltage, and the maximum voltage stress is only half of the output voltage.

The voltage stress of the power switches and diodes can be calculated as follows.

$$V_{VpsS1} = V_{VpsS2} = \frac{1}{3+4n+D}V_o \tag{27}$$

$$V_{VpsD11} = V_{VpsD21} = \frac{1}{3+4n+D}V_o \tag{28}$$

$$V_{VpsD12} = V_{VpsD22} = \frac{1+2n}{3+4n+D}V_o \tag{29}$$

$$V_{VpsD13} = V_{VpsD23} = \frac{1+2n}{3+4n+D}V_o. \tag{30}$$

According to (27)–(30), the voltage stress across the power switches and diodes are lower than the output voltage. Therefore, it is possible to utilize the semiconductors with lower parasitic parameters (MOSFETs with lower $R_{DS(on)}$ and diodes with lower forward drop voltage V_F), which reduces the power losses and the cost.

According to the charge conservation law of the clamping capacitors, the average current of the output diodes can be obtained as follows:

$$I_{D12} = I_{D13} = I_{D22} = I_{D23} = \frac{1}{1-D}I_o. \tag{31}$$

From the analysis of the converter operating in continuous conduction mode (CCM), the average current of the magnetizing

and leakage inductor is

$$I_{Lk1(Avg)} = I_{Lk2(Avg)} = I_{Lm1} = I_{Lm2} = \frac{3+4n+D}{2\left(1-D\right)} I_o. \tag{32}$$

IV. Efficiency and Loss Analysis of the Proposed Converter

The loss analysis of the proposed converter is performed by considering the loss of the power switches, diodes, capacitors, and magnetic components.

A. Switch and Diode Loss

The power switches realize the ZCS conduction, so the losses of power switches can be calculated as follows.

$$P_s = I_{rms-s1}^2 R_{s1} + I_{rms-s2}^2 R_{s2} + \frac{C_r\left(V_{s1}^2 + V_{s2}^2\right) + \left(V_{s1} I_{s1-off} + V_{s2} I_{s2-off}\right) t_f}{2} f_s \tag{33}$$

where t_f and C_r are the falling time and output capacitance of the switches; V_{s1}, V_{s2}, $I_{s1\text{-}off}$, and $I_{s2\text{-}off}$ are the voltage and current stress. And the RMS current of the power switches are

$$I_{rms-s1} = I_{rms-s2} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-s1}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-s2}^2 dt}{T}} = \frac{\left(3+4n+D\right) I_o}{2\left(1-D\right)} \sqrt{3-2D}. \tag{34}$$

The loss of the diodes can be expressed as follows.

$$P_D = \sum_{j=1,2} \sum_{k=1,2,3} \left(V_F I_o + I_{rms-Djk}^2 r_{Djk}\right) \tag{35}$$

where V_F is the forward voltage drop of diodes, and the RMS current of diodes are

$$I_{rms-D11} = I_{rms-D21} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-D11}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-D21}^2 dt}{T}} = \frac{I_o}{6} \sqrt{\frac{6(3D(D+8n+2)+24n(2n+1)+7)}{\left(4n+D+1\right)\left(1-D\right)}} \tag{36}$$

$$I_{rms-D12} = I_{rms-D22} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-D12}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-D22}^2 dt}{T}} = \frac{2I_o}{\sqrt{3\left(1-D\right)}} \tag{37}$$

$$I_{rms-D13} = I_{rms-D23} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-D13}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-D23}^2 dt}{T}} = \frac{2I_o}{\sqrt{3\left(1-D\right)}}. \tag{38}$$

B. Capacitance and Magnetic Loss

The loss of the capacitors can be expressed as follows:

$$P_c = \sum_{k=1,2} \sum_{j=1,2} I_{rms-ckj}^2 R_{ckj} + \sum_{k=1,2} \left(I_{rms-ck}^2 R_{ck} + I_{rms-coutk}^2 R_{coutk}\right). \tag{39}$$

The RMS current of the capacitors are

$$I_{rms-C11} = I_{rms-C21} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-C11}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-C21}^2 dt}{T}} = I_o \sqrt{\frac{\left(4n+D+3\right)\left(12n+3D+5\right)}{6\left(1-D\right)\left(4n+D+1\right)}} \tag{40}$$

$$I_{rms-C12} = I_{rms-C22} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-C12}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-C22}^2 dt}{T}} = \frac{2I_o}{3} \sqrt{\frac{6}{1-D}} \tag{41}$$

$$I_{rms-Cout1} = I_{rms-Cout2} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Cout1}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Cout2}^2 dt}{T}} = I_o \sqrt{\frac{3D+1}{3\left(1-D\right)}} \tag{42}$$

$$I_{rms-C1} = I_{rms-C2} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-C1}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-C2}^2 dt}{T}} = \frac{I_o}{3} \sqrt{\frac{6}{1-D}}. \tag{43}$$

The loss of the TW-CI includes the loss of copper and magnetic.

$$P_{CI} = P_{cu,CI} + P_{core,CI} \tag{44}$$

$$P_{cu,CI} = \sum_{i=1,2} I_{rms-Lki}^2 r_{pi} + \sum_{i=1,2} I_{rms-Lsi}^2 r_{si} + \sum_{i=1,2} I_{rms-Lti}^2 r_{ti} \tag{45}$$

where $I_{rms\text{-}Lpi}$, $I_{rms\text{-}Lsi}$, and $I_{rms\text{-}Lti}$ are the current of TW-CI; and r_{pi}, r_{si}, and r_{ti} are the resistance of TW-CI.

$$I_{rms-Lk1} = I_{rms-Lk2} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Lk1}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Lk2}^2 dt}{T}}$$

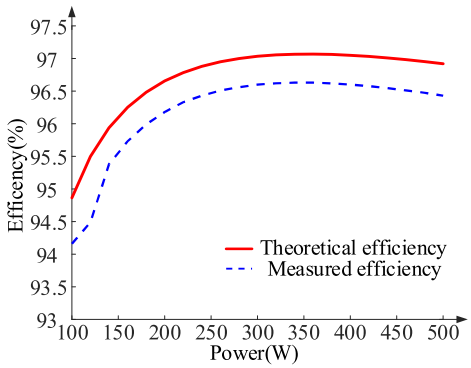

Fig. 6. Output efficiency of the proposed converter.

$$= \frac{I_o\sqrt{\frac{24n(2n-3D+7)-(21D+62)D+131}{3}}}{2\left(1-D\right)} \tag{46}$$

$$I_{rms-Ls1} = I_{rms-Ls2} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Ns1}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Ns2}^2 dt}{T}}$$

$$= \frac{2I_o}{3}\sqrt{\frac{6}{1-D}} \tag{47}$$

$$I_{rms-Lt1} = I_{rms-Lt2} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Nt1}^2 dt}{T}} = \sqrt{\frac{\int_0^{\mathrm{T}} i_{rms-Nt2}^2 dt}{T}}$$

$$= \frac{2I_o}{3}\sqrt{\frac{6}{1-D}} \tag{48}$$

$$P_{core,CI} = V_e K_c f_s^{\alpha} B_{\max}^{\beta} \tag{49}$$

where V_e represents the volume of the magnet. $B_{\max}$ is the maximum magnetic flux of the magnetic component. The K_c, α, and β are an empirical constant.

The overall loss of the proposed converter is calculated as follows.

$$P_{Loss} = P_s + P_D + P_c + P_{CI}. \tag{50}$$

The theoretical efficiency is calculated as follows.

$$\eta = \frac{\mathrm{P}}{P + P_{Loss}} \tag{51}$$

where P represents the output power.

The theoretical efficiency of the proposed converter can be deduced from equations (33)–(51). When the power is 360 W, the highest theoretical efficiency is 97.068%, and the measured efficiency is 96.62%. When the converter is operating at the rated power of 400 W, the theoretical efficiency is 97.05% and the measured efficiency is 96.60%. The effect of power on the theoretical efficiency is illustrated in Fig. 6. Moreover, the loss distribution at 400 W rated power is depicted in Fig. 7.

The loss of the proposed converter can be further mitigated by choosing the components with smaller parasitic parameters. In order to decrease the loss of the magnetic component, magnetic integration and expanding the cross-sectional area of wire can be used.

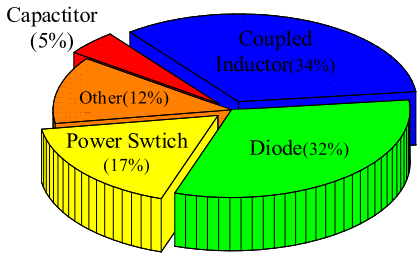

Fig. 7. Loss distribution map when power is 400 W.

V. Parameter Design of the Proposed Converter

This article has built an experimental prototype with 24–400 V, the switching frequency is 50 kHz, and the rated power is 400 W.

A. Design of TW-CI

According to (21), the turns-ratio of the TW-CI is related to the voltage gain and duty D. The turns-ratio of TW-CI is calculated as follows:

$$n \geq \frac{1-D}{4V_{in}}V_o - \frac{D}{4} - \frac{3}{4}. \tag{52}$$

The turns-ratio is taken as $n = 1$ when D is selected as 0.55.

Considering the maximum ripple current, the ripple current coefficient is selected as γ. The minimum value of magnetizing inductance can be calculated as follows:

$$L_{m1} = L_{m2} = L_m \geq \frac{V_{in}D}{\Delta i_{Lm\max} f_s} = \frac{V_{in}D}{\gamma I_{Lm} f_s}. \tag{53}$$

The current ripple coefficient is selected as $\gamma = 0.3$. According to (53), the value of TW-CIs should be larger than 52.93 μH. Therefore, the value of TW-CIs is chosen as 60 μH.

B. Design of Capacitance

The capacitance is limited by the maximum ripple of the output voltage and the power. Assuming the voltage ripple coefficient is $\alpha\%$, the capacitance can be calculated as follows:

$$C_{out1} = C_{out2} \geq \frac{I_o}{\Delta V_{cout1} f_s} = \frac{2P_o}{\alpha\% V_o^2 f_s}. \tag{54}$$

The voltage ripple coefficient is taken $\alpha = 0.3$. According to (54), the capacitance of C_{out1} and C_{out2} should be larger than 33.3 μF. Considering the commonly used value of capacitor, the capacitance of C_{out1} and C_{out2} is taken as 47 μF.

The values of C_{C11}, C_{C12}, C_{C21}, and C_{C22} are obtained as follows:

$$C_{C11} = C_{C21} \geq \frac{I_o}{\Delta V_{C11} f_s} = \frac{3+4n+D}{\alpha\% D V_o^2 f_s} P_o \tag{55}$$

$$C_{C12} \geq \frac{I_o}{\Delta V_{C12} f_s}$$

$$= \frac{3+4n+D}{\alpha\%\left(1+kn_{t2}+k\left(n_{s1}-n_{t2}\right)\left(1-D\right)\right)V_o^2 f_s} P_o \tag{56}$$

TABLE I
MAIN CIRCUIT OF THE CHANGER'S PARAMETERS

Parameter/Component	Specification
Input voltage V_{in}	24 V
Output voltage V_o	400 V
Rated power P_o	400 W
Magnetizing inductance L_{m1}	60.37 μH
Magnetizing inductance L_{m2}	60.13 μH
Leakage inductance L_{k1}	1.39 μH
Leakage inductance L_{k2}	1.55 μH
Turns ratio	$N_p/N_s/N_t$=1:1:1
Input capacitance C_1 and C_2	47 μF /63 V
Capacitance C_{11} and C_{21}	47 μF /100 V
Capacitance C_{12} and C_{22}	10 μF /250 V
Output capacitance C_{out1} and C_{out2}	47 μF /250 V
Diode D_{11} and D_{21}	MBR10100CT
Diode D_{12}, D_{13}, D_{22}, and D_{23}	MBR10200CT
Power switch S_1 and S_2	CRSS042N10N

$$C_{C22} \geq \frac{I_o}{\Delta V_{C22} f_s} = \frac{3+4n+D}{\alpha\%\left(1+kn_{t1}+k\left(n_{s2}-n_{t1}\right)\left(1-D\right)\right)V_o^2 f_s} P_o. \tag{57}$$

The turns-ratio is selected as $n_{s1} = n_{s2} = n_{t1} = n_{t2} = 1$, the coupling coefficient is selected as $k = 1$, and the voltage ripple coefficient is selected as $\alpha = 3$. According to (55)–(57), the capacitance of the C_{C11} and C_{C21} are obtained as 22.8 μF, and the C_{C12} and C_{C22} are calculated as 6.29 μF. Considering the commonly used value of capacitor, the capacitance of the C_{C11} and C_{C21} are taken as 47 μF and the C_{C12} and C_{C22} are selected as 10 μF. The input C_1 and C_2 are used to realize the voltage balance of the capacitors and power switches. The requirement of the capacitance is not strict, so the capacitance of the C_1 and C_2 is selected as 47 μF. According to the design of components, the major components of the proposed converter are shown in Table I.

VI. COMPARATIVE ANALYSIS AND EXPERIMENTAL RESULTS ANALYSIS

A. Comparative Analysis

The proposed converter is compared with other proposed high step-up converters based on CI. Table II summarizes the number of switches, diodes, capacitors, voltage gain, voltage stress, and magnetic components for each converter. A high step-up converter was obtained by integrating the SC with the coupling inductor in [4]. By utilizing the CI with VMC, the interleaved technique was presented in [8], [15], [16], and [21]. A symmetric dual-switched high step-up converter was proposed in [15]. The active switched-inductor high step-up converters with TW-CI was presented in [17] and [20], which has enhanced the overall performance. The single switch high step-up converters with

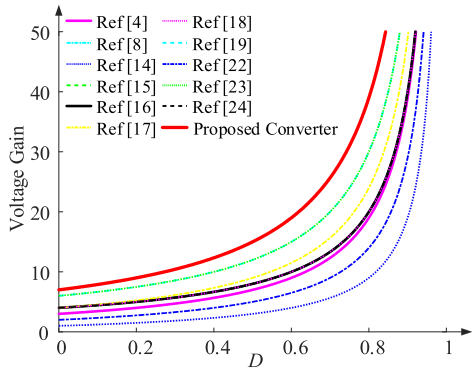

Fig. 8. Comparison of voltage gain when $n = 1$.

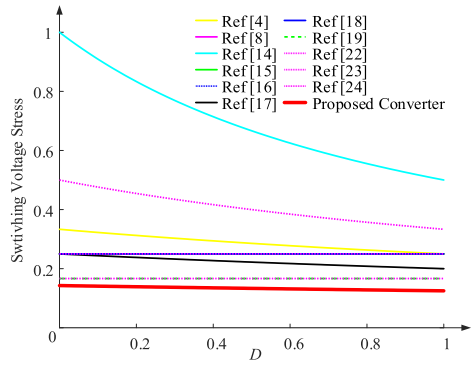

Fig. 9. Comparison of voltage stress when $n = 1$.

TW-CI are proposed in [18], [19], [20], and [21]. The TW-CI was combined with SCs in [24].

As shown in Fig. 8, the voltage gain of these converters is illustrated to better compare the difference between the TW-CI and the CI converters. In the same conditions of turn-ratios of $n = 1$, Fig. 9 has compared the voltage stress of the proposed and the converters in Table II. According to the above-mentioned discussions, the proposed converter with low voltage stress across semiconductors can achieve ultrahigh voltage conversion ratio.

B. Experimental Results Analysis

A 400 W prototype is built to verify the accuracy of the proposed converter. Fig. 10(a) shows the input and output voltage waveforms, which achieves a high voltage conversion ratio of 24–400 V. The current waveform of TW-CI is shown in Fig. 10(b) and (c). According to Fig. 10(d), the power switches turn-ON under ZCS with low voltage stress. As shown in Fig. 10(e) and (f), the voltage stress across the power switches is about 55 V, which is lower than the output voltage. The stress waveforms of diodes D_{11} and D_{21} are shown in Fig. 10(g) and (j). The voltage stress of the diodes is about 55 V, which is approximately 0.1375 times of the output voltage. The waveforms of diodes D_{12}, D_{22}, D_{13}, and D_{23}, are shown in Fig. 10(h), (k), (i), and (l), respectively. The waveforms of i_{Lk1} and i_{Lk2} are depicted in Fig. 10(m). As illustrated in Fig. 10(n), which depicts the voltage waveforms of output voltage when the load changes quickly, the output power immediately changed from 200 to 400 W when

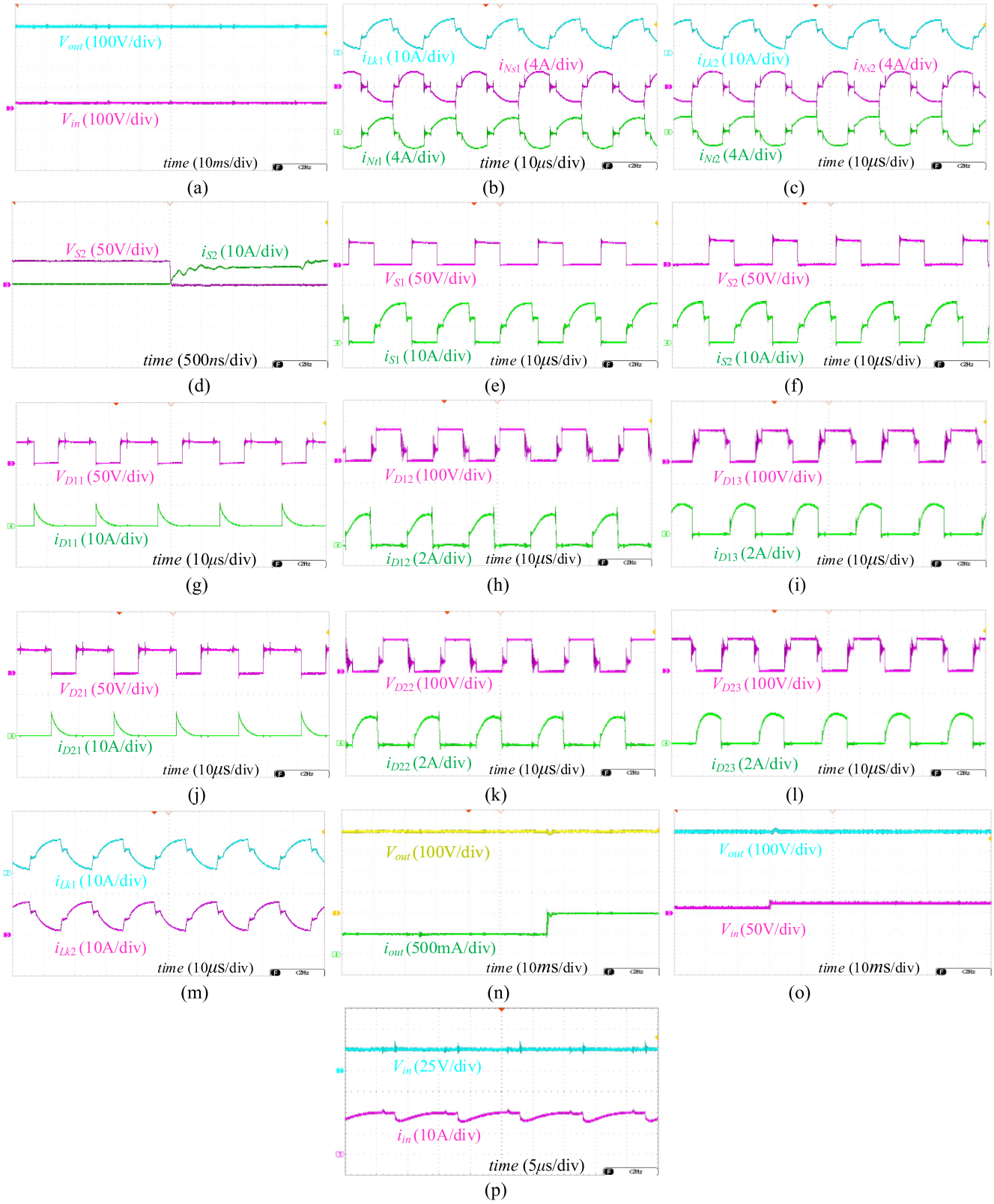

Fig. 10. Experimental waveforms. (a) Input and output voltage. (b) Current of the TW-CI 1. (c) Current of the TW-CI 2. (d) ZCS of switches. (e) Voltage and current stress of S_1. (f) Voltage and current stress of S_2. (g) Voltage and current stress of D_{11}. (h) Voltage and current stress of D_{12}. (i) Voltage and current stress of D_{13}. (j) Voltage and current stress of D_{21}. (k) Voltage and current stress of D_{22}. (l) Voltage and current stress of D_{23}, 4. (m) Waveforms of i_{Lk1} and i_{Lk2}. (n) Dynamic response of the change in the load (200 to 400 W). (o) Dynamic response of the change in the input voltage. (p) Input voltage and input current.

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER EXISTED CONVERTER

Converter	Voltage gain	No. of components				Voltage stress	Power	Input and output	Efficiency	Symmetrical	Input Current Type	Common ground
		S	D	C	CI							
[4]	$\frac{1+2n+nD}{1-D}$	1	6	6	1	$\frac{V_o}{1+2n+nD}$	200 W	24 V/400 V	93.8 %	No	High ripple	Yes
[8]	$\frac{2(n+1)}{1-D}$	2	4	4	2	$\frac{V_o}{2(n+1)}$	500 W	18~36 V/ 200 V	92.76 %	No	Low ripple	No
[14]	$\frac{1+D}{1-D}$	2	2	4	2	$\frac{V_o}{1+D}$	200 W	20~40 V/ 200 V	97.1 %	Yes	Low ripple	No
[15]	$\frac{2n+2}{1-D}$	2	6	6	2	$\frac{V_o}{2n+2}$	400 W	40~50 V/ 400 V	--	No	High ripple	No
[16]	$\frac{3n+1}{1-D}$	2	5	4	2	$\frac{V_o}{3n+1}$	400 W	40 V/400 V	97%	No	Low ripple	Yes
[17]	$\frac{3+n+D}{1-D}$	2	3	3	1	$\frac{V_o}{3+n+D}$	600 W	36~48 V/ 400~600 V	97%	No	High ripple	No
[18]	$\frac{2n+2}{1-D}$	1	4	4	2	$\frac{V_o}{2n+2}$	300 W	20~25 V/ 400 V	94.43 %	No	High ripple	No
[19]	$\frac{3+2n_2+n_3}{1-D}$	1	5	5	1	$\frac{V_o}{3+2n_2+n_3}$	216 W	28 V/418 V	94%	No	High ripple	Yes
[22]	$\frac{1+n+D}{1-D}$	2	4	3	1	$\frac{V_o}{1+n+D}$	500 W	30~50 V/ 400 V	94.5 %	No	High ripple	No
[23]	$\frac{4n+2}{1-D}$	2	8	7	3	$\frac{V_o}{4n+2}$	1000 W	45 V/675 V	96%	No	High ripple	Yes
[24]	$\frac{2n+2}{1-D}$	4	6	9	2	$\frac{V_o}{2n+2}$	1000 W	15~30 V/ 270 V	95.04 %	No	High ripple	Yes
Proposed	$\frac{3+4n+D}{1-D}$	2	6	8	2	$\frac{V_o}{3+4n+D}$	400 W	24 V/400 V	97.05 %	Yes	Low ripple	No

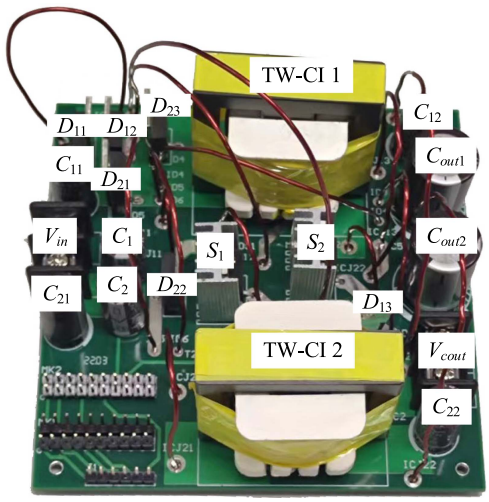

Fig. 11. Photograph of the experimental prototype.

the load changed. Fig. 10(o) represents the dynamic response of the proposed converter when the input voltage quickly changes from 24 to 48 V. The registered results demonstrate the stability and good dynamics of the converter, which can be experimented under other variable conditions. The voltage and current waveform of input is shown in Fig. 10(p). Finally, the accuracy of the proposed converter is verified through the experimental results of the laboratory prototype. The photograph of the prototype is shown in Fig. 11.

VII. CONCLUSION

By integrating two high step-up dc–dc converters with TW-CI, this article has proposed an interleaved high step-up dc/dc converter-based TWCI with symmetrical structure. The theoretical analysis and experimental results demonstrate that the main characteristics of the proposed converter can be regarded as follows:

1) The proposed converter has a symmetrical structure, the stress of the circuit semiconductors is small, and it is suitable for the high power transfer ability.
2) With the help of input and output capacitors, the voltage stress of power switches is reduced. As the voltage stress of semiconductors is smaller than output voltage, low-voltage-rating semiconductors are used. The voltage balance of the power switches and the capacitors can be realized under steady and dynamic states.
3) Because the power switches achieve ZCS and the diode D_{11}, D_{21} turn OFF naturally, the measured efficiency was measured as 96.6%.

4) The range of adjustment for voltage gain of the proposed converter is wide. As seen, the voltage gain of the proposed converter is about 16.67 when the winding turns-ratio $k = 1$ and $D = 0.55$.

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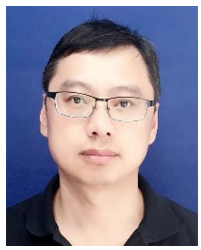

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