An Adaptive Constant-on-Time-Controlled Hybrid Multilevel DC–DC Converter Operating From Li-Ion Battery Voltages With Low Spurious Output

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***Abstract*—This article describes a multilevel hybrid plug-and-play dc–dc converter capable of converting a Li-ion battery input voltage range of 2.7–4.5 V to a system-on-chip voltage range of 0.6–1.3 V with an output spur as low as −53.5 dBm, a switching frequency variation of 0.13%, and peak efficiency of 88.6% at a corresponding power density of 0.061 W/mm^2. The converter, designed in 65-nm CMOS, uses a small 470-nH inductor and is stable with a multilayer ceramic output capacitor with only a 2-m Ω series resistance. A fully on-chip adaptive constant-on-time controller is employed, enabling a minimum efficiency of 70% for load currents as low as 30 mA with a response time of 3 μ s from a rapid 1-A load current step, without any need for external power supplies or control circuits.**

***Index Terms*—Buck converter, constant-on-time (COT) controller, dc–dc converter, hybrid converter, Li-ion battery, low ripple, low spur, multilevel, power management, switched capacitor.**

I. Introduction

MOBILE and IoT devices often centralize many features into system-on-chips (SoCs) that are implemented in nm-sized CMOS processes, which tend to operate at $\leq$1.2 V. Since Li-ion batteries are typically employed in such devices for energy density reasons, a dc–dc converter is required to translate the 2.8–4.2 V Li-ion battery voltage down to the desired SoC supply voltage. Since mobile and IoT devices are typically small, the dc–dc converter must be physically small and efficient across a wide variety of light-to-heavy load conditions to maximize the battery life while supporting worst-case load demands (i.e., it must operate at high power density)—all at Li-ion battery voltages in a nm-sized process that may not have 5-V transistors. Since transitions from light to heavy loads and vice versa can occur quickly, the dc–dc converter needs to have fast enough control—and yet must also maintain stability with low output ripple and output noise. In particular, sensitive blocks, such as phased-locked loops (PLLs), low noise amplifiers (LNAs), and analog to digital converters (ADCs), require low spurious content on their supply voltages to operate correctly, which can be problematic to address in a switching dc–dc converter [1], [2]. In addition, electro magnetic interference (EMI) issues can easily arise in switching converters without careful design.

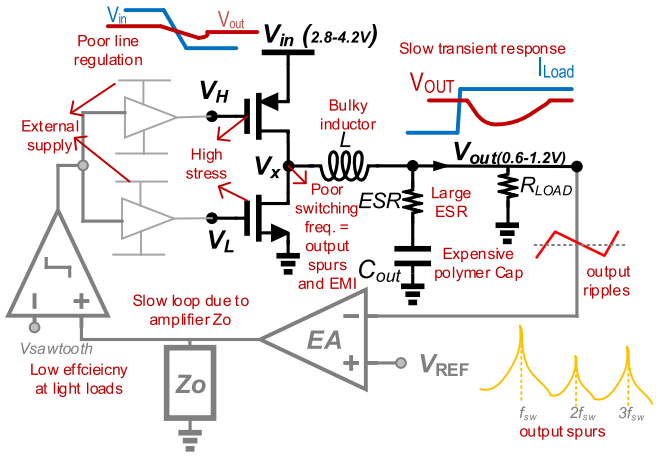

Fig. 1. Summary of challenges facing a conventional buck converter utilizing a traditional PWM controller when powering SoCs in a scaled CMOS process for size-constrained devices.

There has been significant prior work [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16] exploring solutions to these challenges, although, in most cases, not all problems have been addressed simultaneously. This is the main motivation behind this work.

For example, Kim et al. [3] utilized a fast dynamic comparator in a traditional buck converter to achieve high light-load efficiency of more than 80% for less than 1 mA of load current, all with 3 mV ripple voltage in a pulse-frequency modulation (PFM) scheme for IoT applications. Nevertheless, the maximum

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load current is limited to only 100 mA, restricting its application in SoCs.

The same issue exists in [4], where three modes (pulsewidth modulation (PWM), PFM, and multiple-sawtooth PWM) can be detected by a load current prediction scheme, resulting in 70%–91% light-load efficiency, yet with a maximum load current of only 200 mA.

Stacking transistors can enable direct processing of high voltages in basic nm-sized bulk CMOS processes [5]. However, when used in a traditional buck converter, such structures have difficulty achieving a good tradeoff between efficiency and power density.

Hybrid multilevel converters exploit the transistor stack by inserting flying capacitors between stacked nodes, which shrinks the size of the inductor compared with a traditional buck converter, resulting in a power density of 0.11 W/mm^2 and a near 90% heavy-load efficiency in [6], for example. Nevertheless, the start-up process to balance the flying capacitor was performed manually by gradually increasing the input voltage, which is not pragmatic. Moreover, much prior art in hybrid converter design has not carefully considered control mechanisms for rapid enough response times and, more importantly, for acceptable light-load efficiency, which results in designs not suitable for the emergent needs of mobile and IoT devices. Designs that have considered control in a hybrid converter, for example, in [7] where a multilevel structure achieving better than 90% peak efficiency and capacitor balancing with an acceptable transient response is proposed, have room for improvement in power density and do not necessarily address all of the aforementioned challenges, such as EMI.

To address control issues, constant-on-time (COT) schemes have been implemented, for example in [8], toward the achievement of more than 95% peak power efficiency and a fast transient response of less than 3 μs, while supporting a wide current range of 0–2 A with more than 80% efficiency at light loads. However, using a separate auxiliary external supply of $AV_{DD} = 1.2$ V prevented a fully integrated, plug-and-play solution. The same issue is present for the design in [9] that uses external supplies of V_{DIG} and $V_{\text{AUX}} = 0.5V_{\text{IN}}$.

Variations in the switching frequency of COT controllers—which is due to the dependency of the switching frequency to the input/output voltages and load—cause EMI, noise, and heavy-load efficiency degradation. To address this, Tsai et al. [2], for example, decreased the variations by more than 4$\times$ and achieved frequency variations of less than 3% with an adaptive voltage positioning technique implemented in an adaptive-constant-on-time (ACOT) controller. This design, however, did not focus on addressing other issues, such as high power density, heavy-load efficiency, or dynamic range, and is, thus, not appropriate for use in SoC applications.

Other prior art also proposed ACOT control mechanism with improved switching frequency variations. In [10], for instance, a predicting correction technique was employed in an ACOT controller to suppress the variations of the switching frequency to be only 0.32%. To further improve this, Chen et al. [11] utilized a phase detector and a voltage-to-current converter block to regulate the frequency of the COT buck converter and achieved the switching frequency error of less than 0.16%. However, the power transistors were not integrated on the same die as the controller, preventing a compact fully integrated power management unit with a high power density, which is necessary for the small form factor of mobile and IoT devices.

Adaptive on-time control mechanism showed promising results for ultra-low load currents in [12] in a trimode configuration to facilitate more than 70% efficiency for 10-μA load ranges with better than 0.06% line regulation for IoT applications. However, other parameters of a typical SoC are fast settling time [more than 17.5 μS for an 80 mA load current change possibly because of using an error amplifier (EA)] and high-load efficiency (maximum load current is only 100 mA).

The benefits of ACOT control mechanism are not limited to mobile and IoT devices, as it was used in [13] for automotive USB chargers, where the switching frequency of the converter is synchronized to a fixed reference frequency to minimize the variations. Nonetheless, other concerns, such as light-load efficiency, were not fully addressed in that design, as the final results achieved by only postlayout simulations show an efficiency of less than 60% for a conversion ratio of 2.4 and a load current of 200 mA. As another example, Xue et al. [14] presented a wide input range three-level buck converter topology controlled by a constant-frequency adaptive-on-time V^2 scheme for automotive and industrial applications, achieving a frequency deviation of less than 0.55% with a considerable power density. However, utilizing an amplifier-based error correction block resulted in a 20 μs settling time from only a 400-mA load current change—which likely requires improvement to match the high-speed demands of today's SoCs.

At the same time, some prior art worked on other aspects, such as minimizing the output dc offset, for example, to 8 mV for a 0.9-A load current, in [15]. However, a bulky 10-μH inductor was used. The same sizing issue is present in [16], where a hybrid synchronous/asynchronous control loop was introduced to achieve a rather high response speed for ultra-low power applications. This resulted in more than 90% peak efficiency with a wide dynamic range at 0.9 V output. To accomplish that, however, a 22-μH inductor and about 15 μF of overall decoupling capacitors were used that limited the power density to be less than 0.1 mW/mm^2.

Fig. 1 summarizes all of the abovementioned challenges for a conventional buck converter using a conventional PWM controller. The goal of this work is to consider all of these challenges simultaneously toward the design of a plug-and-play dc–dc converter that:

1) provides a very low spurious output, eliminating the need for an low drop out regulator (LDO) that would, otherwise, add cascaded losses to the system;
2) reduces the switching frequency variations to minimize noise/jitter and EMI issues;
3) performs without any need for external supply rails or circuits, requiring a rather complex switching operation;
4) achieves high power density compared with the prior art, which is required for compact IoT devices.

To achieve these, a hybrid flying capacitor multilevel (FCML) dc–dc converter with three levels, also known as a three-level converter, utilizing a fully on-chip ACOT controller, is

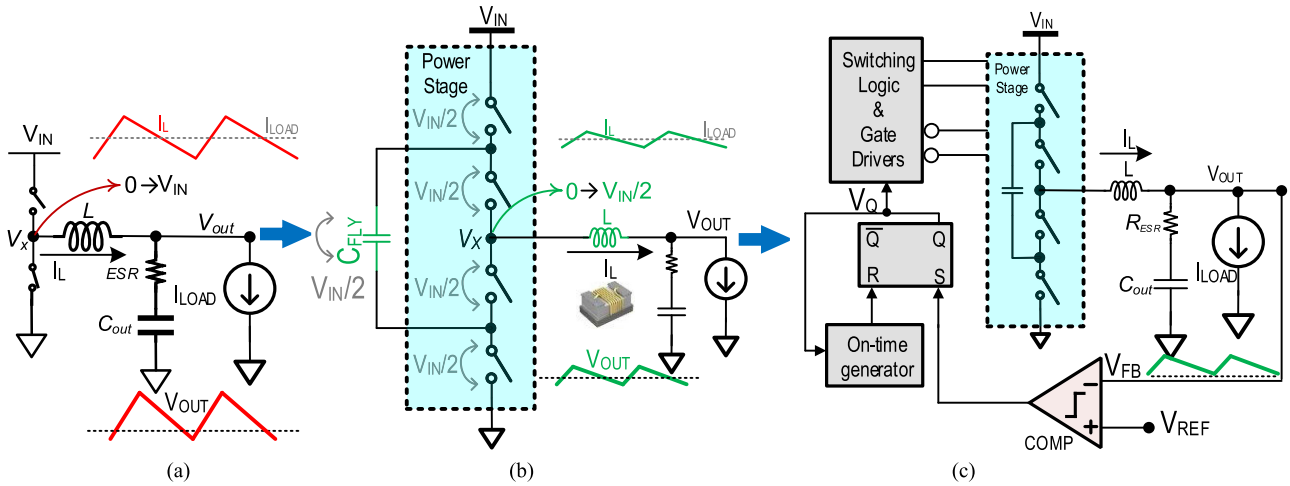

Fig. 2. Evolution of the hybrid FCML converter with a COT controller from a conventional buck converter. (a) Conventional buck converter. (b) Hybrid FCML structure with smaller L and less stress. (c) Hybrid FCML converter with COT control.

presented. The addressed challenges, along with the solutions used in this work, are briefly outlined in the following.

1) *Challenge*: Many scaled CMOS processes do not have 5-V transistors and, thus, cannot directly process Li-ion voltages using a conventional two-switch buck converter. *Solution*: Stacking low-voltage transistors enables integration into scaled CMOS processes while processing high voltages.
2) *Challenge*: Conventional buck converters require a large, bulky inductor to achieve high efficiency and power delivery specifications. *Solution*: A hybrid flying capacitor structure that effectively decreases the average voltage of the inductor switching node (V_X in Fig. 1), resulting in a smaller inductor with higher efficiency and/or power density.
3) *Challenge*: Efficiency at light loads is typically poor with PWM-controlled converters, as switching losses do not scale with load conditions; in addition, such approaches have slow transient recovery times due to a bandwidth-limited EA to amplify the output ripple in the control loop. *Solution*: An on-chip ACOT controller as a part of the PFM control technique is used instead of the traditional PWM technique, resulting in more than 70% efficiency for load currents from mA to A range in a fast loop without adding any high-impedance nodes.
4) *Challenge*: In a typical ACOT controller, large inductors contribute to larger jitter [17]. *Solution*: The hybrid FCML structure needs a smaller inductor for the same efficiency, which in turn results in lower jitter.
5) *Challenge*: COT (or ACOT) control schemes explicitly require output voltage ripple and an expensive polymer output capacitor with a large effective series resistance (ESR) for robustness (i.e., immunity to the output noise) and to prevent subharmonic issues in the controller loop. *Solution*: A saw-tooth wave generator block equivalently emulates the output ripple signal in the loop, but importantly not at the output node, enabling the proposed design to work properly with a small 0402 output capacitor.
6) *Challenge*: PWM schemes have a strongly defined switching frequency, whereas COT schemes have a poorly defined switching frequency in the continuous conduction mode (CCM), either of which can result in spur and EMI issues. *Solution*: An all-digital frequency-locked-loop (ADFLL) block in an ACOT structure that dynamically adjusts the switching frequency while maintaining its average value constant.
7) *Challenge*: Line regulation in CCM, used at high-power density conditions, is poor in a typical COT scheme because the output ripple amplitude is proportional to the input/output voltages. *Solution*: A dc regulation enhancement block that improves line regulation by increasing the loop dc gain.
8) *Challenge*: Many hybrid converters require external power supply rails for level shifters and start-up or external circuits for control signals. *Solution*: A bootstrap technique to provide all the required level-shifter voltages from internal nodes of the multilevel structure along with a fully on-chip closed-loop controller employing a soft start-up (SS) mechanism without using any external supplies or circuits.

More details on all these solutions are provided in the following sections. Section II explains how, by starting from a conventional buck converter and adding the solutions abovementioned, a compact plug-and-play hybrid three-level converter with a fully integrated ACOT controller was built in this work. The circuit detail of the switching operation of the power stage is explained in Section III, whereas measurement results provided in Section IV show the highest power density, the lowest switching frequency variations, and the lowest output spurs among the state-of-the-art plug-and-play solutions.

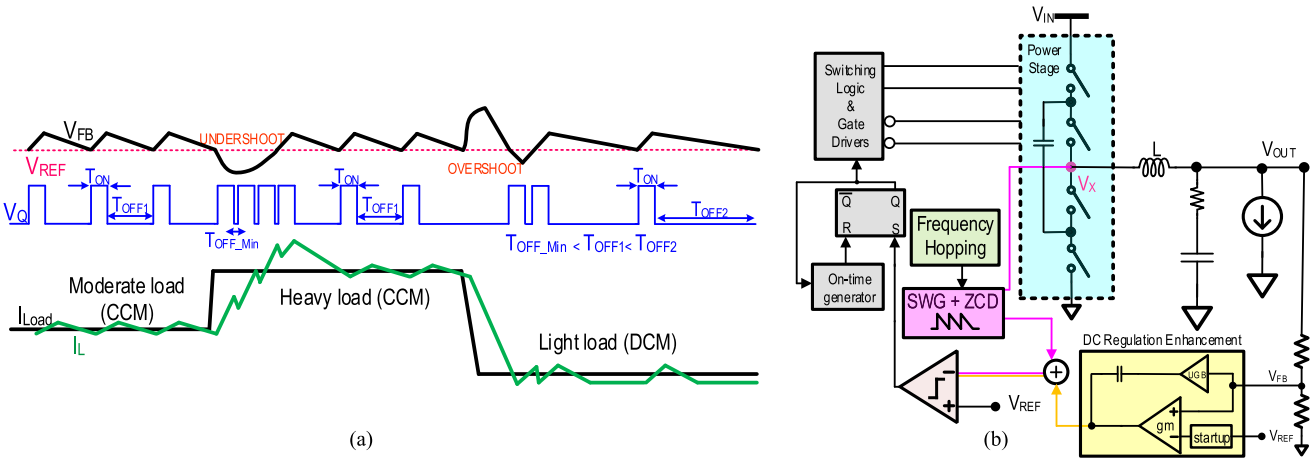

Fig. 3. (a) Transient behavior of COT controller. (b) Hybrid three-level converter with COT controller employing the proposed DC regulation enhancement, saw-tooth wave generator, and frequency hopping blocks.

II. From the Conventional Buck to the Proposed ACOT-Controlled Hybrid FCML Converter

A. From a Buck Converter to an FCML Structure

The basic buck structure, shown in Fig. 2(a), does not natively work in a low-voltage CMOS process if it has to process high voltages, as the internal node of the converter V_X swings between 0 and V_{IN}, which can exceed the safe operating voltages of the constituent power switches. Switching to a stacked structure, as shown in Fig. 2(b), enables voltage division across the transistors, and thus can potentially enable safe operation. Interestingly, if the stack is required for voltage rating purposes, it often makes sense to add in a flying capacitor, C_{FLY}, and build an FCML converter. Doing so only requires the addition of one (typically small) flying capacitor, and yet, it reduces node V_X's switching amplitude to be between 0 and $V_{\text{IN}}/2$, which increases the efficiency of the converter, as the equivalent conversion ratio is now lower than before [18], [19], [20]. Moreover, one can keep the inductor value the same as before, but reduce the switching frequency to achieve higher efficiency or, keep the switching frequency the same as before and choose a smaller inductor, which increases the power density—crucial for handheld mobile devices. A smaller inductor also has the advantage of increasing the output ripple slope, which in turn lowers the output jitter and noise components [17] when it is used in an ACOT controller (to be described next). Using an FCML structure only, however, cannot solve other issues, such as light-load efficiency and dynamic range. Hence, the role of the control mechanism should also be explored carefully to achieve an SoC-compliant converter.

B. From a PWM Controller to a COT Controller

DC–DC converters used in mobile and IoT applications require high power density and efficiency across a wide dynamic range of load conditions. In addition, the output voltage should be well regulated, even during large and/or rapid load transient events.

The two main types of control schemes are based on PWM and PFM, respectively). Since PWM controllers use a variable pulsewidth at a constant switching frequency, switching losses stay constant over load conditions, resulting in poor light-load efficiency [21]. In contrast, PFM controllers naturally scale switching losses with load conditions, resulting in superior light-load efficiency [3]. PWM controllers also tend to be slower than PFM controllers, since they require an EA with limited bandwidth and compensation networks (e.g., EA and Z_O blocks in Fig. 1). Nevertheless, in PFM controllers, the output voltage (or a divided portion of it) is compared directly with a reference voltage in a fast comparator without adding any additional low-frequency poles (i.e., high-impedance nodes) [2]. For these reasons, PFM-based controllers are generally preferred for such applications.

One possible way to implement PFM control is to use a COT pulse created by an on-time generator block, as shown in Fig. 2(c) [22]. The output of the on-time generator is a pulse with a constant width, when its input from V_Q of the SR latch is high. To fully understand the operation of this COT controller, the transient waveforms of a representative converter under different load currents are shown in Fig. 3(a).

When the load current (I_{Load}) is moderate, and the operation is in CCM, V_{FB} always stays above V_{REF} in the steady-state because if V_{FB} goes below V_{REF}, the output of the comparator and the SR latch (V_Q) would go high, making the on-time generator circuit trigger a constant-width pulse, which would charge up the output and increase V_{FB} to be more than V_{REF}.

If there is a rapid current increase in I_{Load} (the heavy load mode), and the converter still works in CCM, the initial load current would be provided by the output capacitor since the inductor current (I_L) cannot change instantly. As the output capacitor discharges, there is an undershoot in V_{OUT} and V_{FB}. In this situation, V_{FB} goes below V_{REF}, requesting the on-time generator to provide constant-width pulses continuously until V_{FB} becomes greater than V_{REF}. On the other hand, since the pulse width is constant, there is a discontinuity equal to the minimum off-time of the on-time generator block ($T_{\text{OFF\_Min}}$).

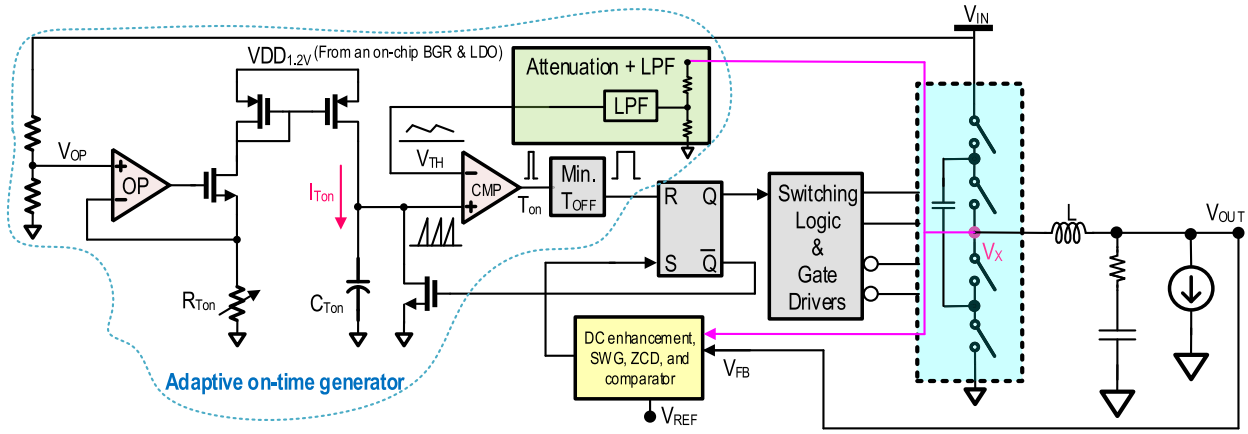

Fig. 4. Circuit details of the SWG block with frequency hopping.

The output capacitor continues to get charged by constant-width pulses with the minimum off-time, until V_{FB} reaches a voltage greater than V_{REF}. At this point, the steady state is achieved, and the off-time is equal to the one before the rapid current change (T_{OFF1}).

When the load demand suddenly drops, the converter will naturally enter discontinuous conduction mode (DCM) operation. Since, in this case, the load requests a current less than the actual inductor current, the extra inductor current goes to the output capacitor rather than the load, charging up the output capacitor, which makes V_{OUT} and V_{FB} overshoot. In this situation, V_{FB} stays above V_{REF} longer than usual, which makes the output of the comparator and V_Q stay low for a long time, allowing I_L to decrease until V_{FB} becomes less than V_{REF}. In this case, the constant-width pulse increases V_{OUT} and V_{FB} once again. Meanwhile, by forcing T_{OFF2} to be more than before (T_{OFF1}), I_L stays low and proportional to the load current demand.

Note that COT operation does not necessarily mean constant-frequency operation. As illustrated in Fig. 3(a), the COT controller works at a constant frequency during steady-state operation, but will automatically change its frequency during load transitions, and during DCM operation.

Despite having great advantages in light-load conditions and also in load transitions, there are three main issues associated with a baseline COT controller.

The first basic controversy is that the operation of the controller depends on the amplitude of the output voltage ripple (the COT controller is sometimes called a ripple-based controller)—the larger the ripple, the more immunity to noise, and more accurate comparisons can be made by the comparator. However, a larger output ripple generates spurious components that are not favorable in many applications. Since the output capacitor and its ESR are the main sources of the ripple [22], one way to decrease the ripple is to use a capacitor with a low ESR. On the other hand, a low ESR means that the output capacitor is the main source of output ripples, and due to the phase difference between the output capacitor voltage and the inductor current, a subharmonic instability issue occurs, requiring the switching frequency to be more than the zero frequency generated by the output capacitor and its ESR [1], [23].

The second major concern is that the inductor current ripple and, consequently, the output voltage ripple amplitude depend on V_{IN}, resulting in a poor line regulation [24].

The third main problem for a typical COT controller is the dependency of the switching frequency of the controller to the input and output voltages in CCM [1]

$$f_{SW} = \frac{V_{OUT}}{T_{ON} V_{IN}} \tag{1}$$

any variation in the load (V_{OUT}) and the line (V_{IN}) can change the switching frequency, since the T_{ON} is constant in a COT controller. As a consequence, EMI, spur, and jitter issues can happen with load and line variations.

The solutions utilized in this work to tackle these problems are provided in the following section.

C. Proposed ACOT Controller

In this work, the ESR tradeoff is addressed by utilizing a capacitor with a low ESR, but then compensating this by intentionally enhancing the ripple amplitude (for reliable comparator operation) in another part of the control loop instead of at the output. The general concept is depicted in Fig. 3(b). Here, the initial switching frequency of the converter is set by a saw-tooth generator (SWG). Therefore, the inductor current and V_{OUT} also have the same frequency. This builds an appropriate ripple signal at the negative input port of the comparator, all without a large ESR output capacitor. The comparator input is now independent of the output ripple amplitude and can work robustly without any subharmonic issues. As a result, the proposed solution can function with a small and low-cost multilayer ceramic capacitor (MLCC).

The SWG block also manages the switching behavior of the converter at steady state, which in turn controls the noise and the ripple of the output voltage. The switching nature of the buck converter makes the existence of output spurs at the switching frequency and its harmonics unavoidable. However, as

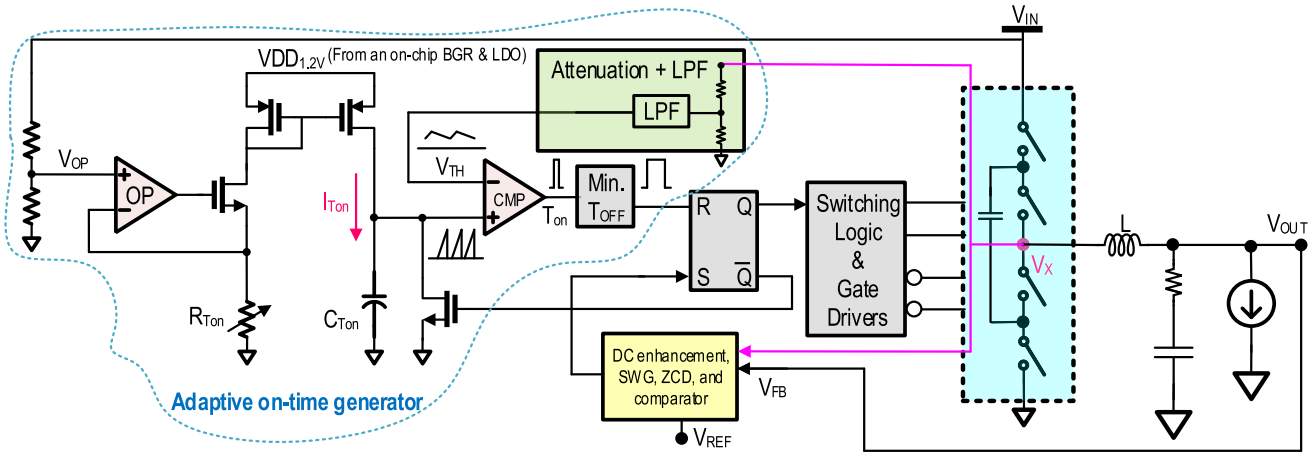

Fig. 5. Simplified block diagram of the proposed hybrid three-level DC–DC converter with ACOT controller.

mentioned before, some blocks inside an SoC, such as oscillators and PLLs, are very sensitive to any ripple or spur on the supply rail, since any periodic fluctuation on the supply line can turn into spurs at an offset frequency equal to the dc–dc converter switching frequency from the frequency of the oscillation. The amplitude of such spurs should be minimized (typically less than -50 dBc at MHz offset ranges), since in some cellular radio applications with strict spur requirements, such as [25], a large MHz offset range spur is not acceptable because it can downconvert the blockers from adjacent channels on the wanted signal channel, corrupting the desired information.

Two well-known techniques to mitigate the spurious output of buck converters operate by converting the spur power, which exists at a single frequency, into power that is spread over a wider bandwidth, such that it appears like noise—ideally below the noise floor itself. This is typically accomplished via either sigma–delta modulation (SDM) or frequency hopping [26]. Since SDM often results in additional quantization noise that can potentially increase the noise floor [27], the frequency hopping method, shown in Fig. 3(b), is employed in this work. In the proposed design, eight different frequencies (2–3 MHz) are used that can spread out the spurs by 18 dB theoretically [28]. The circuit schematic of the SWG block with the frequency hopping mechanism is shown in Fig. 4. A pseudorandom bit generator controls a capacitor bank (HP $< 0:6 >$) with 70 fF unit capacitors. When the frequency hopping is enabled (HPEN is 1), these capacitors are in parallel to default capacitors (C_0) present for generating the basic saw-tooth wave. The overall capacitor bank is then charged with a current source and compared with a reference voltage coming from an on-chip band-gap reference (BGR) block in a comparator. Once the comparator reaches the defined value, the SWG RESET pin turns ON M_0 to discharge the capacitors in C_0 after going through a delay line for fine adjustments of the final frequency of the OFF-time portion of the output signal that appears at the SWG Vout pin. This results in a 16.7 dB reduction in spur amplitude in measurement results (see Section IV). Regardless of the frequency hopping mechanism, and as mentioned before, the SWG block can generate a ripple

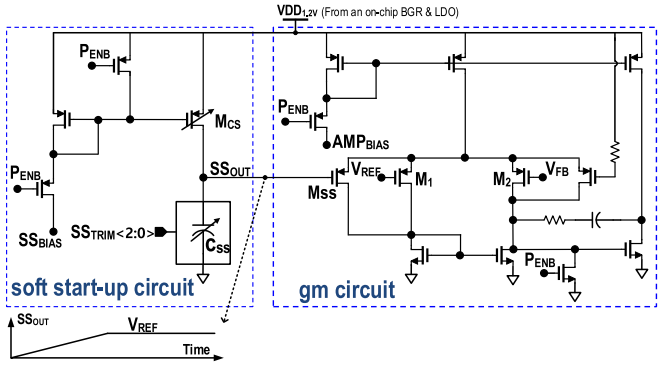

Fig. 6. SS circuit schematic used with the g_m cell of the DC regulation enhancement block.

at the same frequency as the output by changing the default capacitor value using CTRL $< 0:2 >$.

In order to improve line regulation, a dc regulation enhancement block is used in this work, as depicted in Fig. 3(b). This block includes a g_m cell that provides more than 60 dB of gain at dc. As a result, when the input dc voltage varies from 2.7 to 4.5 V, the output ripple amplitude variations are minimized by the very high dc gain of the control loop. The g_m cell is in parallel to a unity-gain buffer that passes the output voltage ripple signal (the ac component that works at the converter switching frequency) without any changes not to degrade the speed of the control loop. The dc regulation enhancement block can be bypassed when the maximum speed of the control loop is required—which usually happens during load transitions.

The solution employed in this work to break the dependency of the converter switching frequency to $V_{\rm OUT}$ and $V_{\rm IN}$ in CCM is to employ an adaptive-COT controller, as shown in Fig. 5. Here, the on-time generator is built from ($V_{\rm OUT}$) and ($V_{\rm IN}$) in a feedback network in such a way that ($f_{\rm SW}$) can stay constant on average by changing $T_{\rm ON}$ slightly based on load and line variations in CCM [1]. In the adaptive on-time generator circuit

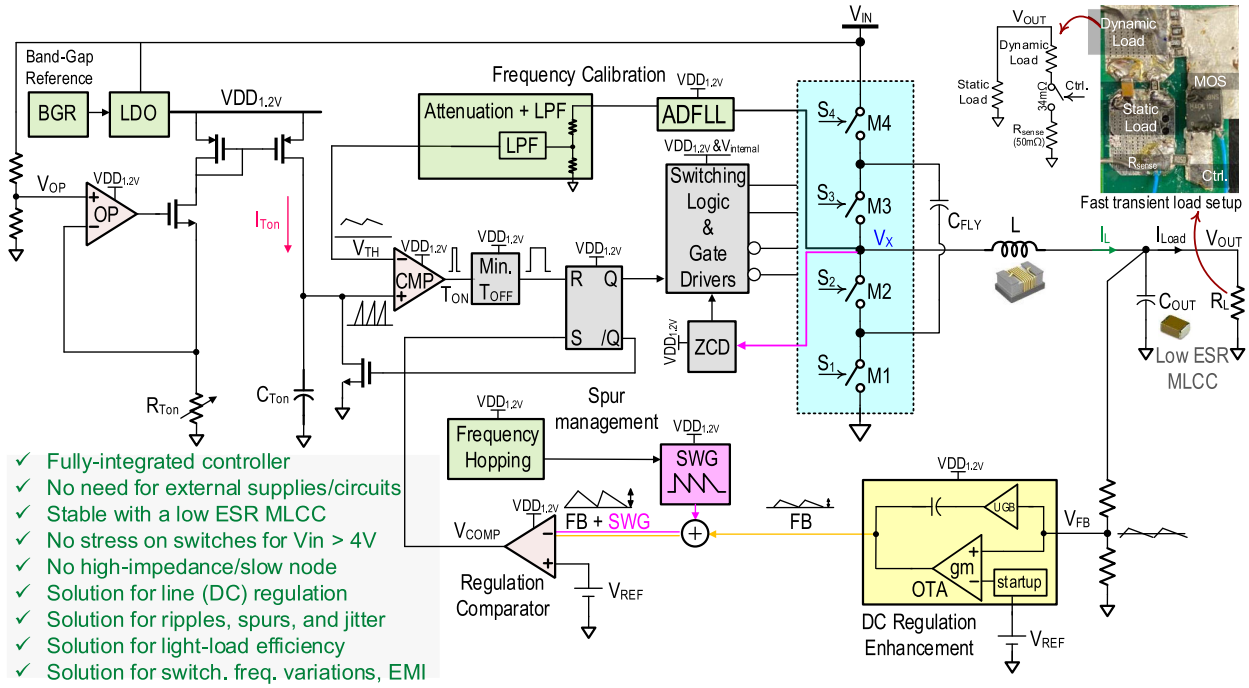

Fig. 7. Complete block diagram of the proposed hybrid three-level DC–DC converter with the ACOT controller, offering solutions for all the issues mentioned in Section I.

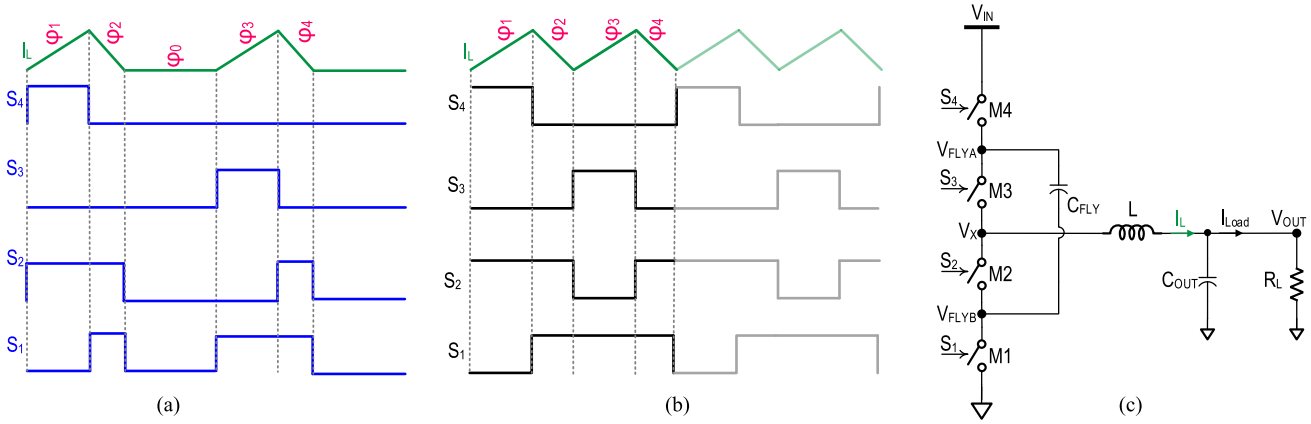

Fig. 8. Switching operation of the power stage of the proposed hybrid three-level converter. (a) Controller signals with a light load (DCM). (b) Controller signals with a heavy load (CCM). (c) Power stage schematic.

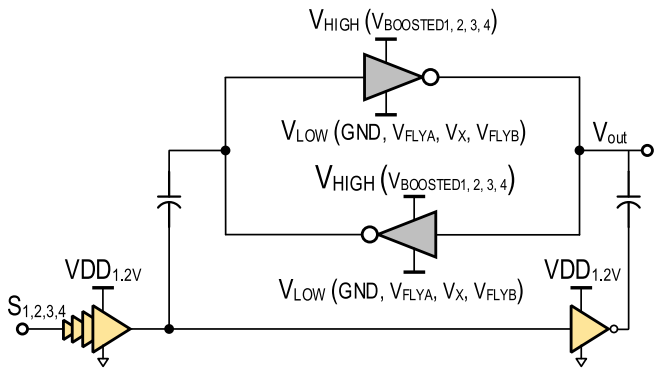

Fig. 9. Level shifter circuit.

of Fig. 5

$$I_{T\text{on}} = C_{T\text{on}} \times \frac{\Delta V}{\Delta t}, V_{TH} = k_1 \times V_{\text{OUT}}, V_{OP} = k_2 \times V_{\text{IN}} \tag{2}$$

where k_1 and k_2 are constants. When $C_{T\text{on}}$ charges to V_{TH} during T_{on}

$$I_{T\text{on}} = C_{T\text{on}} \times \frac{V_{TH}}{T_{\text{on}}}. \tag{3}$$

Because of the current mirror

$$I_{T\text{on}} = \frac{V_{\text{OP}}}{R_{T\text{on}}} \times k_3 \tag{4}$$

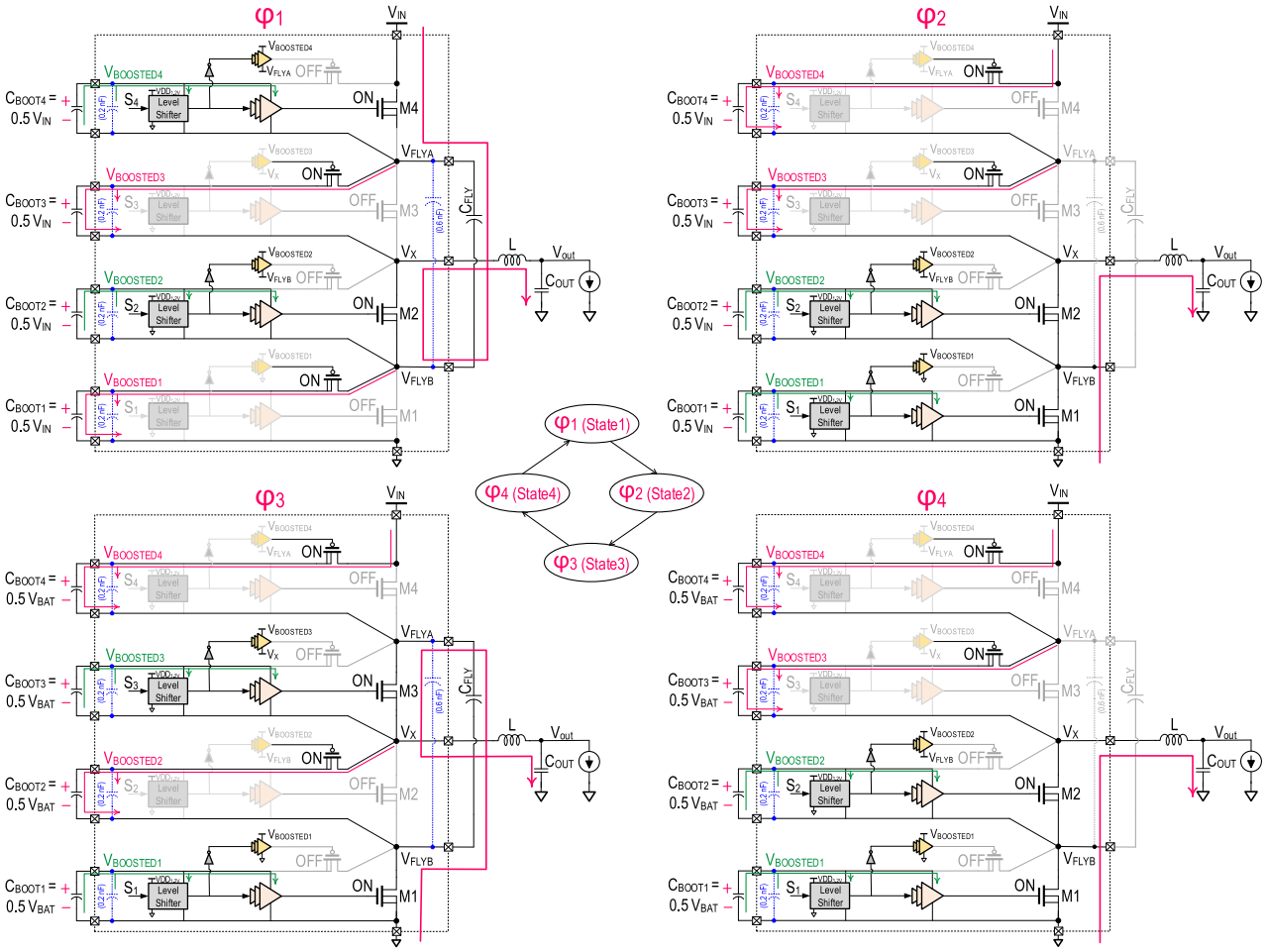

Fig. 10. Circuit details of the power stage switching operation during each phase.

where k_3 is a constant. From (2) and (4)

$$I_{T\text{on}} = \frac{k_2 V_{IN}}{R_{T\text{on}}} \times k_3 \tag{5}$$

and by having T_{on} from (3)

$$T_{\text{on}} = \frac{R_{T\text{on}} C_{T\text{on}} k_1 V_{\text{OUT}}}{k_3 k_2 V_{\text{IN}}}. \tag{6}$$

By defining k as a constant and D as the conversion ratio

$$k = R_{T\text{on}} C_{T\text{on}} \frac{k_1}{k_3 k_2}, \quad D = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \tag{7}$$

T_{on} is equal to

$$T_{\text{on}} = k \times D \tag{8}$$

which [by using (1)] results in

$$f_{\text{SW}} = \frac{1}{k}. \tag{9}$$

Hence, based on (8), T_{on} can change due to variations in V_{OUT} or V_{IN}, whereas according to (9), f_{sw} (and f_X) stay constant on average, regardless of load and line variations. In a practical design, however, k_1 in (2) can change based on the load, line, and PVT variations, resulting in a not completely robust and constant frequency for V_{TH}, V_X, and V_{OUT}. In more detail, the analysis provided here is valid only at dc when no noise at different frequencies (or jitter in general) is present. In reality, when jitter is present, the instantaneous frequency of V_{OUT}, V_X, and V_{TH} vary at all times, making the assumptions in (2) not realistic.

The proposed solution for this second-order effect is to use an ADFLL based on [29] that uses a relaxation oscillator as the reference clock and the signal generated by the dc–dc loop—that appears at the switching node V_X—instead of the DCO. The ADFLL receives V_X, compares it with the reference, and generates a signal with the desired frequency using an 18-bit counter, which is in line (via the digital code) with the frequency at which the SWG block is currently working. This signal goes through the adaptive on-time generator loop that includes the comparator (CMP), min T_{OFF}, and SR latch blocks, trying to achieve a robust on-time at V_X, typically in less than 22 μs. Since the hopping rate is slower than the ADFLL settling time, the ADFLL adjusts the on-time before the next hopping happens. This makes variations in the switching frequency less than 1%.

Finally, in order to gradually start up the circuit by charging the flying capacitor (C_{FLY}), one possible solution is to apply the input voltage of the converter in a ramp shape instead of the regular step shape. This would make the circuit start-up

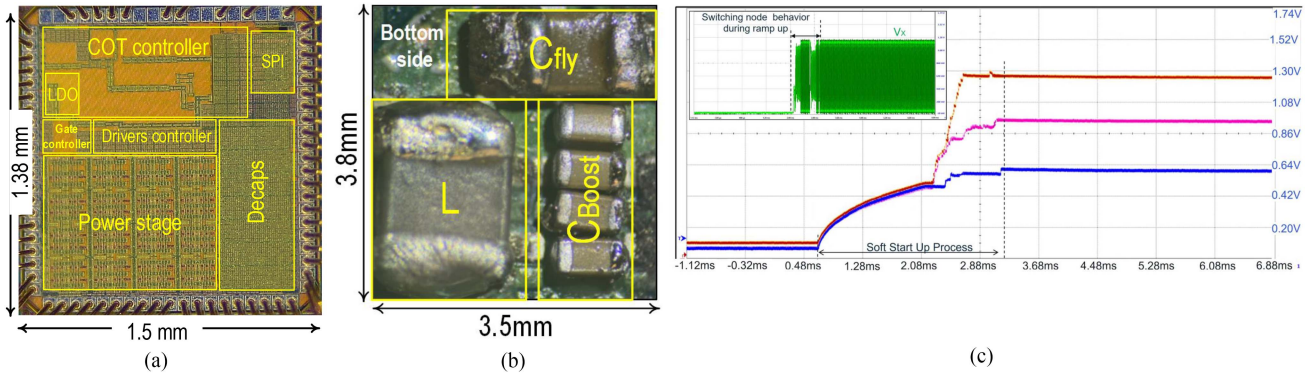

Fig. 11. (a) Die photograph. (b) PCB photograph. (c) Output voltage measurement result during SS.

dependent on the variable input voltage and, more importantly, not in the user's control.

Instead, the proposed solution is to gradually ramp up the reference voltage rather than the input voltage using a SS circuit, whose schematic is shown in Fig. 6. Here, a tunable capacitor ($C_{\rm ss}$) is charged with a tunable current mirror (M_{cs}), providing a ramp voltage smaller than $V_{\rm REF}$ at the output of the start-up circuit ($\rm SS_{OUT}$). During the start-up process, this ramp voltage is compared with $V_{\rm FB}$ in the feedback loop. The ramp voltage goes up until the transistor $M_{\rm ss}$ turns OFF, at which the steady state is achieved, and the output of the start-up circuit is equal to $V_{\rm REF}$, which is now being compared with $V_{\rm FB}$ in the feedback loop. Simulation results show that this SS process can also reduce the inductor peak current (inrush current). The pin $P_{\rm ENB}$ is used to bypass the entire dc enhancement block for load transitions, as mentioned before.

The complete block diagram of the proposed hybrid three-level dc–dc converter with the ACOT controller is shown in Fig. 7. The proposed system simultaneously offers solutions for all the challenges mentioned in Section I. For stability analysis purposes, it should be noted that the proposed final system follows a general structure of a ripple-based COT converter, as is explained in Section II in a step-by-step manner. In other words, by tracing back, the final system could be simplified to the COT-based system shown in Fig. 2(c). All the blocks that participate in the on-time signal generation process (such as ADFLL, attenuation and LPF, and min. $T_{\rm OFF}$) are included in the on-time generator block, as shown in Fig. 5. In this case, the stability analysis of the proposed system is simplified to the analysis of a typical COT-based converter [shown in Fig. 2(c)] that is already done in the literature. In [1], for instance, a sampled-data modeling technique is used with the assumption that the output voltage ripple has negligible influence on the response of the inductor current, which is valid in this design as well. The analysis resulted in the stability condition expressed by $R_{\rm ESR}C_{\rm out} > T_{\rm on}/2$, when the dominant source of the output ripple is the ESR resistance of the output capacitor ($R_{\rm ESR}$). In this work, however, the ripple used in the main loop mostly comes from the SWG block, which is added to the output ripple, as explained in Section II-C. The amplified ripple at the output of SWG is equivalent to a large ESR resistor without actually using a capacitor with a large ESR (as mentioned before, this is the main point of using the SWG block). Showing this equivalent resistor as $R_{\rm eq.}$, the stability of the proposed system is ensured when $R_{\rm eq.}C_{\rm out} > T_{\rm on}/2$, which is satisfied in this design.

III. Power Stage Circuits and Details

This section aims to explain how the power stage is managed to achieve a multilevel performance while integrating bootstrap, level shifting, and the flying capacitor balancing without using any off-chip supply rails or circuits, as opposed to prior art [6], [7], [9], [30], [31], [33]. More specifically, the switching logic along with the operation of the power stage reveals how all the available voltages are used to result in a design that is independent of any external resources. The switching operation of the power stage is depicted in Fig. 8. In ϕ_1, switches M_4 and M_2 turn ON, which charges the inductor current and the flying capacitor voltage. In ϕ_2, transistors M_2 and M_1 turn ON, resulting in the discharge of the inductor current while also providing load current. By having switches M_3 and M_1 ON during ϕ_3, the flying capacitor charges the inductor current by the voltage stored from $V_{\rm IN}$ in ϕ_1, and finally, in ϕ_4, switches M_2 and M_1 turn ON once again to provide the load current by discharging all the inductor current received in the previous phase.

When the converter operates in DCM, the inductor current could be negative, wasting energy. To prevent this and improve efficiency at light load, a zero-current detector (ZCD) block is employed to turn OFF all the switches in ϕ_0 [see Fig. 8(a)], when the inductor current is zero.

Although using the multilevel structure reduces the V_{DS} of each power transistor to be $V_{\rm IN}/2$—which is lower than 2.5 V that VDS of the power transistors of the employed technology can tolerate—the absolute voltage at the drain and source of each power transistor could be higher than this, thereby requiring the use of level shifters. The level shifters employed in this work are shown in Fig. 9. They use the internal node voltages ($V_{\rm FLY}B$, V_X, and $V_{\rm FLY}A$) as $V_{\rm SS}$ of the inverters and bootstrapped voltages ($V_{\rm BOOSTED1-4}$) as their V_{DD}, generated by the well-known bootstrap technique (details in Fig. 10). The bootstrapped circuit provides the required supply voltage of the level shifters by using

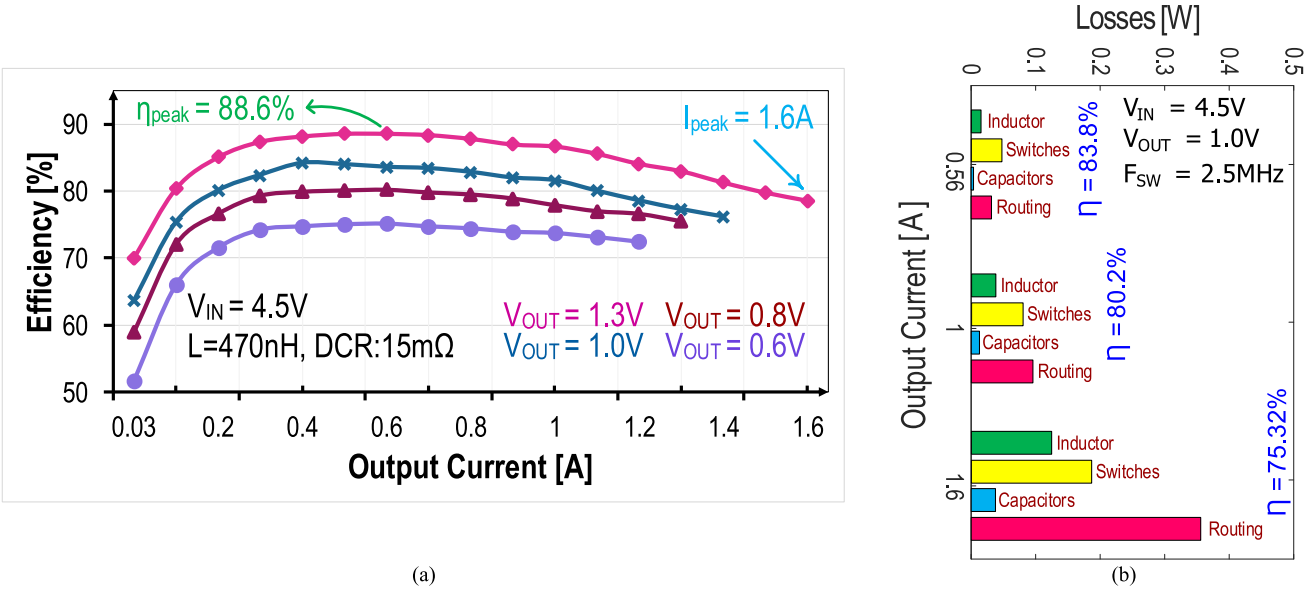

Fig. 12. (a) Proposed hybrid three-level DC–DC converter efficiency versus load current. (b) Loss mechanism.

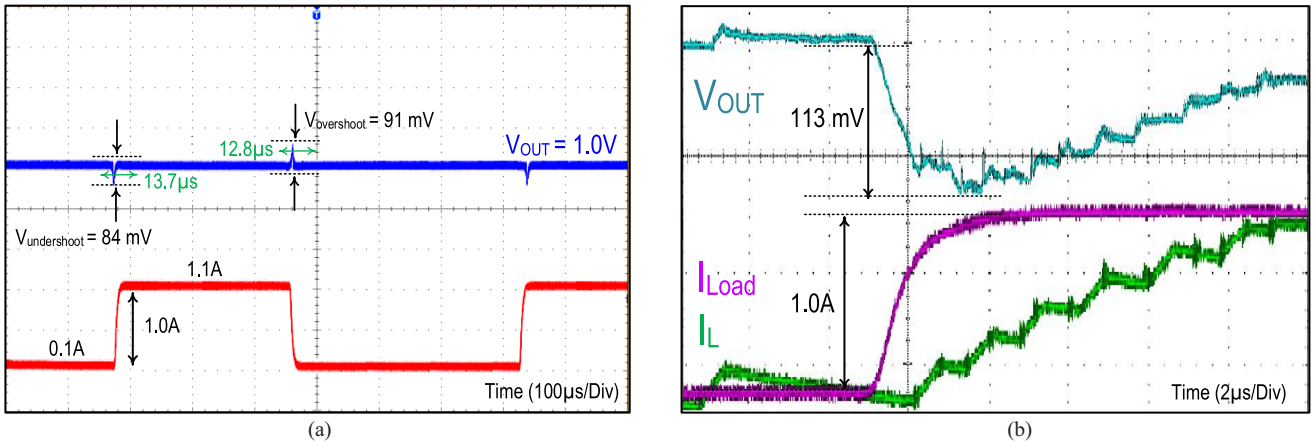

Fig. 13. Measurement results of DC–DC settling and response time from: (a) fast and (b) ultra-fast transient load current change.

only the internal voltage of the power stages without using any external supply rail [6].

A detailed schematic showing the operation of the power stage and the driving circuits during each phase is shown in Fig. 10. During ϕ_1, M_4 and M_2 turn ON. The level shifter for M_4, uses $V_{\text{FLY}A}$ as V_{SS} and V_{BOOSTED4} as V_{DD}. C_{BOOT4} had been already charged to $V_{\text{IN}}/2$ from the previous phase (ϕ_4). As a result, the V_{DD} voltage for the level shifters is equal to $V_{\text{FLY}A}$ + $V_{\text{IN}}/2$, turning ON M_4 properly. All the bootstrapped capacitors ($C_{\text{BOOT1}-4}$) have a small on-chip part (0.2 nF)—to partially tune out the effect of the bond-wire inductance—and a large off-chip part (100 nF). As shown in Fig. 10, during ϕ_4 and ϕ_2 when transistors M_1 and M_2 turn ON, the capacitors C_{BOOT3} and C_{BOOT4} are connected (ideally) between V_{IN} and GND, charging each of them to $V_{\text{IN}}/2$ to be used in ϕ_1 and ϕ_3, respectively.

It should be noted that in the proposed structure, the flying capacitor stays balanced inherently without any need for particular voltage balancing methods, such as precharging of the flying capacitor [30] or active balancing [7]. This is because the voltage across the flying capacitor is well defined during all phases and does not change in each phase, thanks to $C_{\text{BOOT1}-4}$ [6]. In more detail, in each phase, there is exactly two C_{BOOT} in series between V_{DD} and GND, making the voltage across them be well defined and equal to $V_{\text{IN}}/2$. This means that in ϕ_1, for instance, the voltage at $V_{\text{FLY}B}$ is equal to $V_{\text{IN}}/2$. Since the $V_{\text{FLY}A}$ node is connected to V_{DD}, the voltage across C_{FLY} is $V_{\text{IN}}/2$. In ϕ_2, C_{BOOT3} and C_{BOOT4} are in series with V_{IN}, making the voltage across them to be $V_{\text{IN}}/2$. This means that the voltage at $V_{\text{FLY}A}$ is equal to $V_{\text{IN}}/2$, and because the $V_{\text{FLY}B}$ node is connected to GND, the voltage across the flying capacitor stays at $V_{\text{IN}}/2$. The same analysis is valid for ϕ_3 and ϕ_4, ensuring the voltage across CFLY stays at $V_{\text{IN}}/2$ and balanced.

IV. Measurement Results

The proposed hybrid three-level dc–dc converter was implemented in a 65-nm bulk CMOS process. The die photograph is shown in Fig. 11(a), occupying an area of 2.07 mm^2. Fig. 11(b) shows a photograph of the PCB-based interposer used

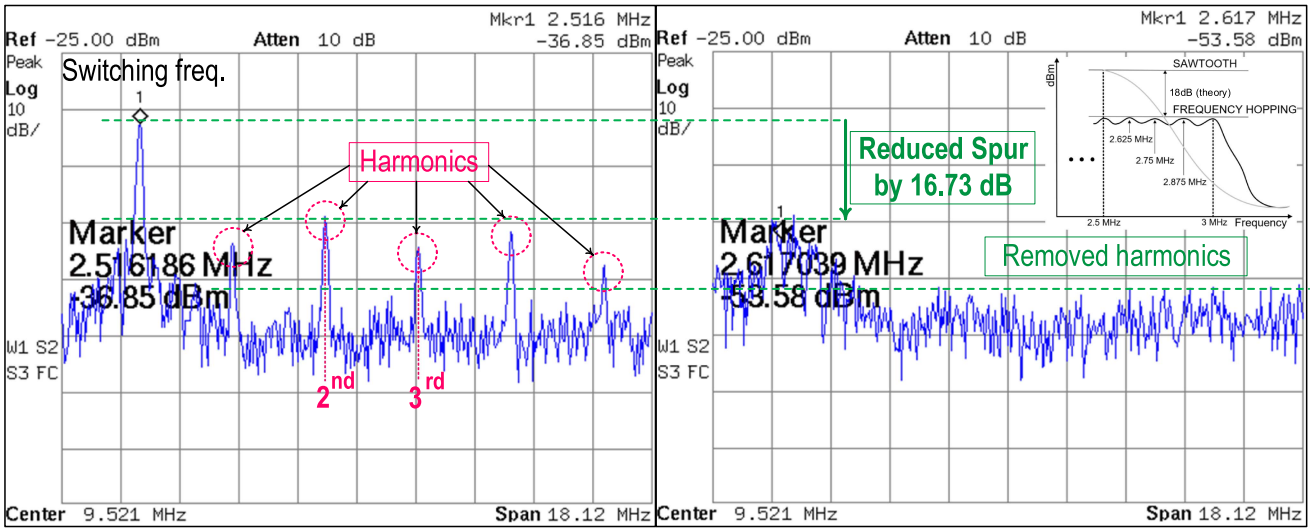

Fig. 14. Output spectrum. (a) Without using the frequency hopping technique. (b) With the frequency hopping technique.

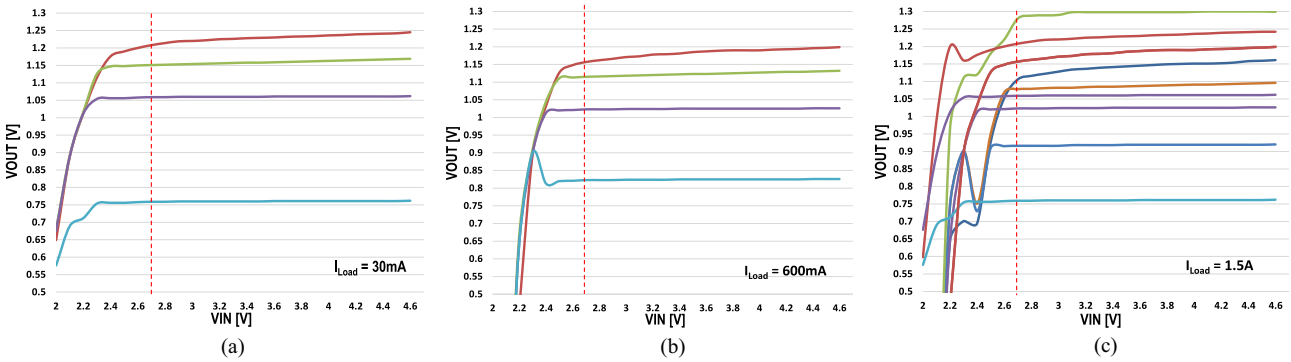

Fig. 15. Effect of input voltage variations on the various output voltage values for (a) light load ($I_{\text{Load}} = 30$ mA), (b) rated load ($I_{\text{Load}} = 600$ mA), and (c) heavy load ($I_{\text{Load}} = 1.5$ A).

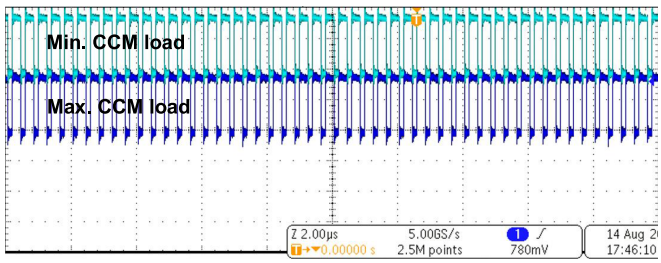

Fig. 16. Switching node (V_X) measurement result at min. and max. CCM loads.

for testing, where the entire footprint of the design, including all necessary passives, occupies an overall area of 13.3 mm^2. Moreover, a 470 nH 0806 SMD inductor with a 15 m Ω dc resistance (DCR), a 1-μ F 0603 flying capacitor, and four 0402 100-nF bootstrap capacitors are the only off-chip components required for this converter. Based on measurement results, the proposed solution is capable of converting a Li-ion battery input voltage range of 2.7–4.5 V to an SoC-compatible voltage range of 0.6–1.3 V with a power density of 0.061 W/mm^2 at the peak efficiency point, all without any need for external supply rails, external control signals, or even an FPGA. All the tests are done with a 10 μF multilayer ceramic capacitor at the output with an ESR as low as 2 mΩ, without showing any subharmonic issues.

The measurement result of the circuit behavior at the start up is shown in Fig. 11(c) for three different output voltages (0.6, 0.95, and 1.3 V). Here, the SS block gradually ramps up the reference voltage toward a steady-state output in less than 2.5 ms, enabling an automatic start-up without any external mechanism. The switching node behavior V_X during the start-up when the output voltage is 1.3 V and is shown in the top left corner.

Fig. 12(a) shows the efficiency of the converter versus load current. Peak efficiency of 88.6% with a conversion ratio of 3.5 is achieved. The efficiency stays above 70% for a 30 mA to 1.6 A load current range when the output is 1.3 V, thanks

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER LI-ION COMPATIBLE DC–DC CONVERTERS.

	Using external supplies or circuits (e.g. FPGA)				Plug&play solutions w/o any external supplies or circuits								
	[9] ISSCC'17, JSSC'20	[31] JSSC'19	[33] ISSCC'19	[6] JSSC'20	[32] TI-Module TPS8268120	[37] Intel EN6310QI	[2] TPE'16	[15] TCASII'20	[7] CICC'20	[10] TPE'16	[36] TPE'18	[34,35] ISSCC'21 JSSC'22	This Work
Structure	Hybrid	Hybrid	Hybrid	Hybrid	Buck	Buck	Buck	Buck	Hybrid	Buck	Buck	Hybrid	Hybrid
Input Voltage [V]	3.0 – 4.5	3.2 – 4.2	5	3.0 – 5	2.5–5.5	2.7–5.5	2.7–3.6	3.3	5.5	3.3	2.6-3.6	4-6	2.7–4.5
Output Voltage [V]	0.3 – 1.0	0.8 – 1.5	1.8	0.3 – 1.2	1.2	0.6-3.3	1.0–1.2	1.03	0.4 – 1.2	1.05	1.05	0.4 – 1.2	0.6–1.3
Peak Output Current [A]	1.53	1.5	10	2.5	1.6	1	1.1	1	1.4	1.7	1.7	1	1.6
L [µH], C_{out} [µF]	0.47, 22	0.012, 2.8	0.01, 18	0.22, 1	NR	On-chip,47	NR	10, 10	0.24, 10	1, 4.7	1, 4.7	0.24, 14.1	0.47, 10
Area*[mm²]	>6**	14.4	75.6	5.5	6.7	20†	NR	4.08**	>9.97**	NR	NR	11	13.3
Peak Efficiency (PE) @ ratio	94.2% @ 4.4	87.2% @ 3.2	93.8% @ 2.8	89.5% @ 4.2	82% @ 3.5	86% @ 4.2	88.2% @ 2.7	93.4% @3.2	92.4% @ 4.6	89% @ 3.1	94% @ 3.1	96.9% @ 4.2	88.6% @3.5
Power Density* [W/mm²] @ PE	<0.031	0.083	0.071	0.11	0.053	0.024	NR	0.038	<0.036	NR	NR	<0.016	**0.061**
Max. Power Density* [W/mm²]	0.16	0.11	0.23	0.38	0.28	0.06	NR	0.25	0.11	NR	NR	0.1	0.15
Light load efficiency* **	80%	<<40%	NR	<70%	47%	<65%	84%	88%	75%	NR	NR	91%	70%
Heavy load efficiency #	88%	87.2%	91%	88%	78%	82%	50%	78%	86%	NR	90%	90%	86%
Output spur	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	**-53.58 dBm**
Switching Freq. & Variations	0.3 - 0.5MHz NR	20 - 50MHz NR	5MHz NR	5MHz NR	5.5MHz 27%	2.2MHz NR	1MHz 2.6%	NR NR	NR NR	2.5 - 3.4MHz 0.32%	2.5MHz NR	NR NR	2.5MHz **0.13%**
Response Time## Settling Time##	NR 45µs	1µs NR	0.5µs### 3µs###	NR	1µs### 4µs###	25µs### 40µs###	NR 10.7µs	10µs### 30µs###	1.75µs >10µs###	2.5µs### 10µs	2µs### 5µs	1µs### 6µs###	3µs, 13.7µs
Controller	PWM	PWM	PWM	PWM	PWM	VM PWM	ACOT	COT	Ripple-injection	ACOT	COT	Ripple-injection	ACOT
Process (nm)	65	150	22	180	NR	NR	180	180	180	28	28	180	65

NR : Not Reported * Die, PCB, and passive components ** Estimated from die and PCB photos, including SMD components size ***Estimated from plotted data at 30mA load current #Estimated from plotted data at 1A load current ## From load transient ###Estimated from graph † including an on-chip inductor

to the PFM nature of the controller. Efficiency degradation at light load is mainly due to up to 2.1-mA quiescent current that the control loop draws. The loss mechanism for several loads from postlayout simulations is shown in Fig. 12(b). At low-load currents, $R_{\rm on}$ of the power switches are the dominant source of loss, whereas the routing loss is dominant at higher load currents due to IR losses.

To investigate how the proposed converter can be operated for SoC applications during rapid load current changes, different load transient tests were completed using a fast transient load test setup, shown in the top right corner of Fig. 7, where an external MOSFET was used to switch between load states. A fast load current change of 1 A results in a settling time less than 14 μs when the output is 1 V, as shown in Fig. 13(a). On the other hand, the response time to a faster load current change of 1 A is less than 3 μs, as depicted in Fig. 13(b).

In order to show how the frequency-hopping technique attenuates the spurs at the switching frequency and its harmonics, the spectrum of $V_{\rm OUT}$ is shown in Fig. 14 before and after using frequency hopping. An attenuation of 16.73 dB is achieved at the switching frequency of around 2.5 MHz, while all the harmonics are attenuated below the noise floor. This rather clean output spectrum makes the proposed design a practical solution for very sensitive blocks of a typical SoC without any need for an additional LDO (which would, otherwise, degrade the overall efficiency due to cascaded losses).

In order to investigate the operation of the dc regulation enhancement block, Fig. 15 shows the effect of input voltage variations on different output voltage values when the load current is light, rated, and high. When the input voltage is greater than 2.7 V, the variations of the output voltage for different values stay below 6 mV, verifying the effectiveness of the dc regulation enhancement block. For an input voltage of lower than 2.7 V, the converter power switches cannot turn ON/OFFcompletely, corrupting the charging/discharging process. Nevertheless, this will not be any problem in practice since the minimum voltage of a typical Li-ion battery will be more than 2.7 V even after a long period of operation [19].

Finally, to investigate the robustness of the switching frequency of the controller in CCM (steady state) when the load current changes, the transient waveform of the switching node (V_X) is shown in Fig. 16 for minimum and maximum CCM load currents. The switching frequency remains almost constant (only 0.13% variations) in CCM, thanks to the ADFLL, in contrast to some commercial parts that report a frequency variation up to 27% [32].

Table I summarizes the performance of the proposed hybrid three-level converter, and compares with other Li-ion-compatible-input and SoC-compatible-output converters. To compare the cost and size, this work occupies 2.07 mm^2 of chip area in a 65-nm technology, whereas the design in [10] that utilizes an ACOT controller in a buck converter with similar transient results, peak efficiency, and switching frequency variations, occupies 2.4 mm^2 of chip area in a 28-nm process, for instance. The design in [36] that employs a COT controller in a buck converter with similar transient results, maximum output

current, and switching frequency, occupies 2.5 mm^2 of chip area in a 28-nm process, as another example. As a result, this work shows a more cost-efficient design with better performance.

When the size of the entire package is considered, this work occupies an overall size of 13.3 mm^2, whereas a similar commercialized chip [37], for instance, needs a solution area of 20 mm^2 and shows less power density than this work. The design in [34] and [35], which achieved similar maximum power density and efficiency compared with this work, needs more than 11.02 mm^2 of package area, but with almost 4× less power density at peak efficiency compared with this work.

In general, the proposed solution has the highest power density among all converters that do not use external circuits or supplies when the area of the die, PCB, and passive components are all considered. In addition, this work achieves less than −53.5-dBm output spur, whereas all other references did not measure or report the output spur. The switching frequency variations (during the steady state) of 0.13% shows an improvement of more than 2.5× compared with [10] and is the lowest compared with all prior art in a fully integrated manner (both power switches and the entire controller). The proposed system fulfills the design goals mentioned in Section I and proposes an attractive option for general and sensitive blocks of SoCs.

V. Conclusion

This article has presented a hybrid multilevel dc–dc converter with a fully on-chip ACOT controller, achieving a power density of 0.061 W/mm^2 at peak efficiency of 88.6% when the area of the die, PCB, and off-chip passive components are considered. This work improved the performance of a traditional COT converter, by proposing solutions for key issues, which are the switching frequency variations, output spurs and ripples. A frequency hopping block resulted in a relatively pure output spectrum with a −53.58-dBm spur at the switching frequency and no harmonic spurs - eliminating a need for a cascade LDO for most blocks of a typical IoT SoC. An ADFLL block resulted in only 0.13% switching frequency variations, limiting the output jitter and EMI. When a similar commercialized product [32] is considered for comparison, this work has better peak efficiency and power density while maintaining an efficiency of more than 70% for a load current range of 30 mA to 1.6 A. When compared with the state-of-the-art nm-scaled SoC-compatible converters, the proposed solution can work without the need for external circuits while achieving high power density at peak efficiency.

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