Letters

A Fully Integrated Heterogenous Si-CMOS/GaN 500 MHz 6 V-to-18 V Boost Converter Chip

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***Abstract*—This article presents a fully integrated 500 MHz single-switch resonant boost converter using heterogeneous integrated gallium nitride (GaN) and Si-CMOS. Seeking for high level of integration with watt-level power delivering capabilities, the high-speed driver circuitries are implemented in Si-CMOS with customized on-chip inductors, whereas the power switches adopt GaN devices. Two chips are co-designed and integrated using standard flip-chip process. In the proof-of-concept, a 500 MHz single-switch resonant boost dc/dc converter is implemented, fabricated, and measured. The chip occupies an area of 3 mm × 3 mm. It features V_{OUT}/V_{in} of 14–20 V/6 V and P_{OUT} of 3.98–4.2 W with 50–100 Ω loads. The obtained maximal conversion efficiency of 58% and power density of 460 mW/mm^2 are the highest among the similar fully integrated state of the arts.**

***Index Terms*—Gallium nitride (GaN), GaN_2BCD, heterogeneous integration (HI), resonant dc/dc converter, silicon-on-insulator.**

I. Introduction

Chip-level power electronics and systems are greatly desired in advanced Internet of Things [1] and portable equipment [2], with no necessity of bulky off-the-shelf passive elements. Gallium nitride (GaN)-based power converters have shown excellency in conversion efficiency and operation frequencies, thanks to the low conduction resistance and high electron mobility of GaN power switches [3]. Toward a higher level of integration, the heterogeneous integration (HI) of the GaN and the silicon technologies with optimization in both precise control circuitry and low-loss power devices becomes a promising candidate [4].

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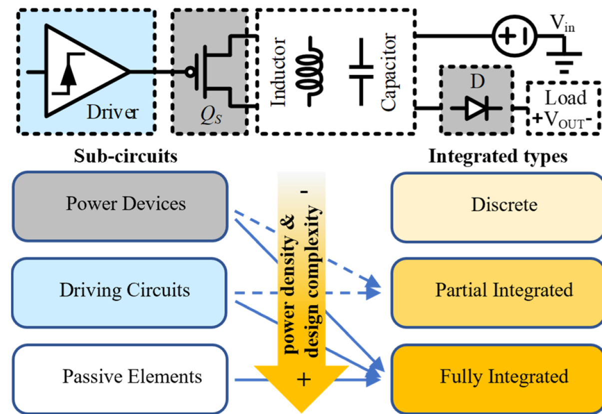

Fig. 1. Simple diagram of a DC/DC converter and the overview of chip-level heterogeneous integration technologies of DC/DC converters.

This work aims to design a watt-level fully integrated power converter IC for the 4–6 V lithium-ion battery management devices [5], [6], e.g., the wearable backlight LEDs.

Fig. 1 shows a typical dc/dc power converter. The power device switches the input voltage V_{in} to ac signal and rectifies it to the load, which forms a new voltage level V_{OUT}. Using HI technology, the following three main types have been widely adopted in hybrid GaN and Si-CMOS converters.

1) Board-level planar integration using wire bonding of Si-CMOS control circuits, GaN power devices, and off-the-shelf *LC* components [7], [8], [9]. It features <30 MHz switching frequency, watt-level P_{OUT} but bulky size.
2) Integration of Si-CMOS control circuit and GaN power devices into one chip, but wire bond with off-the-shelf *LC* components on PCB [10], [11] and GaN_2BCD technologies in [12] and [13]. It achieves higher operation frequency at MHz range due to less parasitic of interconnections and better conversion efficiency compared with type 1). But the off-chip components confront further integration.
3) Full integration with the *LC* components. The integrated passive devices platform [14] and monolithic GaN-on-SiC platform [15] were explored; however, compromises in conversion efficiency and voltage conversion ratio were observed.

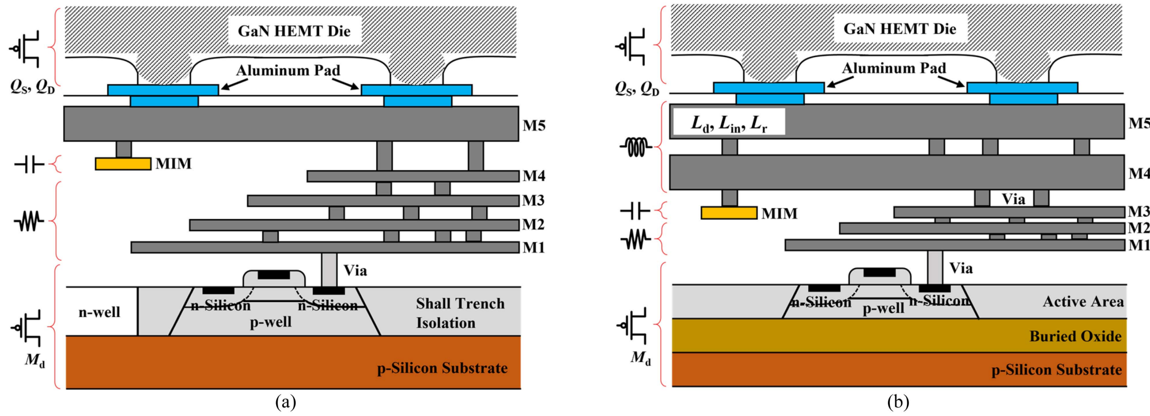

Fig. 2. Cross sections of the (a) GaN_2BCD technology using GF's 0.18-μm BCD process [12] and (b) this work using GF's 0.13-μm CMOS SOI process.

In this article, a tridimensional fully integrated HI dc/dc boost converter chip is presented. The high-speed driver circuitries are implemented in Si-CMOS with customized on-chip inductors and flip-chip integrated with GaN devices. Compared with our previous patented GaN_2BCD technology and circuits using high-voltage BCD [12], [13], the Si-CMOS platform is adopted to demonstrate the feasibility of HI with GaN switches. In addition, the resonating inductors are co-designed for on-chip integration, to achieve higher level of integration and form-factor miniaturization, and fully utilizing the switching-speed advantages of GaN power devices. The fabricated prototype demonstrates excellences in terms of form factor, power density, switching frequency, and conversion efficiency.

II. Circuit Design and Implementation

In the GaN_2BCD design flows [12], the Si-CMOS is designed and implemented with PDK model. Then, the GaN die is a flip-chip stacked onto the silicon die through the top metal layer openings. Fig. 2(a) shows the cross-sectional view of the 3.3-to-70 V boost converter prototype [13] in the GaN_2BCD technology. The front-end-of-line process hosts the Si-CMOS devices while the back-end-of-line process forms the interconnects, resistors, capacitors, and pad opens for GaN devices. This work uses the GlobalFoundries's (GF's) 0.13-μm CMOS SOI technology as the silicon platform.

As shown in Fig. 2(b), the thick top metal layers M4 and M5 are stacked and customized for on-chip inductors.

Fig. 3 gives the inductance values and quality factor (Q-factor) for two-turn and three-turn inductors, at a wide range of radius values. It is noted that inductors are obtained with 2.8–9 nH inductances and Q-factor of 20–26, which is suitable for the MHz dc/dc converter realizations.

In Fig. 4, a 500-MHz Class-E resonant dc/dc boost converter is targeted in this work. The converter comprises a resonant driving stage circuit (M_d, C_Q, and L_d) and a power stage circuit (L_{in}, L_r, C_S, C_D, Q, and Q_D). The M_d is driven by a dc-shifted radio frequency signal where the metal-line resistor R_{lim} is used to prevent current overshooting.

Fig. 5 shows three essential voltages waveforms of the converter, as the converter comprises two LC pairs of L_{in}-C_S and L_r-C_D. When the upper half of the RF_{in} occurs on the gate of M_d and turns it ON, the V_{GS} is pulled to ground and the GaN switch Q_S turns OFF. The V_{DS} voltage and the V_{REC} voltage forms pseudosinusoidal shapes, because the resonant tanks L_{in}-C_S and L_r-C_D function as bandpass filters that enhancing power transferred to the load at fundamental switching frequency. At the lower half of the RF_{in} cycle, the M_d turns OFF and switch Q_S turns ON. The circuit parameters are chosen according to the following steps to ensure zero-voltage switching (ZVS) operations.

It is assumed that all resonant capacitors (C_Q, C_S, and C_D) are treated as part of the parasitic capacitance of GaN devices. For example, as shown in Fig. 4, the collective capacitance seen from DRAIN terminal of Q_S is $C_{GD}+C_{DS}$ (obtained from datasheet [16]) during OFF state, whereas the collective capacitance seen

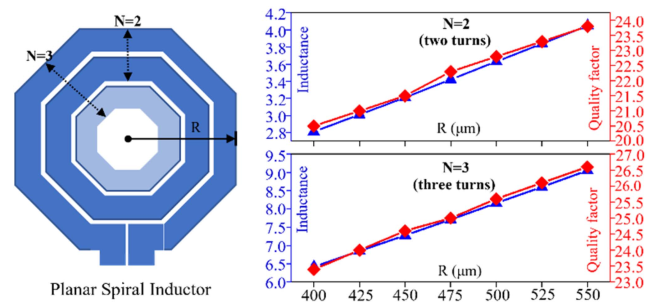

Fig. 3. Top view of three-turn on-chip planar spiral inductor and its extracted inductances/Q-factors versus radius with two-turn and three-turn at 500 MHz.

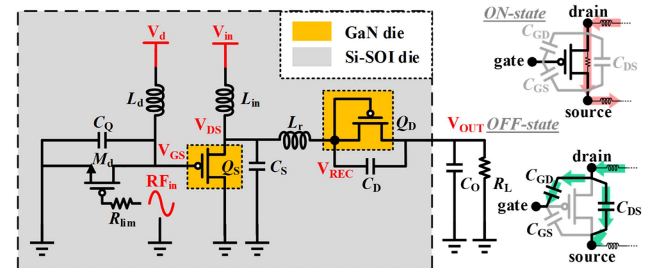

Fig. 4. Schematic diagram of the 500 MHz resonant boost converter, and simplified equivalent models of the flip-chip GaN power switch (Q_S) during turning-ON and turning-OFF states, respectively.

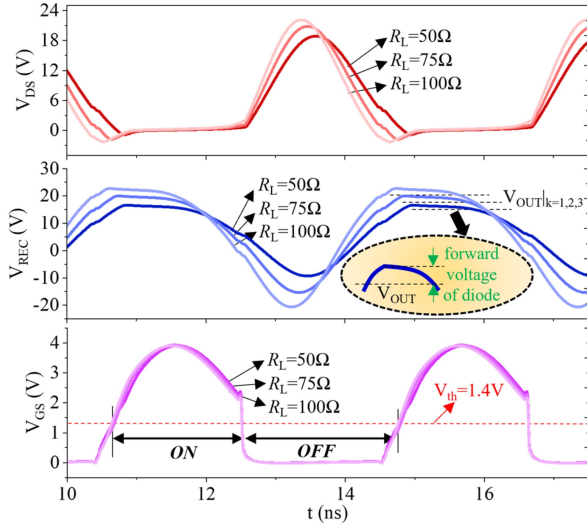

Fig. 5. Simulated V_{DS}, V_{REC}, and V_{GS} waveforms under V_{in}=6 V, R_L=50, 75, and 100 Ω. The threshold voltage of GaN switch is 1.4 V [16].

from the DRAIN of diode-connected GaN device Q_D also equals $C_{GD}+C_{DS}$. The resonant frequency of L_r-C_D is determined with the voltage gain of the boost converter, which is defined as [14]:

$$\frac{V_{OUT}}{V_{in}} = \frac{8}{\pi^2}\frac{1}{\sqrt{\left(1-\left(\omega_S\big/L_rC_D\right)^2\right)^2+\left(\frac{\omega_S/L_rC_D}{\sqrt{L_r/C_D}\big/R_{rec}}\right)^2}} \tag{1}$$

where ω_S is the angular switching frequency and R_{rec} is the resistance seen to the diode Q_D's input. Compared with L_r, the L_{in} works as an RF choke, a large inductance value (several times of L_r) must be chosen. Thus, an 8.1-nH planar spiral inductor with N = 3 is chosen as L_{in} from Fig. 3, whereas the L_r is implemented by two parallel 3.4-nH inductors, which reduces the current density to facilitate on-chip implementation. The driver stage uses a 2.8-nH L_d with N = 2 as the resonant inductor to form a resonating voltage generator with M_d and C_Q.

From Fig. 5, the main switch Q_S maintains ZVS operations at 50–100 Ω loads when the V_{in} = 6 V, with a conversion ratio of 2–3 times. It is noted that the V_{DS} voltage rises up to 22 V that exceeds most of voltage rating in the silicon technologies. The waveforms of V_{GS} show a voltage swing up to 4 V, and a near 50% duty cycle is realized.

III. Experimental Verification and Discussion

Fig. 6 shows the chip microphotograph. The Si-CMOS die occupies only 3 mm × 3 mm in area, on which two GaN devices (one is configured as a diode) are directly flip-chip stacked. All the power inductors surround the GaN devices to minimize the electromagnetic interferences.

Fig. 7 shows the measured V_{OUT} waveforms. The switching frequency of prototype is 500 MHz. An external capacitor C_O = 10 nF is used to emulate the output conditions. Small ripples less than 80 mV are observed under 4–6 V input. Fig. 8(a) plots the output power and conversion efficiency. The converter delivers >4 W P_{OUT} with a maximal conversion efficiency of

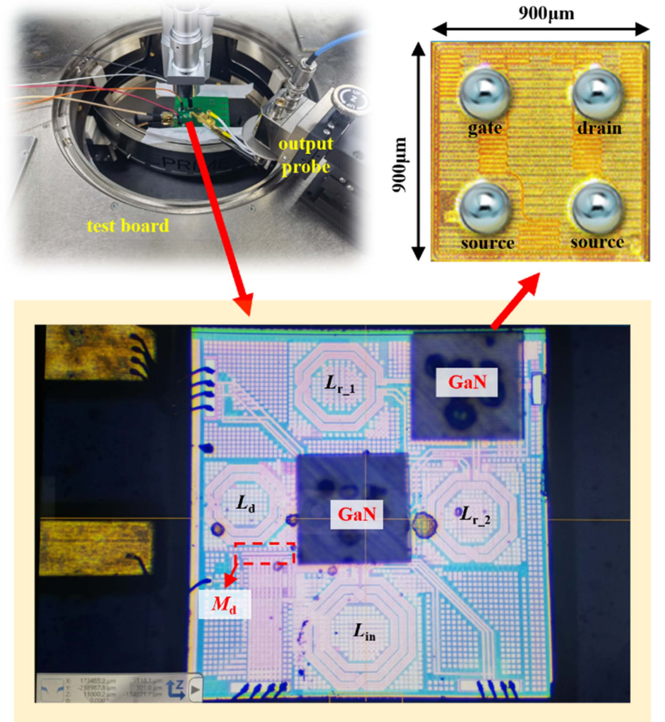

Fig. 6. On-board chip measurement set up (top left), bottom view of a die of GaN power devices (top right), and microphotograph of the fully integrated dc–dc converter in the area of chip is 3 mm×3 mm (bottom).

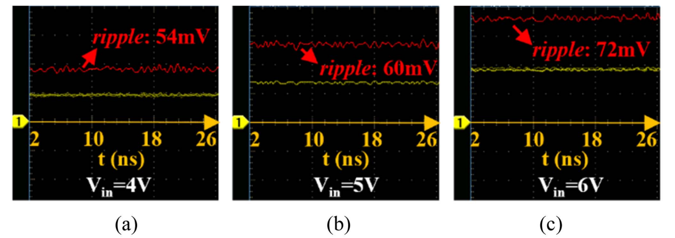

Fig. 7. Measured V_{OUT} waveforms at R_L = 50 Ω and (a) V_{in} = 4 V, (b) V_{in} = 5 V, and (c) V_{in} = 6 V.

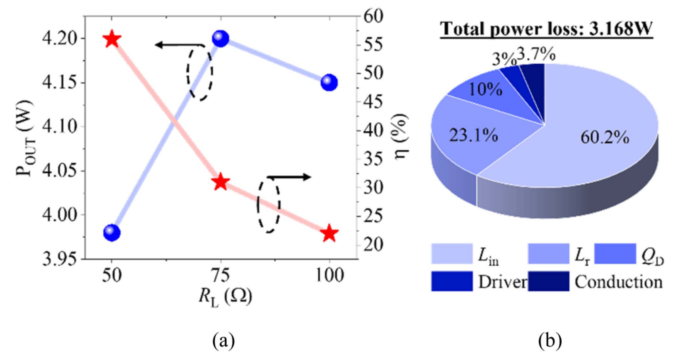

Fig. 8. (a) P_{OUT} and conversion efficiency at V_{in} = 6 V and R_L = 50/75/100 Ω. (b) Bar chart of the calculated power loss caused by Joule heat in L_{in}, Joule heat in L_r, forward voltage of the diode D, driver stage, and conduction losses of the GaN power devices, at V_{in} = 6 V and R_L = 75 Ω.

TABLE I
PERFORMANCE COMPARISON OF RECENTLY REPORTED ON-CHIP DC–DC BOOST CONVERTERS

Design	2022[11]	2019 [13]	2016 [15]	2018 [14]	This Work
Process	0.18 µm Si-CMOS + low-voltage GaN nMOS	0.18 µm Si-BCD + Commercial GaN (GaN2BCD)	0.25 µm GaN-on-SiC	0.18 µm Si-CMOS + 0.25 µm GaN + IPD	0.13 µm CMOS-SOI + Commercial GaN
Integration Level	Package-integrated with Off-the-shelf Components	Package-integrated with Off-the-shelf Components	Fully Integrated	Fully Integrated	Fully Integrated
Switching Frequency	10 MHz	50 kHz	680 MHz	300 MHz	500 MHz
V_{OUT}/V_{in}	1 V /5 V	70 V/3.3 V	20 V/12 V	18 V/12 V	14–20 V/6 V
Max power density	N.A.	N.A.	240 mW/mm^2	45 mW/mm^2	466 mW/mm^2
Area*	4 mm×4 mm (exclude off-chip inductors)	3.2 mm×1.8 mm (exclude off-chip inductors)	3 mm×3 mm	9.4 mm×9.8 mm	3 mm×3 mm
Max. efficiency	83.5%	70.3%	34%	47.3%	58%

*The chip area in all the references do not include the I/O filtering capacitors.

58% at 75 Ω load. Fig. 8(b) analyzes the calculated power loss dissipation, which is mainly from the Joule heating in power inductors. It indicates that the on-chip inductor is the key to the efficiency bottlenecks for fully integrated conversion ICs. If nominal off-chip inductors with Q-factor of 100 at 500 MHz are adopted in this design, the theoretical maximum conversion efficiency can be improved to 78%, calculated based on the measured results and system resimulation. In addition, a serial-diode-connected GaN device with 2.2 V forward voltage [16] causes 10% of power losses, meaning that a more efficient high-frequency power diode should be explored.

However, the power loss caused by power devices conduction is as low as 3.7%, indicating that the proposed Si-CMOS/GaN hybrid prototype is suitable for high-power and high switching frequency operations. Table I summarizes the results and compares this work to the state of the arts. The fully integrated works in [13] and [14] and this work generally show poorer conversion efficiency due to low Q-factor on-chip inductors, compared with the package-level integrated converters with off-chip inductors [11], [13]. Compared with other fully integrated converters [14], [15], this work operates at similar frequency and conversion ratio, and demonstrate the highest power density and conversion efficiency. In addition, comparing to the works in [11] and [14], the entire fabrication procedures leverage on traditional and mature semiconductor fabrication and assembly equipment without any other types of substrates.

IV. CONCLUSION

In this work, a 500-MHz fully integrated dc/dc boost converter was designed and fabricated. The resonant gate driver and all power inductors are processed with GF's 0.13-μm CMOS SOI technology, whereas the commercial EPC GaN high electron mobility transistor (HEMT) is selected as the power switch and diode. The converter occupies only 9 mm^2, achieves a power density of 466 mW/mm^2. Thus, as a technology extension of GaN_2BCD technology reported in our patent [12], the proposed fully integrated converter IC indicates a promising candidate for integrated and power-dense power electronics.

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