A Design Method of Partially Interleaved Winding Structure With Low Leakage Inductance for Planar Transformer Application

Xuetong Zhou, Yufei Tian, Yuhua Quan, Xuefei Zhang, Tiantian Liu, Junhong Feng, Da Wang, Xinhong Cheng, *Member, IEEE*, Li Zheng, *Member, IEEE*, and Yuehui Yu

***Abstract*—For the planar transformer with turns ratio away from 1:1, the leakage inductance of fully interleaved winding structure is not the minimal and the structure should be optimized. In this article, a design method for partially interleaved winding structure is proposed to achieve the minimal leakage inductance at arbitrary turns ratio. According to the analysis of magnetomotive force, the tradeoff among the total number of layers, the number and the position of consecutive primary-side layers will be executed through the recursive design flow to minimize the leakage inductance. Based on this design method, the optimal partially interleaved structures for the transformers with 16:12 turns ratio and 25:3 turns ratio are "$(P\text{-}S\text{-}P\text{-}S\text{-}P\text{-}S\text{-}P)_4$" and "5P-S-5P-S-5P-5P-S-5P," respectively, and the leakage inductances are verified by the finite element analysis and the experiment data. For the proposed structure, the measured leakage inductance drops 50%, and its dependence of frequency and the series resistance also decrease compared to the fully interleaved structure. Furthermore, the transformers with the proposed structures were tested in an *LLC* converter, where the loss of the converter and the change of resonant frequency are the smallest compared to other structures.**

***Index Terms*—Fully interleaved, high-frequency transformer, leakage inductance, partially interleaved, planar transformer.**

I. Introduction

Leakage inductance usually plays a negative role in switching converter. A large leakage inductance may cause voltage spike in switching devices due to high d*i*/d*t*. Besides, it slows down the change of switch current, which may increase the switching losses. Therefore, leakage inductance makes converter inefficient and leads to reliability problems [1], [2], [3].

Fully interleaved structure is considered to have the minimal leakage inductance among typical structures including noninterleaved structure and "sandwiches" structure. Fully interleaved structure reduces leakage flux by tightly coupling the windings and thus reduces leakage inductance. Nonetheless, fully interleaved structure does not always have the minimal leakage inductance. Several structures with lower leakage inductances, such as half turn structure [4], shunt magnetic circuit structure [5], partially interleaved structure [6], [7], have been proposed recently. However, these structures are designed for transformers with 1:1 turns ratio or a specific turns ratio. In order to design transformers for different applications, a design method of winding structure for arbitrary turns ratio is required to obtain the minimal leakage inductance.

To find the optimized winding arrangement with the minimal leakage inductance at arbitrary turns ratio and arbitrary turns per layer, a design method of partially interleaved winding structure is proposed in this article. The essence of the proposed method is a tradeoff among the total number of layers, the number and the position of consecutive same-side layers. As the representatives of 1 turn per layer case and multiple turns per layer case, transformers with 16:12 turns ratio and 25:3 turns ratio are analyzed, simulated and tested. The transformer with 16:12 turns ratio is required for the 400/300 V onboard charger (OBC). To meet the large current requirements of the primary and secondary sides of OBC, there should be only one turn per layer. The 400/48 V dc/dc converter is usually applied in data center [8], where the transformer with 25:3 turns ratio is required. Since the current ratio of the primary side to the secondary side is 3:25, the minimum coil width of the primary side can be less than 1/8 of the secondary side. Thus, based on the transformer with 25:3 turns ratio, the case with multiple turns per layer is also analyzed.

The calculation of leakage inductance at low frequency is based on the calculation method in [4] and [9] and the calculation at high frequency is based on the theory in [10].

The rest of this article is organized as follows. In Section II, the calculation method of leakage inductance is presented and the magnetic field and leakage inductance of fully interleaved

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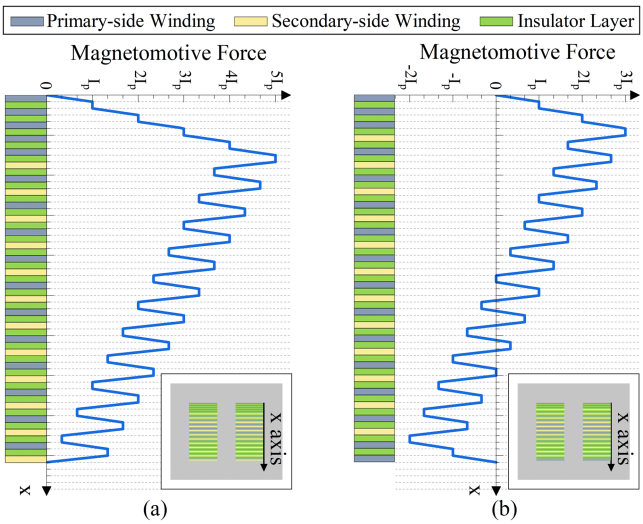

Fig. 1. Arrangements and MMF distribution of two types of fully interleaved structure (Turns ratio = 16:12). The inset is the diagram of the transformer. (a) Asymmetric structure. (b) Symmetric structure.

structure are discussed. In Section III, the principles and the design flow of the proposed design method are illustrated. The proposed design method applied in transformers with 16:12 turns ratio and 25:3 turns ratio is analyzed and simulated in Sections IV and V. In Section VI, loss, parasitic capacitance and high-frequency performance of the proposed structure are discussed. The experiment results are shown in Section VII. Finally, Section VIII concludes the article.

II. Leakage Inductance of Fully Interleaved Structure

A. Leakage Inductance Calculation

Some of the flux generated by ac current in primary-side winding will leak from the core, which makes the transformer imperfectly-coupled and results in leakage inductance. Leakage inductance of the primary-side winding can be calculated by the energy stored in the magnetic field

$$\frac{1}{2}L_{lk}I_p^2 = E = \frac{1}{2}\int B\cdot H\cdot dV = \frac{\mu_0}{2}\sum\int_0^h H^2\cdot l\cdot b\cdot dx \tag{1}$$

where h is the thickness of each winding layer, l is the length of the coil in each layer, and b is the width of the coil. The diagrams of the transformers are shown in the inset of Fig. 1, where the light gray marks the magnetic core, the dark gray, the yellow, and the green depict the primary-side winding, the secondary-side winding, and the insulator layer, respectively.

To simplify the leakage inductance calculation, the eddy current effect is not considered so that the magnetic field strength varies linearly in winding layers. According to Ampère's circuital law, the magnetic field strength in primary-side winding layer is illustrated in (2). Since the flux disperses rapidly after leaving the coil and the magnetic reluctance of the core is much less than that of winding layers and insulator layers, the magnetic field strength in each primary-side winding layer can be computed by the following:

$$H(x) = H(0) + \frac{n_pI_p}{b}\cdot\frac{x}{h_p} \tag{2}$$

where $H(0)$ is the magnetic field strength at the top of the primary-side winding layer, n_p is the number of turns in each primary-side winding layer, and h_p is the height of each primary-side winding layer. The magnetic field strength in each secondary-side winding layer can be computed by the following:

$$H(x) = H(0) - \frac{n_sI_s}{b}\cdot\frac{x}{h_s} \tag{3}$$

where $H(0)$ is the magnetic field strength at the top of the secondary-side winding layer, n_s is the number of turns in each secondary-side winding layer, and h_s is the height of each secondary-side winding layer. The magnetic field strength keeps constant in insulator layer since there is no extra current.

The total energy is the sum of energy stored in primary-side winding layers, secondary-side winding layers, and insulator layers. Thus, the leakage inductance can be calculated by the following:

$$\begin{aligned}
L_{lk} &= \frac{\mu_0}{I_p^2}\sum\int_0^h H^2\cdot l\cdot b\cdot dx \\
&= \frac{\mu_0}{I_p^2}\cdot l\cdot b\cdot\left[\sum_{\text{primary}}\int_0^{h_p}\left(H(0)+\frac{n_pI_p}{b}\cdot\frac{x}{h_p}\right)^2\cdot dx\right. \\
&\quad+\sum_{\text{secondary}}\int_0^{h_s}\left(H(0)-\frac{n_sI_s}{b}\cdot\frac{x}{h_s}\right)^2\cdot dx \\
&\quad\left.+\sum_{\text{insulator}}H^2\cdot h_i\right] \\
&= \frac{\mu_0}{I_p^2}\cdot l\cdot b\cdot\left[\sum_{\text{primary}}\frac{bh_p}{3n_pI_p}\cdot H^3\Big|\begin{matrix}H(h_p)\\H(0)\end{matrix}\right. \\
&\quad\left.-\sum_{\text{secondary}}\frac{bh_s}{3n_sI_s}\cdot H^3\Big|\begin{matrix}H(h_s)\\H(0)\end{matrix}+\sum_{\text{insulator}}H^2\cdot h_i\right]
\end{aligned} \tag{4}$$

where h_i is the height of each insulator layer.

B. Fully Interleaved Structure

Fully interleaved structure can be divided into symmetric and asymmetric structures as shown in Fig. 1, where the magnetomotive force (MMF) is defined as $b\cdot[H(x)-H(0)]$ and the turns ratio is 16:12.

The maximum value of MMF in asymmetric structure appears between the 5th primary-side winding layer and the 1st secondary-side winding layer. According to (4), the leakage

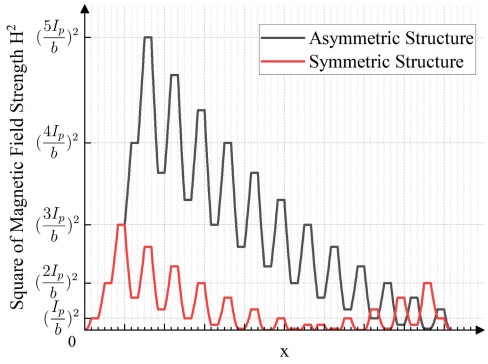

Fig. 2. Distribution of H^2 in asymmetric and symmetric fully interleaved structure.

inductance of the asymmetric fully interleaved structure is

$$L_{lk} = \frac{\mu_0 \cdot l}{b} \cdot \left(\frac{1112}{9} h_p + \frac{278}{3} h_s + \frac{2002}{9} h_i \right). \quad (5)$$

The maximum value of MMF in symmetric structure appears between the 3rd primary-side winding layer and the 1st secondary-side winding layer. The leakage inductance is

$$L_{lk} = \frac{\mu_0 \cdot l}{b} \cdot \left(\frac{248}{9} h_p + \frac{62}{3} h_s + \frac{490}{9} h_i \right). \quad (6)$$

For fully interleaved structures, the leakage inductance of the symmetric structure is less than 25% of asymmetric structure's according to (5) and (6). Since leakage inductance is proportional to the integral of the square of magnetic field strength ($\int H^2 dx$) according to (4), the distribution of H^2 can show leakage inductance more intuitively. As shown in Fig. 2, the $H^2 - x$ curve of symmetric structure is far below the curve of asymmetric structure, which indicates that the symmetric fully interleaved structure has a lower leakage inductance.

III. Proposed Design Method of Partially Interleaved Winding Structure

A. Design Principles

For transformers with 16:12 turns ratio, the square of magnetic field strength (H^2) reaches its maximum value after five consecutive primary-side winding layers and begins to decrease in oscillation from the first secondary-side winding layer in asymmetric fully interleaved structure. H^2 reaches its maximum value after three consecutive primary-side winding layers in symmetric fully interleaved structure. Additionally, in noninterleaved structure and sandwich structure, there will be 16 and 8 consecutive primary-side winding layers, respectively. The fewer the consecutive primary-side winding layers, the lower the leakage inductance.

Besides, the position of the consecutive primary-side winding layers further affects leakage inductance. For instance, if the bottommost secondary-side winding layer is above the topmost primary-side layer in asymmetric fully interleaved structure, the

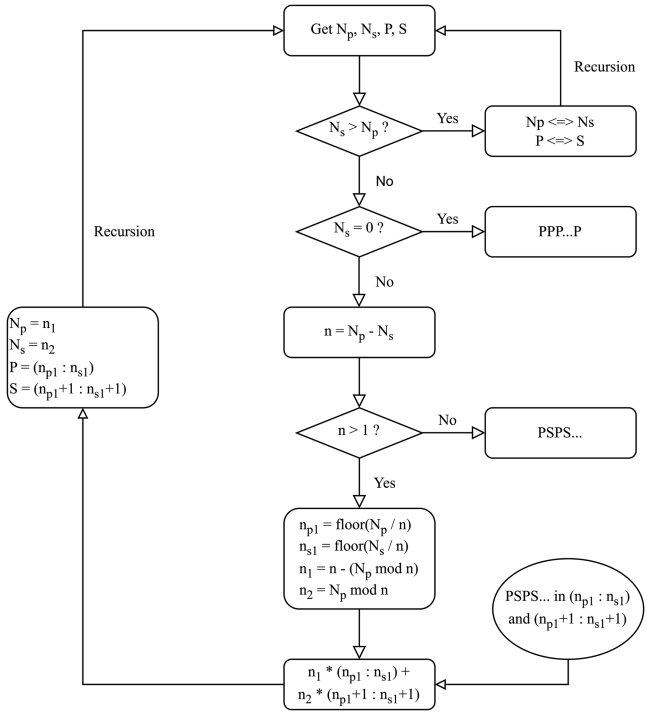

Fig. 3. Design flow of the proposed design method of partially interleaved structure.

leakage inductance is as follows:

$$L_{lk} = \frac{\mu_0 \cdot l}{b} \cdot \left(\frac{5716}{81} h_p + \frac{102}{3} h_s + \frac{770}{9} h_i \right). \quad (7)$$

Equation (7) shows that the leakage inductance will decrease by over 50% once putting the bottommost secondary-side winding layer onto the topmost primary-side layer. Once there are several secondary-side winding layers on the top of the consecutive primary-side winding layers, the maximum value of H^2 will decrease, which leads to a lower leakage inductance. Based on these principles, the specific proposed design method is given as follows.

B. Design Flow

A recursive design flow of the proposed of partially interleaved structure is illustrated in Fig. 3, and a pseudocode in python style is shown in the Appendix.

If N_p is less than N_s, the primary-side winding layers should exchange the position with secondary-side winding layers first as illustrated in design flow. Consequently, the following discussion is based on that of $N_p \geq N_s$. According to the design flow, the case for a transformer with $N_p : N_s$ turns ratio and one turn in each winding layer will be discussed in detail. If $N_p = N_s + 1$ or $N_p = N_s$, the fully interleaved structure with the minimal leakage inductance can be achieved. If $N_p > N_s + 1$, the proposed structure will be a combination of two subgroups. In each subgroup, the arrangement is "PSPS …" to guarantee minimal leakage flux. Then regarding the two subgroups as new primary-side and secondary-side windings to further partially interleave and recurse to achieve a partially interleaved structure with the

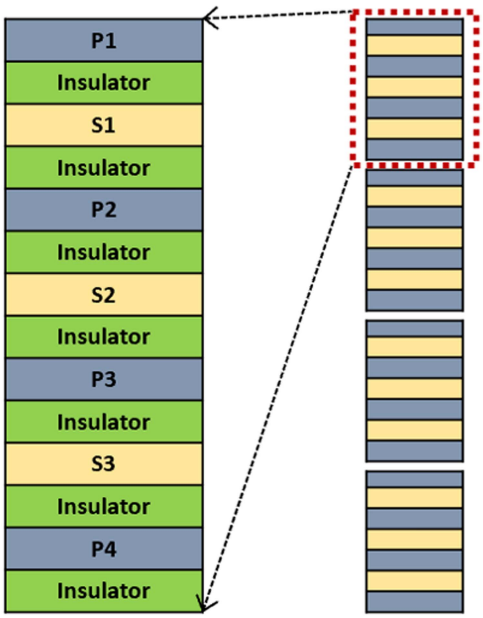

Fig. 4. Arrangement of the proposed partially interleaved structure (Turns ratio = 16:12).

minimal leakage inductance. The mathematical induction can prove that the proposed partially interleaved structure has the minimal leakage inductance. Therefore, the transformers with arbitrary turns ratio can be designed with the proposed method to achieve the minimal leakage inductance.

IV. Proposed Design Method for Transformers With 16:12 Turns Ratio

A. Arrangement of the Proposed Structure

Since the primary-side winding has four more turns than the secondary-side winding, they can be divided into four groups according to the proposed design method. In each group, four turns of primary-side winding and three turns of secondary-side winding are fully interleaved. The arrangement of the proposed structure is shown in Fig. 4.

B. Leakage Inductance Calculation

Fig. 5 shows the MMF distribution of the proposed structure for the transformer with 16:12 turns ratio. According to (4), the leakage inductance can be computed by the following:

$$L_{lk} = \frac{\mu_0 \cdot l}{b} \cdot \left(\frac{32}{9} h_p + \frac{8}{3} h_s + \frac{112}{9} h_i \right). \tag{8}$$

The leakage inductance of the proposed partially interleaved structure is less than 25% of that of the symmetric fully interleaved structure and 6.25% of that of the asymmetric fully interleaved structure, according to (5), (6), and (8). The $H^2 - x$ curves show the difference intuitively in Fig. 6.

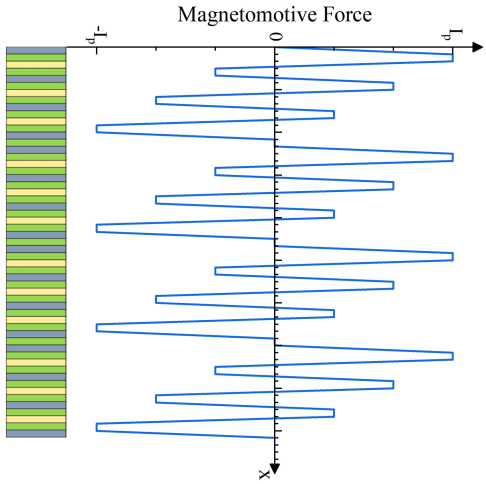

Fig. 5. MMF distribution of the proposed partially interleaved structure (Turns ratio = 16:12).

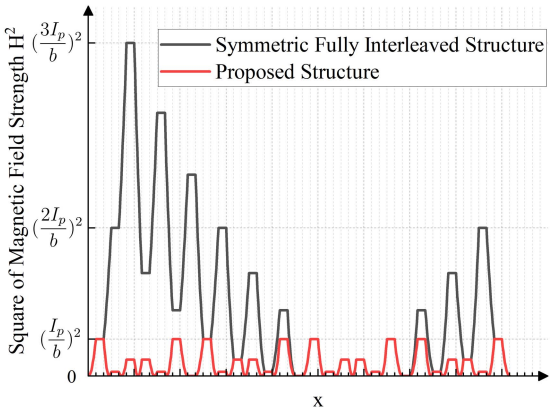

Fig. 6. Distribution of H^2 in symmetric fully interleaved structure and proposed partially interleaved structure from mathematical calculation.

TABLE I
Transformer Parameters in Simulation

Parameters	Values
Primary-side Conductor Thickness	70 μm
Secondary-side Conductor Thickness	70 μm
Insulator Thickness	330 μm
Core Type	EQ40/20
Core Window Width	8 mm
Core Effective Area	286.9 mm^2
Core Effective Length	53.291 mm
Mean Turn Length of Conductors	87.96 mm

C. Finite-Element Analysis Results

In order to verify that the proposed partially interleaved structure has a lower leakage inductance, a finite element analysis (FEA) simulation is built with the software of Ansys Maxwell. The ferrite core EQ40/20 used in planar transformer is selected for simulation. The parameters of the transformers are shown in Table I.

The switching frequency in simulation is set to 100 kHz since it is a typical working frequency for dc/dc converters. The

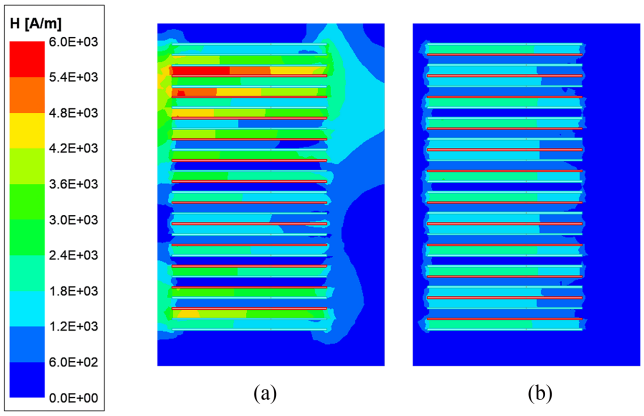

Fig. 7. Distribution of magnetic field strength H for symmetric fully interleaved structure and proposed structure from FEA simulation. (a) Symmetric fully interleaved structure. (b) Proposed structure.

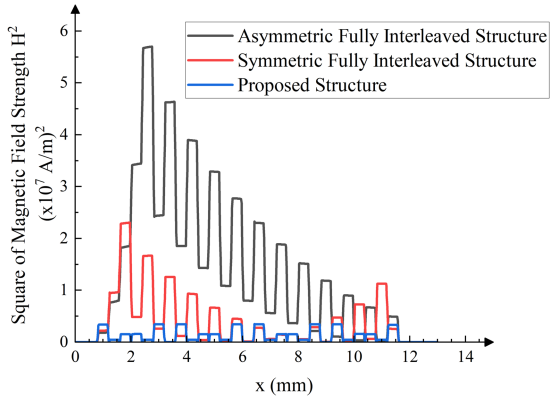

Fig. 8. Distribution of H^2 for asymmetric fully interleaved, symmetric fully interleaved, and proposed partially interleaved structure from FEA simulation.

TABLE II
LEAKAGE INDUCTANCE OF CALCULATION AND SIMULATION

	Calculation (nH)	Simulation (nH)
Asymmetric Fully Interleaved Structure	1631.15	1740
Symmetric Fully Interleaved Structure	393.17	454
Proposed Partially Interleaved Structure	83.69	117

distribution of magnetic field strength H is shown in Fig. 7. Fig. 8 shows the $H^2 - x$ curves of the proposed structure and fully interleaved structures in FEA simulation. The leakage inductance values of calculation and simulation are compared in Table II. The figures of FEA and theoretical analysis of H^2 distribution and leakage inductance show highly agreement to indicate that the proposed structure has a lower leakage inductance compared with fully interleaved structure.

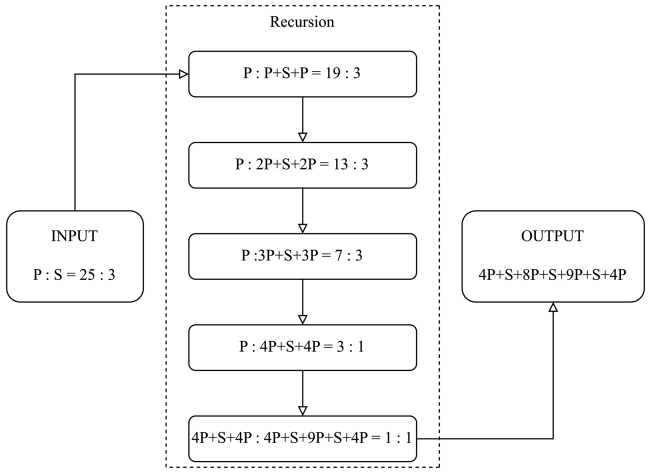

Fig. 9. Design flow of the proposed partially interleaved structure for transformers with 25:3 turns ratio.

V. PROPOSED DESIGN METHOD FOR TRANSFORMERS WITH 25:3 TURNS RATIO

A. Arrangement of the Proposed Structure

For transformers with 25:3 turns ratio, the arrangement of the proposed structure can be designed according to the design flow in Section III, as shown in Fig. 9.

The current ratio between primary-side and secondary-side is 3:25, which means that the width of primary-side winding can be less than 1/8 of secondary-side winding. Therefore, for each primary-side winding layer, there can be multiple turns of coil. The cases of five turns per layer and seven turns per layer are considered. The reason of not choosing six turns per layer case is that its number of layers is the same as five turns per layer case and there are more consecutive primary-side windings to increase the leakage inductance. The reason of choosing seven turns per layer instead of eight turns per layer is similar.

Fig. 10(a) shows the arrangement and MMF distribution of symmetric fully interleaved structure in five turns per layer case. According to the design flow shown in Fig. 3, the arrangement of the proposed partially interleaved structure in five turns per layer case is "5P-S-5P-S-5P-5P-S-5P" and the arrangement of the proposed structure in seven turns per layer case is "4P-S-7P-S-7P-S-7P," as shown in Fig. 10(b) and (c). A special arrangement of five turns per layer case is designed as shown in Fig. 10(d). Viewed from top to bottom, the special arrangement is the same as the arrangement shown in Fig. 9 ("4P-S-8P-S-9P-S-4P"), which is designed according to the design flow of proposed structure for 1 turn per layer case. In the following, these structures will be referred to as structure A, B, C, and D.

B. Leakage Inductance Calculation

As shown in Fig. 11, the proposed partially interleaved structures (Structure B, C, D) have lower leakage inductances compared to the fully interleaved structure (Structure A). Structure D with six primary-side layers has the minimal leakage inductance and structure B and C with four to five primary-side

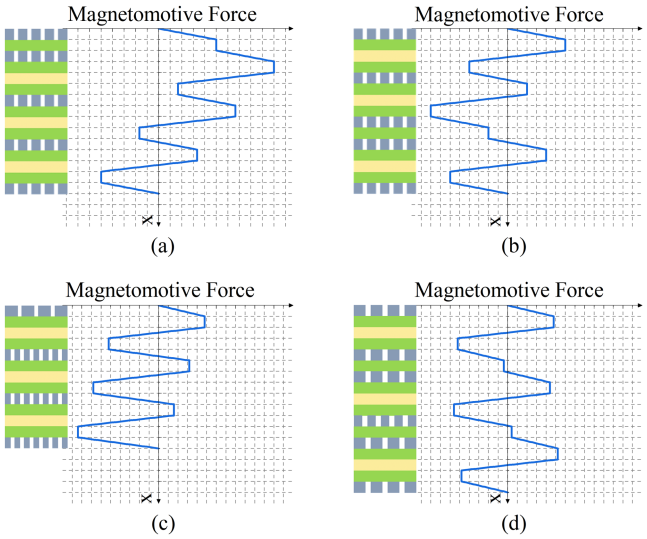

Fig. 10. Arrangements and MMF distribution of transformers with 25:3 turns ratio. (a) Symmetric fully interleaved structure with five turns per layer. (b) Proposed partially interleaved structure with five turns per layer. (c) Proposed partially interleaved structure with seven turns per layer. (d) Special proposed partially interleaved structure with five turns per layer.

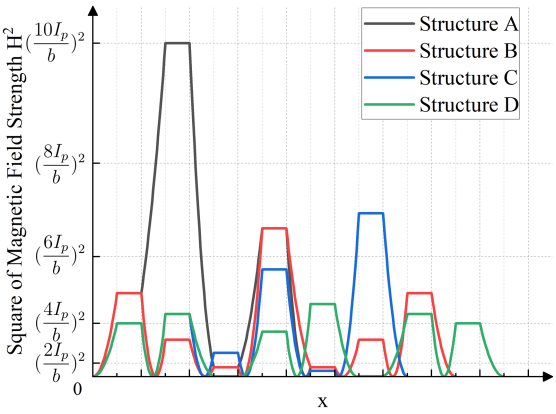

Fig. 11. Distribution of H^2 for four structures from mathematical calculation.

TABLE III
CALCULATION OF LEAKAGE INDUCTANCE

	Leakage Inductance
Structure A	$\frac{\mu_0 \cdot l}{b} \cdot \left(\frac{875}{9} h_p + \frac{175}{3} h_s + \frac{2200}{9} h_i\right)$
Structure B	$\frac{\mu_0 \cdot l}{b} \cdot \left(\frac{125}{3} h_p + 25 h_s + \frac{1100}{9} h_i\right)$
Structure C	$\frac{\mu_0 \cdot l}{b} \cdot \left(\frac{317}{9} h_p + \frac{83}{3} h_s + \frac{1123}{9} h_i\right)$
Structure D	$\frac{\mu_0 \cdot l}{b} \cdot \left(\frac{5689}{162} h_p + \frac{53}{3} h_s + 105 h_i\right)$

layers have slightly higher leakage inductances due to more consecutive primary-side windings. The calculation equations of the leakage inductances for the four structures are shown in Table III.

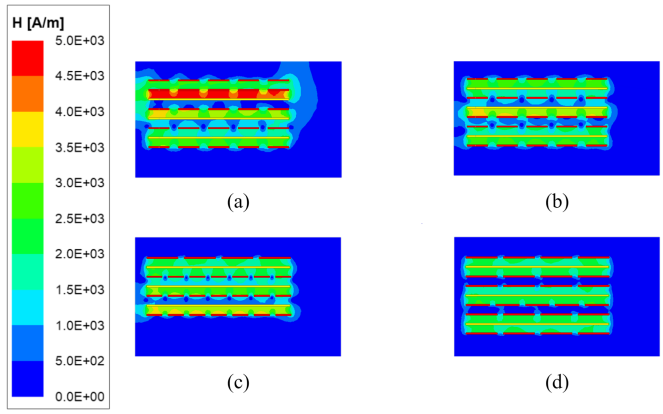

Fig. 12. Distribution of magnetic field strength H for four structures from FEA simulation. (a) Structure A. (b) Structure B. (c) Structure C. (d) Structure D.

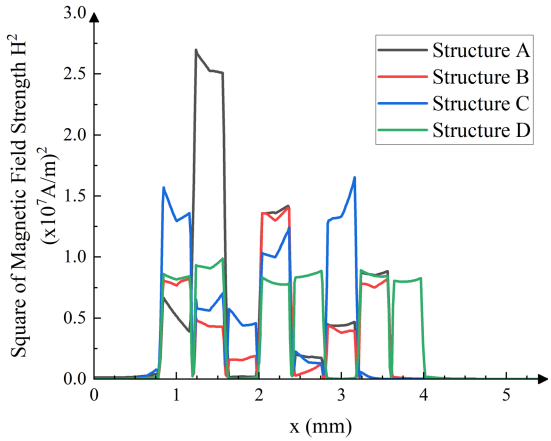

Fig. 13. Distribution of H^2 for four structures with 25:3 turns ratio from FEA simulation.

C. Finite-Element Analysis Simulation Results

The parameters of the transformer and switching frequency in simulation are the same as those in Section IV. The distribution of magnetic field strength H is shown in Fig. 12 and the $H^2 - x$ curves are shown in Fig. 13. The leakage inductance simulating value of structure A–D are 2.12, 1.28, 1.45, and 1.23 μH, respectively. The simulation results are consistent with the calculation results. For transformers with 25:3 turns ratio, the proposed structures have lower leakage inductances.

D. Design Flow for Multiple Turns Per Layer Case

Increasing the number of turns in each layer has a positive effect on reducing leakage inductance since it can reduce the value of $\int H^2 dx$ by reducing the number of layers. However, if there are more turns in each layer, there will be more consecutive windings, which may lead to a larger leakage inductance.

To design a transformer with multiple turns per layer, the first step is to arrange for 1 turn per layer case according to the design flow in Section III, and then keep the overall arrangement unchanged and increase the number of turns in each layer. This is the design flow of structure D for the transformer with 25:3

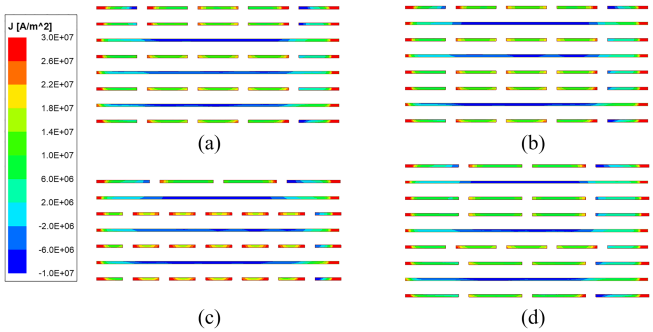

Fig. 14. Current density of four structures with 25:3 turns ratio from FEA simulation. (a) Structure A. (b) Structure B. (c) Structure C. (d) Structure D.

turns ratio, which has the minimal leakage inductance identified by the calculation and simulation results.

Sometimes for the convenience of design, the number of turns in each primary-side winding layer is set to the same. The designers should follow the design flow for 1 turn per layer case by regarding 1 layer of primary-side winding as 1 turn. This is the design flow of structure B with a slightly higher leakage inductance compared to structure D.

VI. Loss, Parasitic Capacitance, and High-Frequency Performance of the Proposed Partially Interleaved Structure

A. Loss

As the frequency increases, due to the eddy effect and the proximity effect, the current in conductors no longer homogeneously distributes, which increases the resistance of the conductors and thus increases the winding loss. The ratio between the ac resistance and dc resistance can be calculated by

$$\frac{R_{ac}}{R_{dc}} = \frac{\xi}{2} \cdot \left[\frac{\sinh(\xi) + \sin(\xi)}{\cosh(\xi) - \cos(\xi)} + (2m-1)^2 \frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) + \cos(\xi)} \right] \tag{9}$$

where $\xi = h/\delta$, h is the height of conductor, δ is the skin depth, m is given by the following:

$$m = \frac{\mathrm{MMF}(h)}{\mathrm{MMF}(h) - \mathrm{MMF}(0)}. \tag{10}$$

The winding loss of the transformers with 25:3 turns ratio were analyzed in detail. By comparing the width of conductor, the dc resistances can be obtained: $R_{\mathrm{DC},D} < R_{\mathrm{DC},A} = R_{\mathrm{DC},B} < R_{\mathrm{DC},C}$. Compared to structure A, the MMF in the proposed structure B, C, and D is significantly lower, which leads to the smaller value of m. Thus, the second term in (9) is neglectable and the first term (skin effect) plays a dominate role. The ac resistances of the four structures satisfy $R_{\mathrm{AC},D} < R_{\mathrm{AC},B} < R_{\mathrm{AC},A} < R_{\mathrm{AC},C}$. The distribution of current density in windings of the four structures is shown in Fig. 14. The current density in structure C is a bit nonuniform, which leads to its large $R_{\mathrm{AC},C}$. Furthermore, the ac resistance is simulated by FEA and the results are shown in Fig. 15. Structure C has the largest ac resistance and the ac resistance of Structure D is the lowest.

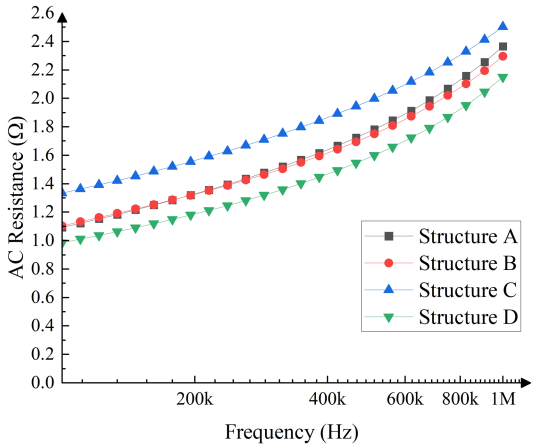

Fig. 15. AC resistances of four structures with 25:3 turns ratio from FEA simulation.

Steinmetz equation is widely used in calculating core loss as given by the following:

$$P_v = K \cdot f^{\alpha} \cdot \left(\frac{\Delta B}{2} \right)^{\beta} \tag{11}$$

where K, α, and β are parameters related to the core material, f is the switching frequency, ΔB is the peak-to-peak flux density that can be calculated by the following:

$$\Delta B = \frac{V \cdot \Delta t}{N \cdot A_e} \tag{12}$$

where $V \cdot \Delta t$ is volt-seconds, N is the number of turns, and A_e is the core section.

For a transformer with high leakage inductance, the large voltage spike caused by di/dt will increase the value of $V \cdot \Delta t$ and thus will increase the core loss. Therefore, the proposed structure with low leakage inductance will have a low core loss.

In summary, the proposed structure has lower winding loss and core loss compared to the fully interleaved structure.

B. Parasitic Capacitance

Planar transformers usually have large parasitic capacitances between primary-side and secondary-side windings (C_{ps}) due to large overlapping printed circuit board (PCB) traces. C_{ps} can be expressed by the following:

$$C_{ps} = \varepsilon_0 \, \varepsilon_r \frac{S}{h_\Delta} \tag{13}$$

where ε_0 is the permittivity of free space, ε_r is the relative permittivity of the insulator, S represents the overlapping surface area, and h_Δ is the distance between the conductive plates.

For transformers with 25:3 turns ratio, structure A has a lower parasitic capacitance compared to structure B since the distance between the top primary-side winding layer and the secondary-side layer is slightly longer. Structure C has more turns in each primary-side winding layer, which reduces the

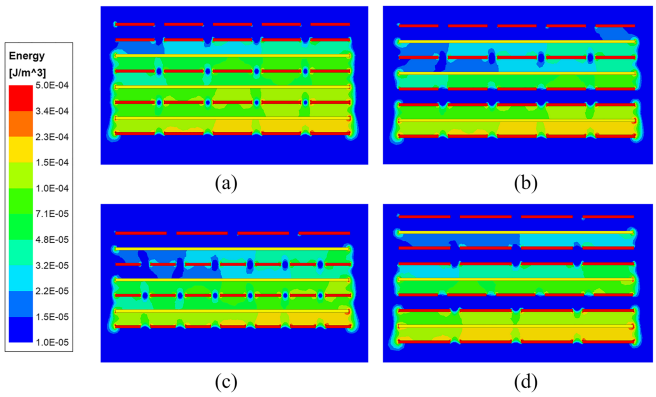

Fig. 16. Capacitive energy of four structures from FEA simulation. (a) Structure A. (b) Structure B. (c) Structure C. (d) Structure D.

TABLE IV
FEA SIMULATION RESULTS OF PARASITIC CAPACITANCE

	Parasitic Capacitance C_{ps} (pF)
Structure A	380.92
Structure B	382.37
Structure C	376.33
Structure D	386.98

overlapping surface area and thus reduces its parasitic capacitance. The parasitic capacitance of structure D is higher due to the larger overlapping surface area. The capacitive energy and the parasitic capacitances of the four structures are simulated by FEA and the results are given by Fig. 16 and Table IV. Structure C has the smallest capacitive energy in the whole space and thus has the smallest parasitic capacitance among the four structures.

The difference of the parasitic capacitance among the four structures is small for the number of intersections between the primary-side and secondary-side winding layers is the same. The difference comes from the overlapping surface area and the distance between the conductive plates. By properly arranging the winding layers, the proposed structure can even achieve lower leakage inductance and lower parasitic capacitance at the same time.

C. High-Frequency Performance of Leakage Inductance

Frequency independence of leakage inductance is critical for transformers, especially for transformers in resonant converters, where a well-matched resonant frequency is usually required. The magnetic field strength develops the "concave shape" at high frequency [10], which changes the distribution of MMF and thus reduces the leakage inductance at high frequency.

Consider the transformer with 25:3 turns ratio, the coefficients of h_p and h_s for the proposed partially interleaved structures (Structure B–D) are much smaller than symmetric fully interleaved structure's (Structure A) according to Table III. Consequently, the "concave shape" of magnetic field strength has less influence on the proposed structures.

The FEA simulation results for leakage inductance at different frequencies are shown in Table V. The leakage inductance reductions of the four structures are 42, 27, 30, and 21 nH,

TABLE V
FEA SIMULATION RESULTS OF LEAKAGE INDUCTANCE AT DIFFERENT FREQUENCY

	Leakage Inductance @100kHz	Leakage Inductance @1Mhz	Variation
Structure A	1.951 μH	1.909 μH	42 nH
Structure B	1.178 μH	1.151 μH	27 nH
Structure C	1.214 μH	1.184 μH	30 nH
Structure D	1.019 μH	0.998 μH	21 nH

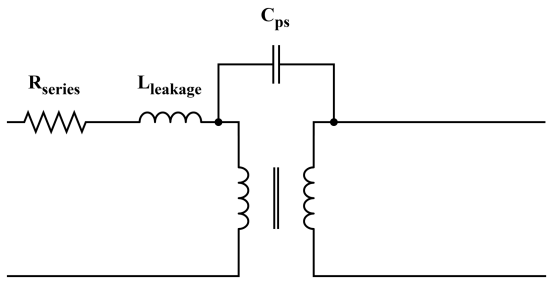

Fig. 17. Equivalent circuit model of the transformer.

respectively. The leakage inductance reductions of the proposed structures are significantly smaller than that of the symmetric fully interleaved structure. Therefore, the leakage inductance of the proposed partially interleaved structure is slightly dependent on frequency, so that the proposed structure is more suitable for high-frequency resonant converters application.

VII. EXPERIMENTAL VERIFICATIONS

Transformers with 16:12 and 25:3 turns ratio were fabricated, where the type of the planar core is EQ40/20, the core material is PC40, the copper thickness is set to 2 OZ, the layer thickness is 0.2 mm, and an insulator layer is inserted between each two winding layers to ensure the insulation of the transformer. Fig. 18 shows the physical decomposition of the transformers in the experiments. The transformers are composed of the magnetic cores and multilayer PCBs. In each multilayer PCB, different winding layers are connected with vias holes. Different PCBs are connected with pads.

Fig. 17 shows the equivalent circuit model of the transformer. Leakage inductance L_{leakage}, series resistance R_{series}, and parasitic capacitance C_{ps} were measured with an impedance analyzer and the frequencies are in the range of 100 kHz–1 MHz. Moreover, to verify the performance in realistic application, the transformers were used in an *LLC* converter with the resonant frequency of 100 kHz as shown in Fig. 18. The resonant frequency was measured to evaluate the leakage inductance of the transformers and the loss was measured at full load (200 W for transformers with 16:12 turns ratio, 100 W for transformers with 25:3 turns ratio).

A. Transformers With 16:12 Turns Ratio

For 16:12 turns ratio cases, the leakage inductances of the proposed partially interleaved structure and the fully interleaved

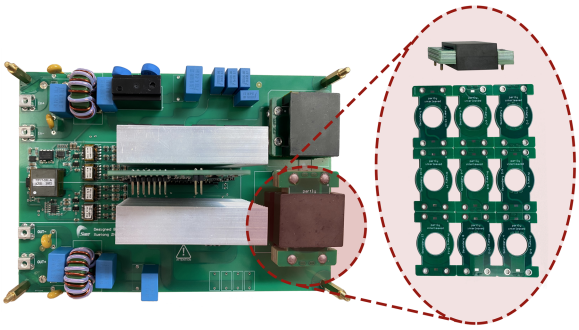

Fig. 18. Photograph of the 100 kHz *LLC* converter with the planar transformer using the proposed winding structure.

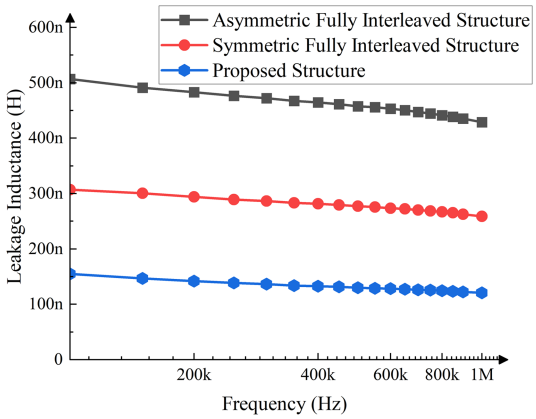

Fig. 19. Measurement values of the leakage inductance of the proposed partially interleaved structure and fully interleaved structures (Turns ratio = 16:12).

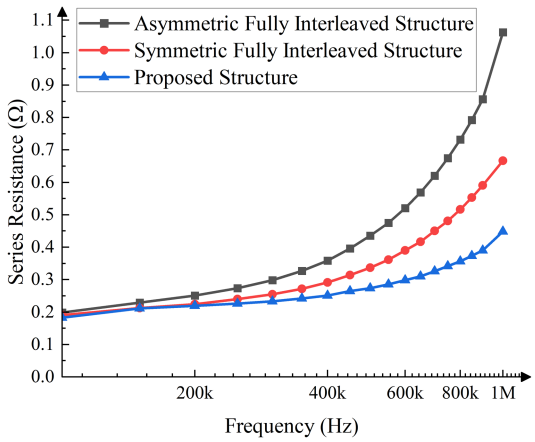

Fig. 20. Measurement values of the series resistance of the proposed partially interleaved structure and fully interleaved structures (Turns ratio = 16:12).

structures are shown in Fig. 19 and Table VI. The leakage inductance of the proposed partially interleaved structure is only 155.05 nH, which decreases 50% and 70% compared to the symmetric and asymmetric fully interleaved structure, respectively. Moreover, as the frequency increasing from 100 kHz to 1 MHz, the change of leakage inductance of the proposed structure is much small and neglectable.

The measurement values of series resistance are shown in Fig. 20. The series resistance of the proposed structure is 4% at 100 kHz and 33% at 1 MHz lower than the symmetric fully interleaved structure, respectively.

TABLE VI
EXPERIMENT RESULTS OF THE TRANSFORMERS WITH 16:12 TURNS RATIO

Structure	Asymmetric Fully Interleaved	Symmetric Fully Interleaved	Proposed Partially Interleaved
Leakage Inductance @100 kHz	507.13 nH	307.12 nH	155.05 nH
Leakage Inductance @1 MHz	428.92 nH	258.89 nH	120.72 nH
Reduction of Leakage Inductance	78.21 nH	48.23 nH	34.33 nH
Series Resistance @100 kHz	198.37 mΩ	190.68 mΩ	183.05 mΩ
Series Resistance @1 MHz	1.06 Ω	666.53 mΩ	448.57 mΩ
Parasitic Capacitance	2.15 nF	2.17 nF	2.08 nF
Resonant Frequency	96.46 kHz	98.68 kHz	99.67 kHz
Input of LLC Converter	240 V 0.891 A 213.84 W	240 V 0.890 A 213.60 W	240 V 0.888 A 213.12 W
Output of LLC Converter	181.01 V 1.1043 A 199.88 W	180.88 V 1.1034 A 199.62 W	180.27 V 1.1134 A 200.70 W
Loss of LLC Converter	13.96 W	13.98 W	12.42 W

As shown in Table VI, the parasitic capacitance measurement value of the proposed structure is the smallest and it decreases relatively 4% compared to the fully interleaved structures. Notice that the difference of parasitic capacitance is relatively slight, which is consistent with FEA simulation.

The voltage waveforms of the primary side of the transformer in the *LLC* converter are shown in Fig. 21, where no spike is observed in the voltage curves for the leakage inductances of the three structures are very small as 507.13, 307.12, and 155.05 nH compared to the resonant inductor of 27 μH.

With the increasing of the leakage inductance of main transformer, the resonant frequency of *LLC* converter will decrease due to the increasing of series inductance (L_r). As shown in Table VI, the measured resonant frequency of the *LLC* converter with the proposed structure, the symmetric, and asymmetric fully interleaved structures relatively decrease 0.33%, 1.32%, and 3.54%, respectively. These results confirm that the proposed structure has the smallest leakage inductance. The

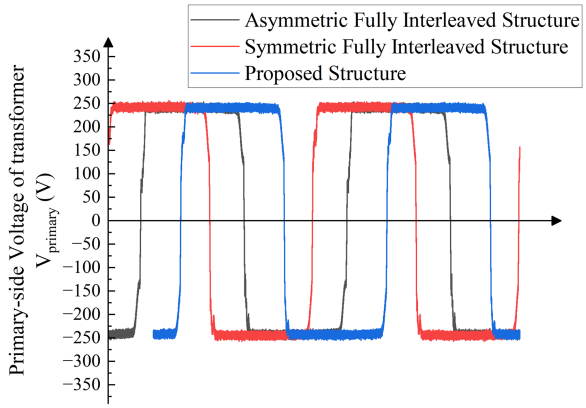

Fig. 21. Voltage waveform of the primary side of transformer in *LLC* converter (Turns ratio = 16:12).

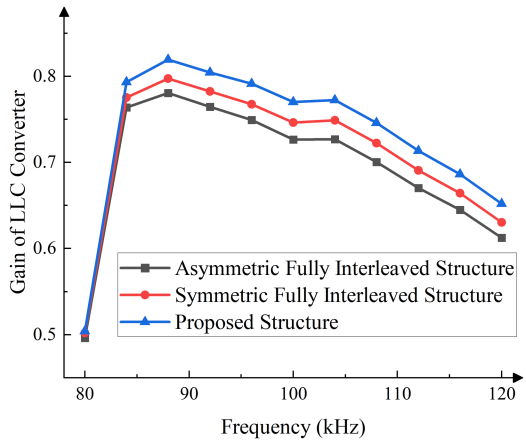

Fig. 22. Gain of the *LLC* converter with different transformers (Turns ratio = 16:12).

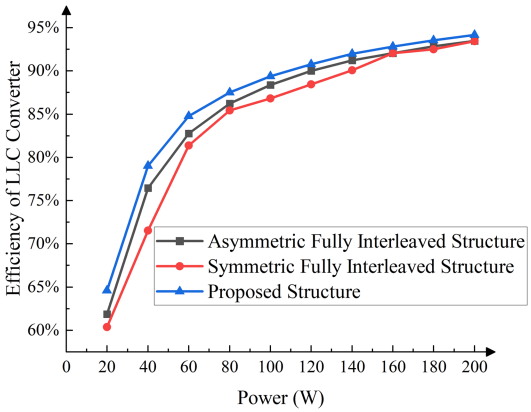

Fig. 23. Efficiency of the *LLC* converter with different transformers (Turns ratio = 16:12).

gain-frequency curves of the *LLC* converter are shown in Fig. 22. Among three structures, the proposed structure has the highest gain and the peak of its curve is closer to high frequency, which further indicates that the proposed structure has the smallest leakage inductance and the small secondary-side leakage inductance can improve the gain.

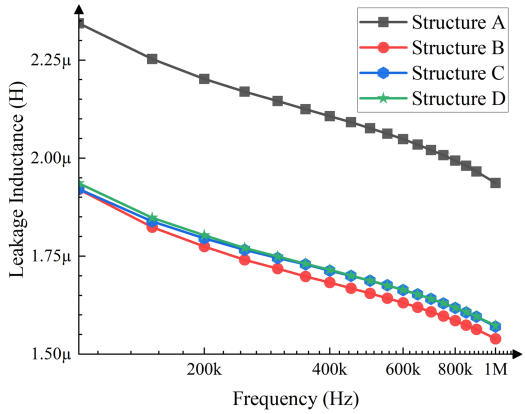

Fig. 24. Measurement values of the leakage inductance of four structures (Turns ratio = 25:3).

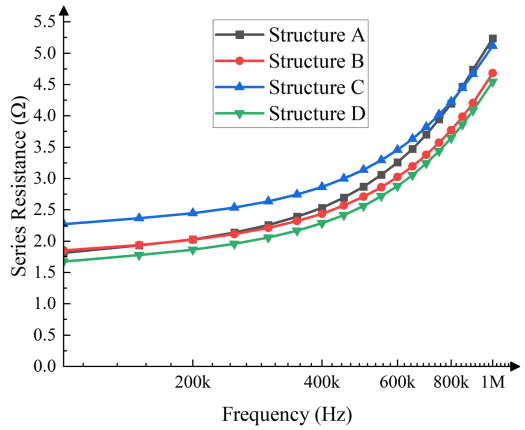

Fig. 25. Measurement values of the series resistance of four structures (Turns ratio = 25:3).

The efficiencies of the *LLC* converter are shown in Fig. 23 and the case with the proposed structure has the largest efficiency in the load range of 10% to 100%, which is consistent with the measurement results shown in Fig. 20. The measurement values of loss are shown in Table VI. The proposed structure has the smallest value of 12.42 W.

In summary, for transformers with 16:12 turns ratio, the proposed structure performs better in leakage inductance, loss and parasitic capacitance.

B. Transformers With 25:3 Turns Ratio

Four transformers with 25:3 turns ratio mentioned in Section V are experimentally analyzed and the measurement results are shown in Figs. 24 and 25 and Table VII.

The leakage inductance of the proposed structures (structures B, C, D) is about 20% lower than that of structure A and structure B has the smallest value. With the increasing of frequency, the reductions of leakage inductance for structures B, C, and D are smaller than structure A, which indicates that the proposed structures are less sensitive to frequency variation. The leakage inductance of structure C is the most insensitive to frequency.

TABLE VII
EXPERIMENT RESULTS OF THE TRANSFORMERS WITH 25:3 TURNS RATIO

Structure	A	B	C	D
Leakage Inductance @100 kHz	2.34 μH	1.92 μH	1.92 μH	1.94 μH
Leakage Inductance @1 MHz	1.94 μH	1.54 μH	1.57 μH	1.57 μH
Reduction of Leakage Inductance	0.40 μH	0.38 μH	0.35 μH	0.37 μH
Series Resistance @100 kHz	1.82 Ω	1.85 Ω	2.27 Ω	1.68 Ω
Series Resistance @1 MHz	5.24 Ω	4.68 Ω	5.12 Ω	4.54 Ω
Parasitic Capacitance	432.2 pF	447.4 pF	417.9 pF	504.5 pF
Resonant Frequency	94.94 kHz	95.85 kHz	95.85 kHz	96.15 kHz
Input of LLC Converter	240 V 0.435 A 108.8 W	240 V 0.433 A 108.3 W	240 V 0.435 A 108.8 W	240 V 0.434 A 108.5 W
Output of LLC Converter	29.38 V 3.418 A 100.4 W	29.21 V 3.438 A 100.4 W	29.16 V 3.432 A 100.1 W	29.22 V 3.439 A 100.5 W
Loss of LLC Converter	8.32 W	7.85 W	8.70 W	8.00 W

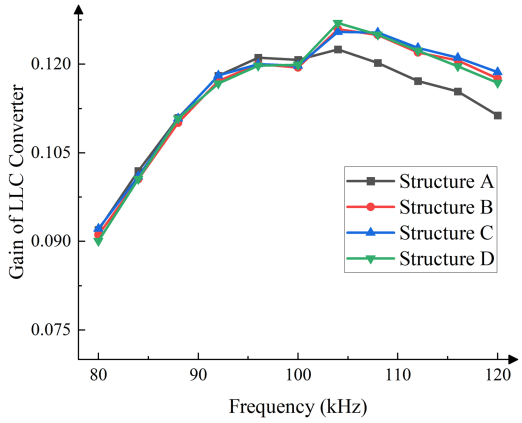

Fig. 26. Gain of the *LLC* converter with different transformers (Turns ratio = 25:3).

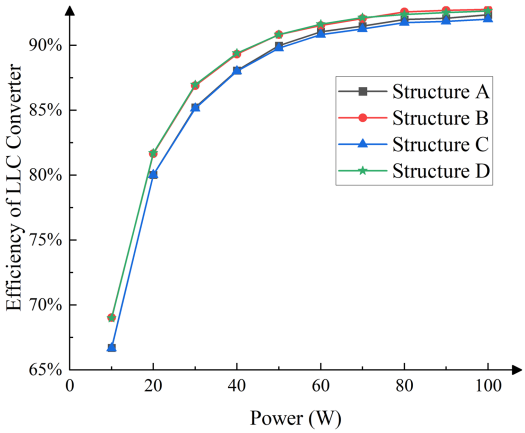

Fig. 27. Efficiency of the *LLC* converter with different transformers (Turns ratio = 25:3).

The series resistance of structure D decreases 8% compared to that of structure A. The series resistance of structure C is the largest at 100 kHz, but is lower than structure A at 1 MHz.

As for the parasitic capacitance, the measurement value for structure C is the smallest, and the difference between structures A, B, and C is only 30 pF. These measurement values of parasitic capacitances are consistent with the FEA simulation results, which indicates that the differences are mainly determined by the width of the coils.

As for the change in resonant frequency of the *LLC* converter, structure A has the largest change of 5.06% and structure D has the smallest change (3.85%). The gain-frequency curves are given by Fig. 26. The peak of the curves of structure B, C, and D are higher and are closer to high frequency, which confirms that the proposed structures have larger gain and smaller change of resonant frequency due to their smaller leakage inductance.

When structure B is adopted in the 100 W *LLC* converter, the loss can be reduced at least 9.4%. Besides, *LLC* converters with structures B and D have higher efficiency as shown in Fig. 27, which is consistent with the measurement results of series resistance.

In summary, for transformer with 25:3 turns ratio, the proposed structures perform better in leakage inductance and loss. Each structure of the proposed structures has its own advantages in leakage inductance, loss or parasitic capacitance.

C. Error Analysis

The PCB of the planar transformer tested is made by attaching multiple multilayer boards and the actual thickness of the insulator layer is slightly higher due to imperfect board-to-board bonding, which can increase the leakage inductance.

Besides, different layers of PCB are connected with vias holes, which may change the distribution of the magnetic field. Therefore, the actual leakage inductance is slightly different from the expectation. To test the error caused by the manufacturing process, for each kind of winding structure, three transformers are manufactured. As shown in Fig. 28, even with the inevitable error, the proposed structure still has a significant advantage in leakage inductance.

When measuring the leakage inductance by the impedance analyzer, the wire used to short the secondary-side winding will inevitably introduce additional inductance and increase the error. Therefore, the wire for short circuit should be as short as possible and the same length of wire should be used when measuring the leakage inductance of different structures.

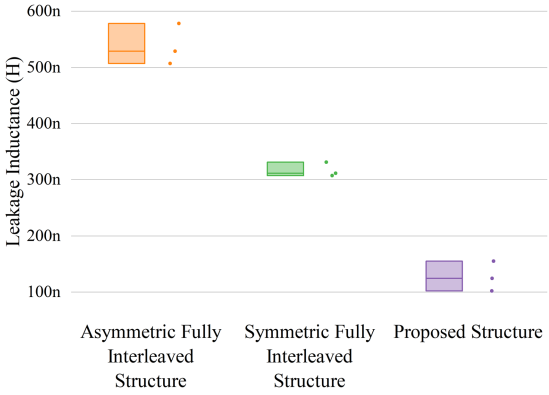

Fig. 28. Measurement values of the leakage inductance of transformers with 16:12 turns ratio at 100 kHz.

VIII. Conclusion

A design method of partially interleaved structure planar transformer with arbitrary turns ratio is proposed to minimize the leakage inductance. If $N_p > N_s + 1$, the proposed structure will be a combination of two subgroups. The arrangement of each subgroup is "PSPS …" to guarantee minimal leakage flux. Then regarding the two subgroups as new primary-side and secondary-side windings to further partially interleave and recurse to achieve a partially interleaved structure with the minimal leakage inductance. The design flow for 1 turn per layer case and multiple turns per layer case is illustrated and its superiority is proved mathematically in this article. Transformers with 16:12 turns ratio and 25:3 turns ratio are analyzed, simulated, and tested to validate the proposed design method. For transformers with 16:12 turns ratio, the leakage inductance of the proposed structure is 50% lower than the fully interleaved structures for frequencies in the range of 100 kHz to 1 MHz. For transformers with 25:3 turns ratio, the leakage inductances of the proposed structures are about 18% less than that of the fully interleaved structure. The leakage inductances of the proposed structures are independent on frequency, especially the proposed structure with 16:12 turns ratio. In addition, the series resistance and the parasitic capacitance of the proposed structure also decrease compared to the fully interleaved structures. The proposed structures are used in a 100 kHz *LLC* converter and the change of resonant frequency and the loss are in consistent with the measurement results of leakage inductance and series resistance.

In general, except for considering special structures like half-turn structure, the proposed partially interleaved structure with the minimal leakage inductance, the minimal loss, and the best frequency-independence can be achieved based on the proposed design method.

Appendix

A. Pseudocode of the Proposed Structure

See Algorithm 1.

Algorithm 1: Pseudocode of the proposed partially interleaved structure in Python style.

Input: the number of primary-side turns (N_p),
the number of secondary-side turns (N_s),
the arrangement of turns in primary-side layer (p),
the arrangement of turns in secondary-side layer (s);
(p and s are in string format)
Output: the arrangement of the proposed structure

```
def getArrangement(N_p, N_s, p, s):
    if N_p < N_s:
        return getArrangement(N_s, N_p, s, p)
    if N_s == 0:
        return N_p*p
    n = N_p - N_s
    if n ≤ 1:
        return p + s + p + s + ...
    n_p1 = int(N_p/n)
    n_s1 = int(N_s/n)
    n_p2 = n_p1 + 1
    n_s2 = n_s1 + 1
    n_2 = N_p %n
    n_1 = n − n_2
    # Get arrangement of (n_p1 : n_s1)
    p_new = p + s + p + s + ...
    # Get arrangement of (n_p2 : n_s2)
    s_new = p + s + p + s + ...
    return getArrangement(n_1, n_2, p_new, s_new)
# Print the arrangement of 16:12 case as an example
print(getArrangement(16, 12, "P", "S"))
# Output: "PSPSPSPPSPSPSPPSPSPSPPSPSPSP"
```

B. Design Files of the Transformers Tested in Experiment

The PCB design files have been uploaded to https://ieee-dataport.org/10025.

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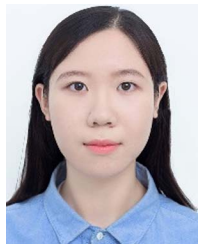

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