A Class of Bidirectional Single-Phase Z-Source AC–AC Converter With Continuous Input Current and Reduced Component Count

Seyyed Mohammad Javad Mousavi, Ebrahim Babaei, *Senior Member, IEEE*, Mehran Sabahi, and Hasan Komurcugil, *Senior Member, IEEE*

***Abstract*—In this article, a class of single-phase Z-source ac–ac converters is proposed. Share ground and continuous input current are the common features of the proposed converters. The proposed converters have unique features that differentiate them from their counterparts. These features include the buck operation in both in-phase and out-of-phase mode, being bidirectional, the minimum component counts, the ability to boost without duty cycle limitation, and reducing total power rating of switches is known as switching device power (SDP) parameter. Reducing SDP leads to a reduction in the voltage and current rating of the semiconductors and converter cost. A safe commutation strategy is applied to eliminate voltage and current spikes on the switches. The experimental results verify the performance of the laboratory prototype of the proposed converters.**

***Index Terms*—AC–AC converter, buck in-phase operation, continuous input current, safe commutation strategy, shared ground, Z-source.**

I. Introduction

ONE of the main purposes of ac–ac converters is to change the constant voltage of the network for applications, such as lighting adjustment, motor drives, etc. AC–AC converters can be divided into matrix converters [1], [2], [3], two-stage (ac–dc–ac) converters [4], [5], and direct pulsewidth modulation (PWM) converters [6], [7]. Matrix converters and ac–dc–ac converters can change the output voltage and frequency. In applications such as dynamic voltage restorer (DVR) [8] and solid-state transformers (SST) [9] where only voltage amplitude adjustment is required, direct PWM converters are considered a more suitable option, due to easier control, and higher efficiency. The buck, boost, and buck–boost type PWM ac–ac converters are obtained from conventional dc–dc converters, employing bidirectional switches instead of unidirectional switches [10]. Z-source ac–ac converters with unique features have drawn more attention [11]. Z-source inverter (ZSI) was first introduced in 2003 by Peng [12].

Subsequently, the traditional Z-source ac–ac converter (TZSC) was introduced in 2005 [13]. This converter can operate in both boost in-phase and buck out-of-phase. However, TZSC suffers from discontinuous input current, lack of shared ground, and the need for a snubber circuit. In [14], by implementing a safe commutation strategy, using a snubber circuit is eliminated. But its input current is discontinuous. The quasi Z-source converter (QZSC) [15] solves the problems of conventional Z-source converter with continuous input current and common ground. In modified QZSC (MQZSC) [16], by using the filtering property of the impedance network, the load is connected directly to it without an output filter. As a result, MQZSC saves one inductor and one capacitor. Although TZSC, QZSC, and MQZSC have various topologies, they have the same voltage gain ($1-D/1-2D$). In parallel, with the advances made in transformer-based ZSIs [17], an ac–ac Z-source converter based on a transformer was first introduced in 2015 [18]. Trans-ZSCs have two types of isolated [19], [20] and nonisolated [21], [22], [23], [24]. By changing the transformer's turn ratio and duty cycle, T-ZSC [18] and $\Gamma-$ ZSC [21] canproduce a wide range of output voltages. However, [21] has a discontinuous input current and requires an *LC* input filter. Both Trans-Z-source converters presented in [18] and [22] have a similar structure, except that the output filter inductor in [22] has been removed and replaced with a bidirectional switch. The effect of this change is an improvement in voltage gain and an increase in efficiency compared to [18]. In [23], like MQZSC, the load is connected directly to the impedance network. Due to eliminating the output filter, the efficiency increases and the volume and weight of the converter reduces. The converters presented in [24] have two coupled inductors. Although these converters have a high-voltage gain, they still have an output *LC* filter.

However, the single-phase Z-source converters are a good choice for voltage amplitude regulating, but existing Z-source-based DVRs faced some drawbacks that limited their application, like lack of compensation for voltage sag less than 50% [25], lack of compensation for voltage swell [26], and need the extra switches [27]. The origin of all

Manuscript received 15 April 2022; revised 13 August 2022 and 6 November 2022; accepted 27 December 2022. Date of publication 10 January 2023; date of current version 10 March 2023. Recommended for publication by Associate Editor J. Itoh. *(Corresponding author: Ebrahim Babaei.)*

Seyyed Mohammad Javad Mousavi and Mehran Sabahi are with the Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666, Iran (e-mail: smj_mousavi@tabrizu.ac.ir; sabahi@tabrizu.ac.ir).

Ebrahim Babaei is with the Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666, Iran, and also with the Engineering Faculty, Near East University, 99138 Nicosia, North Cyprus, Mersin 10, Turkey (e-mail: e-babaei@tabrizu.ac.ir).

Hasan Komurcugil is with the Computer Engineering Department, Eastern Mediterranean University, 99628 Famagusta, Turkey (e-mail: hasan.komurcugil@emu.edu.tr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3235892.

Digital Object Identifier 10.1109/TPEL.2023.3235892

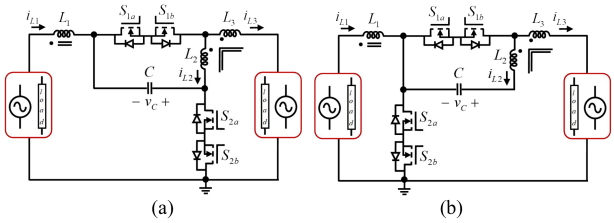

Fig. 1. Proposed bidirectional Z-source AC–AC converters. (a) Topology-1 (load at the right) and topology-2 (load at the left). (b) Topology-3 (load at the right) and topology-4 (load at the left).

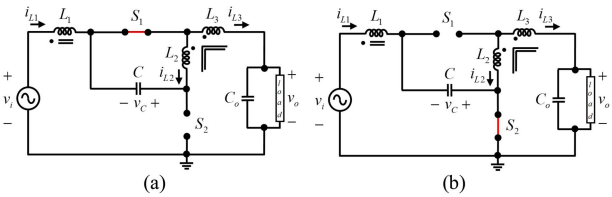

Fig. 2. Equivalent circuits of topology-1. (a) NST interval. (b) ST interval.

these drawbacks is the lack of buck in-phase operation in the ZSC.

In this article, two bidirectional structures are proposed. The common properties of the proposed converters are shared ground, continuous input current, and minimum component count. In addition, buck in-phase operation and lowering SDP are the unique features of some proposed converters.

II. Proposed Converters

The topologies of the proposed converters are shown in Fig. 1. All proposed converters consist of two capacitors, two bidirectional switches, a three-winding coupled inductor, and the load.

The proposed converters have two operating modes. In analyzing the proposed converters, the following assumptions are considered: 1) the converter operates in continuous conduction mode, 2) all elements are ideal, and 3) the secondary tertiary to primary winding ratios are indicated by n_1 and n_2, respectively.

A. Analysis of Topology-1

The equivalent circuit of NST state is shown in Fig. 2(a). In this operation mode, S_1 is ON, while S_2 is OFF. By applying KVL and KCL in this mode, the following equations are obtained:

$$v_{L1} = \frac{1}{n_2+1}(v_i - v_o) \tag{1}$$

$$i_C = i_{Ls1} \tag{2}$$

$$i_{Co} = i_i - \frac{v_o}{R}. \tag{3}$$

The equivalent circuit of ST state is shown in Fig. 2(b). In this operation mode, S_1 is OFF, while S_2 is ON. By applying KVL and KCL in this mode, the following equations are obtained:

$$v_{L1} = v_i + v_C \tag{4}$$

$$i_C = i_i \tag{5}$$

TABLE I
Key Relationships of Proposed Converters

		Topology-1	Topology-2	Topology-3	Topology-4
V_o		$\frac{1\text{-D}}{1\text{-}(n_1+1)\text{D}}\text{V}_\text{i}$	$\frac{1\text{-}(n_1+1)\text{D}}{1\text{-D}}\text{V}_\text{i}$	$\frac{1+n_2\text{D}}{1\text{-D}}\text{V}_\text{i}$	$\frac{1\text{-D}}{1+n_2\text{D}}\text{V}_\text{i}$
V_C		$\frac{n_1\text{D}}{1\text{-}(n_1+1)\text{D}}\text{V}_\text{i}$	$\frac{n_1\text{D}}{1\text{-D}}\text{V}_\text{i}$	$\frac{n_1\text{D}}{1\text{-D}}\text{V}_\text{i}$	$\frac{n_1\text{D}}{1+n_2\text{D}}\text{V}_\text{i}$
I_i		$\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$
I_{Lm}		$\frac{n_1}{1\text{-D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{n_1}{1\text{-}(n_1+1)\text{D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{n_1}{1+n_2\text{D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{n_1}{1\text{-D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$
V_{S-max}	V_{S1}	$\frac{\sqrt{2}n_1}{1\text{-}(n_1+1)\text{D}}\text{V}_\text{i}$	$\frac{\sqrt{2}n_1}{1\text{-D}}\text{V}_\text{i}$	$\frac{\sqrt{2}n_1}{1-\text{D}}\text{V}_\text{i}$	$\frac{\sqrt{2}n_1}{1+n_2\text{D}}\text{V}_\text{i}$
	V_{S2}	$\frac{\sqrt{2}}{1\text{-}(n_1+1)\text{D}}\text{V}_\text{i}$	$\frac{\sqrt{2}}{1\text{-D}}\text{V}_\text{i}$	$\frac{\sqrt{2}}{1\text{-D}}\text{V}_\text{i}$	$\frac{\sqrt{2}}{1+n_2\text{D}}\text{V}_\text{i}$
I_{S-max}	I_{S1}	$\frac{\sqrt{2}}{1\text{-D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\sqrt{2}}{1\text{-}(n_1+1)\text{D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\sqrt{2}}{1+n_2\text{D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\sqrt{2}}{1\text{-D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$
	I_{S2}	$\frac{\sqrt{2}n_1}{1\text{-D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\sqrt{2}n_1}{1\text{-}(n_1+1)\text{D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\sqrt{2}n_1}{1+n_2\text{D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$	$\frac{\sqrt{2}n_1}{1\text{-D}}\frac{\text{P}_\text{o}}{\text{V}_\text{i}}$

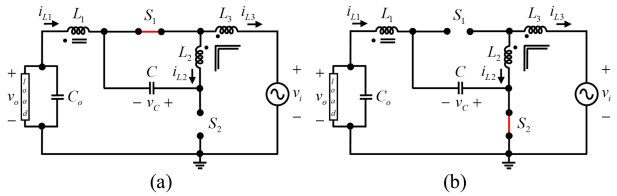

Fig. 3. Equivalent circuits of topology-2. (a) NST interval. (b) ST interval.

$$i_{Co} = i_{L3} - \frac{v_o}{R}. \tag{6}$$

By applying the voltage balance law to the primary winding and the current balance law to the capacitors, the voltage gain and other main relationships are calculated as follows:

$$G = \frac{v_o}{v_i} = \frac{(n_1-n_2)(1-D)}{n_1-n_2-(n_1+1)D} \tag{7}$$

$$v_C = \frac{n_1 D}{1-(n_1+1)D} v_i \tag{8}$$

$$I_{in} = \frac{n_1-n_2-D(n_1+1)}{n_1-n_2-D(2n_1-n_2)}\frac{P_o}{V_i} \tag{9}$$

$$I_{Lm} = \frac{n_2+1-D(1+n_2-n_1)}{1-D} I_{\text{in}}. \tag{10}$$

Using (9) and assuming $n_1 - n_2 = 1$, the simplified relationships above are presented in Table I.

B. Analysis of Topology-2

The equivalent circuit of the NST state is shown in Fig. 3(a). By applying KVL in this operating mode, the voltage across the primary winding is obtained as follows:

$$v_{L1} = \frac{1}{n_2+1}(v_o - v_i). \tag{11}$$

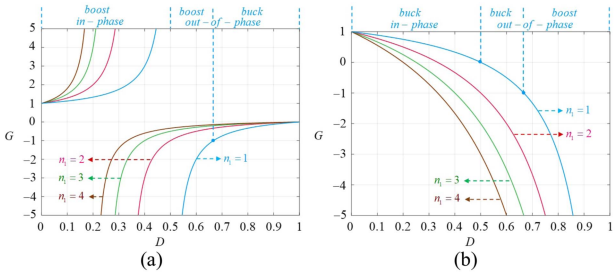

Fig. 4. Voltage gain versus the duty cycle for various conversion ratios. (a) Topology-1. (b) Topology-2.

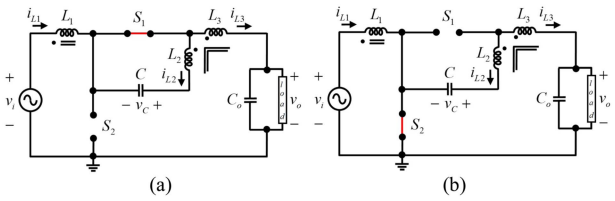

Fig. 5. Equivalent circuits of topology-3. (a) NST interval. (b) ST interval.

The equivalent circuit of the ST state is shown in Fig. 3(b). By applying KVL in this operating mode, the voltage across the primary winding is obtained as follows:

$$v_{L1} = v_o + v_C. \tag{12}$$

By applying the voltage balance law on the primary winding and using (11) and (12), the voltage gain of the proposed topology-2 is calculated

$$G = \frac{1-(n_1+1)D}{1-D}. \tag{13}$$

Fig. 4(a) shows the voltage gain in terms of the duty cycle of topology-1 for various turn ratios. In Fig. 4(b), the voltage gain versus duty cycle of topology-2 for various turn ratios.

C. Analysis of Topology-3

The equivalent circuit of the NST state is shown in Fig. 5(a). Applying KVL to the equivalent circuit can be written

$$v_{L1} = \frac{1}{n_2+1}(v_i - v_o). \tag{14}$$

The equivalent circuit of the ST state is shown in Fig. 5(b). Applying KVL to the equivalent circuit can be written

$$v_{L1} = v_i. \tag{15}$$

By applying the voltage balance law on the primary winding and using (14) and (15), the voltage gain of the proposed topology-3 is calculated

$$G = \frac{1+n_2D}{1-D}. \tag{16}$$

D. Analysis of Topology-4

The equivalent circuit of the NST state is shown in Fig. 6(a). Applying KVL to the equivalent circuit can be written

$$v_{L1} = \frac{1}{n_2+1}(v_o - v_i). \tag{17}$$

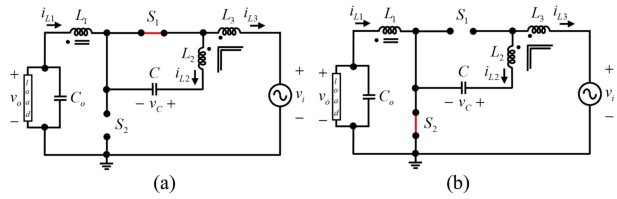

Fig. 6. Equivalent circuits of topology-4. (a) NST interval. (b) ST interval.

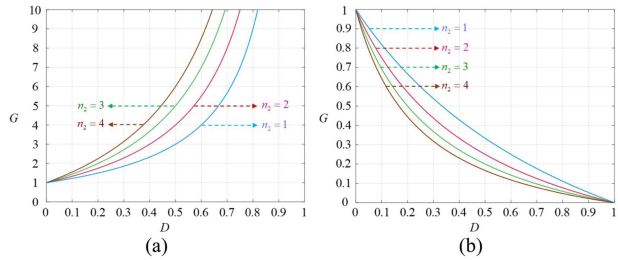

Fig. 7. Voltage gain versus the duty cycle for various conversion ratios. (a) Topology-3. (b) Topology-4.

The equivalent circuit of the ST state is shown in Fig. 6(b). Applying KVL in the equivalent circuit can be written

$$v_{L1} = v_o. \tag{18}$$

Using (17) and (18), and applying the voltage balance law on L_1, the voltage gain of topology-4 is calculated

$$G = \frac{1-D}{1+n_2D}. \tag{19}$$

Table I includes the voltage gain, voltage across the capacitor, input current, magnetizing current, and the maximum voltage and current of bidirectional switches of the proposed converters. The voltage gain of topologies-3 and 4 for various turn ratios are plotted in Fig. 7.

E. Switching Strategy of Proposed Converters

All proposed converters have two bidirectional switches. In practice, due to the nonideal characteristics of switches, an undesirable transient interval may occur.

In [12], to solve the commutation problem, a snubber circuit has been used for each of switches. Using snubber causes permanent losses and reduces the efficiency. Another solution is implementing a safe commutation strategy. In the proposed converters, a safe commutation strategy is adopted to provide the flow path of the current windings at dead times. In the investigation carried out for the proposed converters, the input voltage is positive ($v_i > 0$), and the converter is at the end of the ST interval. Applying KCL in the topology-1 circuit, it can be written as

$$i_{L1} + i_C = i_{S1} \tag{20}$$

$$i_C = i_{S2} + i_{L2}. \tag{21}$$

By replacing (20) with (21), it can be written as

$$i_{L1} + i_{L2} = i_{S1} - i_{S2}. \tag{22}$$

The equivalent circuit of the topology-1 in ST state is shown in Fig. 8(a). As soon as S_{2a} is turned ON, the sum of v_i and

TABLE II
COMPARISON OF THE PROPOSED CONVERTERS AND THE OTHER Z-SOURCE CONVERTERS

Ref.		[16]	[18]	[21]	[22]	[24]	[23]	Topology-1	Topology-3
Component Counts ($L^1/CL^2/C^3/S^4$)		2/-/2/4	2/1*2*w*/3/4	2/1*2*w*/3/4	1/1*2*w*/3/6	1/2*2*w*/3/4	1/1*2*w*/2/4	-/1*3*w*/2/4	-/1*3*w*/2/4
Shared ground		✓	✓	✓	✓	✓	✓	✓	✓
Continuous Input Current		✓	✓	×	✓	✓	✓	✓	✓
(Input or output) Filter		-	O	I/O	-	O	-	-	-
$D(G)$		$\frac{G-1}{2G-1}$	$\frac{G-1}{G(n+2)-1}$	$\frac{G-1}{G\left(\frac{n}{n-1}\right)-1}$	$\frac{G-1}{G(n+2)}$	$\frac{G-1}{G(n_1+n_2+2)-1}$	$\frac{G-1}{G\left(\frac{2n-1}{n-1}\right)-1}$	$\frac{G-1}{G(n_1+1)-1}$	$\frac{G-1}{G+n_2}$
$I_{S-\max}$	I_{S1}	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\sqrt{2}(n+2)\frac{P_o}{V_i}$	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}}{1+n_2D}\frac{P_o}{V_i}$
	I_{S2}	$\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}(n+1)}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}[2n(1-D)-1]}{(1-D)(n-1)}\frac{P_o}{V_i}$	$\frac{\sqrt{2}[1-D(n+2)]}{1-D}\frac{P_o}{V_i}$ $\frac{\sqrt{2}}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}(n_1+n_2+1)}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}n}{(1-D)(n-1)}\frac{P_o}{V_i}$	$\frac{\sqrt{2}n_1}{1-D}\frac{P_o}{V_i}$	$\frac{\sqrt{2}n_1}{1+n_2D}\frac{P_o}{V_i}$
$V_{S-\max}$	V_{S1}	$\frac{\sqrt{2}}{1-2D}$	$\frac{\sqrt{2}(n+1)}{1-D(n+2)}V_i$	$\frac{\sqrt{2}}{n(1-D)-1}V_i$	$\frac{\sqrt{2}}{1-D(n+2)}V_i$	$\frac{\sqrt{2}(n_1+n_2+1)}{1-D(n_1+n_2+2)}V_i$	$\frac{\sqrt{2}n}{(n-1)-D(2n-1)}V_i$	$\frac{\sqrt{2}n_1}{1-(n_1+1)D}V_i$	$\frac{\sqrt{2}n_1}{1-D}V_i$
	V_{S2}	$\frac{\sqrt{2}}{1-2D}$	$\frac{\sqrt{2}}{1-D(n+2)}V_i$	$\frac{\sqrt{2}(n-1)}{n(1-D)-1}V_i$	$\frac{\sqrt{2}(n+1)}{1-D(n+2)}V_i$	$\frac{\sqrt{2}}{1-D(n_1+n_2+2)}V_i$	$\frac{\sqrt{2}(n-1)}{(n-1)-D(2n-1)}V_i$	$\frac{\sqrt{2}}{1-(n_1+1)D}V_i$	$\frac{\sqrt{2}}{1-D}V_i$
$\frac{SDP_{peak}(G)}{P_o}$		$\frac{4(2G-1)^2}{G}$	$\frac{4(G(n+2)-1)^2}{G(n+1)}$	$\frac{4n(nG-n+1)}{n-1}$	$\frac{[2G(n+2)]^2+2G(n+2)}{G(n+1)+1}$	$\frac{4[G(n_1+n_2+2)-1]^2}{G(n_1+n_2+1)}$	$\frac{4[(2n-1)G-n+1]^2}{n(n-1)G}$	$\frac{4[G(n_1+1)-1]^2}{Gn_1}$	$\frac{4(G+n_2)^2}{G(n_2+1)}$
Numerical example (G=5, n=1.5)		64.8	87.12	84	93.33	115.12	96.26	70.53	13.52

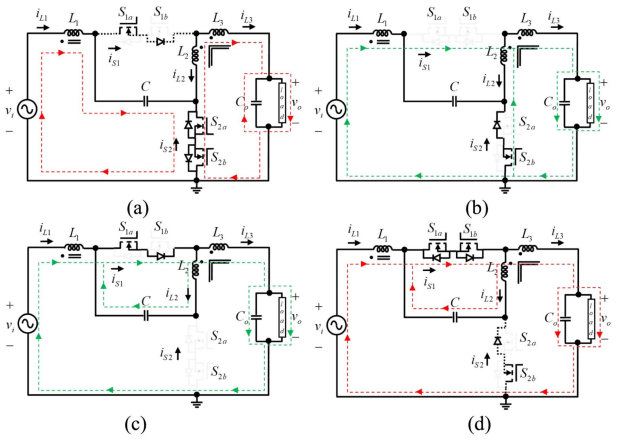

Fig. 8. Commutation states in topology-1 when $v_i > 0$. (a) Shoot-through state. (b) Commutation state I if $i_{L1} + i_{L2} < 0$. (c) Commutation state II if $i_{L1} + i_{L2} > 0$. (d) Non-shoot-through state.

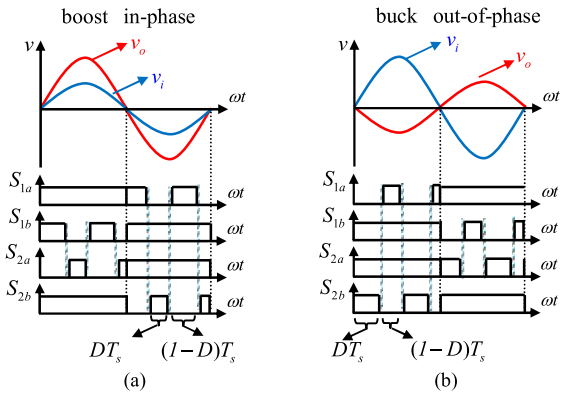

Fig. 9. Switching pattern of the proposed converter with safe commutation strategy. (a) Boost in-phase mode. (b) Buck out-of-phase mode.

v_C is put across L_1. According to the current direction of the windings, there will be two possible situations: Commutation state I) if $i_{L1} + i_{L2} < 0$, according to (22), the S_{2b} provides the current path for L_2 and the load and prevents its sudden change. The S_{1a} also provides a current path for L_1 and prevents it from being cut off. This commutation situation is shown in Fig. 8(b). Commutation state II) if $i_{L1} + i_{L2} > 0$, according to (22), S_{1a} provides a proper path for L_2 current, as shown in Fig. 8(c). At the end of the dead-time interval, the NST state begins, in which equivalent circuit is shown in Fig. 8(d).

The switching pattern of topology-1 in both buck and boost operating modes is shown in Fig. 9.

III. PARAMETER DESIGN OF THE PROPOSED CONVERTERS

A. Passive Element Design

The parametric design is presented for topology-1. The following relationships are obtained based on $\Delta t = DT_S$. The

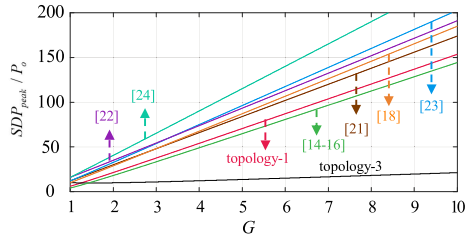

Fig. 10. Normalized SDP versus voltage gain.

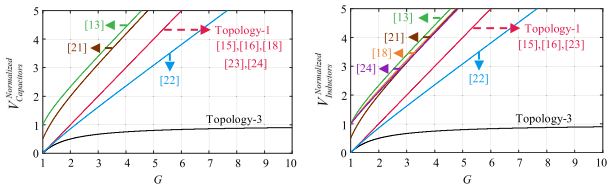

Fig. 11. Normalized total volume metric of the proposed converters and other Z-source AC–AC converters (a) for capacitors and (b) for inductors.

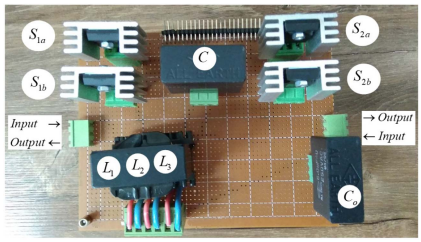

Fig. 12. Laboratory prototype of proposed converters.

TABLE III
PARAMETERS USED IN EXPERIMENT

V_i	L_m	C	C_o	f_S	Turn ratios	D
$100V_{peak}$	$410uH$	$4.5\,\mu F$	$6\,\mu F$	$30\,kHz$	1:2:1	0.15 0.6
Inductive load		*Non-linear load*				
$50\Omega + j15.7\Omega$		*Diode Bridge* $C = 470\,\mu F$ $R = 50\Omega$				
Elements		Part Number				
Switches		SiHG20N50C				
Magnetic core		EE 42 ferrite core				
Capacitors		All Earth				

minimum value of the inductor is calculated by following equation:

$$L_m = \frac{|V_{Lm}|\,\Delta t}{\Delta I_{Lm}} \tag{23}$$

where ΔI_{Lm} is the magnetizing inductor current ripple. The allowable current ripple of L_m is considered as $\Delta I_{Lm} = x_{Lm}\%I_{Lm}$. According to Table I and (23), the minimum value of L_m is obtained

$$L_m \geq \sqrt{2}\frac{D(1-D)^2}{n_1\,[1-(n_1+1)D]}\frac{V_i^2}{x_{Lm}\%f_S P_o}. \tag{24}$$

The minimum value of the capacitor is calculated by following equation:

$$C = \frac{|I_C|\,\Delta t}{\Delta V_C} \tag{25}$$

where ΔV_c is the capacitor voltage ripple. The allowable voltage ripple of the capacitors is considered as $\Delta V_C = y\,\%V_C$. According to Table I and (25), the minimum value of C and C_o are obtained

$$C \geq \sqrt{2}\frac{1-(n_1+1)D}{n_1}\frac{P_o}{y_C\%f_S V_i^2} \tag{26}$$

$$C_o \geq \sqrt{2}\frac{n_1 D\,[1-(n_1+1)D]}{1-D}\frac{P_o}{y_{Co}\%f_S V_i^2}. \tag{27}$$

B. Magnetic Core Selection and Design

In order to select the appropriate magnetic core, a step-by-step method is presented in [28]. In the first step, the geometrical constant of the core (K_g) for the coupled inductor of the proposed converter is calculated, which is defined as

$$K_g = \frac{A_C^2 W_A}{\text{MLT}} \geq \frac{\rho L^2 I_{\max}^2}{r_L K_u B_{\max}^2} \tag{28}$$

where A_C is the effective cross-section of the core, W_A is the window area, MLT is the mean length turn, ρ is the resistivity of the copper, $B_{\max}$ is the maximum flux density of the ferrite core, and K_u is the window utilization factor.

By replacing the values obtained from Table I and (24) in (28), K_g for the coupled inductor is calculated as follows:

$$K_g = \frac{A_C^2 W_A}{\text{MLT}} \geq \frac{\rho}{r_L K_u B_{\max}^2}\left[\frac{D(1-D)}{1-(n_1+1)D}\right]^2\left(\frac{V_i}{x_{Lm}\%f_s}\right)^2. \tag{29}$$

In second step, after choosing the appropriate core, according to the value of A_c, the number of winding turns (n_{turn}) and the air gap (l_g) are calculated as follows:

$$n_{\text{turn}} = \frac{LI_{\max}}{A_C B_{\max}} \tag{30}$$

$$l_g = \frac{\mu_0 L I_{\max}^2}{2B_{\max}^2 A_C} \tag{31}$$

where μ_0 is the permeability of air.

IV. Comparison of the Proposed Converters With Other Z-Source AC–AC Converter

The advantages of the proposed converters are presented in Table II. All proposed converters have a less magnetic core than other competitors. Also, all proposed converters have a continuous input current and no input or output filters are required. Another feature of the proposed converters is the reduction of the SDP index, which is introduced in [29]. SDP of each converter is calculated as follows:

$$\text{SDP}_{\text{peak}} = \sum_{i=1}^{n} V_{S-\max,i} \cdot I_{S-\max,i} \tag{32}$$

where n is the number of bidirectional switches. As can be seen, the SDP value of topology-1 is reduced compared to the [18], [21], [22], [23], and [24]. But, the SDP value of topology-3

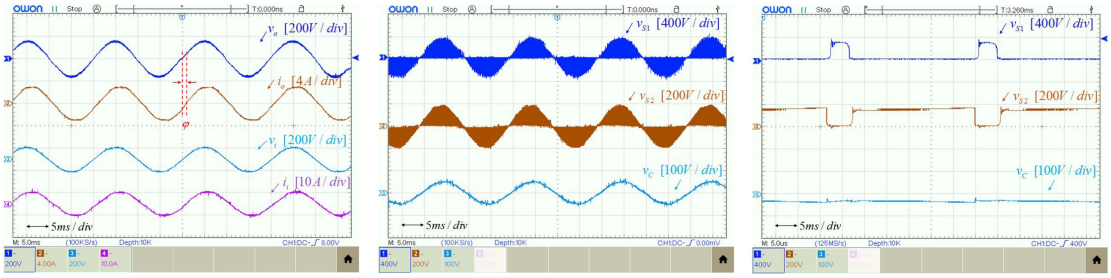

Fig. 13. Experimental results of the topology-1 with *RL* load ($D = 0.15$). (a) V_o, I_o, V_i, and I_i. (b) V_{S1}, V_{S2}, and V_C. (c) Zoom-in of V_{S1}, V_{S2}, and V_C.

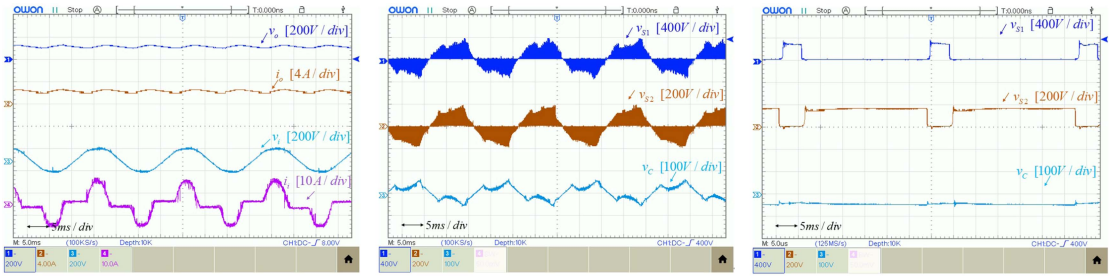

Fig. 14. Experimental results of the topology-1 with nonlinear load ($D = 0.15$). (a) V_o, I_o, V_i, and I_i. (b) V_{S1}, V_{S2}, and V_C. (c) Zoom-in of V_{S1}, V_{S2}, and V_C.

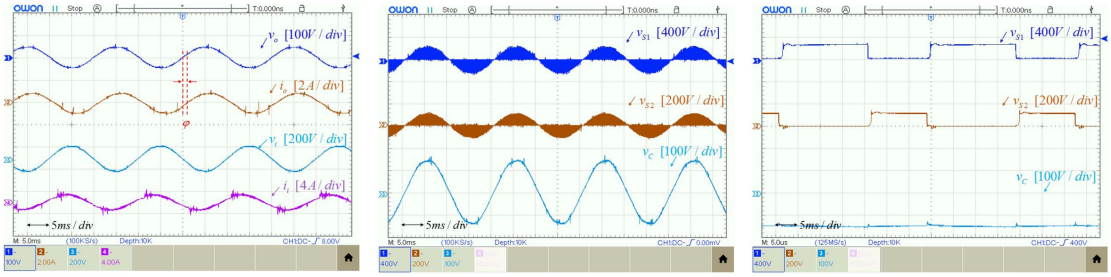

Fig. 15. Experimental results of the topology-1 with *RL* load ($D = 0.6$). (a) V_o, I_o, V_i, and I_i. (b) V_{S1}, V_{S2}, and V_C. (c) Zoom-in of V_{S1}, V_{S2}, and V_C.

has decreased significantly. The normalized SDP versus voltage gains is shown in Fig. 10.

The power density of each converter is directly related to the energy stored in the inductors ($E_L = 1/2LI^2$) and capacitors ($E_C = 1/2CV^2$) using an analytical method presented in [30], the total capacitors and inductors volume metric is evaluated as follows:

$$V_{\text{Capacitors}} = \sum \frac{E_C}{\rho_{E,C}} \tag{33}$$

$$V_{\text{Inductors}} = \sum \frac{E_L}{\rho_{E,L}} \tag{34}$$

where $\rho_{E,C}$ and $\rho_{E,L}$ are the volumetric energy density of capacitor and inductor, respectively. In Fig. 11, the comparative curve of the normalized total volume metric of capacitors and inductors versus voltage gain is plotted.

V. Experimental Results

A laboratory prototype has been built to confirm the performance of the proposed converters, which is shown in Fig. 12. The experimental result of the topology-1 is obtained based on the parameters given in Table III.

The experimental results of topology-1 for boost in-phase mode with *RL* load are shown in Fig. 13. Fig. 13(a) shows the output voltage, output current, input voltage, and input current waveforms from top to bottom. The input and output voltages are 100 and 148 V, respectively. The main component of the input current is 4.54 A and the output current peak is 2.81 A.

The voltage waveforms of S_1, S_2, and V_C and their zoom-in are shown in Fig. 13(b) and (c). The maximum voltage stress of S_1, S_2, and V_C are 375, 183, and 51 V, respectively. The experimental results of topology-1 with nonlinear load are shown in Fig. 14. The experimental results of topology-1 for buck out-of-phase mode with *RL* load are shown in Fig. 15. As can be seen, the

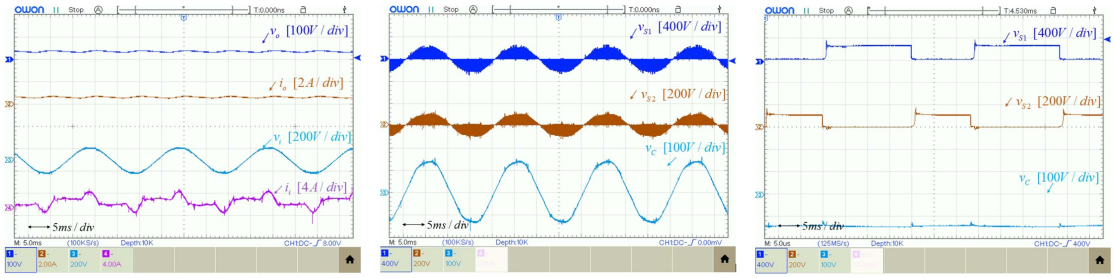

Fig. 16. Experimental results of the topology-1 with nonlinear load ($D = 0.6$). (a) V_o, I_o, V_i, and I_i. (b) V_{S1}, V_{S2}, and V_C. (c) Zoom-in of V_{S1}, V_{S2}, and V_C.

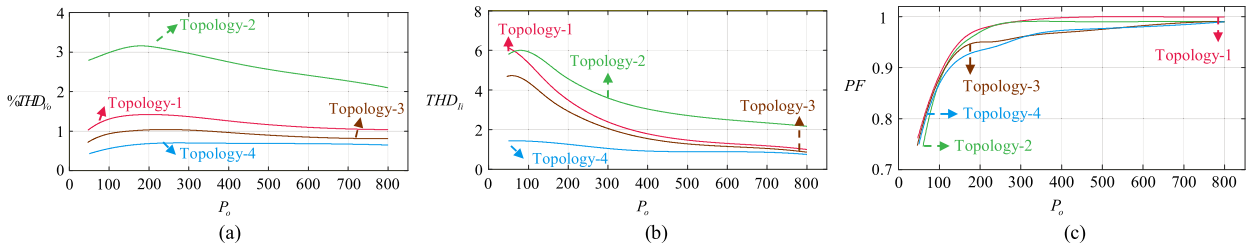

Fig. 17. THD and power factor of the proposed converters versus output powers. (a) Output voltage THD. (b) Input current THD. (c) Input power factor.

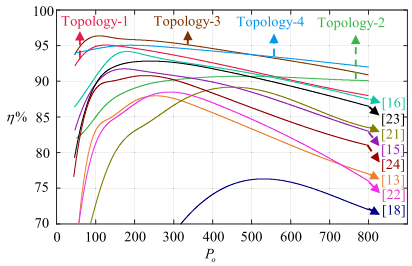

Fig. 18. Comparing the efficiency of the proposed converter with other Z-source AC–AC converters.

output voltage has been reversed and reduced to 48 V. The voltage waveforms across the switches and capacitor C are shown in Fig. 15(b) and (c). The experimental results of topology-1 for buck out-of-phase mode with nonlinear load are shown in Fig. 16. The THD of the output voltage is shown in Fig. 17(a). As can be seen, the THD_{Vo} of all topologies is less than 5% and is within the permissible range. The THD_{Ii} of the proposed topologies is shown in Fig. 17(b). The THD_{Ii} of topology-4 is constant against power changes and is less than 2%. As shown in Fig. 17(c), the input power factor of the proposed converters has an increasing trend with increasing output power. In Fig. 18, the efficiency curve of the proposed converters is compared with existing ZSC.

VI. Conclusion

In this article, a new class of Z-source converters is proposed, benefiting all of them from being bidirectional, shared ground, continuous input current, buck and boost operation, and minimum components. Some features make the proposed topologies more applicable, like presence of buck in-phase and buck/boost out-of-phase operations in topology-2 makes it a good option for DVR. It can compensate for voltage sag and swell without additional elements.

The significant reduction of SDP in topology-3 and the ability to power transfer in both directions make this topology suitable for use as an SST. Finally, the performance of the proposed converters has been verified by a 100 V/50 Hz laboratory prototype.

References

[1] O. Simon, J. Mahlein, M. N. Muenzer, and M. Bruckmarm, "Modern solutions for industrial matrix-converter applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 401–406, Apr. 2002.

[2] Y. Sun, M. Su, X. Li, H. Wang, and W. Gui, "A general constructive approach to matrix converter stabilization," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 418–431, Jan. 2013.

[3] S. Pipolo, A. Formentini, A. Trentin, P. Zanchetta, M. Calvini, and M. Venturini, "A novel matrix converter modulation with reduced number of commutations," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 4991–5000, Sep./Oct. 2021.

[4] X. Liu, P. C. Loh, P. Wang, F. Blaabjerg, Y. Tang, and E. A. Al-Ammar, "Distributed generation using indirect matrix converter in reverse power mode," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1072–1082, Mar. 2013.

[5] L. Tarisciotti et al., "Modulated predictive control for indirect matrix converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4644–4654, Sep./Oct. 2017.

[6] S. Sharifi, F. Jahani, and M. Monfared, "Direct single-phase AC–AC converters based on series impedance networks," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10380–10389, Dec. 2018.

[7] K. Rahman, M. Meraj, M. S. Bhaskar, and A. Iqbal, "Single-phase Z_{AC}-source AC–AC converter with high buck and boost voltage conversion capability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9251–9259, Nov. 2020.

[8] U. A. Khan, H.-K. Yang, A. A. Khan, and J.-W. Park, "Design and implementation of novel noninverting buck–boost AC–AC converter for DVR applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9346–9357, Oct. 2021.

[9] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.
[10] F. L. Luo and H. Ye, "DC-modulated power factor correction AC/AC converters," in *Proc. Ind. Electron. Appl.*, 2007, pp. 1477–1483.
[11] S. M. J. Mousavi, E. Babaei, and M. Sabahi, "Modified single-phase Z-source converter based on gamma structure," in *Proc. 11th Power Electron., Drive Syst., Technol. Conf.*, 2020, pp. 1–6.
[12] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.
[13] X. P. Fang, Z. M. Qian, and F. Z. Peng, "Single-phase Z-source PWM AC–AC converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 121–124, Dec. 2005.
[14] Y. Tang, S. Xie, and C. Zhang, "Z-source AC–AC converters solving commutation problem," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2146–2154, Nov. 2007.
[15] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, "Single-phase AC–AC converter based on quasi-Z-source topology," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2200–2210, Aug. 2010.
[16] M. K. Nguyen, Y. C. Lim, and Y. J. Kim, "A modified single-phase quasi-Z-source AC–AC converter," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 201–210, Jan. 2012.
[17] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3453–3463, Dec. 2011.
[18] M. R. Banaei, R. R. Ahrabi, and M. Elmi, "Single-phase safe commutation trans-Z-source AC–AC converter," *IET Power Electron.*, vol. 8, no. 2, pp. 190–201, Feb. 2015.
[19] H. F. Ahmed and H. Cha, "A new class of single-phase high-frequency isolated Z-source AC–AC converters with reduced passive components," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1410–1419, Feb. 2018.
[20] S. Fathi, S. M. J. Mousavi, and E. Babaei, "A high-frequency isolated four-switch single-phase quasi-Z-source AC–AC converter with inherent commutation and step-changed frequency operation," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2022.3228939.
[21] M. R. Banaei, R. Alizadeh, N. Jahanyari, and E. Seifi Najmi, "An AC Z-source converter based on gamma structure with safe-commutation strategy," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1255–1262, Feb. 2016.
[22] L. He, J. Nai, and J. Zhang, "Single-phase safe-commutation trans-Z-source AC–AC converter with continuous input current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5135–5145, Jun. 2018.
[23] S. M. J. Mousavi, E. Babaei, D. Alizadeh, and H. Komurcugil, "Single-phase AC–AC Z-source converter based on asymmetrical gamma structure with continuous input current and safe commutation strategy," *IET Power Electron.*, vol. 14, pp. 680–689, 2020.
[24] Z. Aleem, H. -K. Yang, H. F. Ahmed, S. L. Winberg, and J. W. Park, "A class of single-phase Z-source AC–AC converters with magnetic coupling and safe-commutation strategy," *IEEE Trans Ind. Electron.*, vol. 68, no. 9, pp. 8104–8115, Sep. 2021.
[25] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, "Voltage swell/sag compensation with single-phase Z-source AC–AC converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–8.
[26] A. Kaykhosravi, N. A. Azli, F. Khosravi, and E. Najafi, "The application of a quasi Z-source AC–AC converter in voltage sag mitigation," in *Proc. IEEE Int. Conf. Power Energy*, 2012, pp. 548–552.
[27] S. M. J. Mousavi and E. Babaei, "Single-phase dynamic voltage restorer based on AC–AC Trans-Z-source converter for voltage sag and swell mitigation," in *Proc. 12th Power Electron., Drive Syst., Technol. Conf.*, 2021, pp. 1–6.
[28] C. W. McLyman, *Transformer and Inductor Design Handbook, Third Edition, Revised and Expanded.* Boca Raton, FL, USA: CRC Press, 2004.
[29] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453–1463, Jul. 2007.
[30] Y. T. Lei, W. C. Liu, and R. C. N. P. Podgurski, "An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018.

Seyyed Mohammad Javad Mousavi received the B.Sc. degree in power electrical engineering from the Shahid Madani Azarbayejan University, Tabriz, Iran, in 2017, and the M.Sc. degree in power electronics from the Department of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical and Computer Engineering, University of Tabriz.

His research interests include ac–ac converters.

Ebrahim Babaei (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2007.

He has authored and coauthored 1 book and more than 650 journal and conference papers. His research interests include the analysis, modeling, design, and control of power electronics converters and their applications, renewable energy sources, and FACTS devices.

Prof. Babaei has been the Editor-in-Chief of the *Journal of Electrical Engineering* of the University of Tabriz, since 2013. He is currently an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, *Open Journal of the Industrial Electronics Society*, *Iranian Journal of Science and Technology*, *Transactions of Electrical Engineering*, and *International Journal of Circuit Theory and Applications*.

Mehran Sabahi he received the B.S. degree in electronic engineering from the University of Tabriz, Tabriz, Iran, in 1991, the M.S. degree in electrical engineering from the Tehran University, Tehran, Iran, in 1994, and the Ph.D. degree in electrical engineering from the University of Tabriz, in 2009.

His research interests include power electronic converters and renewable energy systems.

Hasan Komurcugil (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Eastern Mediterranean University (EMU), Famagusta, Cyprus, in 1998.

In 2010, he was elected as the as the Board Member of Higher Education, Planning, Evaluation, Accreditation and Coordination Council North Cyprus. From 2010 to 2019, he played active role in evaluating the universities in North Cyprus. He has authored more than 70 science citation index expanded journal papers and 80 conference papers. He has coauthored one book chapter. He is currently serving as the Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS. His research interests include power electronics and innovative control methods for power converters, such as sliding mode control, Lyapunov-function-based control, and model predictive control.