Variable OFF-Time and Deadtime Scheme With Optimized Control Frequency for Soft-Switching Single-Phase Inverters

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***Abstract*—Controlling current at critical conduction mode (CRM) is an effective way to achieve zero voltage switching (ZVS) of switches for inverters. However, the higher reverse inductor current and fixed deadtime in fully digital soft-switching control, such as reverse current boundary-based (RCB-based) schemes, lead to higher rms inductor current and higher power losses. Besides, the digital control frequency for CRM-based inverters is not well designed, resulting in the contradiction between high performance and high digital calculation burden. Therefore, this article proposes a fully digital soft-switching control based on the variable OFF-time and deadtime with an optimized designed digital control frequency. First, the variable OFF-time and deadtime design guidelines are addressed with the established mathematical model of the CRM-based inverter. Then, the power losses of the inverter with different digital control frequencies and control schemes are quantitatively analyzed and compared. Finally, a 1 kW single-phase three-level neutral-point-clamped grid-tied inverter was built. Experimental results show that the proposed scheme can achieve the ZVS turn-ON of switches without additional components, and the maximum efficiency is 98.3%. Compared with the RCB-based scheme, the proposed method achieves higher efficiency with the same hardware cost.**

***Index Terms*—Critical conduction mode, digital control, single-phase inverter, zero voltage switching.**

NOMENCLATURE

$U_{\rm dc}$	Dc-link voltage.
$u_{\rm g}$	Grid voltage.
$i_{\rm L}$	Inductor current.
MI	Modulation index.
u_{gs_act}	Gating signals of active switches.
u_{ds_act}	Drain-source voltage of active switches.
u_{gs_sync}	Gating signals of synchronous switches.
u_{ds_sync}	Drain-source voltage of synchronous switches.
$u_{\rm gs1}-u_{\rm gs4}$	Gating signals of S_1 to S_4.
$u_{\rm ds1}-u_{\rm ds4}$	Drain-source voltage of S_1 to S_4.
C_1–C_4	Junction capacitor of S_1 to S_4.
$u_{\rm C1}-u_{\rm C4}$	Voltage of C_1 to C_4.
$t_{\rm r}$	Resonance period of the equivalent resonance circuit during the deadtime.
$t_{\rm dead}$	General nomenclature of deadtime between the turn-OFF of S_3 and the turn-ON of S_1.
$tdead\_ZVS$	Variable deadtime between the turn-OFF of S_3 and the turn-ON of S_1 at the ZVS region.
$t_{dead\_non-ZVS}$	Variable deadtime between the turn-OFF of S_3 and the turn-ON of S_1 at the non-ZVS region.
$i_{\rm L}(t_4)$	Minimum value of the reverse inductor current when analyzing the switching state.
i_{L_min}	Minimum value of the reverse inductor current.
$t_{\rm ext}(t)$	Turn-OFF extension time of synchronous switches.
$t_{\rm ON}$, $t_{\rm OFF}$	On-time and OFF-time of active switches (S_1 and S_4).
t_{on_k}, $t_{\rm off\_k}$	Calculation results of $t_{\rm ON}$ and $t_{\rm OFF}$ at kth digital control period.
t_{dead_k}	Calculation results of deadtime (t_{dead_ZVS} or $t_{dead\_non-ZVS}$) at kth digital control period.
$I_{\rm ref}$	Grid-tied current reference.
i_{L_fb}	Inductor current feedback.
$t_{\rm c}$	On-time adjustment step.
$t_{\rm vsb}$	Preliminary OFF-time calculation results.
$f_{\rm sw}$	Switching frequency.
$f_{\rm g}$	Utility grid fundamental frequency.
$f_{\rm c}$	Digital control frequency.
k_1, k_2	Discrete deviation coefficient of $t_{\rm OFF}$ and $t_{\rm dead}$.
$k_{\rm L}$	Inductor ripple coefficient.
t_{dead_theo}	Theoretical deadtime without discrete deviation.
$W_{\text{conduction-}x}$	Conduction energy loss of x ($x = S_1$, S_2, S_3, D_1, D_2).

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$P_{\text{conduction-}x}$	Conduction power loss of x ($x = S_1$, S_2, S_3, D_1, D_2).
$W_{\text{turn-OFF-}y}$	Turn-OFF energy loss of y ($y = S_1$, S_3).
$P_{\text{turn-OFF-}y}$	Turn-OFF power loss of y ($y = S_1$, S_3).
W_{PostRes}	Postresonance energy loss.
P_{PostRes}	Postresonance power loss.
k_{sw}	Number of the switching period included within one control period.
k_{c}	Number of the digital control period within a half fundamental period.
P, P_{r}	Output power, rated power.

I. Introduction

WIDE bandgap (WBG) devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), can significantly improve the power density of converters by increasing the switching frequency [1], [2], [3], [4], [5], [6], [7]. Since the turn-ON energy loss of a SiC device is dominant and the turn-OFF energy loss is almost negligible, implementing the soft-switching turn-ON of SiC MOSFETS is essential for higher switching frequency operation [8], [9], [10].

The auxiliary resonant circuit (ARC) between the dc-side and bridge arms periodically the dc-link voltage drops to zero. Thus, zero-voltage-switching (ZVS) can be achieved by eliminating turn-ON loss. In [11], an active dc-link clamped resonant auxiliary circuit was utilized in a three-phase two-level inverter. All SiC MOSFETS can achieve the ZVS turn-ON, resulting in 98.6% peak efficiency at 300 kHz switching frequency. On the other hand, the ARC between the ac-side and bridge arms can also implement the ZVS turn-ON of switches since the voltage across resonant capacitors in parallel with switches goes down to zero periodically. The peak efficiency is reported as over 98.5% at 20 kHz switching frequency [12]. But the ARC technology has disadvantages of complex circuit topology and extra hardware cost.

The critical conduction mode (CRM) is another effective solution to implement the ZVS turn-ON of switches for rectifiers and inverters [13], [14], [15], [16], [17]. The basic principle is to form a resonant network between the filter inductor and junction capacitors of switches. Thanks to the resonant network, the junction capacitor voltage could be decreased to zero during the deadtime. Compared with ARC-based converters, the main circuit of CRM-based converters is simple. In the previous work [11], both the ZVS and non-ZVS regions are defined during half a fundamental period, as shown in Fig. 1(a), where the MI represents the ratio of u_{g} to U_{dc}, also named as modulation index. u_{g} and U_{dc} are the utility grid voltage and dc-link voltage, respectively. i_{L} is the inductor current. Unfortunately, the ZVS turn-ON of switches cannot be naturally achieved when $U_{\text{dc}} > 2u_{\text{g}}$. The resonance energy is not large enough to discharge the junction capacitor completely, which means the drain-source voltage of switches cannot go down to zero naturally. Therefore, it is necessary to increase the resonance energy by generating an additional reverse inductor current at the non-ZVS region, as depicted in Fig. 1(b). However, the conduction loss is increased

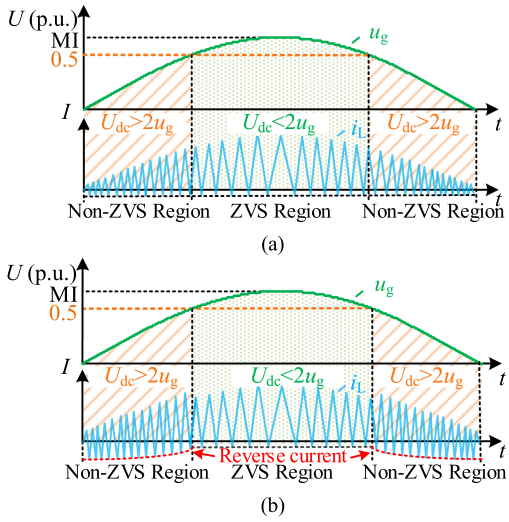

Fig. 1. ZVS implementation region during the positive half period for CRM-based inverters. (a) Without the reverse current. (b) With the reverse current.

with the additional reverse inductor current. Thus, the reverse inductor current should be controlled carefully.

The reverse inductor current can be accurately controlled by using the zero-crossing detection (ZCD) circuit. A dedicated scheme for the on-board charger with the ZCD circuit and synchronous switches turn-OFF extension control was proposed in [18]. The ZCD circuit is employed to realize the CRM operation, and the turn-OFF extension after the ZCD signal for synchronous switches is used to generate the reverse inductor current. The active switch is ZVS turned ON when the drain-source voltage goes down to zero. This ZCD-based soft-switching technology has also been employed in the single-phase two-level full-bridge inverter [19], [20], [21] and the T-type five-level inverter [22].

However, the high-bandwidth comparators and current sensors contained in the ZCD circuit lead to expensive hardware costs. In contrast, a fully digital scheme without high-bandwidth components is cost-effective. Several fully digital control schemes have been reported, such as SVPWM-based variable switching frequency control [23], [24] and DPWM-based inductor current ripple predictive control [25], [26]. Unfortunately, these schemes are only applicable to three-phase systems and cannot be applied to single-phase systems.

A fully digital scheme based on hysteresis current control was proposed for single-phase and three-phase systems. In addition, different reverse current boundary (RCB) modes were designed to achieve ZVS turn-ON of switches [27], [28], [29]. The constant boundary current mode (CBCM) and the variable hysteresis current mode (VHCM) are illustrated in Fig. 2(a) with dashed lines. But the theoretical minimum reverse current boundary for achieving ZVS turn-ON should be the solid line. Besides, a fully digital method based on variable frequency average current control was proposed to achieve full power range ZVS operation for dual-buck inverters [30]. However, the minimum RCB for achieving ZVS is also ignored. In [31], an adaptive hysteresis current-based ZVS modulation for three-phase converters was proposed. The minimum RCB for achieving ZVS was studied,

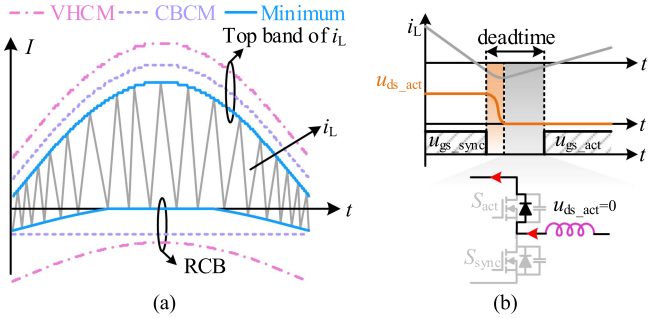

Fig. 2. Existing RCB hysteresis current control shortcomings: (a) Higher rms inductor current caused by nonminimum reverse current. (b) Body diode conduction issues are caused by fixed deadtime.

but the current should be controlled by internal high-bandwidth comparators of a high-performance digital signal processor (DSP). Therefore, most fully digital-based schemes operate with a higher rms inductor current, resulting in higher conduction loss and turn-OFF loss. It is necessary to dynamically regulate the OFF-time of active switches to minimize the reverse inductor current.

Besides, the inappropriately fixed deadtime used in [28] leads to body diode conduction issues on active switches, as shown in Fig. 2(b). u_{gs_act} and u_{gs_sync} represent the active and synchronous switch gating signals, respectively. u_{ds_act} is the drain-source voltage of the active switch. When u_{ds_act} goes down to zero before the ending of deadtime, the inductor current is freewheeling through the body diode of the active switch, which increases the power loss. Furthermore, due to the high switching frequency under light load conditions, the negative effect of the deadtime on current THD becomes more apparent, which means worse current THD. Thus, the deadtime should also be appropriately controlled.

However, since the switching frequency of the CRM-based inverter is varied from several hundred kilohertz to megahertz, regulating the OFF-time of active switches and deadtime cycle-by-cycle leads to a huge calculation burden on the digital controller. Consequently, a constant digital control frequency is preferred for the fully digital control scheme. Thus, the theoretical OFF-time and the deadtime cannot be updated at each switching period. The deviations between the practical and theoretical values will lead to extra loss, including the conduction loss of switches and body diodes. Thus, the design of digital control frequency is vital, but it is rarely discussed in previous work.

This article proposes a fully-digital soft-switching control scheme with a well-designed digital control frequency. Furthermore, the dynamic OFF-time and deadtime regulation is proposed to achieve the ZVS turn-ON of switches with the minimum reverse current during a whole fundamental period. The rest of this article is organized as follows. Section II establishes the mathematical model of the CRM-based single-phase three-level neutral-point-clamped (3L-NPC) inverter. Then, the proposed dynamic OFF-time and deadtime regulation and its control diagram are presented in Section III. In Section IV, the power loss of the CRM inverter with different digital control frequencies and different control schemes is quantitatively calculated and compared. Then, an optimized digital control frequency and its design guideline are given. Experiments are carried out in Section V. Finally, Section VI presents the comparative study and applicability discussion. Finally, Section VII concludes this article.

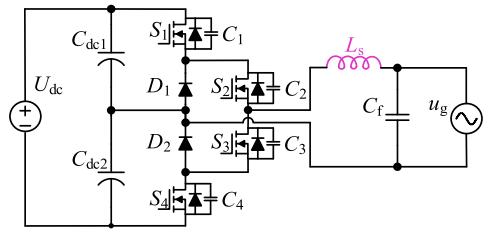

Fig. 3. Topology of the 3L-NPC inverter.

II. Analysis and ZVS Implementation of the CRM-Based 3L-NPC Inverter

A. Topology and Operation Modes

The topology of the 3L-NPC inverter is shown in Fig. 3, where C_{dc1} and C_{dc2} are dc-link capacitors. C_1 to C_4 represent the junction capacitor of S_1 to S_4, respectively. The capacitance of C_1 to C_4 is regarded as C. L_s is the filter inductor, and C_f is the filter capacitor. U_{dc} is defined as the dc-link voltage, and u_g represents the utility grid voltage.

During the positive half period, S_2 is always turned ON, and S_4 is always turned OFF. S_1 and S_3 are complementary pairs with the switching frequency. During the negative half period, S_3 is always turned ON, and S_1 is always turned OFF. S_2 and S_4 are complementary pairs with the switching frequency. Thus, the deadtime should be set between complementary gating signals to avoid the shoot-through issue.

The positive half period is taken as an example for analysis, and the key waveforms of switches and the inductor current with a single switching period at the ZVS and non-ZVS regions are drawn in Fig. 4(a) and (b), respectively. u_{gs1} and u_{gs3} represent the gating signals of S_1 and S_3, t_r is defined as the resonance period, and can be represented by $2\pi\sqrt{2L_sC}$. t_{dead_ZVS} and $t_{dead\_non-ZVS}$ represent the deadtime between the turn-OFF of S_3 and the turn-ON of S_1 at the ZVS and non-ZVS regions, respectively, and both of them are assumed as $t_r/2$. Besides, the deadtime between the turn-OFF of S_1 and the turn-ON of S_3 can be set as a constant value to avoid the short-through issue.

Based on Figs. 3 and 4, equivalent circuits of each switching state are depicted in Fig. 5.

State #1 [t_0-t_1]: At t_0, S_1 is ZVS turned ON, and S_3 is OFF. The inductor current is flowing through S_1 and S_2, as shown in Fig. 5(a). It can be seen that the initial inductor current is equal to 0 at the ZVS region, as depicted in Fig. 4(a). In contrast, the inductor current is lower than zero at the non-ZVS region, as depicted in Fig. 4(b). Thus, the turn-ON loss of S_1 is zero. Then, S_1 is turned OFF at t_1. The turn-OFF loss of S_1 and the conduction loss of S_1 and S_2 are generated during *State* #1.

State #2 [t_1-t_2]: At t_1, S_1 is hard-switching turned OFF. The junction capacitor, C_1 is charged by the inductor current,

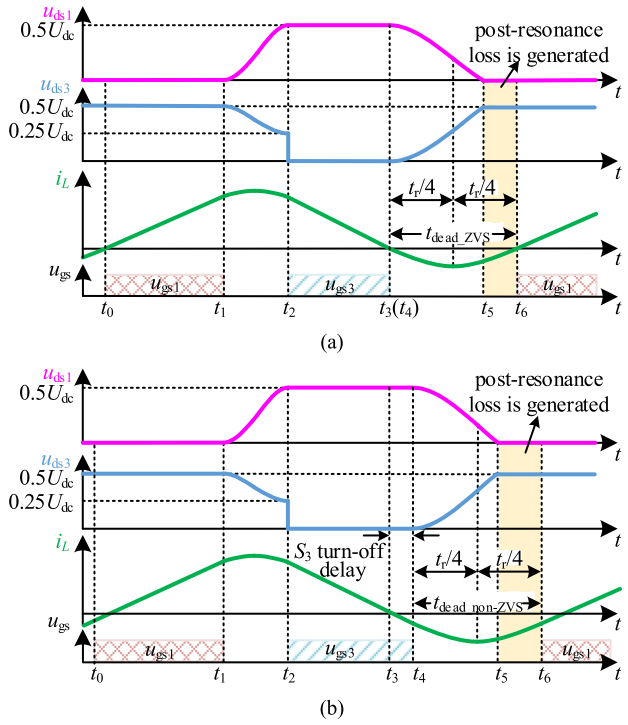

Fig. 4. Waveforms of the drain-source voltages, the inductor current, and gating signals during one switching period at the positive half period. (a) At the ZVS region (b) At the non-ZVS region.

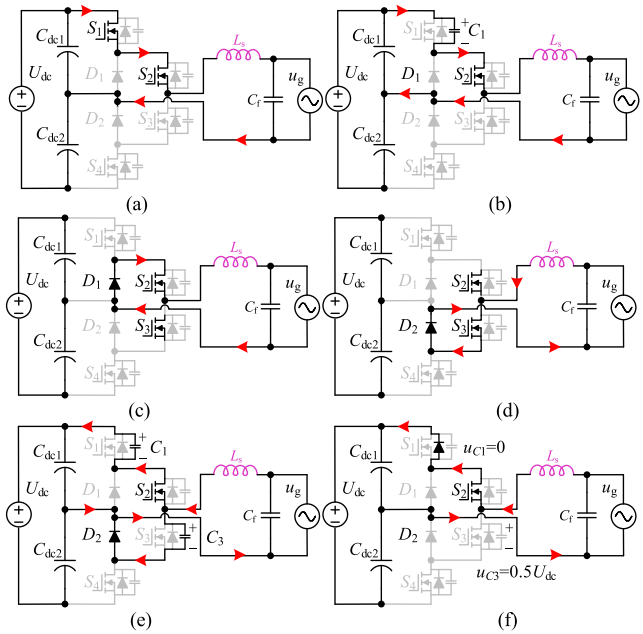

Fig. 5. Equivalent cicutis of each switching state. (a) State#1: [t_0-t_1]. (b) State#2: [t_1-t_2]. (c) State#3: [t_2-t_3]. (d) State#4: [t_3-t_4]. (e) State#5: [t_4-t_5]. (f) State#6: [t_5-t_6].

as shown in Fig. 5(b). Thus, the drain-source voltage of S_1, u_{ds1} is increased and equal to $0.5U_{dc}$ at t_2. Besides, with the increase of u_{ds1}, u_{ds3} is decreased and equal to $0.25U_{dc}$ at t_2, as depicted in Fig. 4(a) and (b).

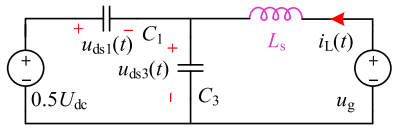

Fig. 6. Equivalent resonant circuit of *State* #5.

State #3 [t_2-t_3]: At t_2, S_3 is hard-switching turned ON. The inductor current is still freewheeling through D_1 and S_2, as shown in Fig. 5(c). During this state, the inductor current is decreased and equal to 0 at t_3, as depicted in Fig. 4(a) and (b). Moreover, from Fig. 4(a), S_3 is turned OFF at t_3. Since there is no current flowing through S_3, S_3 is free of switching loss at the ZVS region.

State #4 [t_3-t_4]: This is a dedicated state of the non-ZVS region. The additional resonance energy should be generated, and the turning OFF of S_3 is extended from t_3 to t_4. The reverse inductor current is flowing through S_3 and D_2, as shown in Fig. 5(d). Thus, S_3 is hard-switching turned OFF at the non-ZVS region. The turn-OFF loss of S_3 and the conduction loss of S_3 and D_2, are generated during this state.

State #5 [t_4-t_5]: At t_4, the turning OFF of S_3 forces L_s to resonate with C_1 and C_3, as shown in Fig. 5(e). After $0.25t_r$, i_L is decreased to its minimum value. At t_5, u_{ds1} is decreased to 0, and u_{ds3} is increased to $0.5U_{dc}$, as depicted in Fig. 4(a) and (b). The conduction loss of S_2 and D_2, are generated during this state.

State #6 [t_5-t_6]: After t_5, u_{ds1} is equal to 0, and the reverse current is freewheeling through the body diode of S_1, as shown in Fig. 5(f). From Fig. 4(a) and (b), the conduction loss of the body diode of S_1 is generated, and it is defined as the post-resonance loss. Thus, the postresonance loss should be reduced by dynamic regulating the deadtime.

B. Implementation of ZVS Turn-on

Based on the analysis of operating states, *State* #5 is the key operating state to achieve the ZVS turn-ON of active switches. The equivalent circuit of *State* #5 is depicted in Fig. 6.

According to Fig. 6, (1) can be derived

$$\begin{cases} L_s \frac{di_L(t)}{dt} + u_{ds3}(t) = u_g(t) \\ u_{ds1}(t) + u_{ds3}(t) = U_{dc}/2 \\ C\frac{du_{ds3}(t)}{dt} - C\frac{du_{ds1}(t)}{dt} = i_L(t). \end{cases} \tag{1}$$

The initial value $u_{ds1}(0)$, $u_{ds3}(0)$, and $i_L(0)$ are defined as, $u_{ds1}(0) = u_{ds1}(t_4) = 0.5U_{dc}$, $u_{ds3}(0) = u_{ds3}(t_4) = 0$, and $i_L(0) = i_L(t_4)$. Thus, $u_{ds1}(t)$ and $i_L(t)$ can be yielded as follows:

$$u_{ds1}(t) = \frac{U_{dc}}{2} - u_g(t) + u_g(t)\cos\frac{t}{\sqrt{2L_sC}} - \frac{|i_L(t_4)|\cdot\sqrt{2L_sC}}{2C}\sin\frac{t}{\sqrt{2L_sC}} \tag{2}$$

$$i_L(t) = \frac{2u_g(t)C}{\sqrt{2L_sC}}\sin\frac{t}{\sqrt{2L_sC}} + |i_L(t_4)|\cos\frac{t}{\sqrt{2L_sC}}. \tag{3}$$

It is worth mentioning that the waveforms of u_{ds1} and i_L in Fig. 4 are drawn according to (2) and (3). If there is no reverse current, by substituting $i_L(t_4) = 0$ into (2), $u_{ds1}(t)$ can be solved as follows:

$$u_{ds1}(t) = \frac{U_{dc}}{2} - u_g(t) + u_g(t)\cos\frac{t}{\sqrt{2L_sC}} \geq \frac{U_{dc}}{2} - 2u_g(t). \tag{4}$$

To achieve the ZVS turn-ON of S_1, $u_{ds1}(t)$ should be equal to 0. By substituting $u_{ds1}(t) = 0$ into (4), it can be concluded that. the ZVS region is $0.5U_{dc} \leq 2u_g$, and the non-ZVS region is $0.5U_{dc} > 2u_g$.

Rewriting (2) as follows:

$$u_{ds1}(t) = \frac{U_{dc}}{2} - u_g(t) - \sqrt{u_g^2(t) + \frac{L_s}{2C}i_L^2(t_4)}\sin\left(\frac{t}{\sqrt{2L_sC}} - \varphi\right) \tag{5}$$

where $\varphi = \arctan\frac{\sqrt{2L_sC}\cdot u_g(t)}{i_L(t_4)\cdot L_s}$.

According to (5), the higher $|i_L(t_4)|$ leads to the shorter time that $u_{ds1}(t)$ goes down to 0, which means the deadtime should be shorter. However, the higher $|i_L(t_4)|$ also leads to a higher inductor rms current, resulting in higher conduction loss. In particular, the power loss generated during *State* #4 is higher correspondingly. Therefore, $|i_L(t_4)|$ must be set at its theoretical minimum value. Moreover, the deadtime should be dynamically regulated according to $|i_L(t_4)|$. Otherwise, the inappropriate deadtime will lead to additional postresonance loss and aggravate the current THD.

III. Proposed Fully-Digital Control Scheme

A. Minimum Reverse Current and Deadtime Calculation

At the ZVS region, the minimum value of $|i_L(t_4)|$ is zero. Substituting $u_{ds1}(t) = 0$ into (2), t_{dead_ZVS} can be calculated as

$$t_{dead\_ZVS}(t) = \sqrt{2L_sC}\cdot\left[tan^{-1}\frac{\sqrt{U_{dc}\cdot(4u_g(t) - U_{dc})}}{2u_g(t) - U_{dc}} + \pi\right]. \tag{6}$$

However, at the non-ZVS region, the minimum value of $i_L(t_4)$ could be derived from the minimum value of $u_{ds1}(t)$. According to (5), $u_{ds1}(t)$ should be higher than the following equation:

$$u_{ds1}(t) \geq \frac{U_{dc}}{2} - u_g(t) - \sqrt{u_g^2(t) + \frac{L_s}{2C}i_L^2(t_4)}. \tag{7}$$

Then, substituting $u_{ds1}(t) = 0$ into (7), the minimum value of $|i_L(t_4)|$ is calculated as

$$i_{L\_min} = |i_L(t_4)|_{min} = \sqrt{\frac{C}{L_s}U_{dc}\cdot\left(\frac{U_{dc}}{2} - 2u_g(t)\right)}. \tag{8}$$

Further, since $i_L(t_3)$ is equal to 0, the turn-OFF extension time of S_3 can be solved according to Faraday's law, as follows:

$$t_{ext}(t) = \frac{L_s|i_L(t_4)|_{min}}{u_g(t)} = \sqrt{\frac{L_sC}{2}}\cdot\frac{\sqrt{U_{dc}(U_{dc} - 4u_g(t))}}{u_g(t)}. \tag{9}$$

TABLE I
Compensation Coefficients in Different Regions

Region	I	II	III	IV
Adjustment coefficients of t_{off}	1	$1/k_1$	$1/k_1$	$1/k_1$
Adjustment coefficients of t_{dead}	1	$1/k_2$	$1/k_2$	1

TABLE II
Parameters of the Experimental Prototype

Parameter	Value
DC-link (U_{dc})	400 V ~ 600 V
Utility Grid (u_g)	110 V / 50 Hz
L_s	40 μH
C_f	6.6 μF
Rated power	1 kW
Digital control frequency (f_c)	60 kHz
Switching frequency (f_{sw}) @ U_{dc}=400V	100 kHz ~ 300 kHz
Diode (D_1, D_2)	C3D20060
SiC MOSFET (S_1 to S_4)	SCT3060AL
Junction capacitor (C_1 to C_4)	55 pF

Finally, substituting (8) and $u_{ds1}(t) = 0$ into (2), $t_{dead\_non-ZVS}$ is calculated as follows:

$$t_{dead\_non-ZVS}(t) = \sqrt{2L_sC}\cdot\times\left[\frac{\pi}{2} + \tan^{-1}\frac{2u_g(t)}{\sqrt{U_{dc}(U_{dc} - 4u_g)}}\right]. \tag{10}$$

Based on (6), (8), and (10), it is clear that both the reverse inductor current and the deadtime are independent of the output power. Therefore, by substituting parameters listed in Table II, the variation curves of the reverse current $i_L(t_4)$ and the deadtime at the positive half period are drawn in Fig. 7(a) and (b), respectively.

By using the approach reported in [28], the reverse inductor current boundary and the deadtime of the CBCM scheme must be set as -1 A and 650 ns, respectively. However, from Fig. 7(a), the reverse inductor current of the proposed scheme varies with ωt, and the lowest $i_{L(t4)}$ equals -0.4 A. Since the CBCM scheme features the lowest rms inductor current among all of the RCB-based schemes [28], the rms inductor current using the proposed scheme is lower than those of RCB-based schemes, resulting in lower conduction loss. Besides, according to Fig. 7(b), the maximum t_{dead} is shorter than 220 ns. Therefore, compared with the RCB-based scheme, the proposed variable deadtime scheme also features lower postresonance loss and better current THD. Besides, it is worth mentioning that the ZVS turn-ON of active switches can also be achieved by setting $t_{dead} = t_r/2$ (calculated as 300 ns according to Table II). However, the high switching frequency with the constant deadtime will aggravate the efficiency and current THD under the light load condition, and it is discussed in Section IV-C and Section V.

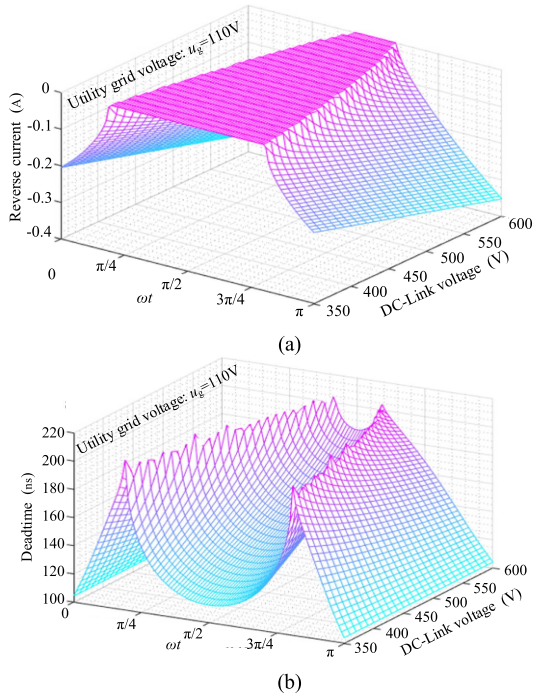

Fig. 7. Reverse current and deadtime variation range at the positive half period: with 350 to 600 V DC-link voltage and 110 V utility grid voltage. (a) Reverse current variation range. (b) Deadtime variation range.

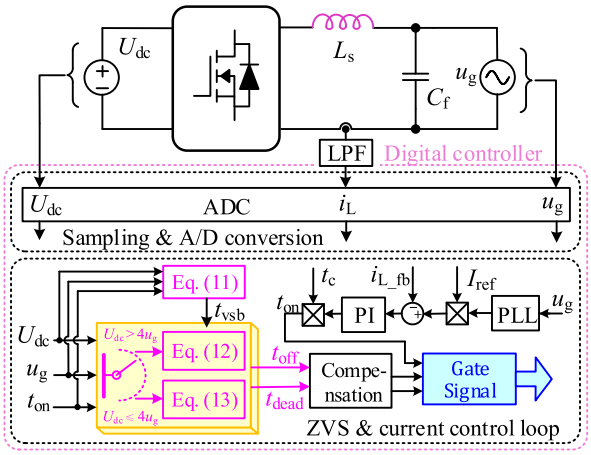

Fig. 8. Control block diagram of the proposed control scheme.

B. Proposed Control Scheme With Variable Off-Time and Deadtime

The control block diagram of the proposed fully digital soft-switching scheme is depicted in Fig. 8, where $I_{\rm ref}$ represents the grid-tied current reference, and i_{L_fb} is the inductor current feedback. $t_{\rm ON}$ and $t_{\rm OFF}$ represent the ON-time and the OFF-time of active switches (S_1 and S_4), respectively. $t_{\rm c}$ is the on-time adjustment step, a constant value equal to the minimum switching period. $t_{\rm vsb}$ represents the preliminary OFF-time. It should be noted that the A/D sampling and ZVS and current control loop are operated with constant frequency.

The ON-time of active switches S_1 and S_4, $t_{\rm ON}$ is equal to the output value of the PI controller multiplied by $t_{\rm c}$. Furthermore,

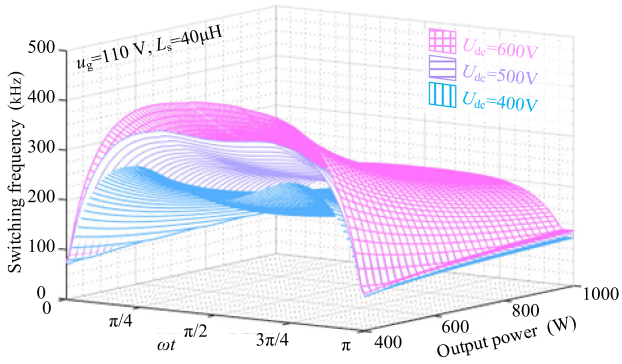

Fig. 9. Variation range of $f_{\rm sw}$ at the positive half period with different output power and DC-link voltages.

$t_{\rm vsb}$ is calculated by the volt-second balance law, as the following:

$$t_{\rm vsb}\left(t\right)=\frac{t_{\rm on}\cdot\left(0.5U_{\rm dc}-\left|u_{\rm g}(t)\right|\right)}{\left|u_{\rm g}(t)\right|}. \tag{11}$$

Finally, the dynamic OFF-time $t_{\rm OFF}$(t), and deadtime $t_{\rm dead}(t)$ at the ZVS region and the non-ZVS region can be calculated by

$$\begin{cases} t_{\rm off}\left(t\right)=t_{\rm vsb}\left(t\right) \\ t_{\rm dead}\left(t\right)=t_{\rm dead\_ZVS}\left(t\right) \end{cases} \tag{12}$$

$$\begin{cases} t_{\rm off}\left(t\right)=t_{\rm vsb}\left(t\right)+t_{\rm ext}\left(t\right) \\ t_{\rm dead}\left(t\right)=t_{\rm dead\_non-ZVS}\left(t\right). \end{cases} \tag{13}$$

From (11) and (13), $t_{\rm OFF}(t)$ approaches infinity near the zero-crossing point of the utility grid, which means the switching frequency approaches zero. Thus, the switching frequency near the zero-crossing point should be fixed, but the ZVS turn-ON of active switches can also be achieved. It is because the inductor current is still reversed near the zero-crossing point. The variation range of the switching frequency, $f_{\rm sw}$ with different output power and dc-link voltages is depicted in Fig. 9.

A cost-effective digital controller can be employed to realize the above control scheme. $t_{\rm ON}$, $t_{\rm OFF}$, and $t_{\rm dead}$ of active switches can be derived by calculating (11) and (12) [or (13)] at the beginning of each digital control period. The implementation of the proposed control scheme is illustrated in Fig. 10. t_{on_k}, t_{off_k}, and t_{dead_k} represents the calculation results at kth digital control period.

C. t_{dead} and $T_{\rm off}$ Compensation

Since the digital control frequency is constant, every single digital control period may include multiple switching periods. Thus, $t_{\rm ON}$, $t_{\rm OFF}$, and $t_{\rm dead}$ can only be updated in each digital control period instead of each switching period. On the other hand, based on (12) and (13) and Fig. 7(b), $t_{\rm OFF}$ and $t_{\rm dead}$ should be varied with $u_{\rm g}$ at each switching period, as shown in the blue and purple shadows in Fig. 10. Therefore, there are discrete deviations between the practical and theoretical values of $t_{\rm OFF}$ and $t_{\rm dead}$ in each switching period, as shown in Fig. 10. During a whole fundamental period, the discrete deviation of $t_{\rm OFF}$ and

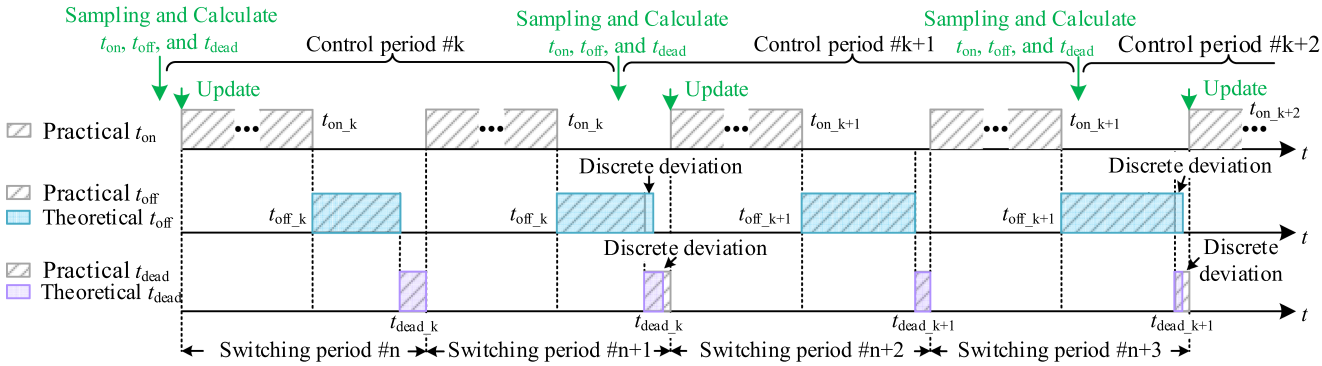

Fig. 10. Implementation of the proposed scheme with a constant digital control period.

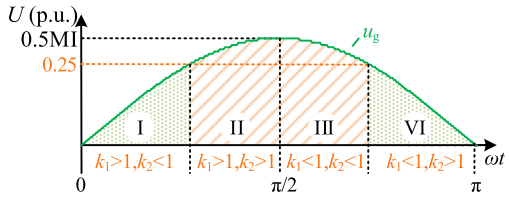

Fig. 11. Distribution of k_1 and k_2 at the positive half period.

t_{dead} at any time t ($0 \le t \le 1/f_g$, for instance, at the peak point of the positive half period. $t = 0.25/f_g$) can be defined as

$$k_1 = \frac{t_{off}\left(\lfloor t \cdot f_c \rfloor \cdot \frac{1}{f_c}\right)}{t_{off}(t)}, k_2 = \frac{t_{dead}\left(\lfloor t \cdot f_c \rfloor \cdot \frac{1}{f_c}\right)}{t_{dead}(t)} \quad (14)$$

where k_1 and k_2 represent the discrete deviation coefficient of t_{OFF} and t_{dead}, respectively. $k_q > 1$ ($q = 1$ or 2) means the practical values are higher than the theoretical values. In contrast, $k_q < 1$ means the practical values are lower than the theoretical values. The calculation symbol $\lfloor f(x) \rfloor$ indicates the bottom integral of $f(x)$.

The distribution of k_1 and k_2 at the positive half period is shown in Fig. 11, where the U-axis represents the ratio of u_g to U_{dc}. Taking region III as an example for analysis. As $k_1 < 1$ and $k_2 < 1$, the practical values of t_{OFF} and t_{dead} are shorter than their theoretical value. According to the analysis in Section II, since t_{OFF} is shorter, $|i_L(t_4)|$ is not higher enough to achieve the ZVS turn-ON of active switches. The analysis of other regions is similar. To summarize, the discrete deviation has a negative effect on ZVS implementation and power loss. To eliminate the discrete deviation, the practical values calculated by (12) and (13) should be multiplied by a compensation coefficient. The compensation coefficients are listed in Table I. However, it should be noted that even though calculation results by (12) and (13) are compensated in each digital control period, the negative effect on efficiency caused by discrete deviation is still apparent if the control frequency is much lower than the switching frequency. Therefore, it is necessary to establish a digital control frequency-related power loss model, quantitatively evaluate its influence on power loss, and design an appropriate digital control frequency.

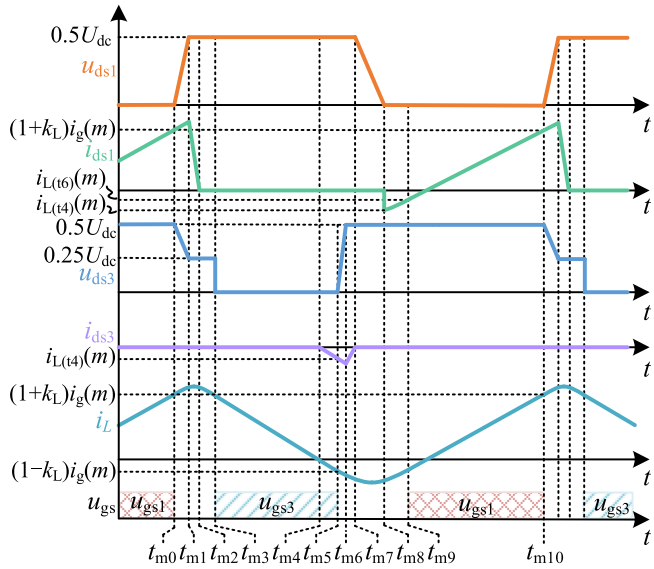

Fig. 12. Switching process of switches under the positive half period. [t_{m0}-t_{m1}]: $t_{d(OFF)}$. [t_{m1}-t_{m2}]: t_f. [t_{m2}-t_{m3}]: Deadtime between the turning-OFF of S_1 and the turning-ON of S_3. [t_{m3}-t_{m4}]: $t_{vsb}(m)$. [t_{m4}-t_{m5}]: $t_{ext}(m)$. [t_{m5}-t_{m6}]: $t_{d(OFF)}$. [t_{m6}-t_{m7}]: t_f. [t_{m7}-t_{m8}]: $t_{dead\_theo}(m)$. [t_{m7}-t_{m9}]: $t_{dead}(m)$. [t_{m9}-t_{m10}]: $t_{ON}(m)$.

IV. Power Losses Analysis and Digital Control Frequency Design

A. Power Losses Models

The following conditions are assumed to simplify the analysis. The parasitic parameters of cable lines are ignored, U_{dc} is a constant value, and the grid-tied inverter is operated with the unity power factor. The positive half period is taken as an example for analysis. S_2 is always turned-ON at the positive half period. Thus, its switching loss is ignored. In addition, SiC Schottky diodes are used for D_1 and D_2, and the switching loss of diodes is also ignored.

Fig. 12 shows the detailed switching process of S_1 and S_3 during the m-th switching period. The turn-OFF delay and rising time of SiC MOSFETS are also considered, and only the non-ZVS region is depicted in Fig. 12. It should be noted that $t_{ext}(m)$ is equal to zero at the ZVS region. k_L represents the inductor ripple

coefficient which can be defined as follows:

$$\begin{cases} i_{\mathrm{L}}(t_{\mathrm{m0}}) = (1+k_{\mathrm{L}}) \cdot i_{\mathrm{g}}(m) \\ i_{\mathrm{L}}(t_{\mathrm{m5}}) = (1-k_{\mathrm{L}}) \cdot i_{\mathrm{g}}(m) \end{cases} \tag{15}$$

where $i_{\mathrm{g}}(m)$ represents the grid-tied current during the mth switching period, which is equal to the average inductor current during the mth switching period.

$t_{\mathrm{d(OFF)}}$ and t_{f} represent the turn-OFF delay time and falling time of SiC MOSFETS, respectively, which can be extracted from datasheets. $t_{\mathrm{vsb}}(m)$ represents the calculated preliminary off-time of S_1. $t_{\mathrm{ON}}(m)$ represents the calculated on-time of S_1. $t_{\mathrm{OFF}}(m)$ represents the compensated OFF-time of S_1. $t_{\mathrm{ext}}(m)$ represents the compensated turn-OFF extension time of S_3. $t_{dead\_theo}(m)$ represents the theoretical deadtime without discrete deviation, and $t_{\mathrm{dead}}(m)$ represents the compensated deadtime. The conduction energy loss expressions of switches can be described as follows:

$$\begin{cases} W_{\mathrm{conduction-S1}}(t) = \int_0^{t_{\mathrm{on}}(m)} [i_{\mathrm{ds1}}(t)]^2 R_{\mathrm{ds(on)}} \mathrm{d}t \\ W_{\mathrm{conduction-S2}}(t) = \int_0^{t_{\mathrm{on}}(m)+t_{\mathrm{vsb}}(m)} [i_{\mathrm{ds2}}(t)]^2 R_{\mathrm{ds(on)}} \mathrm{d}t \\ W_{\mathrm{conduction-S3}}(t) = \int_0^{t_{\mathrm{ext}}(m)} [i_{\mathrm{ds3}}(t)]^2 R_{\mathrm{ds(on)}} \mathrm{d}t \end{cases} \tag{16}$$

where $R_{\mathrm{DS(ON)}}$ represents the ON-state resistance that can be extracted from the datasheet. $i_{\mathrm{ds}}(t)$ is the conduction current.

Based on (15) and (16), during the mth switching period, the conduction energy loss of switches is calculated as

$$\begin{cases} W_{\mathrm{conduction-S1}}(m) = \left[\sqrt{1+\frac{1}{3}k_{\mathrm{L}}^2} \cdot i_{\mathrm{o}}(m)\right]^2 R_{\mathrm{ds(on)}} t_{\mathrm{on}}(m) \\ W_{\mathrm{conduction-S2}}(m) = \left[\sqrt{1+\frac{1}{3}k_{\mathrm{L}}^2} \cdot i_{\mathrm{o}}(m)\right]^2 R_{\mathrm{ds(on)}} (t_{\mathrm{on}}(m) + t_{\mathrm{vsb}}(m)) \\ W_{\mathrm{conduction-S3}}(m) = \left[\frac{i_{\mathrm{L}}(t_{\mathrm{m5}})}{\sqrt{3}}\right]^2 R_{\mathrm{ds(on)}} t_{\mathrm{ext}}(m). \end{cases} \tag{17}$$

Similarly, the conduction energy loss of D_1 and D_2 during the mth switching period is calculated as

$$\begin{cases} W_{\mathrm{conduction-D1}}(m) = \frac{1}{2} i_{\mathrm{L}}(t_{\mathrm{m0}}) U_{\mathrm{F}} t_{\mathrm{vsb}}(m) \\ W_{\mathrm{conduction-D2}}(m) = \frac{1}{2} i_{\mathrm{L}}(t_{\mathrm{m5}}) U_{\mathrm{F}} t_{\mathrm{ext}}(m) \end{cases} \tag{18}$$

where U_{F} represents the forward voltage of the SiC Schottky diodes, which can also be extracted from the datasheet.

From Fig. 12, the turn-OFF energy loss of S_1 and S_3 during the mth switching period can be calculated as follows:

$$\begin{cases} W_{\mathrm{turn-off-S1}}(m) = \int_0^{t_{\mathrm{d(off)}}} u_{\mathrm{ds1}}(t) \cdot i_{\mathrm{L}}(t_{\mathrm{m0}}) \mathrm{d}t \\ \qquad\qquad + \int_0^{t_{\mathrm{f}}} i_{\mathrm{ds1}}(t) \frac{U_{\mathrm{dc}}}{2} \mathrm{d}t \\ W_{\mathrm{turn-off-S3}}(m) = \int_0^{t_{\mathrm{d(off)}}} u_{\mathrm{ds3}}(t) \cdot i_{\mathrm{L}}(t_{\mathrm{m5}}) \mathrm{d}t \\ \qquad\qquad + \int_0^{t_{\mathrm{f}}} i_{\mathrm{ds3}}(t) \frac{U_{\mathrm{dc}}}{2} \mathrm{d}t. \end{cases} \tag{19}$$

Furthermore, the abovementioned equation can be solved as

$$\begin{cases} W_{\mathrm{turn-off-S1}}(m) = \frac{1}{4} U_{\mathrm{dc}} i_{\mathrm{L}}(t_{\mathrm{m0}}) (t_{\mathrm{d(off)}} + t_{\mathrm{r}}) \\ W_{\mathrm{turn-off-S3}}(m) = \frac{1}{4} U_{\mathrm{dc}} i_{\mathrm{L}}(t_{\mathrm{m5}}) (t_{\mathrm{d(off)}} + t_{\mathrm{f}}). \end{cases} \tag{20}$$

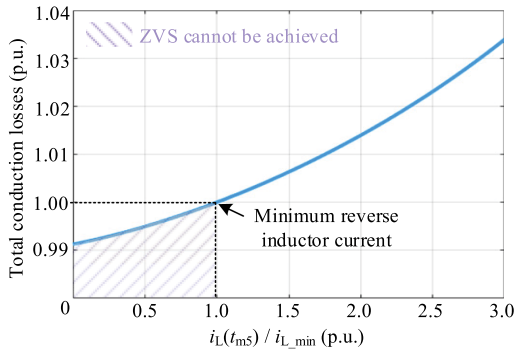

Fig. 13. Total conduction losses with different the reverse current.

For the postresonance energy loss, based on the previous calculation method, it can be expressed as follows:

$$W_{\mathrm{PostRes}}(m) = \frac{1}{2} (i_{\mathrm{L}}(t_{\mathrm{m9}}) - i_{\mathrm{L}}(t_{\mathrm{m8}})) \times (t_{\mathrm{dead}}(m) - t_{\mathrm{dead\_theo}}(m)) U_{\mathrm{FS}} \tag{21}$$

where U_{FS} is the forward voltage of the body diode. $i_{\mathrm{L}}(t_{\mathrm{m8}})$ can be regarded as $i_{\mathrm{L}}(t_{\mathrm{m5}})$, and $i_{\mathrm{L}}(t_{\mathrm{m9}})$ can be calculated by (3).

Based on Fig. 10, the number of the switching period included within one control period k_{sw}, and the number of the digital control period within a half fundamental period, k_{c} can be calculated as follows:

$$k_{\mathrm{sw}}(t) = \left\lceil \frac{f_{\mathrm{sw}}(t)}{f_{\mathrm{c}}} \right\rceil, k_{\mathrm{c}} = \left\lceil \frac{f_{\mathrm{c}}}{2 f_{\mathrm{g}}} \right\rceil \tag{22}$$

where $\lceil g(x) \rceil$ indicates the top integral of $g(x)$. Therefore, the conduction loss of all switches, the turn-OFF loss of S_1 and S_3, and the postresonance loss can be derived as follows:

$$\begin{cases} P_{\mathrm{conduction}-x} = \frac{1}{T_{\mathrm{g}}} \sum_{n=1}^{n=k_{\mathrm{c}}} \left(W_{\mathrm{conduction}-x} \left(\frac{n}{f_{\mathrm{c}}}\right) \cdot k_{\mathrm{sw}} \left(\frac{n}{f_{\mathrm{c}}}\right) \right) \\ P_{\mathrm{turn-off}-y} = \frac{1}{T_{\mathrm{g}}} \sum_{n=1}^{n=k_{\mathrm{c}}} \left(W_{\mathrm{turn-off}-y} \left(\frac{n}{f_{\mathrm{c}}}\right) \cdot k_{\mathrm{sw}} \left(\frac{n}{f_{\mathrm{c}}}\right) \right) \\ P_{\mathrm{PostRes}} = \frac{1}{T_{\mathrm{g}}} \sum_{n=1}^{n=k_{\mathrm{c}}} \left(W_{\mathrm{PostRes}} \left(\frac{n}{f_{\mathrm{c}}}\right) \cdot k_{\mathrm{sw}} \left(\frac{n}{f_{\mathrm{c}}}\right) \right) \end{cases} \tag{23}$$

where $x = S_1$, S_2, S_3, D_1, and D_2. $y = S_1$ and S_3. T_{g} is the fundamental period of the utility grid. At the negative half period, the power loss of switches and diodes can also be calculated by the abovementioned equations.

B. Conduction Loss With Different Reverse Inductor Current

Based on (23), for $i_{\mathrm{L}}(t_{\mathrm{m5}})$ other than the minimum current derived in (8), the total conduction loss variation range can be plotted in Fig. 13, where the x-axis is the ratio of $i_{\mathrm{L}}(t_{\mathrm{m5}})$ to the minimum current derived in (8).

From Fig. 13, it is clear that the total conduction loss is increased with the increase of the reverse current. However, when the x-axis value is lower than 1, as purple shadows in Fig. 13, the reverse current is not higher enough to realize the ZVS of S_1. As a result, the switching loss is increased significantly even if the conduction loss is lower under this condition. Therefore,

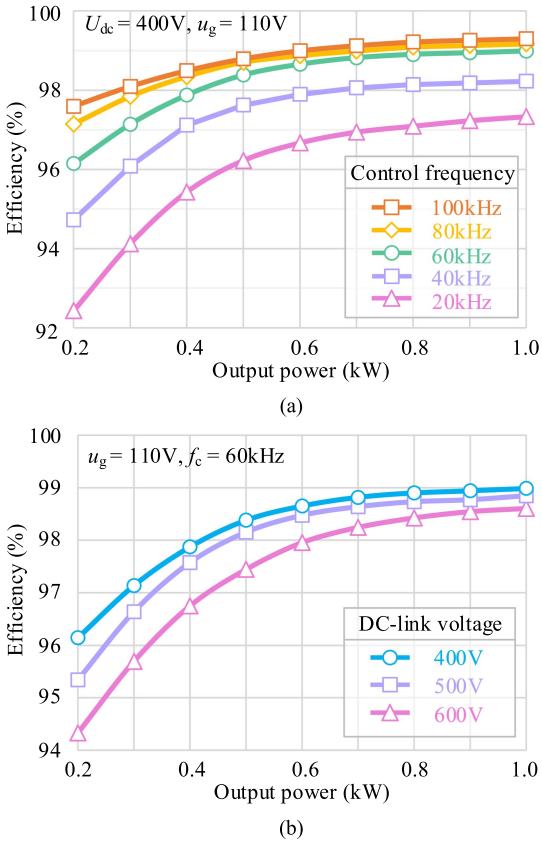

Fig. 14. Efficiency comparison with different control frequencies and DC-link voltages. (a) Efficiency comparison with different control frequencies under the 400 V DC-link voltage. (b) Efficiency comparison with different DC-link voltages at 60 kHz control frequency.

the conduction loss can be minimized when the reverse current is equal to (8).

C. Design of the Digital Control Frequency

Based on the power loss calculation model, the efficiencies with compensated t_{OFF} and t_{dead} under different digital control frequencies can be evaluated. The efficiency curves of the proposed scheme with different digital control frequencies is drawn in Fig. 14(a). The used parameters are listed in Table II.

From Fig. 14(a), it can be seen that the overall efficiency is improved when the digital control frequency, f_c is raised from 20 to 60 kHz. It is because the increase of control frequency decreases the discrete deviation. As a result, the additional power loss caused by discrete deviation is reduced accordingly. However, the efficiency improvement is not significant when f_c is higher than 60 kHz, because the compensated discrete deviation is very small when there are fewer than two switching periods during one control period. However, serious discrete deviation still results in additional power loss when there are more than three switching periods during one control period. Thus, the average switching frequency under different output power can be depicted by using the parameters listed in Table II, as shown in Fig. 15, which can be used to evaluate the relationship between the digital control frequency and efficiency. For instance, the

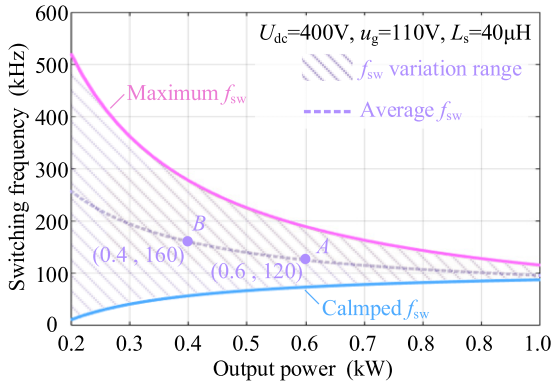

Fig. 15. Average switching frequencies with different output power.

output power and average switching frequency of point *A* in Fig. 15 are equal to 0.6 kW and 120 kHz, respectively. It can be concluded that when the output power is higher than 0.6 kW, the efficiencies are similar under $f_c > 60$ kHz conditions. It is consistent with the curves shown in Fig. 14(a). When the output power is higher than 0.6 kW, the efficiencies are similar with different control frequencies, such as 60, 80, and 100 kHz. Besides, from point *B*, it can also be concluded that when the output power is higher than 0.4 kW, the efficiencies are similar under $f_c > 80$ kHz conditions. It is also consistent with the curves shown in Fig. 14(a). When the output power is higher than 0.4 kW, the efficiencies are similar with different control frequencies, such as 80 and 100 kHz. Therefore, when f_c is the same as (24) and $P > z$, the efficiency is insignificant depression:

$$f_c = \frac{1}{2\pi}\int_0^{\pi} f_{sw}(t)\,|_{P=z}\,\mathrm{d}t \tag{24}$$

where $f_{sw}(t)|_{P=z}$ represents the switching frequency when the output power equals to z, $z \in (0, P_r)$, P_r represents the rated output power.

By using (24), the minimum digital control frequency without significant efficiency depression at any output power can be obtained. However, the digital control frequency should also be considered with the requirement of controller resources. In practice, it is recommended to calculate the digital control frequency in (24) with $z > 0.5P_r$ to ensure the controller has sufficient resources to perform protection, communication, display, and other functions. In this article, 60 kHz is selected.

Further, efficiency curves with different dc-link voltages at the 60 kHz control frequency are depicted in Fig. 14(b). The maximum calculated efficiency is 98.97% with $U_{dc} = 400$ V. Fortunately, the efficiency decrease is not significant with the descending of modulation indices. Thus, the designed digital control frequency has good adaptability.

D. Power Losses Comparison

The calculated power loss distribution of the 3L-NPC inverter with the proposed control scheme with variable t_{dead}, CBCM control scheme with −1A reverse current and 650 ns deadtime, and the ZCD-based scheme is calculated, respectively. The

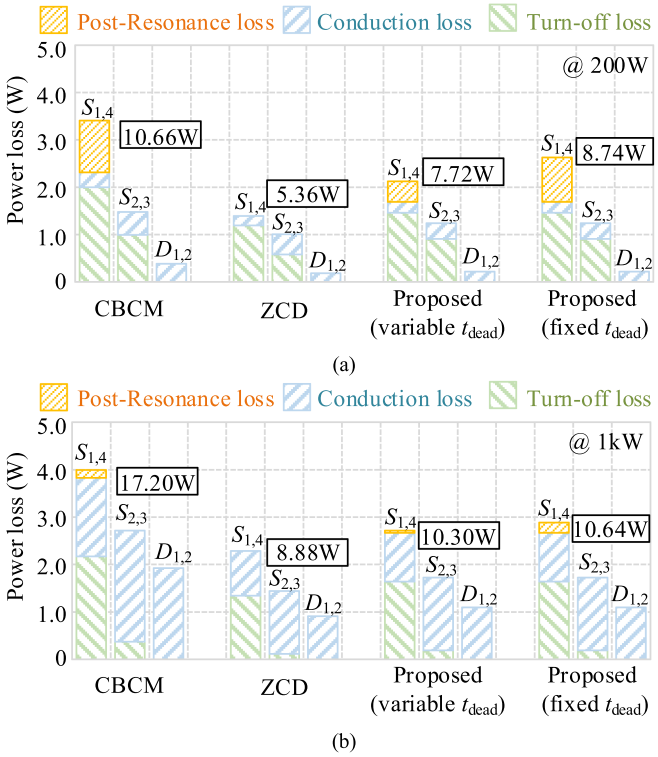

Fig. 16. Theoretical power losses comparison with different control schemes. (a) Under light load (200 W). (b) Under heavy load (1 kW).

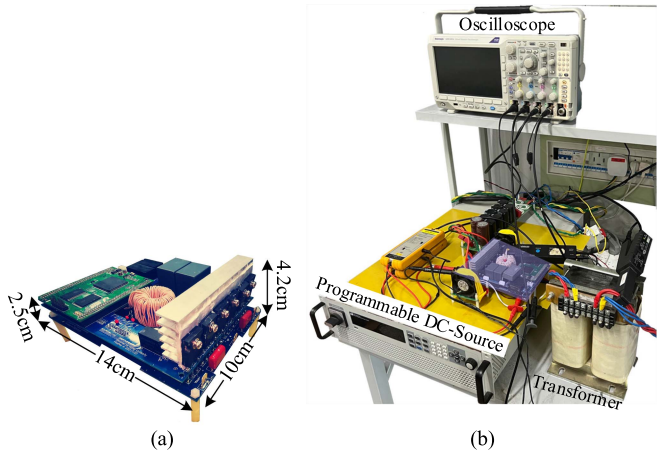

Fig. 17. Photograph of the experimental setup. (a) 1 kW 3L-NPC inverter prototype. (b) Complete experimental setup.

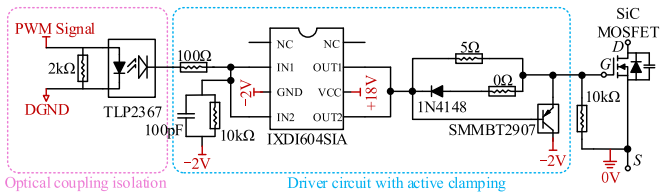

Fig. 18. Schematic diagram of gate driver circuit with detailed parameters.

parameters used are listed in Table II. The power loss distribution is shown in Fig. 16. Because of the symmetry of the modulation strategy, the power losses of S_1, S_2, and D_1 are equal to those of S_4, S_3, and D_2, respectively. Therefore, in Fig. 16, the same power loss is represented by one histogram.

According to Fig. 16, compared with the CBCM scheme, the turn-OFF loss of S_1, conduction loss of S_1 and S_2, and the postresonance loss of the proposed control scheme are reduced. It is because the rms inductor current and deadtime are decreased. Therefore, the proposed control scheme has higher efficiency than the CBCM scheme. At the same time, the reverse current of the proposed scheme cannot be precisely controlled as (8) because of the discreteness of the digital control method. In contrast, for the ZCD-based method, the reverse current can always be precisely controlled as (8) by precisely setting the input signal of the current comparator. As a result, the overall efficiency of the proposed control scheme is 0.3% lower than that of the ZCD-based scheme. It is worth mentioning that when a fixed $t_{\rm dead}$ is used for the proposed scheme, its total loss in Fig. 16(a) and (b) will be increased by 1.02 W and 0.34 W, respectively. Therefore, a variable $t_{\rm dead}$ for the proposed scheme can improve the efficiency by 0.5% under light load conditions.

V. Experimental Results

A 1 kW 3L-NPC inverter prototype was built to conduct experiments, as shown in Fig. 17. The specifications of the prototype are listed in Table II. A power analyzer WT1800 was used to measure the efficiency and the current THD. The control scheme of the prototype was implemented based on the DSP TMS320F28377S. A programable dc-source IT6012B-800-40 is used to supply dc power. The schematic diagram of gate driver circuit with detailed parameters is shown in Fig. 18. The high-speed optocoupler TLP2367 isolates PWM signals. Then, the SiC MOSFETS are driven by high-speed gate driver IXDI604SIA. Finally, the active clamping circuit is applied to turn off the SiC MOSFETS reliably.

A. Verification of the Proposed Scheme

Experimental waveforms of the proposed scheme are shown in Fig. 19, where $u_{\rm ds1}$ represents the drain-source voltage of S_1. $i_{\rm L}$ and $i_{\rm g}$ represent the inductor current and grid-tied current, respectively. $u_{\rm g}$ is the grid voltage. Fig. 19(a) shows that the inverter is operated at the CRM mode without the ZCD circuit. The measured gird-tied current THD is 4.25%. It indicates that the proposed control scheme has good steady-state performance. Besides, the dynamic response of the proposed control scheme is shown in Fig. 19(b). The output power is stepped up from 0.5 to 1 kW, then to 0.5 kW after 0.1 s.

B. Verification of the Digital Control Frequency Design

The efficiencies of the proposed control scheme with different digital control frequencies are measured, as shown in Fig. 20(a). The solid lines represent the measured experimental results, and the dashed lines represent the calculation results. It can be seen that the overall efficiency is increased with the increase of the digital control frequency. Moreover, when the output power is lower than 0.6 kW, efficiencies with the 60 kHz digital

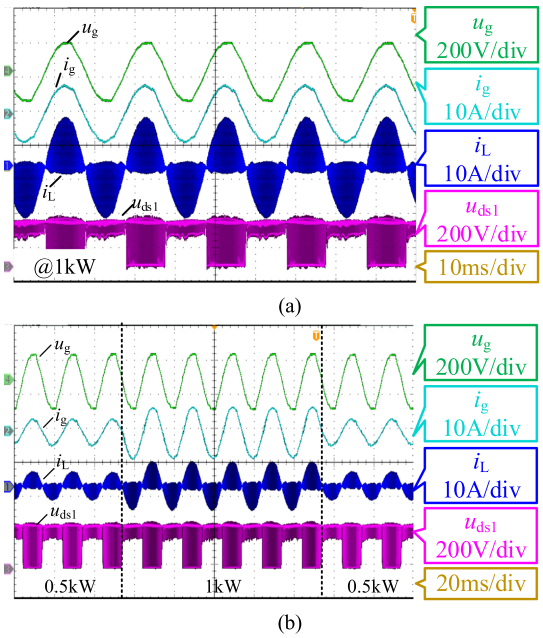

Fig. 19. Experimental waveforms with the proposed control scheme. (a) Steady state. (b) Dynamic response of output current step change.

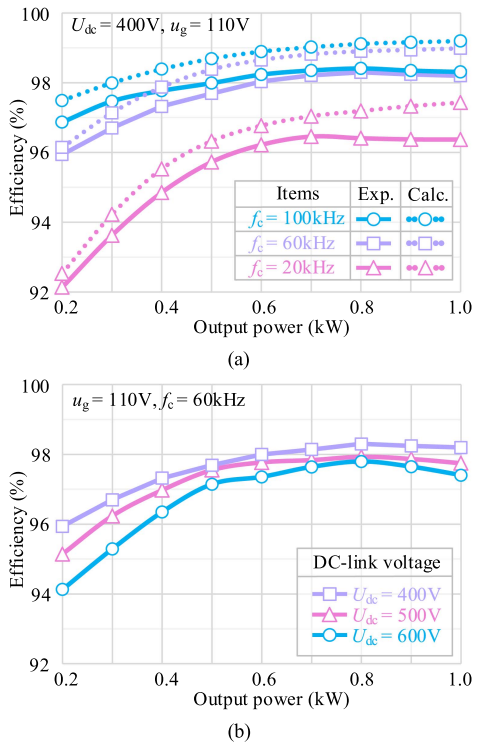

Fig. 20. Efficiency comparison of the proposed control scheme. (a) With different control frequencies. (b) Under different MIs with f_c = 60 kHz.

control frequency are slightly lower than those of the 100 kHz digital control frequency. When the output power is higher than 0.6 kW, efficiencies with the 60 kHz digital control frequency and the 100 kHz digital control frequency are almost the same. The experimental results are consistent with the analysis in Section IV-B. From Fig. 20(b), it can be seen that the efficiencies

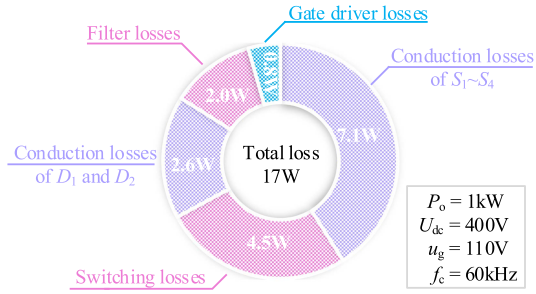

Fig. 21. Estimated power loss distribution of the proposed control scheme.

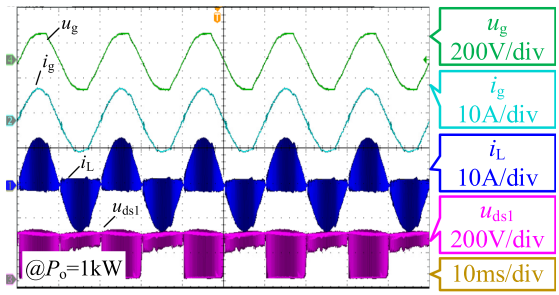

Fig. 22. Steady-state experimental waveforms with the CBCM scheme.

under different dc-link voltages are also similar, which indicates that the optimal designed digital control frequency has good adaptability. The measured efficiency under the rated power with 60 kHz digital control frequency is 98.3%, which is lower than the calculation value. It is because the filter inductor loss is not calculated in Section IV. However, the power loss distribution cannot be accurately measured under experimental conditions. Therefore, the power loss distribution of the proposed scheme under the rated power is estimated and shown in Fig. 21.

C. Comparison Between the Proposed Scheme and CBCM

Furthermore, CBCM experiments were carried out for comparison. The steady-state waveforms are shown in Fig. 22. The detailed switching actions using the proposed scheme and the CBCM at the positive half period are shown in Figs. 23 and 24, respectively.

Fig. 23(a) and (b) shows the measured t_{dead} by using the proposed scheme. It is clear that t_{dead} is dynamically regulated and varied with u_g, and S_1 is ZVS turn-ON during the whole fundamental period, as depicted in Fig. 23(c) and (d). Moreover, from Fig. 23(c), S_1 is turned ON immediately at the non-ZVS region when u_{ds1} goes down to 0. Therefore, it indicates that there is no postresonance loss. But from Fig. 23(d), there is postresonance loss caused by the inevitable discrete deviation mentioned in Section III-C. Furthermore, from Fig. 24(a) and (b), by using the CBCM scheme, S_1 is also ZVS turn-ON with the fixed deadtime during the whole fundamental period. However, from Fig. 24(c) and (d), the fixed deadtime also leads to worse postresonance loss issues compared with the proposed scheme. Thus, the proposed scheme features lower postresonance, as demonstrated in Section IV-C.

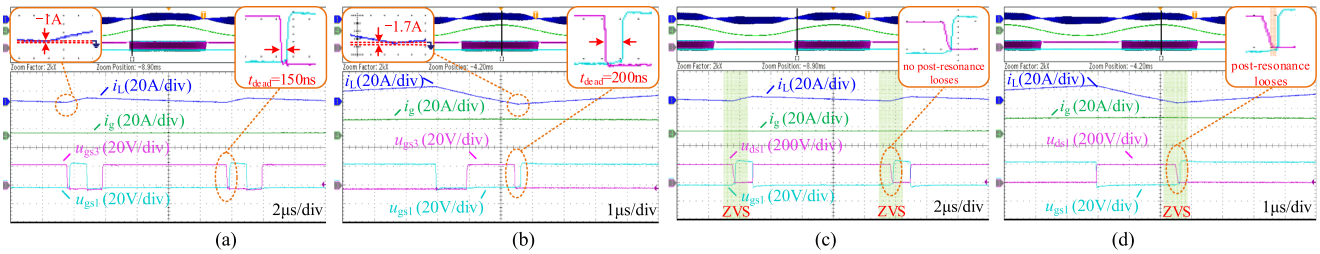

Fig. 23. Detailed switching waveforms at the positive half period with the proposed scheme. (a) Measured deadtime of S_1 and $i_L(t_5)$ at $\omega t = \pi/20$. (b) Measured deadtime of S_1 and $i_L(t_5)$ at $\omega t = \pi/2$. (c) ZVS turn-ON of S_1 at $\omega t = \pi/20$. (d) ZVS turn-ON of S_1 at $\omega t = \pi/2$.

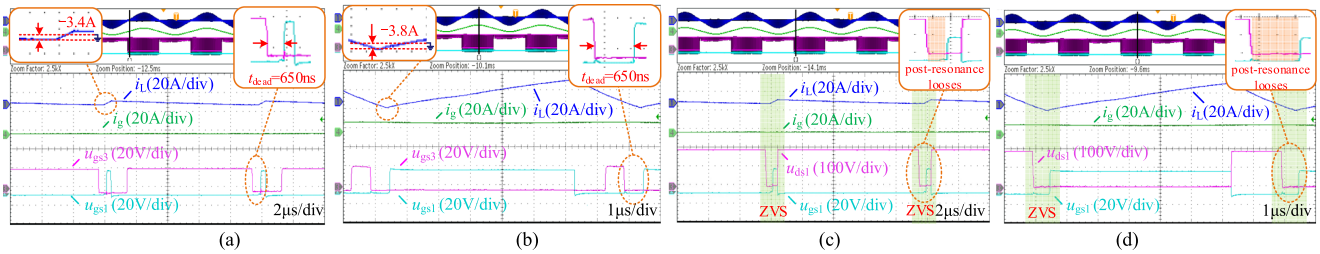

Fig. 24. Detailed switching waveforms at the positive half period with the CBCM scheme. (a) Measured deadtime of S_1 and $i_L(t_5)$ at $\omega t = \pi/20$. (b) Measured deadtime of S_1 and $i_L(t_5)$ at $\omega t = \pi/2$. (c) ZVS implementation of S_1 at $\omega t = \pi/20$. (d) ZVS implementation of S_1 at $\omega t = \pi/2$.

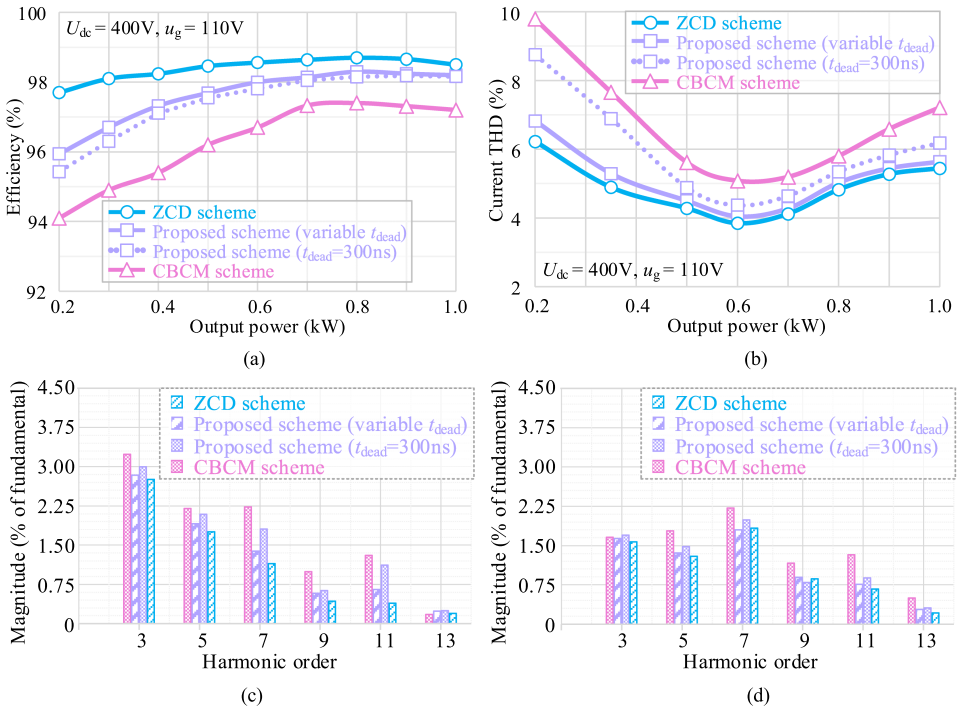

Fig. 25. Comparison of the proposed control scheme (variable $t_{\rm dead}$ and constant $t_{\rm dead}$ with $f_{\rm c}$ = 60 kHz), the ZCD-based scheme ($f_{\rm c}$ = 300 kHz), and the CBCM scheme ($f_{\rm c}$ = 60 kHz): (a) Efficiency comparison. (b) Current THD comparison. (c) Harmonic spectrum at 200 W. (d) Harmonic spectrum at 1 kW.

Besides, the minimum inductor current of the proposed control scheme and the CBCM scheme are also measured during one switching period, as shown in Figs. 23(a) and (b) and 24(a) and (b), respectively. According to Fig. 23(a) and (b) and Fig. 24(a) and (b), it is clear that the minimum inductor current of the proposed control scheme is much higher than that of the CBCM scheme. Since the average inductor current of both control schemes is equal, the higher minimum inductor current means the lower rms inductor current. Thus, the proposed scheme also features lower turn-OFF loss and conduction loss of active switches, as demonstrated in Section IV-C. Therefore, the efficiency of the proposed scheme is

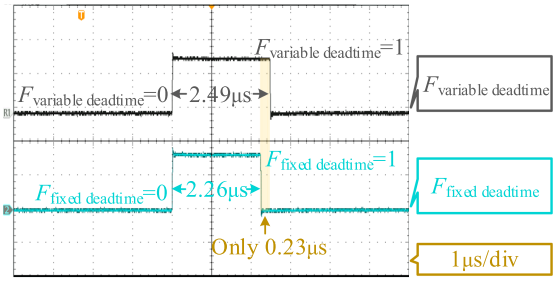

Fig. 26. Measured program execution time of the proposed scheme by using fixed t_{dead} and variable t_{dead}.

higher than that of the CBCM scheme, which can be verified by Fig. 25(a).

Moreover, the measured efficiencies and current THD with different control schemes are depicted in Fig. 25. It should be noted that the digital control frequency of the proposed scheme and the CBCM scheme is equal to 60 kHz. The digital control frequency of the ZCD-based scheme is set as 300 kHz, referring to [17]. From Fig. 25(a), the ZCD-based scheme has the highest efficiency. Thanks to the well-designed digital control frequency, the proposed control scheme features better efficiency than that of the CBCM scheme. On the other hand, from Fig. 25(b) to (d), the current THD and low-order harmonics of the proposed control scheme are the same as the ZCD-based scheme and better than those of the CBCM scheme. These results demonstrate that the CRM-based inverter with the proposed control scheme achieves a tradeoff between hardware cost and performance.

D. Advantage Verification of the Variable Deadtime

The efficiency and current THD of the proposed scheme with a fixed deadtime are also measured to verify the advantages of the variable deadtime. According to the parameters listed in Table II, the value of the fixed t_{dead} is set as 300 ns. From Fig. 25(a), it is clear that compared with the fixed deadtime, the efficiency is increased by 0.48% with the variable deadtime under light load conditions, which is consistent with the theoretical analysis in Section IV-C. Besides, under light load conditions, the negative effect of the deadtime on current THD becomes more apparent due to the higher switching frequency. Therefore, the variable deadtime can improve the current THD under light load conditions, as shown in Fig. 25(b).

Finally, the measured program execution times of the proposed scheme with the fixed deadtime and the variable deadtime are presented in Fig. 26, where F_X represents the running signal of the program. When F_X is set to 1, the program X is running ($X =$ variable deadtime or fixed deadtime). The clock frequency of TMS320F28377S is 200 MHz. From Fig. 26, the program execution time of the variable deadtime and the fixed deadtime is 2.49 μs and 2.26 μs, respectively. It indicates that employing the variable deadtime will not bring a significant calculation burden to the digital controller. It is because the calculation equation of t_{off} and t_{dead} are similar. Thus, the variables generated when calculating t_{OFF} can be directly used to calculate t_{dead}, which simplifies the calculation process of t_{dead}. Therefore, it is valuable to employ the variable deadtime for the proposed scheme regarding the efficiency and current THD improvement under light load conditions.

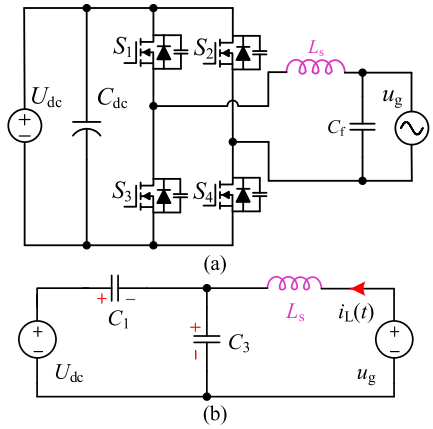

Fig. 27. Topology and equivalent resonance circuit during the deadtime of CRM H-bridge in bipolar mode. (a) Topology. (b) Resonance circuit at the positive half period.

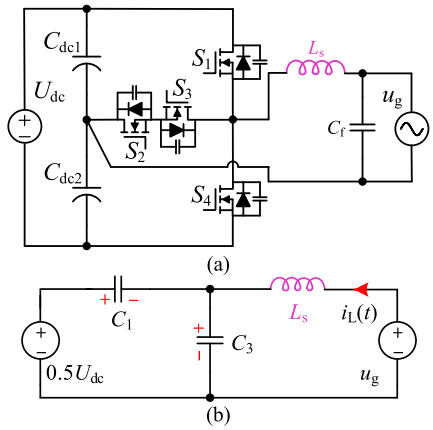

Fig. 28. Topology and equivalent resonance circuit during the deadtime of CRM 3L-THBI. (a) Topology. (b) Resonance circuit at the positive half period.

VI. Discussion

A. Applicability of the Proposed Method in Other Topologies

First, for other single-phase CRM grid-tied inverters, such as the full-bridge inverter with the bipolar modulation and the T-type half-bridge inverter, their deadtime and OFF-time for achieving ZVS turn-ON can be obtained from their equivalent resonance circuit. The topology and the deadtime equivalent resonance circuit of the H-bridge and T-type half-bridge inverters are shown in Figs. 27 and 28. From Figs. 27 and 28, it can be seen that the equivalent resonance circuit of the H-bridge inverter and T-type half-bridge inverter are consistent with Fig. 6, and the difference between them is only the input dc-link voltage. Therefore, for most single-phase CRM grid-tied inverters, the variable deadtime and OFF-time can be calculated by the same formula regardless of the circuit topology. Incidentally, the equivalent resonance circuit during the deadtime of the H-bridge inverter

TABLE III
COMPARISON OF DIFFERENT ZVS METHODS

Method	Topology (With what additional circuits)	ZVS range	RMS inductor current	Deadtime	Digital controller resource requirement	Rated power	Efficiency	Filter parameters and switching frequency	Current THD
ZCD+DPWM in [17]	3Φ H-bridge (ZCD and control winding)	Partial ZVS	Lowest	Variable	High	12.5kW	98.9% (@10kW)	*LCL* filter 3.55μH/1.2μF/6.8μH 300kHz~530kHz	3.85% Ideal grid (@10kW)
ZVS method in [19]	1Φ H-bridge (ZCD)	Partial ZVS	Moderate	Fixed	High	2.4kW	98% (@2kW)	*L* filter 3.5μH × 2 300kHz~1MHz	Unknown
Hysteresis-based ZVS [31]	3Φ H-bridge (High-bandwidth comparator)	Full	Lowest	Fixed	High	5kW	98.5% (@5kW)	*LCL* filter 20μH/2.4μF/Unknown 200kHz~400kHz	1.5% Ideal grid (@5kW)
Hybrid TCM control [21]	1Φ H-bridge (ZCD)	Full	High	Fixed	Moderate	1kW	97.9% (@1kW)	*LC* filter 34μH/3.3μF 300kHz~3MHz	1.3% Resistive load (@600W)
Dual-Mode BCM [29]	3Φ H-bridge (High-bandwidth comparator)	Full	Moderate	Fixed	Moderate	400W	98.5 (@400W)	*LC* filter 270μH/1μF 40kHz~150kHz	2.5% Resistive load (@270W)
ZVS method in [18]	Totem pole PFC (ZCD and control winding)	Full	Low	Fixed	High	6.6kW	98.5% (@3.3kW)	*L* filter Unknown 300kHz~400kHz	3% Ideal grid (@3.3kW)
Trapezoidal wave control [22]	1Φ five-level full bridge (High-bandwidth comparator)	Full	Low	Fixed	High	1kW	99.1% (@600W)	*LCL* filter 120μH/2μF/200μH 50kHz~200kHz	4.2% Ideal grid (@1kW)
CBCM [28]	1Φ H-bridge (None)	Full	Highest	Fixed	Moderate	150W	97.5% (@150W)	*LC* filter 561μH/1μF 15kHz~41kH	2.4% Resistive load (@150W)
Variable frequency SVPWM [23]	3Φ H-bridge (None)	Full	High	Fixed	High	3.5kW	98.7% (@1.75kW)	*LCL* filter 10.3μH/4.7μF/20μH 100kHz~180kHz	3.2% Resistive load (@3.5kW)
Current ripple predictive + DPWM [25]	3Φ H-bridge (None)	Full	High	Fixed	High	3.5kW	99% (@2.8kW)	*LCL* filter 14μH/4.7μF/50μH 135kHz~165kHz	Unknown
ZVS method in [30]	1Φ dual-buck full bridge (None)	Full	High	Fixed	Moderate	1kW	Unknown	*L* filter 16μH × 2 120kHz~800kHz	Unknown
This paper	1Φ three-level half bridge (None)	Full	Low	Variable	Low	1kW	98.3% (@0.8kW)	*LC* filter (40μH/6.6μF) 100kHz~300kHz	3.8% Utility grid (@600W)

Note: I): 3Φ represents three phase and 1Φ represents single phase
II): The LCL filter parameters is listed as converter-side inductor / filter capacitor / grid-side inductor.

in unipolar mode is similar to that of the bipolar modulation. Thus, the proposed methodology is also suitable for the H-bridge inverter in unipolar mode. Second, from (24), the calculation procedure of the digital control frequency is also independent of circuit topology. In conclusion, the proposed method is suitable for any single-phase CRM grid-tied inverters.

For the three-phase grid-tied inverters, the equivalent resonance circuit for achieving ZVS turn-ON becomes a four-order circuit rather than a two-order circuit because of the coupling between the three phases [17]. Since the equivalent resonance circuit of the three-phase three-wire (3P-3W) CRM grid-tied inverters is different from that of the single-phase CRM grid-tied inverters, and the proposed method cannot be applied to the 3P-3W CRM grid-tied inverters. Fortunately, the proposed method can still be employed to the decoupled three-phase topologies, such as the three-phase four-wire full-bridge grid-tied inverter.

B. Comparative Study With Existing Methods

A comparison of the different ZVS methods proposed for the inverter is shown in Table III. The comparison is made in terms of additional hardware circuits, ZVS range, rms inductor current, deadtime for achieving ZVS, digital controller operation resource requirement, rated power, peak efficiency, and output current THD. From Table III, it can be seen that the efficiencies

of the ZCD-based methods are usually high. However, the cost is also increased by the high-precision components. In addition, the minimum reverse inductor current and deadtime for achieving ZVS are rarely considered in existing digital-based control. Furthermore, most existing methods have a high requirement for digital controller operation resources. Fortunately, the proposed scheme has a tradeoff between high efficiency and low required digital controller operation resources.

VII. Conclusion

This article proposes a fully digital soft-switching control with variable OFF-time and deadtime and well-designed digital control frequency. Analysis and experimental results demonstrate the following features of the proposed control scheme.

1) The proposed fully digital control scheme can achieve ZVS turn-ON of switches without the ZCD circuit. Thus, it lowers the hardware cost and the complexity of control circuits.
2) The proposed design guideline of the digital control frequency effectively achieves high efficiency and lowers the required digital controller operation resources.
3) Compared with the CBCM scheme, the proposed method has better efficiency and current THD performance.
4) Compared with the fixed deadtime, the efficiency and current THD are enhanced under light load conditions.

The proposed control scheme achieves the tradeoff between high efficiency and low hardware cost, which can be employed in single-phase inverters for high efficiency and power density.

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