Termination Design Optimization of High-Current PCB-Winding Matrix Transformers

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***Abstract*—Due to their high power densities and efficiencies, high-frequency resonant converters using printed circuit board (PCB)-based transformers are gaining popularity in applications, such as datacenters and automotive. However, in such high-frequency, high-current applications, the PCB transformer's termination losses may become significant if not designed properly. This article aims to highlight multiple design considerations to minimize the termination losses while designing a PCB-based matrix transformer. Various termination techniques for full-bridge and center-tap secondary-rectifiers are studied, and it is shown that placing the devices and output filter capacitors directly on the secondary windings results in the lowest termination loss. However, this results in the output filter capacitors being split between the two secondary PCB layers, resulting in a long paralleling loop between them. It is demonstrated that the parasitic inductance of this loop undergoes parallel resonance with the filter capacitors, resulting in high circulating currents and, hence, high termination losses. Methods to mitigate this effect at the *LLC* converter's switching frequency are discussed. Improvements of the proposed terminations are demonstrated by modeling and measuring the transformer's ac resistance. Furthermore, the *LLC* converters' efficiency improvements are also showcased with the improved terminations.**

***Index Terms*—High-frequency dc–dc, planar transformers, resonant converters, termination.**

I. Introduction

ADVANCEMENTS in power converters for industrial applications have propelled power conversion performances to ever-increasing pinnacles in recent years. With the advent of wide-bandgap devices with better figures-of-merit, the switching frequencies are also being pushed, resulting in higher efficiencies and power densities. With reliable converter topologies being well established for many industrial applications, research efforts must also be focused on improving the design practice for existing topologies, in order to improve efficiency and reliability. Many industrial applications, such as datacenters, electric vehicles, light-emitting diode (LED) drivers, and photovoltaic systems require isolated dc/dc stages running at high frequencies, for which *LLC* resonant converters are desirable candidates [1]. Their ability to step down high voltages, achieve zero-voltage switching (ZVS) over the entire load range, have lower turn-OFF current for the primary switches (compared to hard-switching pulsewidth modulation converters), and achieve zero-current switching (ZCS) for the synchronous rectifiers (SRs) make them suitable for such applications [2].

For high-output current applications, several important challenges must be addressed, including paralleling multiple secondary devices and secondary windings to distribute the high secondary current and placing the multiple parallel SRs close to the termination to mitigate the secondary winding leakage inductances. To address these issues, the concept of matrix transformers was proposed, wherein the output current can be divided among several smaller elementary transformers whose output sets are connected in parallel, thereby facilitating easier SR termination and reducing the associated losses, as shown in

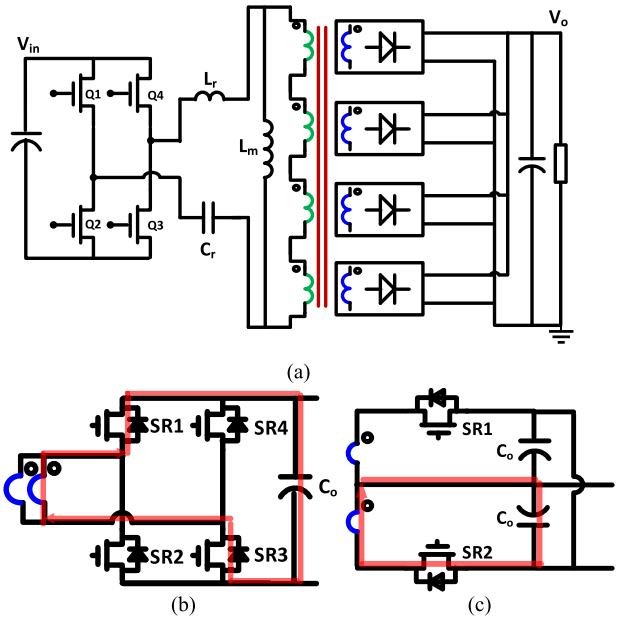

Fig. 1. (a) FB *LLC* converter with matrix transformers and full-wave secondary rectifiers, substituted by either (b) FB rectifier or (c) CT rectifier.

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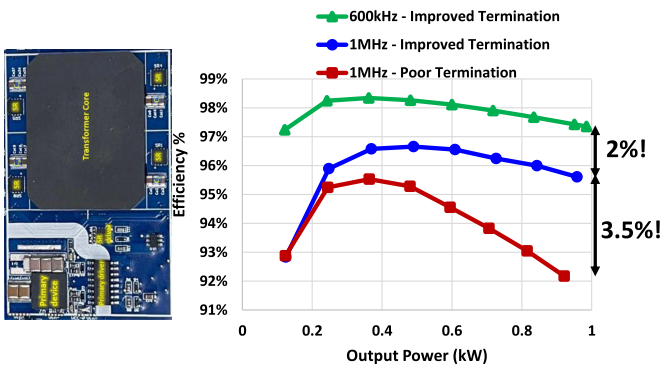

Fig. 2. Measured efficiencies for a 1-kW 400-V/12-V PCB-transformer-based *LLC* converter with different termination designs and switching frequencies.

Fig. 1(a) [3], [4]. Based on the application, the secondary-side full-wave synchronous rectification can either be in a full-bridge (FB) or a center-tap (CT) configuration, as shown in Fig. 1(b) and (c) respectively [5], [6], [7]. The FB rectifiers require $4N_{\text{out}}$ number of devices, where N_{out} is the number of parallel output sets. However, each device only required a maximum voltage rating of the output voltage V_o. On the contrary, the CT configuration requires only $2N_{\text{out}}$ number of devices, resulting in lower switching losses. However, each device requires a voltage rating of $2V_o$, resulting in the devices having higher ON-resistances. Therefore, based on the converter's specifications, either SR configuration is commonly employed.

Moreover, as the magnetic size is reduced, printed circuit board (PCB)-based planar magnetics become relevant. The benefits of switching to PCB winding-based transformers from the traditional litz wire-based transformers are multifold [8]; these include easier manufacturability, strong repeatability, and a larger surface area resulting in low-profile cores and better thermal capabilities. Moreover, the planar magnetic windings can be pushed to higher frequencies, as compared to the traditional litz-wire windings, hence reducing the magnetic core size [9]. However, for high-current applications, multiple winding layers must be paralleled to achieve low dc resistance and prevent overheating.

In high-current, high-frequency applications, designing the secondary SR termination carefully is crucial, as otherwise, it may result in high increments in the transformer's leakage inductance and ac resistance, which in turn results in high conduction losses. Moreover, as shown by the red loops in Fig. 1(b) and (c), the FB and CT SR configurations have different termination loops in one half-cycle of operation, which must be optimized to minimize the termination leakage inductance and ac resistance [10]. Furthermore, paralleling high-current-carrying PCB layers require vias, which must also be designed carefully to minimize via losses [11].

To demonstrate the significance of having a good secondary termination design in high-frequency, high-current PCB-based transformers, Fig. 2 shows the measured efficiencies on a 1-kW 400-V/12-V *LLC* converter with PCB-based matrix transformers. When operating at 1 MHz, the existing secondary termination technique results in very low efficiencies. Improving this termination results in an increase of up to 3.5% efficiency, as will be exhaustively demonstrated in this article. Furthermore, to enhance the performance of the *LLC* converter, the transformer design is tweaked to optimally run at 600 kHz as described in [12], resulting in a further efficiency increase of up to 2%. This article proposes considerations while designing the secondary termination in planar matrix transformers to prevent incurring such extreme losses.

For the purposes of the studies done in this article, a four-leg matrix transformer, as developed by Fei et. al. [13], is used. Moreover, a six-layer PCB is employed, with two layers each for the primary, secondary, and EMI shield windings. For the FB SRs, an 8:1 transformer is implemented, whereas for the CT SRs, a 16:1 transformer is implemented. This way, the impact the termination design has on cases with different numbers of primary turns in each PCB layer is also explored.

This article is an extension of the work presented in [14], where the termination design and optimization for FB rectifiers are discussed. This journal article aims to generalize the analysis to other rectification techniques, thereby proposing an SR termination design guideline in PCB-winding matrix transformers.

The rest of this article is organized as follows. Section II summarizes termination techniques commonly used with FB and CT SRs and compares their performance. Section III then discusses the phenomenon of circulating current between distributed filter capacitors and the implications it has on the transformer ac resistance, with solutions being proposed to mitigate the issue. Section IV verifies the proposed solution with transformer impedance modeling and measurement. The *LLC* converter performance is analyzed and compared in Section V, with conclusions offered in Section VI. Finally, Section VII concludes this article.

II. SR Termination Techniques in Planar Matrix Transformers

In high-frequency, high-current applications, in addition to the winding loss and the core loss, a significant component of the transformer loss is the termination loss. The connection between the SRs, the output filter capacitors, and the secondary layers forms the termination loop and needs to be designed carefully to minimize impedance of the termination loop and, hence, reduce termination loss. Since the termination loops are different in the two cases, the PCB winding arrangements and termination techniques for the FB and CT SRs are studied separately.

A. Center-Tap (CT) Secondary SR

Since CT SRs are typically employed for lower output current applications [13], [15], only one secondary layer conducts in each half-cycle of operation. The PCB-based transformer design and the associated termination challenges were discussed by Huang et al. in [16] and were summarized in this section.

The winding leakage inductance is determined by the magnetomotive force (MMF) between the transformer windings, which depends on how the primary and secondary layers are arranged. Since only one secondary layer conducts current in each half-cycle, the two secondary layers must be placed in the middle two

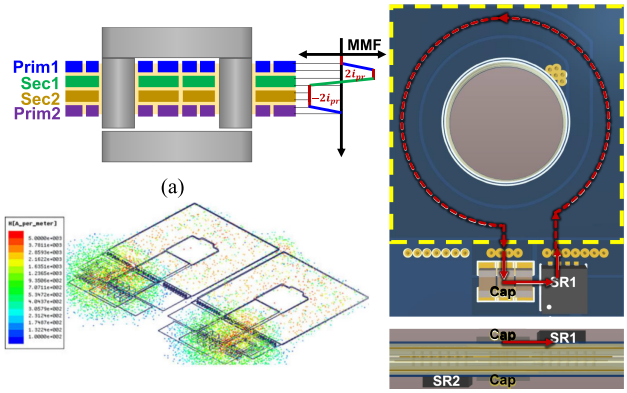

Fig. 3. Winding arrangement with good interleaving but high termination loss. (a) Cross-section view with MMF distribution. (b) Magnetic field intensity plot. (c) Termination layout.

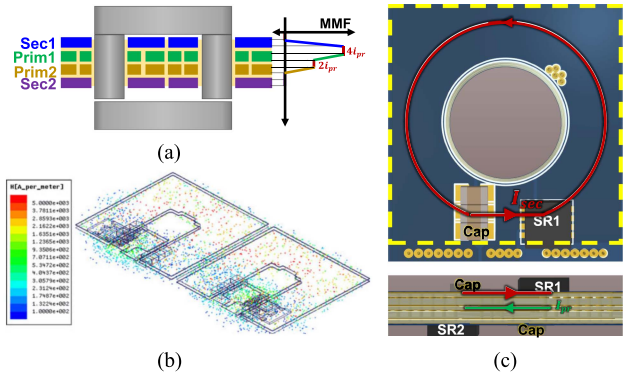

Fig. 4. Winding arrangement with poor interleaving but good termination. (a) Cross-section view with MMF distribution. (b) Magnetic field intensity plot. (c) Termination layout.

layers to achieve perfect interleaving with the primary windings, as shown in Fig. 3(a). The 3-D finite-element analysis (FEA) of the ideal secondary windings (without considering termination effects) results in a low leakage inductance [16].

However, the termination design becomes challenging in this arrangement, as the secondary winding terminals in the middle layers must be connected to the SRs and output filter capacitors on the top and bottom layers using vias, resulting in high via loss. Moreover, the SRs and filter capacitors must be placed outside the transformer area, resulting in a large secondary current loop, as shown by the red arrow (the dotted curves indicate current flowing in the middle layers) in Fig. 3(c). Moreover, there is no interleaving between the primary and secondary currents in the nonoverlapping area outside the transformer [yellow dashed box in Fig. 3(c)]. This causes high flux crowding around the termination in addition to the high via losses from the secondary layers in the middle to the SRs, as shown in Fig. 3(b). As a result of the poor termination, the secondary winding leakage inductance sees a drastic 400% increase, making this winding arrangement an undesirable choice [16].

Clearly, the termination design has a significant impact on the transformer's impedance. Therefore, to improve the termination by eliminating the vias and minimize the termination loop, the secondary layers are moved to the top and bottom layers while moving the primary layers to the middle. This results in the loss of perfect interleaving, as shown by the interwinding MMF distribution in Fig. 4(a). However, the SRs and output filter capacitors can now be placed directly on the secondary windings (inside the dashed yellow box), as shown in Fig. 4(c), resulting in no visible termination loop for the secondary current (red arc) and perfect interleaving between the secondary and primary currents. Fig. 4(b) shows the flux crowding around the termination, which is much lower when compared to Fig. 3(b).

Hence, even with increased leakage inductance of the ideal windings (due to worse interleaving), the significantly improved termination design results in a 65% lower total leakage inductance of the secondary windings [16]. This highlights the importance of the secondary-side termination design, by showing

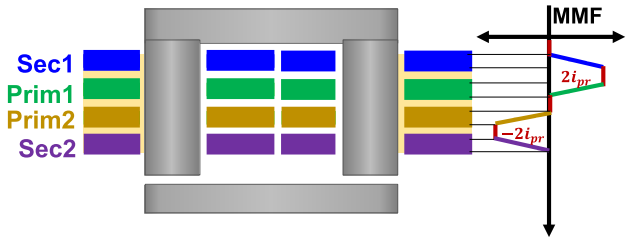

Fig. 5. Cross-section and MMF distribution in the winding arrangement with perfect interleaving for FB SR.

that even with poor interleaving, a better termination can result in significantly lower winding impedances.

B. Full-Bridge (FB) Secondary SR

The 8:1 4-leg matrix transformer with FB SRs can be observed by substituting Fig. 1(b) into the SR blocks in Fig. 1(a). In the case of FB SRs, the two secondary layers are connected in parallel to conduct the high secondary current. This requires additional vias, thereby adding to the transformer impedance. The preferred layer stack-up and MMF distribution are shown in Fig. 5. The two primary layers in series are sandwiched between the two parallel secondary layers. In contrast to the CT SRs case, the benefits of this winding arrangement are twofold: 1) symmetrical MMF distribution across the entire transformer cross-section, and 2) proximity of the secondary layers to the SRs and output capacitors to which they are to be connected. However, placing double the number of SR devices along with the filter capacitors optimally presents a different challenge. Few termination techniques for FB SRs have been proposed by Nabih et al. in [7], as summarized in this section. Fig. 6 shows the termination layout and the 3-D FEA simulated leakage flux distribution for three termination techniques.

Fig. 6(a) shows the lateral loop termination, where two SRs of each half-bridge along with the output filter capacitors, are placed outside each secondary winding (dashed yellow box). The red arrows show the secondary current flowing through the termination. However, as the secondary current leaves the

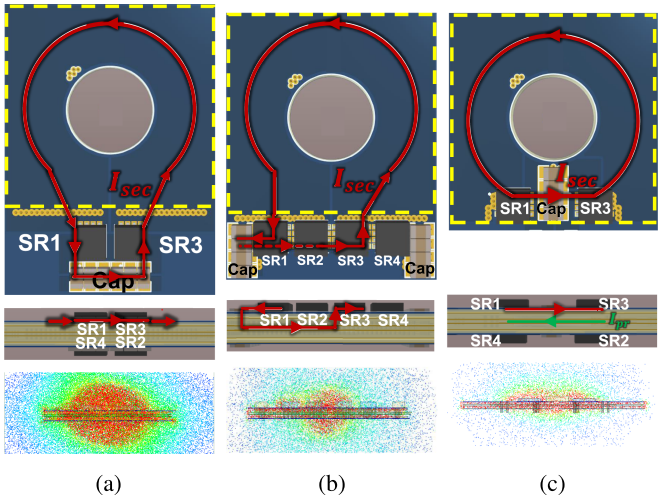

Fig. 6. Top-view, front-view, and magnetic field strength distribution of (a) lateral loop termination, (b) vertical loop termination, and (c) on-winding termination.

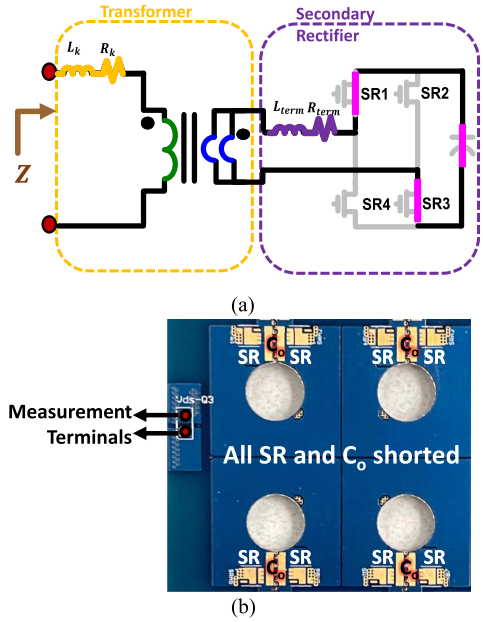

Fig. 7. Transformer winding leakage and termination impedance measurement (a) schematic and (b) hardware prototype.

transformer, there is no interleaving between the primary and the secondary current until it re-enters the transformer, resulting in a large termination loop area. This, paired with the large noninterleaved termination loop, results in high leakage flux densities and termination losses.

To improve upon this, the vertical loop termination was proposed, as shown in Fig. 6(b), where all four SRs and the output filter capacitors are placed on the same side outside the transformer (dashed yellow box). The secondary current, shown by the red arrows, flows from SR1 to the filter capacitors, then flows into SR3 via a middle layer (dashed arrows), after which it enters back into the secondary winding. The termination loop is folded between two layers, such that the secondary current going into the SRs is partially overlapped by the current coming out from the SRs. Even though there is still no interleaving between the primary and secondary currents when the secondary current leaves the transformer, the partial self-interleaving of the secondary current helps reduce the leakage flux densities and termination losses as compared to the lateral loop termination. Moreover, the termination loop area is now much smaller than that of the lateral loop, resulting in an improved termination loop [17]. Furthermore, placing all the SRs on the same layer improves the thermal management of the SRs considerably, as vias can be used underneath the SRs to distribute the current between multiple layers.

Finally, to further improve the termination design, the SRs and output filter capacitors can be placed directly on the secondary windings, as shown in Fig. 6(c), with one half-bridge set being placed on each secondary winding (inside the dashed yellow box). The secondary current in red fully interleaves with the primary current in green, resulting in no visible termination loop, and hence very low leakage flux density and termination losses. Placing the SRs and capacitors directly on the windings also frees up additional space outside the transformer, thereby increasing the converter's power density. However, this comes with the challenge of thermal management of the SRs, since they are placed directly on the hot transformer windings.

TABLE I
HARDWARE MEASUREMENT OF TRANSFORMER IMPEDANCE AT 500 KHZ WITH FB SRS

Termination	$L = L_k + n^2 L_{\text{term}}$	$R = R_k + n^2 R_{\text{term}}$
Lateral	116	82.5
Vertical	99.8	66.5
On-Winding	86.9	56.8

As observed in the CT SR case, the flux crowding due to the termination method can have a significant impact on the transformer's leakage inductance and winding resistance. To verify this, the transformer's winding impedance was measured by shorting the secondary side of one half-cycle, as shown by the pink lines in Fig. 7(a). Fig. 7(b) shows the hardware prototype of the four-leg matrix transformer with the SR and filter capacitor terminals for one half-cycle shorted. The effective inductance and resistance measured from the primary side (red dots) are given by $L = L_k + n^2 L_{\text{term}}$ and $R = R_k + n^2 R_{\text{term}}$ respectively, where L_k and R_k are the combined (primary and secondary) leakage inductance and combined (primary and secondary) winding AC resistance of the transformer, and L_{term} and R_{term} are the inductance and resistance from the termination. Table I summarizes the transformer's impedance measurements for the three termination techniques. Since the winding stack-up and, hence, the MMF distribution, remains the same in the three test cases, L_k and R_k also large remain unchanged. Hence, the only change in measurement occurs due to changes in L_{term} and R_{term}. It can be observed from Table I that the termination inductance and resistance decrease as the interleaving is improved and the termination loop is minimized.

Based on the above studies on the two SR configurations to determine the termination technique with the lowest termination impedance, it can be observed that placing the secondary windings on the top and bottom layers and placing the SRs and output filter capacitors directly on the secondary windings results in the lowest termination impedance. This configuration, henceforth referred to as the "on-winding termination," is the focus of this study.

Although studies like this have investigated the impacts of PCB layer stacking, vias, and the SR placement in planar transformers, the effects of the output filter capacitors have not yet been investigated in detail. As the following sections will discuss, determining the location and capacitance values are crucial to minimize termination losses.

III. Circulating Current Between the Distributed Filter Capacitors

In the case of on-winding termination, the two half-bridge modules in the FB configuration are split and placed on the top and bottom secondary layers, thereby splitting the output filter capacitors between the two secondary layers (C_{top} and C_{bot}, respectively). Similarly, in the CT configuration, the output filter capacitors are split between the two secondary layers alongside the SRs operating in each half-cycle. Moreover, there may be capacitors off-winding to reduce the output voltage ripple. This results in a complex network, which can impact the ac current distribution, resulting in circulating current in the network and, hence, high conduction losses.

To investigate the impact of the capacitors on the termination impedance, the transformer's ac resistance was measured similar to Fig. 7, with the SRs (of one half-cycle) still shorted but the capacitors populated. When only C_{top} is populated, the termination loop is effectively the red loops in Fig. 4(c) and 6(c), hence resulting in expected ac resistance measurements (increase with frequency due to the increasing skin effect) as shown by the red curves in Fig. 8. However, both sets of capacitors (C_{top} and C_{bot}) are populated in the actual *LLC* converter, which operates during the entire switching period. Upon performing the same measurement on this configuration, the blue curves in Fig. 8 are obtained, which show a large peaking in the ac resistance curves. For *LLC* converters running at frequencies ranging from 500 kHz to 1 MHz, this can result in unexpectedly high transformer losses and, hence, low efficiencies. The root cause for this phenomenon is investigated in detail in this section.

The two sets of capacitors on the top and bottom secondary layers must be paralleled and connected to the capacitors from the other output sets, and eventually the load. This parallel connection between C_{top} and C_{bot} is made through vias between the top and bottom secondary layers. However, this results in a long path from C_{top} to C_{bot}, which results in a capacitor ringing loop, as shown in Fig. 9(a) and(b) for the FB and CT configurations, respectively. The red loop indicates the secondary current termination loop, whereas the yellow path represents the circulating current loop between C_{top} and C_{bot}.

This phenomenon can be understood in detail by studying the schematic of the resulting termination. Fig. 10(a) and (b) show the modified schematics of the FB and CT configurations respectively as is laid out on the PCB with the rectifier operating in each half-cycle separated, along with the output filter capacitance being split between C_{top} and C_{bot}. The parasitic loop inductance and resistance that exist between C_{top} and C_{bot} are represented by L_S and R_S, respectively. It can be observed that although the winding and component layouts are different in the two SR configurations, the parasitic ringing loop phenomenon between the split output filter capacitors is very similar in the two cases. Therefore, the equivalent impedance model across the secondary-side termination during one half-cycle of operation for the two SR configurations can be represented by

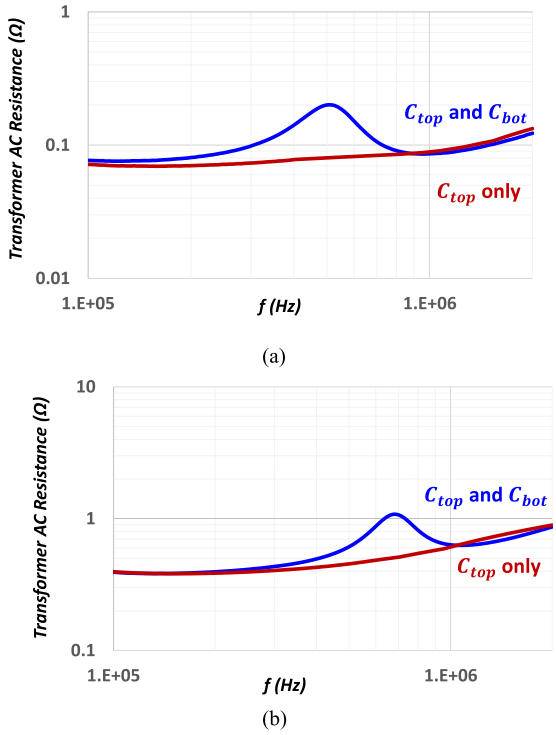

Fig. 8. Measured ac resistance comparison with different capacitors populated in transformers with (a) FB rectifiers and (b) CT rectifier.

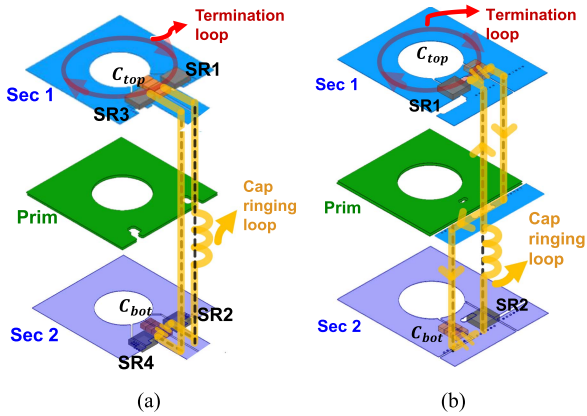

Fig. 9. Split filter-capacitor paralleling through off-winding vias in (a) FB configuration and (b) CT configuration.

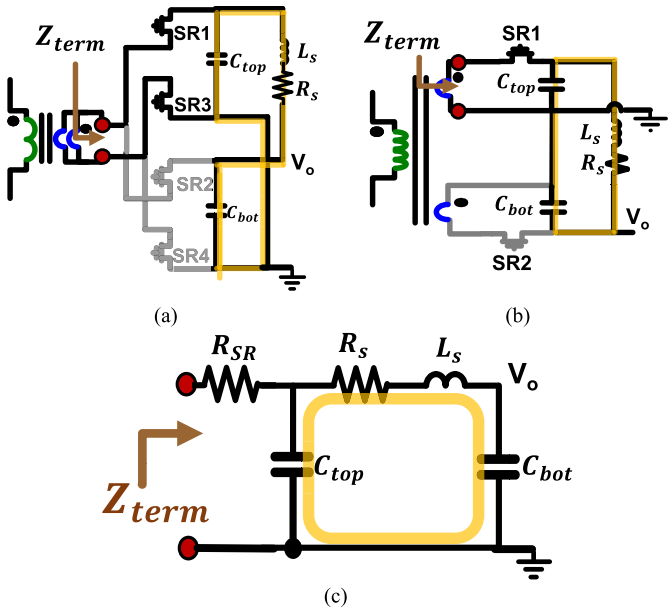

Fig. 10. Schematic of (a) FB and (b) CT rectifiers with the circulating current loop between C_{top} and C_{bot}, and (c) equivalent termination model.

the same schematic as shown in Fig. 10(c), where R_{SR} is the ON-resistance of the SR. The parallel resonant loop (highlighted in yellow) consisting of the filter capacitors and the parasitic inductance and resistance can be clearly observed. Since there is high circulating-energy within this loop during resonance, it is important to analyze any impact it may have on the transformer loss.

The equivalent impedance Z_{term} of the network in Fig. 10(c) can be expressed as

$$Z_{\text{term}} = R_{\text{SR}} + \frac{Z_{C_{\text{top}}} Z_{C_{\text{bot}}}}{Z_{C_{\text{top}}} + Z_{C_{\text{bot}}}} \tag{1}$$

where $Z_{C_{\text{top}}}$ and $Z_{C_{\text{bot}}}$ are the impedances of the C_{top} and C_{bot} parallel branches, respectively, and are given by

$$Z_{C_{\text{top}}} = \frac{1}{sC_{\text{top}}}, \quad Z_{C_{\text{bot}}} = R_s + sL_s + \frac{1}{sC_{\text{bot}}} \tag{2}$$

where $s = j\omega$, with ω being the angular frequency given by $\omega = 2\pi f$. Upon substituting (2) in (1), and under the realistic and reasonable assumption that $C_{\text{top}} = C_{\text{bot}} = C$, (1) can be expressed as

$$Z_{\text{term}} = R_{\text{SR}} + \frac{s^2 L_s C + sR_s C + 1}{s^3 L_s C^2 + s^2 R_s C^2 + s2C} \tag{3}$$

resulting in a third-order transfer function due to the presence of the three energy-storage elements C_{top}, C_{bot}, and L_s.

To study the impact of this parallel resonance on the transformer ac resistance, and hence its loss, the equivalent resistance—or the real part of Z can solely be analyzed. To achieve this, $s = j\omega$ is substituted into (3), and the real and imaginary parts of Z are separated as

$$Z_{\text{term}} = R_{\text{term}} + jX_{\text{term}} \tag{4}$$

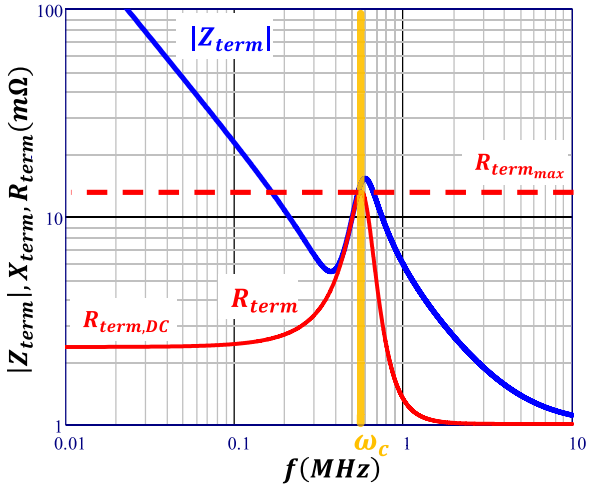

Fig. 11. Magnitude, real and imaginary parts of Z against frequency.

where R_{term} and X_{term} are the equivalent resistance and reactance of the termination impedance network, respectively. The following expressions for R_{term} and X_{term} can then be obtained:

$$R_{\text{term}} = R_{\text{SR}} + \frac{R_s}{C^2 L_s^2 \omega^4 + C^2 R_s^2 \omega^2 - 4CL_s\omega^2 + 4} \tag{5}$$

$$X_{\text{term}} = \frac{L_s\omega - \frac{C(L_s^2\omega^4 + R_s^2\omega^2)}{2\omega}}{C^2 L_s^2 \omega^4 + C^2 R_s^2 \omega^2 - 4CL_s\omega^2 + 4} - \frac{1}{2C\omega}. \tag{6}$$

Clearly, (5) and (6) are a function of frequency, and $|Z_{\text{term}}|$ and R_{term} can be plotted as shown in Fig. 11 ($C = 40\mu$F, $R_s = 5.4\text{m}\Omega$, $L_s = 4.4$nH, $R_{\text{SR}} = 1\text{m}\Omega$). The impedance is capacitive in nature until the parallel resonant frequency ω_c, when there are high circulating currents between the energy storage elements, after which the capacitive nature of the circuit resumes. During the parallel resonant frequency, the high circulating currents also pass through the parasitic resistance R_s and the capacitor's equivalent series resistance (ESR) (not shown in this simplified model), resulting in a spike in the real part R_{term} and, hence, the transformer ac resistance, at that frequency. The parallel resonant frequency ω_c can be evaluated by setting the imaginary part of the loop admittance to zero, resulting in

$$\omega_c = \frac{1}{\sqrt{0.5CL_s}}. \tag{7}$$

The termination resistance without the resonance effect (expected value), $R_{\text{term}_{\text{DC}}}$ can be evaluated by substituting $\omega_0 = 0$ in (5) to obtain

$$R_{\text{term}_{\text{DC}}} = \frac{R_s}{4} + R_{\text{SR}}. \tag{8}$$

Furthermore, the peak termination resistance $R_{\text{term}_{\text{max}}}$ at ω_c can be evaluated by substituting (7) in (5) to result in

$$R_{\text{term}_{\text{max}}} = \frac{L_s}{2CR_s} + R_{\text{SR}}. \tag{9}$$

The operating frequencies of resonant converters today can be easily pushed to 500 kHz or higher, thanks to soft-switching and wide-bandgap technology [13], [18]. Hence, the presence

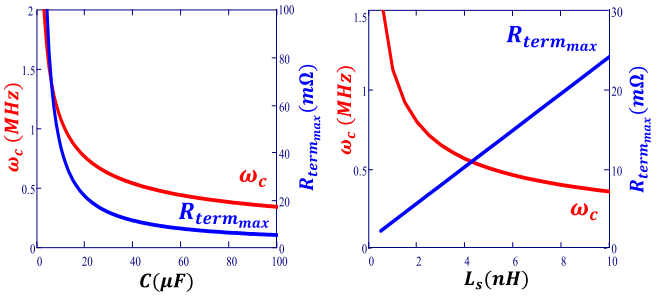

Fig. 12. ω_c and $R_{\text{term}_{\text{max}}}$ versus (a) capacitance C, and (b) parasitic inductance L_s.

of the parallel resonant peak around that frequency range results in increased transformer ac resistances, leading to higher conduction losses than expected. For example, in Fig. 11, the termination resistance increases by approximately 300% when switched at 500 kHz compared to its $R_{\text{term}_{\text{DC}}}$, resulting in a steep increase in conduction losses. Therefore, to mitigate this parallel resonance's impact on the converter efficiency, the parallel resonant frequency must be pushed to a much higher frequency than the *LLC* resonant frequency.

IV. Mitigating the Impact of Termination on Converter Loss

From Fig. 11, a significant peaking in the transformer's ac resistance (red curve) can be observed at frequencies around 200 kHz–1 MHz. This is a cause for concern since most high-frequency, high-current *LLC* converters operate at these frequencies, and any increase in the transformer's ac resistance will result in increased winding losses. Therefore, steps must be taken to move ω_c away, either to a much lower frequency or a much higher frequency than f_{sw}. Since this peak is a result of the parallel resonance between the filter capacitors C and the parasitic loop inductance L_s (as discussed in Section III), the impact of both of these passive elements on the termination impedance, and hence, the loss is studied in this section. Moreover, design guidelines to minimize the increase in transformer loss are also proposed.

1) *Impact of Capacitance C:*
From (7), it can be seen that the parallel resonant frequency ω_c has an inverse relationship with the capacitance C. Moreover, (9) also shows an inverse relationship of the peak termination resistance $R_{\text{term}_{\text{max}}}$ with C. This aspect has been discussed by Mu et al. in [15] and is summarized here with a few caveats. Fig. 12(a) shows the two quantities at different C values.
   a) To move ω_c to a much lower frequency than f_{sw}, the capacitance can be increased. However, it can be noted from Fig. 12(a) that the capacitance must be increased multifold to have any significant reduction in ω_c. Moreover, the real-estate on the transformer winding is typically very limited to accommodate high capacitance.
   b) Alternatively, the capacitance can be reduced to move ω_c to a much higher frequency than f_{sw}. However, as noted in Fig. 12(a), this would also entail an increase in $R_{\text{term}_{\text{max}}}$, resulting in a faster rise in R_{term} and hence more risk of increased loss. Moreover, lower output capacitance also increases the output voltage ripple significantly and, hence, must be considered as a constraint when implementing this option.

   During the *LLC* converter's operation, the dc voltage across the filter capacitors (V_o) will derate the capacitance to a lower value. For example, at an output voltage of 14 V, a 25-V rated capacitor loses around 63% of its rated capacitance [19]. This effect must be considered while performing analyses of filter capacitors, which hold a dc bias during converter operation.

   Although adjusting the capacitance is a quick and easy solution to move ω_c away from f_{sw}, it is assumed in this article that the capacitance is designed to meet the exact output voltage ripple requirement, and there is no additional real-estate on the PCB windings to accommodate higher capacitance. Therefore, the parasitic inductance L_s must be modified to mitigate the impact of termination resonance.
2) *Impact of Parasitic Inductance L_s:*
From (7), it can be seen that the parallel resonant frequency ω_c has an inverse relationship also with the parasitic inductance L_s. However, (9) shows a direct relationship of the peak termination resistance $R_{\text{term}_{\text{max}}}$ with L_s. Fig. 12(b) shows the two parameters as a function of L_s. It should be noted that increasing L_s substantially to move ω_c to lower frequencies will result in higher $R_{\text{term}_{\text{max}}}$, resulting in a faster rise in R_{term} and, hence, is not the optimal method to move ω_c. Instead, reducing L_s can result in a reduction in $R_{\text{term}_{\text{max}}}$ in addition to the increase in ω_c, making it an attractive option. Therefore, the rest of this section will focus on minimizing L_s to maximize ω_c and minimize $R_{\text{term}_{\text{max}}}$.

The parasitic inductance L_s and resistance R_s fundamentally depend on the paralleling path between the two filter capacitors placed on the two secondary layers. Therefore, this path must be optimized to reduce L_s and R_s.

Typically, multiple vias are placed just outside the transformer to parallel the capacitors and connect the different output sets ultimately to the load. Fig. 13(a) and (b) show the typically employed via placements for paralleling the filter capacitors and connecting the elemental transformers to the load for the FB and CT SR configurations, respectively. The vias in red carry current to the load while those in black are for the ground return path. Multiple vias are paralleled to help conduct the high dc currents flowing out from each elemental transformer to the load. For the FB SR configuration, the vias carrying current to the load and those for the ground return paths are interleaved to create negative coupling between them, hence reducing the loop inductance. For the CT SR configuration on the other hand, as the secondary current direction is opposite in the two secondary windings, the filter capacitors are placed diagonally opposite

TABLE II
FEA Q3D SIMULATED LOOP PARAMETERS FOR THE TRANSFORMERS WITH FB AND CT SR CONFIGURATIONS AND DIFFERENT VIA ARRANGEMENTS

SR Configuration	**FB SRs**		**CT SRs**	
$C(\mu\text{F})$	$4 \times 10 \times 0.37$ ($V_o = 14\text{V}$)		$3 \times 10 \times 0.45$ ($V_o = 12\text{V}$)	
Termination via arrangement	Off-winding vias only	On-winding + off-winding vias	Off-winding vias only	On-winding + off-winding vias
$L_s(nH)$	4.4	0.8	2.7	1.15
$R_s(\text{m}\Omega)$	5.4	2.1	4.5	2.3
$\omega_c(\text{kHz})$	860	2070	1180	1800

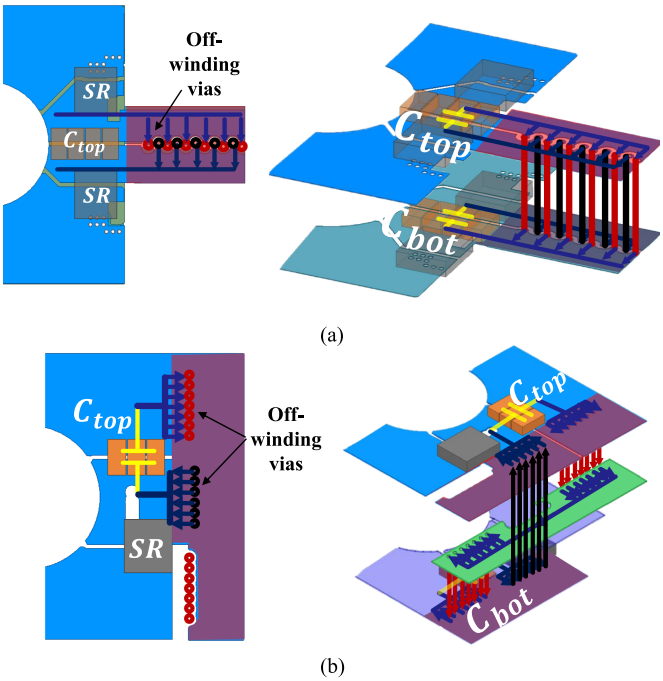

Fig. 13. Top view and isometric view of the via placement for the original capacitor paralleling in (a) FB SR configuration and (b) CT SR configuration.

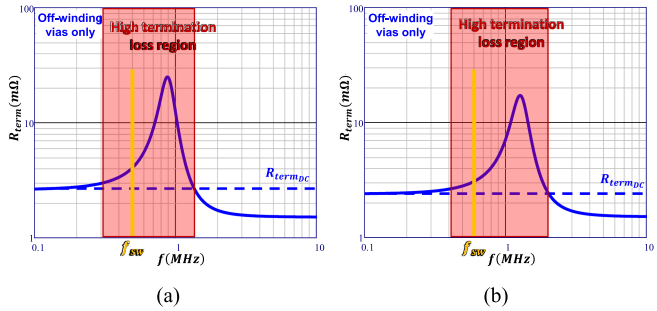

Fig. 14. Termination resistance with off-winding vias only in the transformer with (a) FB rectifiers and (b) CT rectifiers.

to each other. This results in requiring additional middle layers (in green) for paralleling the capacitors. For purposes of clarity, the vias shown in Fig. 13 will be referred to as "off-winding vias" in this article, since they are placed outside the transformer windings (purple region in Fig. 13).

To quantify the loop parasitic parameters L_s and R_s for the termination, one could attempt to measure the impedance between the parallel capacitors on the physical transformer. However, it is impractical to measure such small quantities (typically in the orders of a few nano Henry and micro-Ohm) accurately and consistently. Therefore, FEA Q3D simulations are performed to simulate the L_s and R_s between the two output filter capacitors. However, as the ac inductance and resistance values vary with frequency, and the exact parallel resonant frequency (at which to run the simulation) cannot be determined beforehand, an average over 0.5 MHz–1.25 MHz was taken as a rough estimate for the loop parasitics.

Table II summarizes the simulated L_s and R_s values for the FB and CT SR configurations with off-winding vias. Moreover, the capacitance C used (derated at V_o) and the resulting parallel resonant frequency ($f_c = w_c/2\pi$) are also listed. Multiple 0805-sized multilayered ceramic capacitors (MLCCs) of the highest available capacitance are connected in parallel to completely cover the secondary winding width to facilitate uniform current flow and avoid current crowding in the intermediate shield layers [10]. Therefore, based on the transformer winding widths in the two cases, four and three 0805-sized 10 μF capacitors are connected in parallel, respectively.

Fig. 14 shows the termination resistance curves of the termination with the off-winding vias for the transformers with FB and CT rectifiers. The red region shows the high termination loss region, where the termination resistance is higher than $R_{\text{term}_{\text{DC}}}$. As the corresponding switching frequencies of the two converters fall within this region, there will be increased termination losses, resulting in lower efficiencies. Therefore, the high termination loss region must be moved to higher frequencies by reducing the parasitic inductance L_s.

To reduce L_s, the paralleling path between the filter capacitors must be shortened. Given that the shortest path between any two given points is a straight line connecting them, interleaving vias (henceforth referred to as "on-winding vias") directly underneath the capacitors can be added, as shown in Fig. 15. As the capacitors are already vertically aligned in the FB rectifiers case, the modification simply requires adding vias under them for the interconnection. However, for the CT rectifiers case, since the two secondary layers carry current in opposite directions in the two half-cycles, the capacitors are placed diagonally opposite to each other [see Fig. 13(b)] for easier component layout. Therefore, as can be observed from Fig. 15(b), the capacitors are aligned vertically to facilitate the addition of the vias underneath them.

The low-impedance path created by the newly added on-winding vias carries most of the ac current. Moreover, placing such through-hole vias on the PCB windings of the transformer creates cutouts in the current-carrying PCB layers in

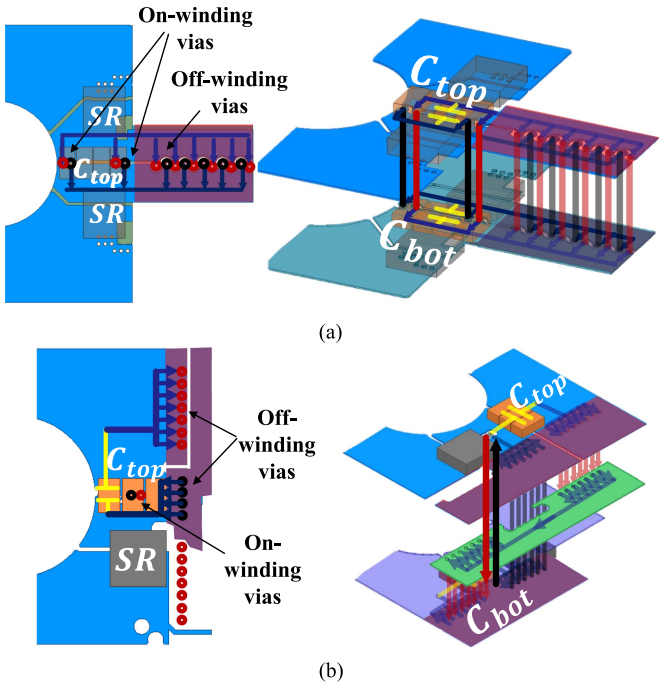

Fig. 15. Top view and isometric view of the via placement for the improved capacitor paralleling in (a) FB SR configuration and (b) CT SR configuration.

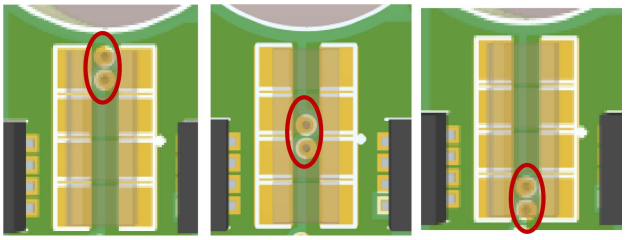

Fig. 16. Different positions for the on-winding vias: (a) close to the core, (b) in the middle, and (c) close to the transformer edge.

the middle, resulting in current crowding, and hence additional winding losses. Therefore, the number and position of the on-winding vias must be carefully considered for optimal design.

In case of the transformer with FB rectifiers, each primary layer contains only one primary turn. Therefore, there is some flexibility in placing the vias. To determine the best location to place the vias, FEA Q3D simulations were performed for the on-winding vias placed in three locations, as shown in Fig. 16. The simulations (including the off-winding vias) result in $L_s = 1.66$nH ($\pm 1\%$ difference) and $R_s = 4.23\,\text{m}\Omega$ for all the three cases, indicating that the via position under the capacitors does not affect the loop parasitics. Based on the required via current and available space on the winding, two sets of interleaved vias are placed at positions shown in Fig. 16(a) and(c) [also shown in Fig. 15(a)]. Although this creates cutouts in the primary windings [see Fig. 17(a)], the primary winding loss

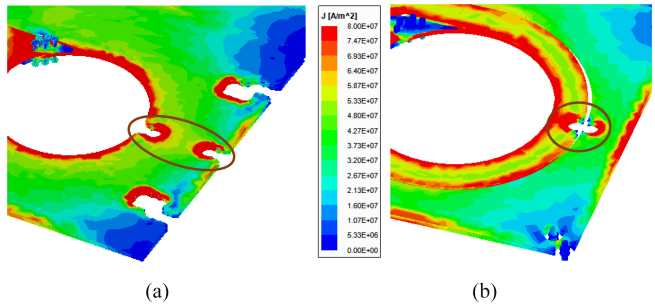

Fig. 17. FEA simulated current density in the primary windings due to the on-winding vias in the transformer with (a) FB rectifiers with single primary turn per layer, and (b) CT rectifiers with two primary turns per layer.

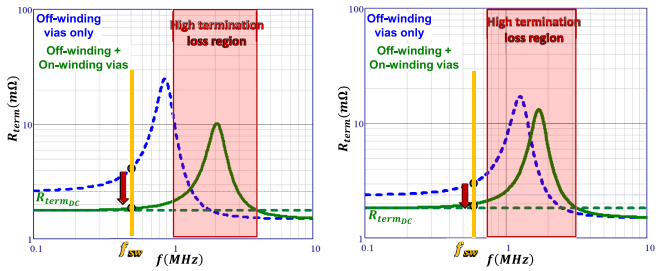

Fig. 18. Movement of the resonance peak in the termination resistance with off-winding and on-winding vias in the transformer with (a) FB rectifiers and (b) CT rectifiers.

only increases by 0.4 W, which is a negligible 0.02% reduction in efficiency at full load (2 kW).

On the other hand, the transformer with the CT rectifiers has two primary turns per primary layer. This results in limited flexibility in terms of via number and location, since their incorrect placement could result in very high-current crowding, or even open circuit (OC), in the narrow primary windings. Therefore, only one set of interleaved vias is placed on the transformer winding with minimum possible cutout in the primary windings [see Fig. 17(b)]. The primary winding loss increases by 0.25 W, which is again a negligibly low-efficiency reduction of 0.02% at full load (1 kW). Furthermore, the single pair of on-winding vias are copper-filled to increase their current-carrying capacity.

To verify the reduction in loop parasitics L_s and R_s, FEA Q3D simulations were performed, and the results are summarized in Table II. It can be observed that with the addition of the on-winding vias, the L_s and R_s values both reduce considerably, thereby moving the parallel resonant frequency f_c to greater than 3–4 times f_{sw} in both cases. This can also be observed from the shift of the parallel resonant peaks, and hence the high termination loss regions, in the R_{term} curves for the two transformers with FB and CT rectifiers in Fig. 18. The reduction in R_{term} at f_{sw} with the improved termination can also be observed.

Moreover, it can also be noted from (9) that $R_{\text{term}_{\text{DC}}}$, which is the minimum achievable termination resistance below ω_c, also decreases with lower R_s. This phenomenon can also be

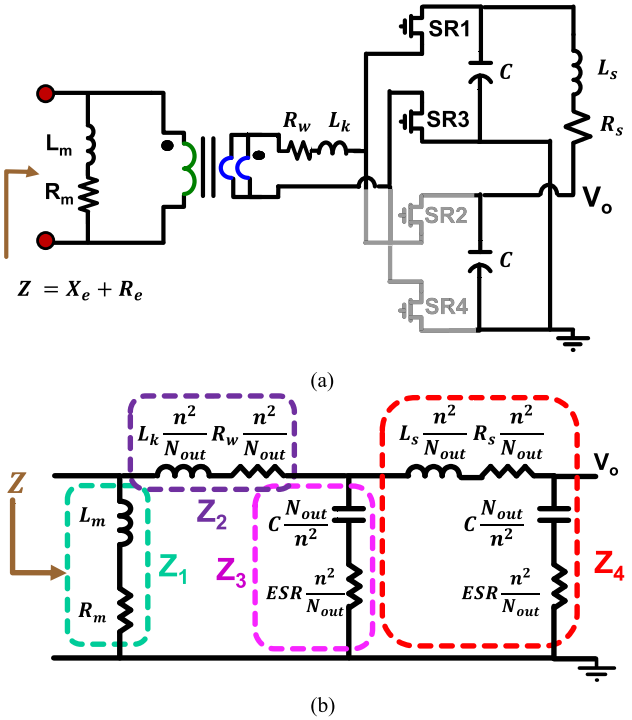

Fig. 19. (a) Complete transformer schematic with FB rectifiers and (b) equivalent circuit model reflected to the primary side.

observed in Fig. 18, where the improved termination with lower R_s reduces $R_{\text{term}_{\text{DC}}}$. Therefore, this is can be seen as an added benefit to minimizing the parallel path between split filter capacitors. Overall, the improvement results in the reduction of the termination resistance and, hence, the transformer loss, at the *LLC* converter's switching frequency.

V. Hardware Verification of Termination Model

The accuracy of the proposed termination model can be verified by measuring the impedance of the same. However, measuring the transformer's impedance from the secondary side is impractical and inaccurate, due to its small magnitude and multiple windings in parallel. Instead, measuring the transformer impedance from the primary side is practical and makes it easier to capture any small differences in secondary components because the high turns ratio will reflect the small resistances of the secondary to the primary with a large gain [15]. The entire transformer must hence be modeled to validate the measurement.

Fig. 19(a) shows the complete transformer schematic with the capacitor ringing loop and FB rectifiers with one elemental transformer, where L_k and R_w are the transformer winding leakage inductance and resistance, respectively. Fig. 19(b) shows the equivalent circuit model reflected to the primary side. The *LLC* converters employ a matrix of N_{out} elemental transformers connected in parallel from the secondary side, resulting in the impedance branches on the secondary side accounting for that. The transformer with the CT rectifiers also has the same model, and hence, the same modeling methodology as described below can be extended to it too. Here, Z_1 represents the magnetizing

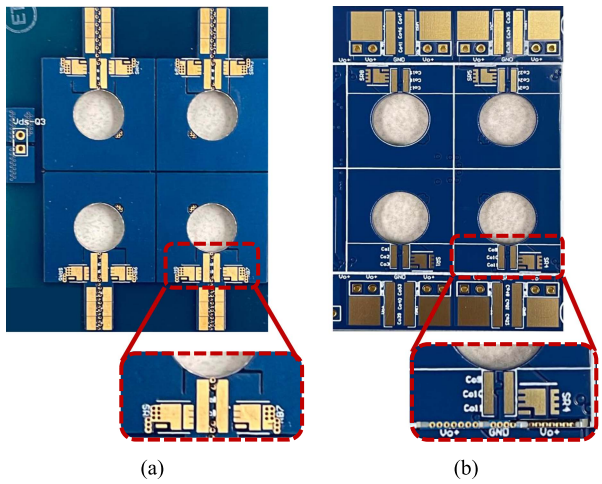

Fig. 20. Hardware prototype of four-leg planar matrix transformer with improved termination and (a) FB rectifiers and (b) CT rectifiers.

inductance branch, Z_2 represents the winding impedance, Z_3 represents the top capacitance branch, and Z_4 represents the bottom capacitance in series with the loop inductance L_s. The equivalent impedance of the transformer Z is given by

$$Z = Z_1 || [Z_2 + (Z_3 || Z_4)]. \tag{10}$$

To validate the transformer impedance measurement with the model, every element in the model must be accounted for, as discussed subsequently. Fig. 20 shows the hardware prototypes of the planar matrix transformers with FB and CT rectifiers, respectively, with zoomed-in images showing the top-view of the on-winding termination layout. The transformer impedance was measured using a Keysight 4990A impedance analyzer with the Keysight 42941A high-bandwidth, in-circuit impedance probe. The setup is calibrated beforehand to minimize any measurement errors, and all tests are performed together with the same setup.

1) *Magnetizing inductance branch Z_1:* Z_1 can be measured by setting the secondary side to be an OC, as shown in Fig. 21(a), resulting in the equivalent circuit model shown in Fig. 21(b). The measured impedance Z is then equal to

$$Z = Z_1 = R_m + j\omega L_m. \tag{11}$$

The measured impedance magnitude and resistance are shown in Fig. 21(c), and L_m and R_m can be extracted from them.

2) *Leakage inductance branch Z_2:* Z_2 can be measured by setting the secondary side to be a short circuit (SC), as shown in Fig. 22(a), resulting in the equivalent circuit model shown in Fig. 22(b). The measured impedance Z is then equal to

$$Z = Z_1 || Z_2 \approx Z_2 = n^2(R_w + j\omega L_k). \tag{12}$$

Since typically $Z_1 \gg Z_2$, paralleling them can be approximated to equal Z_2. The measured impedance magnitude and resistance are shown in Fig. 22(c), and L_k and R_w can be extracted from them.

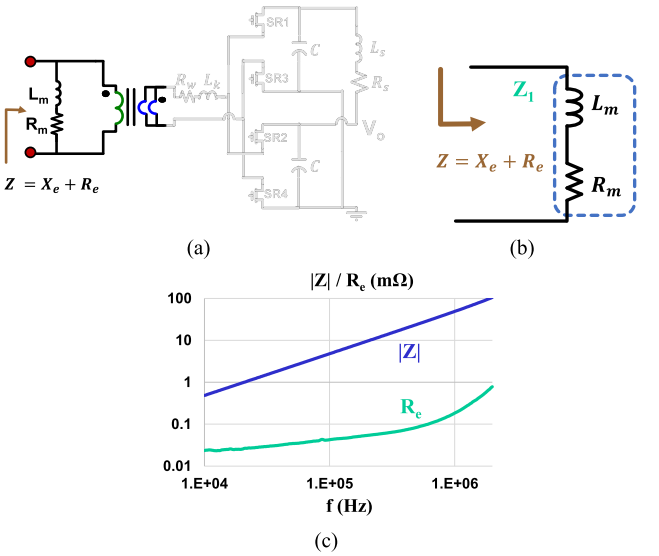

Fig. 21. Transformer secondary OC test. (a) Modified schematic. (b) Equivalent circuit model. (c) Measured impedance.

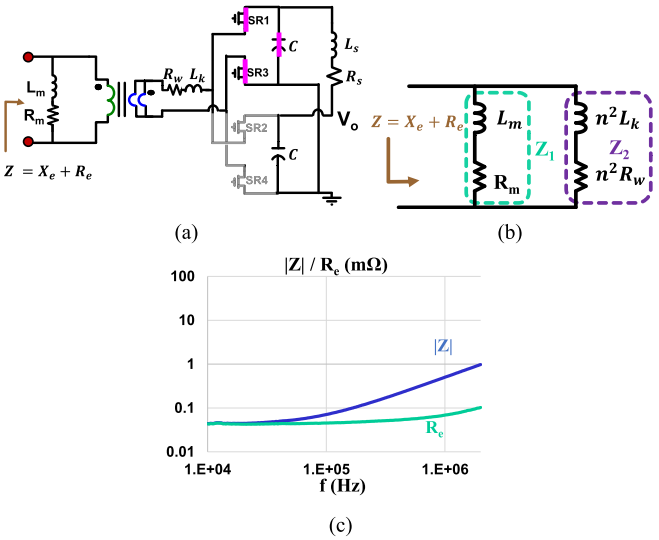

Fig. 22. Transformer secondary SC test: (a) Modified schematic. (b) Equivalent circuit model. (c) Measured impedance.

3) *Capacitor Measurement:* The capacitor parameters are measured using the Keysight 16034E test fixture for surface-mounted devices (SMDs) attached to the Keysight 4990A impedance analyzer, as shown in Fig. 23(a). The capacitor selected for this application is TDKs C2012X7S1E106, a 25 V 10μF X7S 0805 capacitor with low ESR, the measured impedance characteristics of which are shown in Fig. 23(b).
4) *L_s and R_s:* It is impractical to physically measure the leakage inductance and resistance of the termination accurately, due to their small magnitudes. Therefore, FEA Q3D simulations are performed to simulate the *L*s and *R*s, as discussed in Section IV.

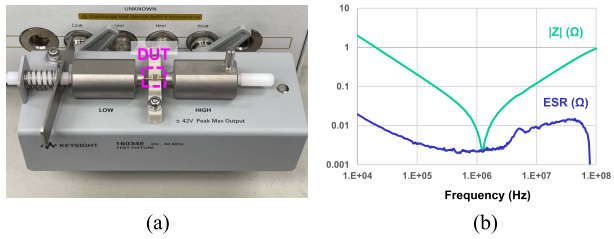

Fig. 23. (a) 16034E probe with device under test (DUT). (b) Capacitor parameter measurement.

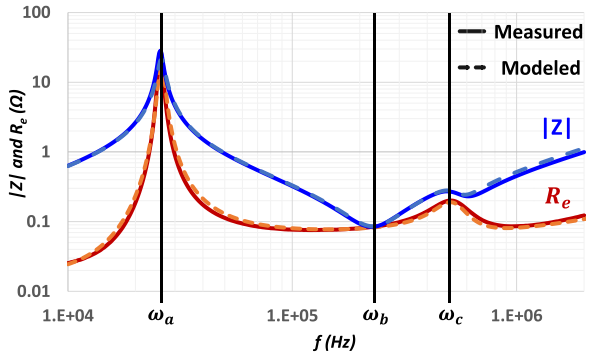

Fig. 24. Measured and modeled $|Z|$ and R_e of transformer with FB rectifiers.

TABLE III
TRANSFORMER MODEL VERIFICATION

Frequency	Measured (kHz)	Modeled (kHz)
ω_a	25.9	26.3
ω_b	228	243
ω_c	530	536

Once all the parameters are accounted for, the hardware measurement can be completely validated by the transformer model. Fig. 24 shows the magnitude of transformer impedance $|Z|$ (blue) and the transformer resistance R_e (red), where it can be seen that the model agrees very well with the measurement within a reasonable margin of measurement and curve-tracing error. Moreover, three main resonant frequencies can be identified from the curves—parallel resonance between L_m and $2\,C/n^2$ at ω_a; series resonance between L_k and $2\,C/n^2$ at ω_b; and parallel resonance between L_s and $C/0.5n^2$ at ω_c. Table III shows the comparison between the three measured and modeled frequencies, where a close resemblance between the two can be observed.

Now that the accuracy of the transformer model has been established, the impact of the parallel resonance between the filter capacitors on the *LLC* converter's loss can be analyzed in depth. For this purpose, the transformer's ac resistance R_e will henceforth be solely analyzed since it provides a direct relation to the transformer winding loss, which ultimately determines converter efficiency.

The impedance analyzer used to perform the above measurements cannot account for the dc bias factor of the capacitors. An external dc bias may be provided to the capacitors but that would

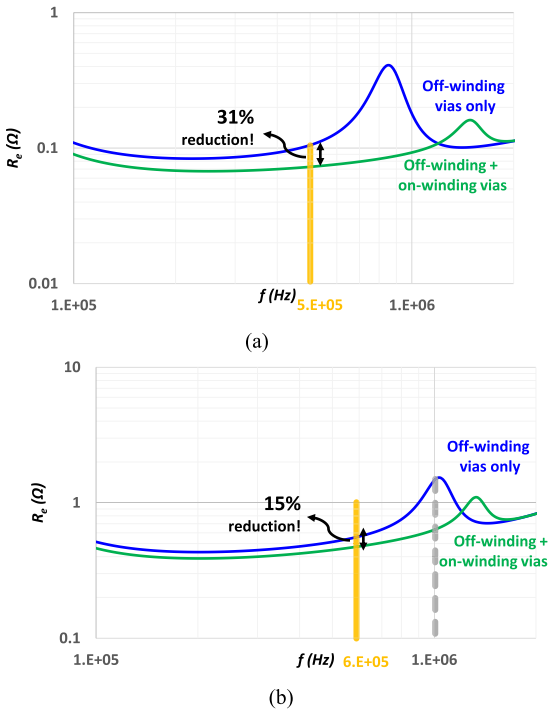

Fig. 25. Modeled transformer ac resistances with the original and improved SR termination in (a) FB rectifiers and (b) CT rectifiers.

TABLE IV
SIMULATED TRANSFORMER AC RESISTANCE

Termination	FB SR	CT SR	
Frequency (kHz)	500	600	1000
Off-Winding vias only (mΩ)	105	563	1511
On-Winding + Off-Winding vias (mΩ)	72	470	641
Reduction %	31	15	87

introduce noise into the measurements. However, the proposed transformer model, which was shown to closely replicate the measurements at 0 V dc bias [see Fig. 24], can be reliably used to predict the transformer impedance and ac resistance when the capacitors are under dc bias.

The ac resistance was modeled on the two transformers with the two rectifiers (including the corresponding dc bias on the capacitors) and with both terminations—1) only off-winding vias and 2) off-winding and on-winding vias, as described in Fig. 25. It can be observed that with lower L_s in the on-winding + off-winding termination [see Table II], the parallel resonant frequency increases and the peak resistance decreases. Moreover, with lower R_s, the minimum transformer resistance also decreases, resulting in lower transformer losses even when operating away from ω_c.

Clearly, the parallel resonance could severely affect the transformer's ac resistance and, hence, the transformer loss, at the converter's switching frequency if not designed carefully. Table IV summarizes the simulated transformer ac resistances in the two converters with the FB and CT rectifiers at their switching frequencies of 500 kHz and 600 kHz, respectively. It can

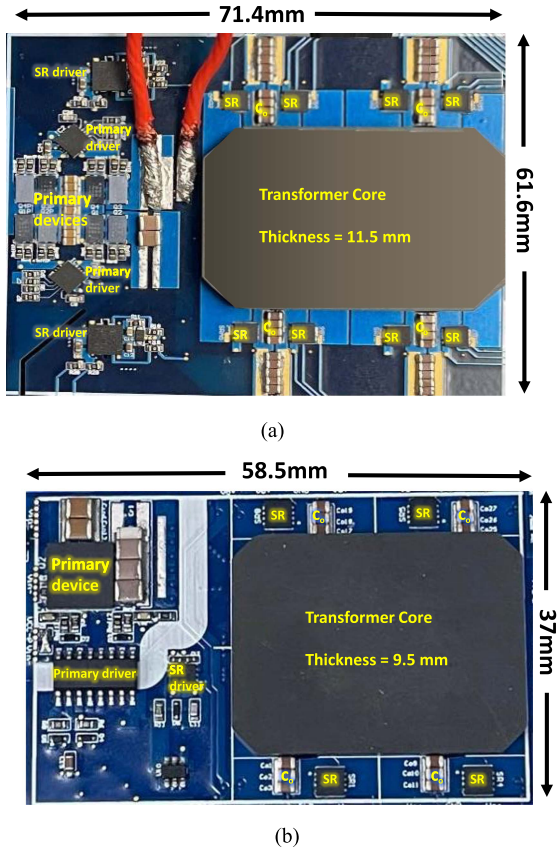

Fig. 26. Hardware prototype of *LLC* converter with a four-leg matrix transformer and the proposed termination implemented with (a) FB SRs and (b) CT SRs.

be observed that there is a 31% and 15% reduction in the transformers' ac resistances at the converters' switching frequencies. In the converter with CT rectifiers, although the improvement may not be remarkable at 600 kHz, the improved termination can result in an 87% reduction in ac resistance if operated at 1 MHz [dotted gray line in Fig. 25(b)]. Therefore, depending on the switching frequency, this significant improvement in the termination will help considerably reduce the conduction losses and, hence, increase the converter efficiency at heavier loads.

VI. *LLC* CONVERTER EFFICIENCY IMPROVEMENT

Once the termination impedance is quantified, its effect on the actual converter's performance must be analyzed to realize its importance with respect to the other losses in the converter. Therefore, the improvement in termination design was verified by developing unregulated *LLC* converters with the two SR configurations, the hardware prototypes of which are shown in Fig. 26. The specifications of the *LLC* converters are summarized in Table V. The two *LLC* converters were originally designed for different applications (automotive and datacenters for the FB and CT SR converters, respectively) and hence have varying specifications. However, this highlights the versatility of this work as a general SR termination design guideline for PCB-based transformers, specifically regarding the splitting of the output filter capacitors. Fig. 27

TABLE V
LLC CONVERTER SPECIFICATIONS

Parameters	*LLC* with SB SR	*LLC* with CT SR
Input Voltage	114V	400V
Output Voltage	14V	12V
Rated Power	2 kW	1 kW
Resonant Frequency	500 kHz	600 kHz
Turns Ratio	8:1	16:1
Primary Device	EPC2034C	IGO60R070D1
Secondary Device	IQE006NE2LM5	IQE008N03LM5
Magnetizing Inductance	8.5 μH	53.6 μH
Leakage Inductance	86 nH	580 nH
Resonant Capacitance	1 μF	82 nF

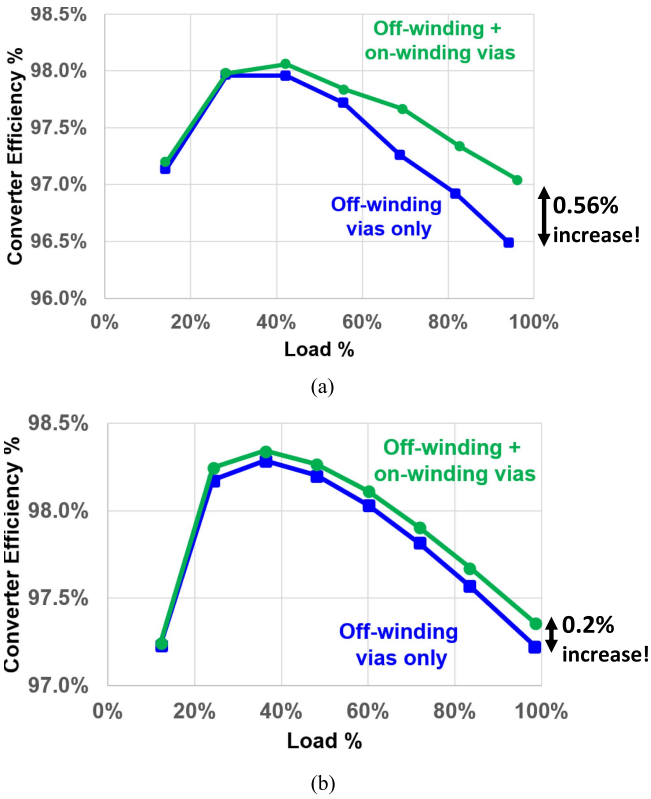

Fig. 27. Efficiency comparison with the two termination designs for the *LLC* converters with (a) FB rectifiers at 500 kHz and (b) CT rectifiers at 600 kHz.

shows the converter efficiency with each termination technique. The efficiency measurements do not include the device driving losses.

For the *LLC* converter with FB rectifiers, the converter with the off-winding termination has a light-load, peak, and full-load efficiency of 97.1%, 98%, and 96.5%, respectively. On the other hand, the converter with the on-winding + off-winding termination has a light-load, peak, and full-load efficiency of 97.1%, 98.1%, and 97.05%, respectively. It can be observed that the conduction losses decrease considerably with the updated termination design, with an improvement of 0.56%, or 11 W at the full load of 2 kW.

On the other hand, for the *LLC* converter with CT rectifiers, the converter with the off-winding termination has a light-load, peak, and full-load efficiency of 97.2%, 98.3%, and 97.2%,

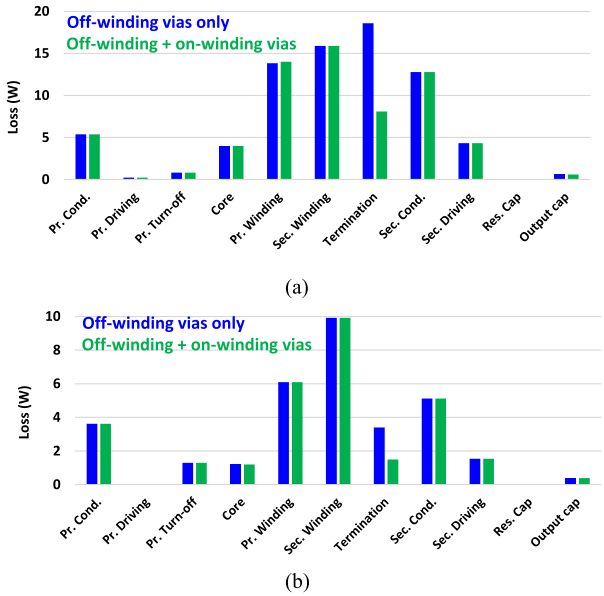

Fig. 28. Loss breakdown at full load for *LLC* converter with (a) FB SRs and (b) CT SRs.

respectively. Alternatively, the converter with the on-winding + off-winding termination has a light-load, peak, and full-load efficiency of 97.2%, 98.35%, and 97.4%, respectively. It can be observed that the conduction losses decrease considerably with the updated termination design, with an improvement of 0.2%, or 2 W at the full load of 1 kW. Furthermore, to demonstrate the competitiveness of the performance of the improved 400-V/12-V *LLC* converter, it is compared to other recent works on the unregulated 400-V/12-V dc–dc converters [12], [20], [21], [22], [23], [24], the results of which are summarized in Table VI.

Fig. 28 also shows the loss breakdown in the two *LLC* converters at full load. It can be observed that the termination loss component results in the efficiency difference, with all other components remaining the same in both converters. Moreover, in the converter with FB SRs, the termination loss has a higher loss percentage than its counterpart with CT SRs due to the presence of vias connecting the two parallel secondary layers.

In the case of the transformer with CT rectifiers, it may be noted that the improvement in transformer ac resistance [see Fig. 25(b)], and hence, the converter efficiency [see Fig. 27(b)] is mostly from the lower R_s in the improved termination, since the parallel resonant peaks are reasonably away from the optimized switching frequency of 600 kHz [12]. Therefore, to definitively corroborate the proposed model, the 400-V/12-V *LLC* converter with CT rectifiers was tested at 1 MHz ($L_m = 22\mu$H, $C_r = 24$ nF). Fig. 29 shows the efficiency curves, where a staggering 3.5% improvement in efficiency at ~95% load, or ~34-W reduction in loss, can be observed. This can be accounted for by the 87% reduction ($\Delta R_{\text{AC}} = 0.87\Omega$) in transformer ac resistance [from Fig. 25(b) and Table IV], resulting in an estimated loss difference of 32 W ($i_{pr_{\text{rms}}} = 6.1$ A). This test also shows that operating at frequencies very close to ω_c can result in incredibly high termination losses and, hence,

TABLE VI
PERFORMANCE COMPARISON OF 400-V/12-V UNREGULATED DC–DC CONVERTERS

Parameters	[20]	[21]	[22]	[23]	[24]	[12]	This work
V_{in}/V_o	380V/12V	380V/12V	380V/12V	380V/12V	400V/12V	400V/12V	400V/12V
Rated Power (W)	1 kW	800 W	1.8 kW	2 kW	800W	1 kW	1 kW
Operating Frequency	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	600 kHz	600 kHz
Peak efficiency	97% *	96.5% *	98.3% *	98.4%	97.6%	98.05%	98.3% *
Power density	640 W/in^3 **	900 W/in^3 **	810 W/in^3	1300 W/in^3	900 W/in^3	960 W/in^3	960 W/in^3

* Without driving loss.
** Without controller.

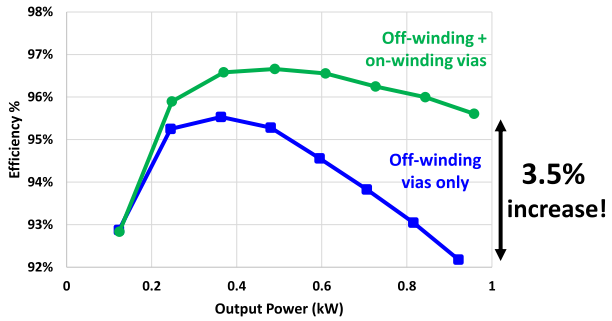

Fig. 29. Efficiency comparison with termination improvement in the 400-V/12-V *LLC* converter with CT rectifiers at 1 MHz.

very low efficiencies, with inevitable transformer and converter damage.

VII. CONCLUSION

For high-frequency, high-current applications, *LLC* converters with planar matrix transformers are promising candidates. Depending on the output-current requirements, the secondary-side rectification can be implemented using either center-tapped or FB rectifiers.

However, placing the SR devices and output filter capacitors with minimum termination loss is challenging, especially within the limited space on the transformer winding. Different termination techniques for the FB and CT rectifiers are discussed, where the SR on-winding termination is shown to have the lowest termination losses due to perfect primary-secondary current interleaving and a minimal termination loop.

However, the output filter capacitors are split between the top and bottom secondary windings, leading to a long parasitic path to parallel them. This loop inductance undergoes parallel resonance with the capacitors, resulting in increased termination resistance at the parallel resonant frequency. In case this parallel resonant frequency occurs around the *LLC* converter's switching frequency, this peaking in the termination resistance can result in high conduction losses.

With the existing termination technique of using off-winding vias to parallel the capacitors and the capacitance values, the parallel resonant frequencies may fall within the proximity of high-frequency *LLC* converters' switching frequencies. To move to higher parallel resonant frequencies, the best option is shown to be reducing L_s, which is done by adding vias directly under the capacitors on the winding itself. This pushes the parallel resonant frequency to higher frequencies, thereby mitigating its effect on the termination resistance at the switching frequency. Moreover, the shorter parallel path also results in lower minimum termination resistance, thereby reducing the total transformer resistance even when operating away from the parallel resonant frequency.

To verify the improvement in termination, the PCB transformers' ac resistances were measured from the primary side and were verified by systematically modeling the transformer, including the termination loop. By adding the on-winding vias, the transformers' ac resistances decreased by 31% at 500 kHz and 15% at 600 kHz for the transformers with FB and CT rectifiers, respectively. This improvement was also verified by measuring the efficiencies of *LLC* converters with FB and CT SRs running at 500 kHz and 600 kHz, respectively, where the full-load efficiencies increased by 0.56% and 0.2%, respectively.

By studying different *LLC* converters with varying SR configurations, which are designed for different applications, this article serves as a general design guideline while paralleling the filter capacitors on the secondary-side in PCB-based transformers. The converter's performance can be maximized if adequate attention is paid to minimize the effect of the parallel resonance between the output filter capacitors.

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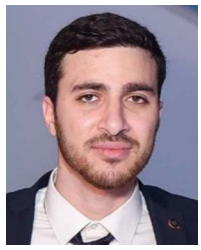

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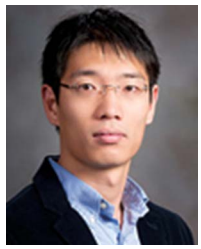

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