# Letters

## Switching Transition Modeling of eGaN HEMT in Power Converters

Guidong Zhang, *Member, IEEE*, Yuanhang He, Samson Shenglong Yu, *Member, IEEE*, Yun Zhang, and Chi K. Tse, *Fellow, IEEE*

***Abstract*—Selection of power switch driver resistance is crucial for power converter design, and an improper resistance value can lead to reduced efficiency and undesired operational behavior such as overvoltage and false turn-ON. To select appropriate resistance, this letter proposes an accurate switching transition modeling method for switches in dc–dc converters, which can help guide engineers design switch drivers. For a converter with multiple components, i.e., a high-order converter system, the traditional analytical methods become very complex due to a large number of operating modes. To alleviate this problem, in the proposed modeling method, all nonlinear switches are modeled as linear systems, and various operating modes are combined into one mode in the proposed model. With the simplified mode, the driver parameters can be easily obtained. To verify the proposed model, we take the enhanced gallium nitride high-electron-mobility transistor (eGaN HEMT) high-order dc–dc converter as an example for experimentation. The eGaN HEMT is highly sensitive to parasitic parameters and switching frequency, and thus, the high-order converter can demonstrate the ease of design with the proposed modeling method. Experiments on a Z-source converter and a quadratic-boost converter validate the feasibility of the proposed modeling method.**

***Index Terms*—Accurate switching modeling, enhanced gallium nitride high electron mobility transistor (eGaN HEMT), high-order dc–dc converter.**

### I. Introduction

As a representative wide band-gap semiconductor device, gallium nitride high electron mobility transistors (GaN HEMTs) have been deployed in a variety of applications, such as fast charging of electronic appliances and electric vehicles, grid-interfacing of renewable energy sources, data storage systems, and 5G equipment [1]. Compared to Si MOSFET, GaN HEMT conducts by 2-D electron gas, which has lower parasitic capacitance, lower ON-state resistance, and zero reverse recovery charge. These characteristics make GaN HEMT have faster switching speed, lower switching loss, and less ON-state loss. GaN HEMT can well reduce the size and increase the efficiency of converters, which further increases the power density.

Unfortunately, due to GaN HEMT's faster switching speed during turn-ON and turn-OFF periods, the change of drain-to-source voltage ($v_{ds}$) and drain-to-source current ($i_d$) of GaN HEMT is much faster than Si MOSFET. This causes interferences to the gate–source voltage ($v_{gs}$). On the other hand, GaN HEMTs have a much narrower gate–source voltage range and lower threshold voltage ($V_{th}$) than Si MOSFET. A smaller $V_{gs,max}$ range can cause overvoltage during the turn-ON transition for the GaN HEMT, and a smaller $V_{th}$ range can lead to false turn-ON during the turn-OFF switching transition. These problems are more prominent in high-order dc–dc converters because of their complex parasitic parameters.

Therefore, driver circuits for converters with GaN HEMTs require more sophisticated design. Using appropriate pull-up and pull-down gate resistances to limit the speed of turn-ON and turn-OFF processes is a common approach, wherein a trial-and-error process is required to identify the optimal driving pattern. However, this procedure is arduous and usually inaccurate due to the existence of nonlinear parameters [2]. Admittedly, optimizing the driver circuit, the driver IC and the control method can achieve optimal driving [2], [3], but system complexity and design expense are further aggravated.

For easier use of GaN devices, it is necessary to develop an accurate and simple model for power electronics engineers to analyze the change of $v_{ds}$, $i_d$, and $v_{gs}$. Some models have been proposed to analyze the switching process and loss for Si MOSFET [4]. However, due to the nonlinear parameters, high frequency resistance, parasitic inductance, and large current and voltage slew rates of the GaN HEMT, these models cannot be applied to GaN devices. In recent years, numerous research attempts have been made in this research field. An accurate analytical model for GaN devices has been proposed in [5], but this model is only applicable to the D-mode (or cascode) GaN HEMT. Some analytical switching models of low-voltage eGaN HEMTs have been proposed [6], [7], wherein the models are simulated and tested with the buck converter and synchronous

Manuscript received 8 November 2022; revised 20 December 2022; accepted 12 January 2023. Date of publication 16 January 2023; date of current version 14 February 2023. This work was supported by Natural Science Foundation for Distinguished Young Scholars of Guangdong Province under Grant 2022B1515020002. *(Corresponding author: Guidong Zhang.)*

Guidong Zhang, Yuanhang He, and Yun Zhang are with the School of Automation, Guangdong University of Technology, Guangzhou 510006, China (e-mail: guidong.zhang@gdut.edu.cn; 2112104460@mail2.gdut.edu.cn; yun@gdut.edu.cn).

Samson Shenglong Yu is with the School of Engineering, Deakin University, Burwood, VIC 3125, Australia (e-mail: s.yu@ieee.org).

Chi K. Tse is with the City University of Hong Kong, Hong Kong (e-mail: cktse@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3237333.

Digital Object Identifier 10.1109/TPEL.2023.3237333

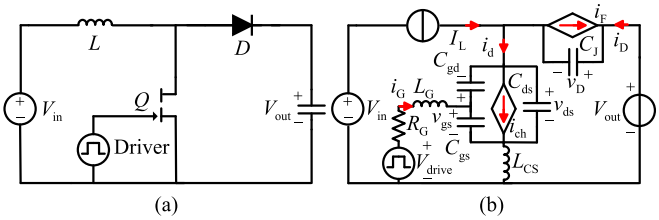


Fig. 1. (a) Topology of the boost converter. (b) Equivalent circuit of the boost converter with VCCS considering parasitic parameters.

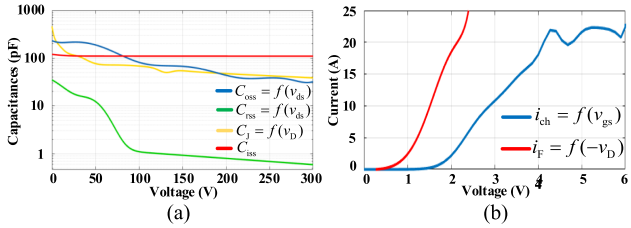


Fig. 3. (a) Curve-fitting results of nonlinear capacitances. (b) Curve-fitting results of nonlinear forward characteristics currents.

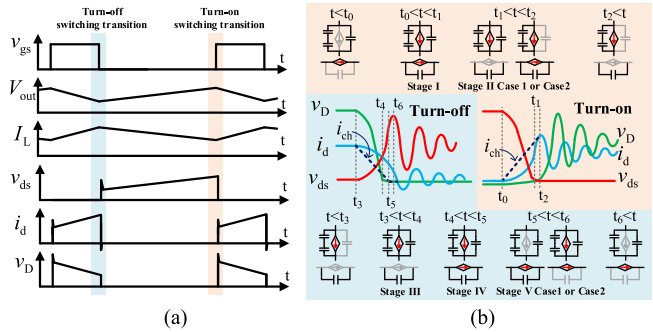


Fig. 2. (a) Key waveforms of the boost converter in one cycle. (b) Waveforms and equivalent processes of the boost converter during a switching transition.

buck converter, but driver circuits have not been analyzed. Also, these models are not suitable for high-order dc–dc converters. In [8], mathematical models have been proposed to analyze the gate-to-source voltage, and experiments on a double-pulse test platform have been conducted. However, practical applications of high-order dc–dc converters are much more complicated than the simplified experimental platform.

In view of the lack of research in eGaN HEMT modeling and parameter design, this letter proposes an accurate generalized method for eGaN HEMT in dc–dc converters to describe the switching transitions. By comparison, this model is much simpler yet with the same level of accuracy as the extensive trial-and-error methods, and only one set of equations is needed to analyze the slew rate of $v_{ds}$, $i_d$, and $v_{gs}$ for the eGaN HEMT during a switching transition.

The rest of this letter is organized as follows. The eGaN HEMT is modeled in Section II. The proposed model is analyzed in Section III. In Section IV, experiments on quasi-boost converter (QBC) and Z-source boost converter (ZSC) converters are conducted for proof-of-concept verification. Finally, Section V concludes this letter.

## II. Modeling of eGaN HEMT and Diodes

Fig. 1 shows the topology of the boost converter and its equivalent circuit with the proposed model, and Fig. 2(a) shows the key waveforms of the boost converter in one switching cycle. During a switching transition, capacitors and inductors can be regarded as ideal voltage and current sources. In order to make the model simpler and more suitable for high-order converters, semiconductors are modeled as the combination of a voltage-controlled current source (VCCS) and capacitors. Considering the interference from the power loop to the driver circuit, the following equations can describe the driver circuit:

$$\frac{di_G}{dt} = \frac{V_{drive} - v_{gs} - R_G i_G - L_{CS}\frac{di_d + di_G}{dt}}{L_G} \tag{1}$$

$$\frac{dv_{gs}}{dt} = \frac{i_G + C_{rss}\frac{dv_{ds}}{dt}}{C_{iss}} \tag{2}$$

where $V_{drive}$ represents the driver supply voltage, and $V_{drive} = 0$ in the turn-OFF period of eGaN-HEMT, $R_G$ and $L_G$ represent the total resistance and parasitic inductance of the driver circuit, respectively, and $L_{CS}$ is the common inductance of the driver loop and power loop.

There are some nonlinear parameters in this model, namely, the nonlinear junction capacitance of diode and eGaN HEMT: $C_J$, $C_{gs}$, $C_{gd}$, and $C_{ds}$, and the forward characteristic currents of eGaN HEMT and diode: $i_{ch}$ and $i_F$. Their relationship is obtained using the MATLAB curve-fitting tool with the parameters provided by the datasheets in [9] and [10]. The curve-fitting results are shown in Fig. 3, where the input capacitance $C_{iss} = C_{gs} + C_{gd}$, which can be treated as a constant, the output capacitance $C_{oss} = C_{ds} + C_{gd}$, and the reverse transfer capacitance $C_{rss} = C_{gd}$. The relationship between the channel current and voltage can be obtained by superimposing multiple Gaussian models

$$i_{ch} = f(v_{gs}) = \sum_{n=1}^{n} a_n e^{-\left(\frac{v_{gs}-b_n}{c_n}\right)^2} \tag{3}$$

$$i_F = f(-v_D) = \sum_{n=1}^{n} a_n e^{-\left(\frac{-v_D-b_n}{c_n}\right)^2}. \tag{4}$$

Fig. 2(b) shows the waveforms and equivalent processes of the boost converter during a switching transition. A turn-ON switching transition can be divided into two stages, and a turn-OFF switching transition can be divided into three stages.

*Stage I ($t_0 \sim t_1$):* $v_{gs}$ rises to $V_{th}$, $i_d$ and $i_{ch}$ start rising, $C_{oss}$ starts discharging, and $v_{ds}$ falls. Meanwhile, $C_J$ starts being charged, and $v_D$ rises, so $i_F$ falls.

*Stage II Case 1 ($t_1 \sim t_2$):* $v_D$ rises to $-V_{D,th}$, so $i_F$ drops to zero, and the diode is turned OFF. At the same time, $v_{ds}$ keeps falling. At $t = t_2$, $v_{ds}$ drops to zero and remains constant, and $i_{ch} = i_d$. The turn-ON switching transition is completed.

*Stage II Case 2 ($t_1 \sim t_2$):* $v_{ds}$ drops to zero, and once $v_D$ rises to $-V_{D,th}$, $i_F$ drops to zero. The turn-ON switching transition is completed, and $v_D$ continues to rise.

*Stage III ($t_3 \sim t_4$):* $v_{gs}$ drops to the platform voltage $V_P$, $i_{ch}$ starts falling, and $C_{oss}$ starts being charged. At the same time, $C_J$ starts discharging, so $v_D$ and $i_d$ fall.

*Stage IV ($t_4 \sim t_5$):* $v_D$ drops below $-V_{D,th}$, and $i_F$ rises from zero. At the same time, $i_d$ keeps falling, and $v_{ds}$ keeps rising.

*Stage V Case 1 ($t_5 \sim t_6$):* $v_{gs}$ drops to below $V_{th}$, and the channel of the eGaN HEMT is closed, so $i_{ch}$ drops to zero. At the same time, $v_D$ continues to fall, and $i_F$ keeps rising. When $v_D$ drops to $-V_r$, the turn-OFF switching transition is completed.

*Stage V Case 2 ($t_5 \sim t_6$):* $v_D$ drops to $-V_r$, the channel of diode is fully open. At the same time, $v_{gs}$ and $i_{ch}$ continue to fall. When $v_{gs}$ drops to below $V_{th}$, the turn-OFF switching transition is completed.

In the proposed model, the difference among multiple stages is the channel switching states of the eGaN HEMT and the diode. By using multiple Gaussian models to describe the channel current, the function relationship between voltage and current is continuous and linear, so multiple switching transition stages can be combined into one stage.

## III. Analysis of Higher Order Converters

In [6] and [7], the buck converters is used as an example to analyze the switching process of the eGaN HEMT, but the buck converter model has only a few variables and low complexity. For high-order dc–dc converters, a systematic analysis method is needed. Here, QBC and ZSC are used as examples for illustration.

### A. Step I: Identify Converter's Variables

In this model, during a switching transition, inductors and capacitors are regarded as a constant independent source, and the input and output voltages are assumed constant. In Fig. 1, the variables of diode consist of $v_D$, $i_D$, and $i_F$, and the variables of eGaN HEMT comprise $v_{ds}$, $i_d$, $i_{ch}$, $i_G$, and $v_{gs}$. The numbers of variables for QBC and ZSC are 14 $(= 3 \times 3 + 5)$ and 11 $(= 3 \times 2 + 5)$, respectively. Here, $i_G$ and $v_{gs}$ can be solved by (1) and (2).

### B. Step II: Apply Loop Current Method

Considering the parasitic parameters of the circuit, the loop current method can be applied for analysis. The number of equations of loop current method is $b - n + 1$, where $b$ and $n$ are the numbers of branches and nodes of the converter, respectively. Topologies and equivalent circuits of QBC and ZSC are shown in Fig. 4. The numbers of loop current equations for QBC and ZSC are both 4 $(= 7 - 4 + 1)$. The process of the independent current source (inductor) can be divided into two types. Take the reference loop selected in Fig. 4(c) and (d) as an example. Type I is the current source in a single loop, such as $I_{L1}$ in Fig. 4(c) and $I_{L1}$ and $I_{L2}$ in Fig. 4(d). For this type of current source, the magnitude of the loop current is equal to the magnitude of the current source. Type II is the current source in a double loop, and a classic analysis method for this type of component is introducing a new variable, i.e., the voltage of current source.

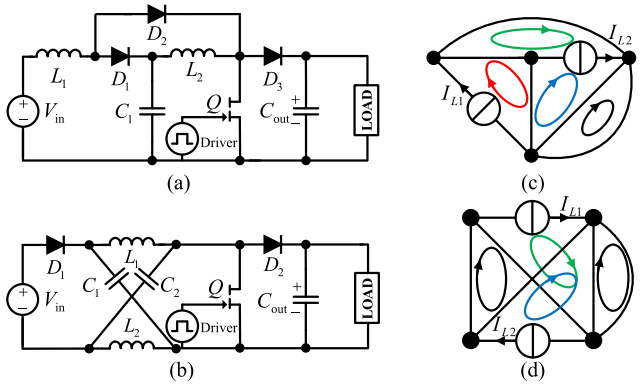


Fig. 4. (a) Topology of QBC. (b) Topology of ZSC. (c) Equivalent schematic of QBC. (d) Equivalent schematic of ZSC.

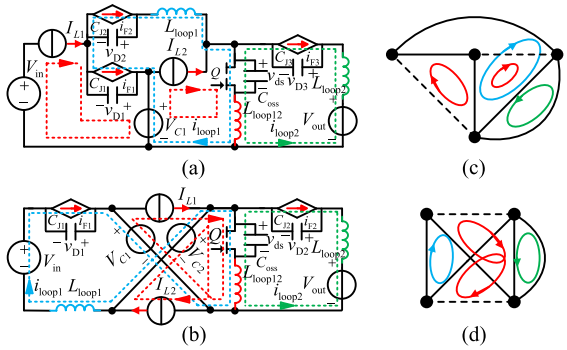


Fig. 5. (a) Equivalent circuit of QBC during switching. (b) Equivalent circuit of ZSC during switching. (c) Loops in the equivalent circuit of QBC. (d) Loops in equivalent circuit of ZSC.

But this method is not applicable for this model because voltage change occurs on the inductor during the switching process.

### C. Step III: Model the Overall Converter

In the power loops, the number of differential equations for voltage is the sum of the number of eGaN HEMT and diodes, and the number of current differential equations is the difference between the number of loops and the number of inductors. According to Fig. 5, the state equations for QBC during the switching transition are written as

$$\frac{dv_{D1}}{dt} = \frac{i_{F1} + i_{loop1} - I_{L1}}{C_{J1}} \tag{5}$$

$$\frac{dv_{D2}}{dt} = \frac{i_{F2} - i_{loop1}}{C_{J2}} \tag{6}$$

$$\frac{dv_{D3}}{dt} = \frac{i_{F3} + i_{loop2}}{C_{J3}} \tag{7}$$

$$\frac{dv_{ds}}{dt} = \frac{i_{loop1} + i_{loop2} + I_{L2} - i_{ch}}{C_{oss}} \tag{8}$$

$$\frac{di_{loop1}}{dt} = \frac{-v_{D1} + v_{D2} - v_{ds} + V_{C1} - L_{loop12}\frac{d_{i_{loop2}}}{dt}}{L_{loop1}} \tag{9}$$

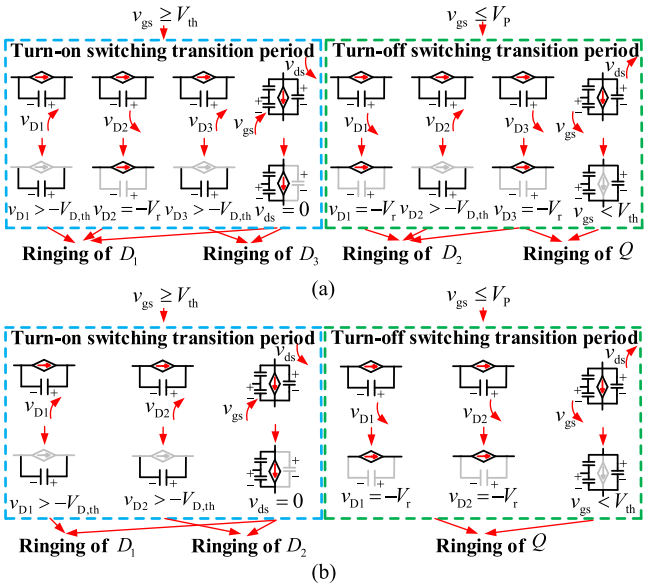


Fig. 6. Equivalent processes during turn-ON and turn-OFF switching transitions for (a) QBC and (b) ZSC.

$$\frac{di_{\text{loop2}}}{dt} = \frac{V_{\text{out}} - v_{\text{D3}} - v_{\text{ds}} - L_{\text{loop12}}\frac{d_{i_{\text{loop1}}}}{dt}}{L_{\text{loop2}}}. \tag{10}$$

The equations for ZSC during the switching transition are shown as follows:

$$\frac{dv_{\text{D1}}}{dt} = \frac{i_{\text{F1}} - i_{\text{loop1}}}{C_{\text{J1}}} \tag{11}$$

$$\frac{dv_{\text{D2}}}{dt} = \frac{i_{\text{F2}} + i_{\text{loop2}}}{C_{\text{J2}}} \tag{12}$$

$$\frac{dv_{\text{ds}}}{dt} = \frac{i_{\text{loop2}} - i_{\text{loop1}} + I_{L1} + I_{L2} - i_{\text{ch}}}{C_{\text{oss}}} \tag{13}$$

$$\frac{di_{\text{loop1}}}{dt} = \frac{V_{\text{in}} + v_{\text{D1}} + v_{\text{ds}} - V_{C1} - V_{C2} + L_{\text{loop12}}\frac{d_{i_{\text{loop2}}}}{dt}}{L_{\text{loop1}}} \tag{14}$$

$$\frac{di_{\text{loop2}}}{dt} = \frac{V_{\text{out}} - v_{\text{D2}} - v_{\text{ds}} + L_{\text{loop12}}\frac{d_{i_{\text{loop1}}}}{dt}}{L_{\text{loop2}}} \tag{15}$$

where $i_{\text{loop1}}$ and $i_{\text{loop2}}$ are the current in the two loops, $L_{\text{loop1}}$ and $L_{\text{loop2}}$ are the parasitic inductances in the two loops. Term $L_{\text{loop12}}$ is the common parasitic inductance of different loops. The switching transition process and the model of the eGaN HEMT $Q$, and diode $D_1$, $D_2$, and $D_3$ are shown in Fig. 6. When the switching process is completed, semiconductor devices will enter the ringing period. Due to the high-frequency oscillations of current and skin effect, high-frequency oscillation resistance $R_{\text{loop}}$ is generated in the power loop. Thus, resistance $R_{\text{loop}}$ is incorporated in (9), (10), (14), and (15).

## IV. Experimental Validation and Discussions

To verify the effectiveness of the proposed method, QBC and ZSC are tested with different values of gate resistances,

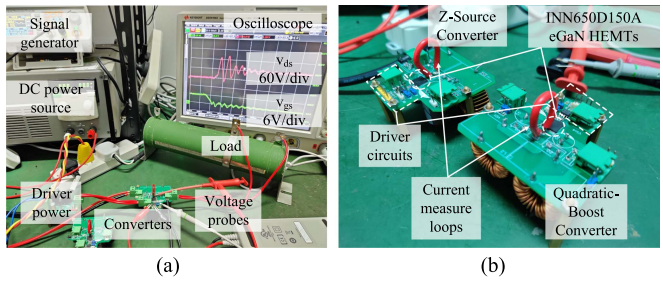


Fig. 7. (a) Experimental platform. (b) Converter test prototypes.

which are compared with the analytical results. The experimental platform and the converter prototypes are shown in Fig. 7. Theoretical and experimental results are presented in Fig. 8. The theoretical results are plotted by solving the differential equations, i.e., the model proposed in this letter, with the built-in Runge–Kutta solver in MATLAB. The simulation results are obtained in LTspice. The value of loop parasitic inductance in the differential equation can be extracted by the ANSYS Q3D Extractor. $L_{\text{Loop1}}$ and $L_{\text{Loop2}}$ consist of the parasitic inductance of the current measurement loop, the device package, and the printed circuit board. $L_{\text{Loop12}}$ is the parasitic inductance of the current measure loop and the device package. $L_{\text{Loop1}} \approx 43$ nH, $L_{\text{Loop12}} \approx 25$ nH, and $L_{\text{Loop2}} \approx 45$ nH in (9) and (10), and $L_{\text{Loop1}} \approx 47$ nH, $L_{\text{Loop12}} \approx 30$ nH, and $L_{\text{Loop2}} \approx 50$ nH in (14) and (15). Due to the influence of high-frequency oscillation resistance and other driver parameters, some differences are observed between experimental results and theoretical analysis, i.e., the results from the proposed model. From Fig. 8(a), (b), and (f), we can see that compared to the simulation results (from LTspice), the results of the proposed model (from MATLAB) are more consistent to the experimental results.

As indicated by the blue words in Fig. 8(b) and (d), with the given voltage and current stresses, for QBC, smaller values of $R_{\text{off}}$ may lead to false turn-ON. Inversely, for ZSC, bigger values of $R_{\text{off}}$ may lead to false turn-ON. The relationship between the voltage spike of $v_{\text{gs}}$ and resistance $R_{\text{off}}$ is not monotonic, which is caused by the nonlinear junction capacitance. A large $R_{\text{off}}$, while reducing the $\frac{dv_{\text{ds}}}{dt}$ in (2), may increase the current across the turn-OFF resistor, leading to false turn-ON.

In Fig. 8(c), experimental results and analytical results have displayed some discrepancy because in the turn-ON transition of ZSC, the output voltage of the dc power source $V_{\text{in}}$ has produced a voltage spike, as shown in Fig. 8(e). The input voltage changes cause $v_{\text{D1}}$ to be clamped, thus preventing any quick shutdown. The rise of $i_{\text{d}}$ becomes slower so that there is no large $L_{\text{CS}}\frac{di_{\text{d}}}{dt}$ on the common source inductance, i.e., there is no $v_{\text{gs}}$ spike. For faster switching speed and smaller switching loss, a smaller resistance $R_{\text{on}}$ can be chosen.

According to Fig. 8, in order to avoid overvoltage and false turn-ON, while improving the switching speed to pursue higher efficiency, for QBC, the most reasonable range of $R_{\text{on}}$ is between 5 and 10 Ω, and $R_{\text{off}}$ between 10 and 15 Ω. For ZSC, the most reasonable values of $R_{\text{on}}$ and $R_{\text{off}}$ are both 1 Ω. Fig. 9 shows the efficiency bar-charts of QBC and ZSC with various driver

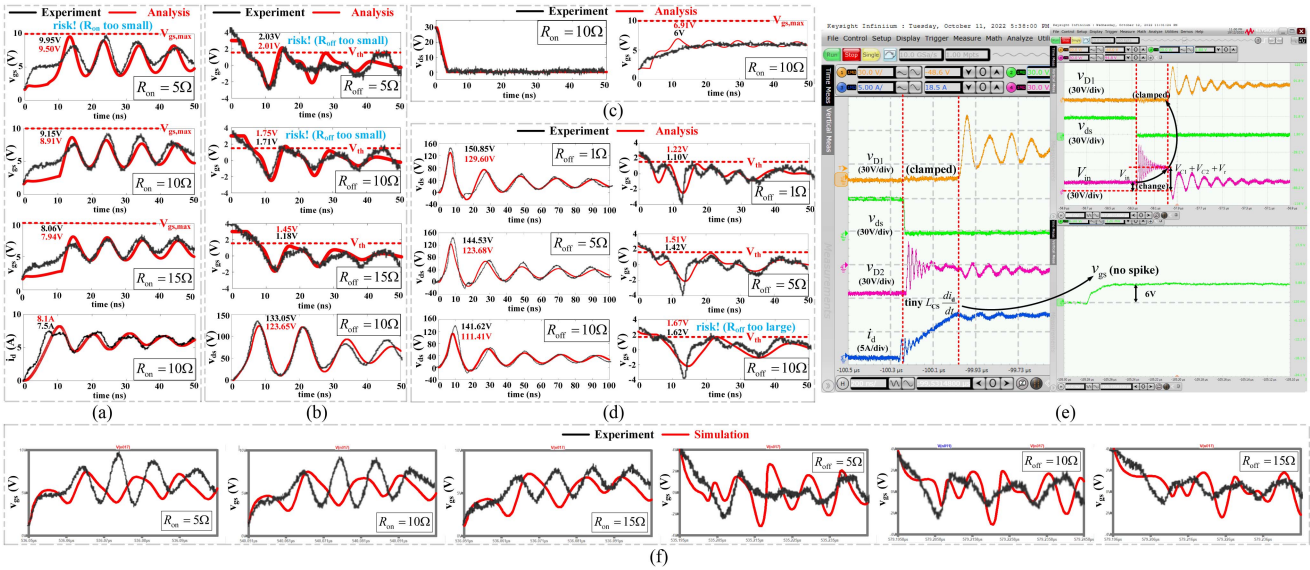


Fig. 8. Comparisons between analysis results (red line) and experiment results (black line). (a) QBC during turn-ON process. (b) QBC during turn-OFF process. (c) ZSC during turn-ON process. (d) ZSC during turn-OFF process. (e) Turn-ON switching process of the ZSC. (f) Comparisons between simulation results (red line) and experimental results (black line) of the QBC.

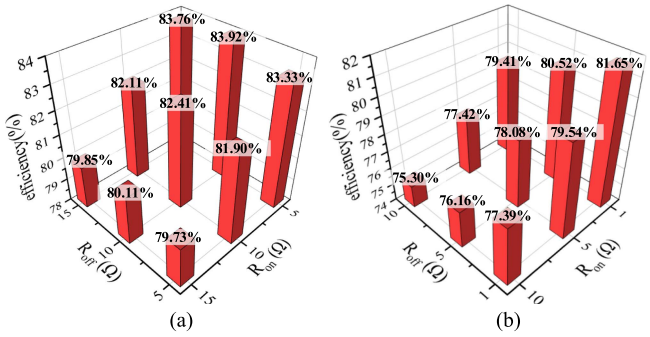


Fig. 9. Efficiency bar charts of (a) QBC and (b) ZSC with various driver resistances.

resistances. Comparing Figs. 8 and 9, a reasonable set of drive resistances can be chosen to ensure that the gate to source of eGaN HEMT is not damaged, and to improve the efficiency. When $R_{\text{off}} = 5\ \Omega$ and $R_{\text{off}} = 15\ \Omega$ in Fig. 9(a), for eGaN HEMT, faster switching speed may result in lower efficiency.

## V. Conclusion

In this letter, an accurate and simple modeling and parameter design method is proposed to describe the switching transitions of the eGaN HEMT. The proposed modeling method reflects the actual relationship between false turn-ON and turn-OFF resistances, and maybe the efficiency is negatively affected by switches' high switching speed. The effectiveness of this method has been verified by experimental results. The proposed modeling and design method can replace the traditional trial-and-error method and help select appropriate driver parameters with ease. It can also facilitate power electronics researchers and engineers to analyze the dynamics of the driver circuits with various driver resistances. However, there are some limitations of the model. Since the initial value of $v_{\text{gs}}$ during the turn-ON transition is the threshold voltage $V_{\text{th}}$ and during the turn-OFF transition, it is the platform voltage $V_{\text{P}}$, the model cannot be used to analyze the entire process of the change of $v_{\text{gs}}$. Hence, this model cannot be used to optimize the dead-time of the eGaN HEMT. There are some other factors that affect the accuracy of the method, which mainly include the following aspects.

1) In the model proposed in this study, the output voltage of dc power source has some unwanted chatterings.

2) The actual inductance current and the capacitance voltage in the experiment may differ from the values calculated from the mathematical model. This may result in a discrepancy between the accuracy of the theoretical analysis and the experimental results.

3) Compared with the models proposed by other scholars, this model neglects the voltage delay of the driver IC, the output characteristics, and the dynamic change of threshold voltage of the eGaN HEMT.

Each of these aspects can have an impact on the accuracy of modeling approach to some degree. In our future work, these contributory factors will be further investigated to construct a more resilient and realistic model.

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