Letters

Spread-Spectrum Frequency Modulation in a DC/DC Converter With Time-Based Control

Mauro Leoncini, Alessandro Bertolini, Paolo Melillo, Alessandro Gasparini, Salvatore Levantino, *Senior Member, IEEE*, and Massimo Ghioni, *Senior Member, IEEE*

***Abstract*—Spread-spectrum frequency modulation is a technique commonly adopted in dc/dc converters with pulse width modulation (PWM) control to reduce electromagnetic interference induced by switching. It typically requires a dedicated circuit. This article introduces a novel technique to implement spread-spectrum modulation in a dc/dc converter with time-based control, requiring only an additional transconductor. Modulating the bias current of the voltage-controlled oscillators used in the controller via a common-mode signal, the switching frequency of the converter is modulated without affecting the duty cycle. A theoretical analysis providing the link between modulation factor and design parameters is shown, and the circuit implementation in a time-based buck converter for general-purpose applications in a bipolar-CMOS-DMOS (BCD) process with 180 nm CMOS is described, together with a comparison between the simulated and the measured spectrum. The measured EMI reduction is 11.2 dB. The area occupation of the SSFM circuit is 0.032 mm^2.**

***Index Terms*—DC-DC power converters, electromagnetic interference, spread spectrum frequency modulation, time-based control.**

I. Introduction

THE reduction of electromagnetic interference (EMI) in switching power converter adopting a constant frequency pulse width modulation (PWM) control is commonly needed to meet the international regulations requirements related to electromagnetic compatibility (EMC) [1]. The preferred solution in dc/dc converters is to perform a frequency modulation of the PWM carrier in order to spread the energy of the switching frequency tones across a wider portion of the spectrum [2], [3], [4]. Depending on the selected modulation profile, the energy of the carrier is either spread into a specific portion of the spectrum i.e., using sinusoidal or triangular waveform [5], [6], or evenly distributed in the whole spectrum i.e., using a chaotic carrier frequency modulation [7], [8]. Although these solutions do not actually reduce the total amount of power that is radiated to the victim circuit, changing a narrow-band disturbance into a wide-band noise is recognized as an effective method to be compliant with the international regulation standards [5].

In the general case, the analytic expression in time domain of a carrier signal $s_c(t)$ with frequency f_c, modulated by a signal $v_m(t)$, which is a periodic function of frequency f_m having normalized amplitude $-1 < v_m(t) < 1$, can be written as

$$s_c(t) = A\cos\left(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} v_m(\tau)d\tau\right) \qquad (1)$$

where Δf is the peak frequency deviation from the carrier frequency f_c [5]. Following the description above, the modulation factor is defined as $m_f = \Delta f/f_m$. We know from theory that frequency modulation is in general a nonlinear operation, creating tones at offset multiples of f_m, and spreading the carrier power, $A^2/2$, over the Carson's bandwidth, that is equal to $2 \cdot \Delta f$ [9].

This article applies for the first time spread-spectrum frequency modulation (SSFM) to dc/dc converters with time-based control, introducing a novel technique requiring only an additional transconductor. It also provides design guidelines (see Section II), illustrates the implementation of the presented technique in a buck converter for general purpose applications in Bipolar-CMOS-DMOS (BCD) process (see Section III), and finally shows the measured results (see Section IV).

II. SSFM in Time-Based Controller

In voltage- or current-mode dc/dc converters, operating with a constant-frequency PWM controller, the periodic reference is provided by means of a clock circuit. In that kind of implementation, the SSFM is implemented using a dedicated frequency-modulated clock signal, typically generated by a phase-locked loop (PLL) circuit, whose schematic diagram is shown in Fig. 1. Frequency modulation is obtained using a programmable counter in feedback of the PLL, which acts as a frequency divider. The counter output is compared with the reference clock (f_{ck}) by the phase detector (PD), filtered by the low-pass filter (LPF) and used as a reference of a voltage-controlled oscillator

Manuscript received 24 October 2022; revised 22 November 2022; accepted 3 December 2022. Date of publication 9 December 2022; date of current version 14 February 2023. *(Corresponding author: Mauro Leoncini.)*

Mauro Leoncini, Paolo Melillo, Salvatore Levantino, and Massimo Ghioni are with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, 20133 Milano, Italy (e-mail: mauro.leoncini@polimi.it; paolo.melillo@polimi.it; salvatore.levantino@polimi.it; massimo.ghioni@polimi.it).

Alessandro Bertolini and Alessandro Gasparini are with the STMicroelectronics, AMG R&D, 20007 Milano, Italy (e-mail: alessandro.bertolini@st.com; alessandro.gasparini@st.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3227954.

Digital Object Identifier 10.1109/TPEL.2022.3227954

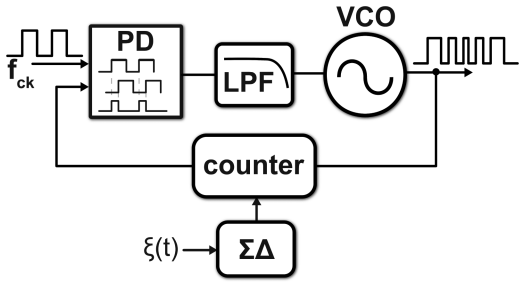

Fig. 1. Simplified block diagram of a PLL-based frequency modulator of the clock signal.

(VCO). Given the low-pass transfer function from the counter modulus-control and the output frequency, the modulation signal $\xi(t)$ has to be chosen with a frequency f_m much lower than the PLL bandwidth f_n. The digital $\Sigma\Delta$ modulator transforms the digital sequence $\xi(t)$ into a high-frequency sequence driving the modulus control of the counter. If the $\Sigma\Delta$ clock frequency $f_{\Sigma\Delta}$ is sufficiently high, i.e., $f_{\Sigma\Delta} \gg f_n$, the PLL tracks the average division ratio $\xi(t)$, generating a frequency modulation at the output, and the high-pass-shaped quantization noise of the $\Sigma\Delta$ is filtered by the PLL [10].

In recent years, time-based controllers have proven to be an effective alternative capable of reducing the area and quiescent power consumption of buck [11], [12] and boost type [13], [14] dc/dc converters. In that case, the clock signal is automatically generated by the integral control, which is implemented using a VCO of the ring-type. The relationship between the control voltage v_{ctrl} and the angular frequency of the oscillator ω_{vco} can be written as

$$\omega_{\text{vco}}(t) = \omega_{fr} + K_{\text{vco}} \cdot v_{\text{ctrl}}(t) \tag{2}$$

with K_{vco} being the oscillator gain and ω_{fr} the free-running angular frequency of the oscillator, i.e., the frequency that the oscillator assumes when the driving signal is zero and only the bias is present.

In a dc/dc converter with time-based control, the integral gain is usually implemented using a differential pair of matched current-starved current-controlled oscillator (CCO) driven by a transconductor with transconductance G_{mi}. Knowing that the oscillation frequency of a CCO is proportional to its bias current, SSFM can be implemented in this scheme by simply injecting a modulation current into the oscillator tuning node. A transconductor with transconductance $G_{m,\text{SSFM}}$ transforms the voltage signal $\xi(t)$ into a modulation current. The schematic diagram of a buck converter with time-based compensation implementing SSFM modulation is shown in Fig. 2, where L is the filter inductance, C is the filter capacitance, I_{Load} is the load current, and V_{ref} is the voltage reference. The proportional and the derivative control are generated using a current-controlled delay line (CCDL) driven by two transconductors (whose transconductance are G_{mp}, G_{md}), that are attached to the output voltage and to the high-pass-filtered output voltage (C_D, R_D), respectively [11].

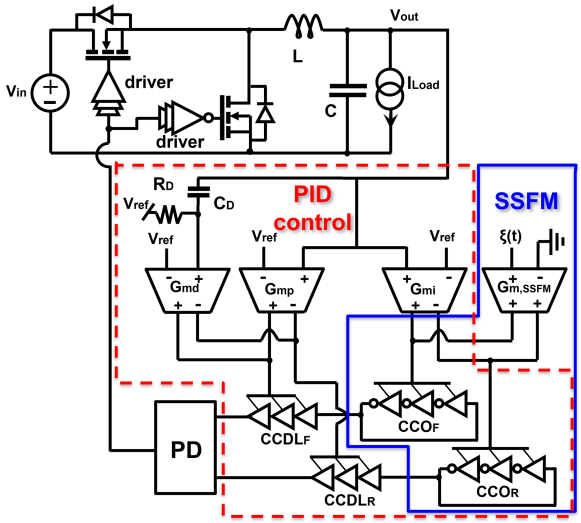

Fig. 2. Block diagram of the buck converter with time-based compensation and SSFM technique.

Starting from (2), and defining as $\xi(t) = A_m \cdot \sin(2\pi f_m t)$ a generic sinusoidal modulation signal, it is possible to write the angular frequency of the CCO circuit in Fig. 2 as

$$\omega_{\text{cco}}(t) = \omega_{fr} + G_{\text{int}}(V_{\text{out}} - V_{\text{ref}}) + G_{\text{SSFM}}\xi(t) \tag{3}$$

where the second term in (3) is related to the integral control, with integral gain equal to $G_{\text{int}} = G_{\text{mi}}K_{\text{cco}}$. Such a control path changes the frequency of the oscillator to provide an integral transfer function between the control voltage, $(V_{\text{out}} - V_{\text{ref}})$, and the oscillator phase, which is the controlled parameter in a time-based loop. The integral path, however, significantly affects the oscillation frequency only during the output voltage transients of the dc/dc converter. At steady-state, the controller matches the two inputs of the transconductor, giving a zero differential current at its outputs. For this reason, the second term in (3) can be neglected in the analysis. The third term in (3) is related to the SSFM and has a gain of $G_{\text{SSFM}} = K_{\text{cco}}G_{m,\text{SSFM}}$. In principle, it would be possible to directly modulate the bias current of the integral transconductor thus saving the extra transconductor $G_{m,\text{SSFM}}$. The modulation of the G_{mi} transconductor bias current, however, should be avoided since it will also affects its gain, changing the converter bandwidth, and stability.

Under these hypothesis, it is possible to derive the evolution in time of the first harmonic of the CCO in Fig. 2 as

$$s_{c,\text{cco}}(t) = A \cdot \cos\left[\omega_{fr}t + A_m G_{m,\text{SSFM}} K_{\text{cco}} \sin(\omega_m t)\right] \tag{4}$$

where $\omega_{fr} = 2\pi f_c$. (4) is equal to the generic expression of the SSFM in (1) with $2\pi\Delta f = A_m G_{m,\text{SSFM}} K_{\text{cco}}$ and $\int_{-\infty}^{t} v_m(\tau)d\tau = \sin(\omega_m t)$. As a result, the modulation factor of the proposed SSFM can be written as

$$m_f = \frac{A_m G_{m,\text{SSFM}} K_{\text{cco}}}{2\pi f_m}. \tag{5}$$

Applying frequency modulation to the PWM signal of a power converter also generates an unwanted amplitude modulation of the converter output voltage. A large amplitude modulation

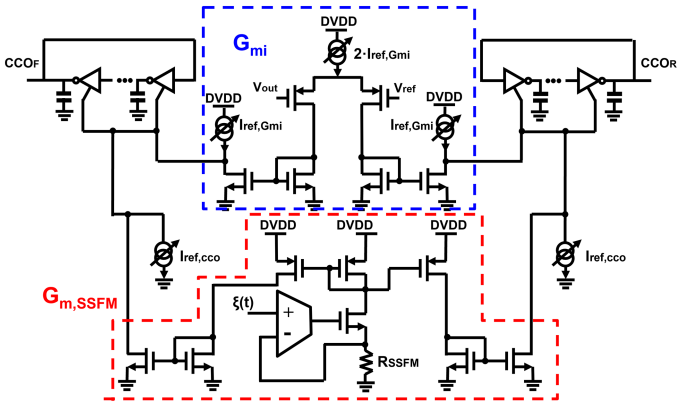

Fig. 3. Simplified circuit schematic of the time-based integral control with integrated SSFM.

generates noise if the modulation frequency f_m is inside the audio bandwidth, or flickering patterns if the converter is used to drive a display [15]. To minimize this effect, the SSFM should only affect the frequency of the PWM signal driving the power MOSFETS, while keeping the same duty cycle. Thanks to the differential nature of the control loop, this can be obtained applying a common-mode modulation current to the two CCOs, as shown in Fig. 2. Thanks to the common mode nature of the frequency modulation, the proposed technique does not significantly affect the dynamic performance of the converter.

When the converter reaches the steady state, $V_{\text{out}} - V_{\text{ref}} = 0$, and the phase difference between CCO_F and CCO_R is equal to the phase difference at the input of the PD $\Delta\phi$, which is proportional to the duty cycle ($D = \Delta\phi/2\pi$). Considering the integral relationship between frequency and phase, it is possible to write

$$\Delta\phi(t) = \phi_0 + \int_0^t \omega_{\text{cco}_F}(\tau)d\tau - \int_0^t \omega_{\text{cco}_R}(\tau)d\tau \qquad (6)$$

where ϕ_0 is the phase in t = 0. Substituting (3) in (6), and remembering that the control loop forces the frequencies of the two oscillators to be equal, (6) is reduced to

$$\Delta\phi(t) = \phi_0 + (G_{\text{SSFM}_F} - G_{\text{SSFM}_R}) \cdot \int_0^t \xi(\tau)d\tau. \qquad (7)$$

This means that, regardless of the modulation signal $\xi(t)$, the proposed modulation technique does not affects the duty-cycle, provided that the feedback G_{SSFM_F} and the reference G_{SSFM_R} gains are equal, i.e., the two VCOs are matched. Although the proposed modulation method has been demonstrated for a time-based converter of the buck-type, it could be easily extended to an arbitrary converter topology with time-based control.

III. Circuit Implementation

The presented SSFM technique has been applied to a buck converter with time-based control implemented in BCD process. The circuit schematic of the SSFM control is shown in Fig. 3. The CCOs are implemented using a set of current-starved inverters that are controlled by selecting the magnitude of their bias current. Each inverter cell is loaded with a small capacitance

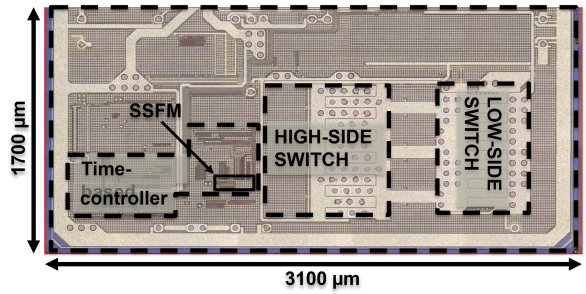

Fig. 4. Die microphotograph of the prototype buck converter with time-based control and SSFM technique.

to meet the target oscillation frequency of 1.5 MHz. The G_{mi} is designed as a simple differential transconductor, where the output current is injected in the two oscillators control nodes. To keep the CCO bias independent of the transconductor, the bias current $I_{\text{ref},Gmi}$ is removed before the injection. This solution is used to decouple the two stages allowing the designer to tune the G_{mi} gain by acting on the $I_{\text{ref},Gmi}$ with no impact on the oscillator gain (K_{cco}) nor on the free running frequency of the oscillator. The SSFM current is obtained by buffering the external modulation signal $\xi(t)$ over the resistance R_{SSFM}. Being all the current mirrors designed with unitary gain, the overall transconductance gain in (4) is $G_{m,\text{SSMF}} = 1/R_{\text{SSFM}}$. The common-mode voltage of the modulation signal has to be selected such that the minimum voltage drop across R_{SSFM} is zero. Considering a sinusoidal modulation, this is achieved using a driving signal of $\xi(t) = A_m/2 + A_m \sin(\omega_m t)$. Under these assumptions, the free-running radiant frequency of the CCO in Fig. 3 can be computed as

$$\omega_{fr} = \left(I_{\text{ref,cco}} + \frac{A_m}{2R_{\text{SSFM}}}\right) K_{\text{cco}}. \qquad (8)$$

IV. Simulation and Measurement Results

The buck converter for general purpose applications with time-based control and with the presented SSFM technique has been fabricated in a BCD process with 180 nm CMOS. Fig. 4 shows the die microphotograph, where the SSFM circuit has an area occupation of 0.032 mm^2. The input voltage ranges from 5 to 40 V to be compliant with industrial and automotive applications, while the output voltage is 3.3 V. The filter inductor L and the output capacitor C are the only external components having a value of 4.7 μH and 30 μF, respectively. The converter was designed to sustain a maximum load current of 1 A while working in CCM mode with a switching frequency of 1.5 MHz. The converters parameters are summarized in Table I.

The SSFM technique has been validated comparing the simulated results obtained from a behavioral model in SIMPLIS with the experimental ones. Using the behavioral model, a transient simulation was performed in the case of no SSFM signal and triangular modulation with amplitude of $A_m = 0.25$ V and frequency of $f_m = 5$ kHz. The model was designed with a $K_{\text{cco}} = 377$ krad/μA and a $G_{m,\text{SSFM}} = 5$ μA/V leading to an overall modulation factor of $m_f = 15$. These values was chosen to match the parameter of the silicon prototype. The spectrum of

TABLE I
MEASURED PERFORMANCE OF THE BUCK CONVERTER

Parameter	Value
Input voltage	5 V – 40 V
Output voltage	3.3 V
L, C	4.7 μH, 30 μH
Max load current	1 A
Switching frequency	1.5 MHz
Measured peak efficiency (@V_{in} = 24 V)	84.4%
Measured peak efficiency (@V_{in} = 12 V)	88.6%

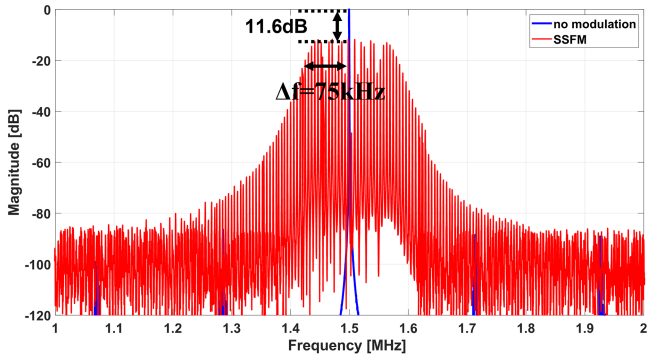

Fig. 5. Simulated spectrum of the buck converter is compared when the SSFM is active (red) or not active (blue).

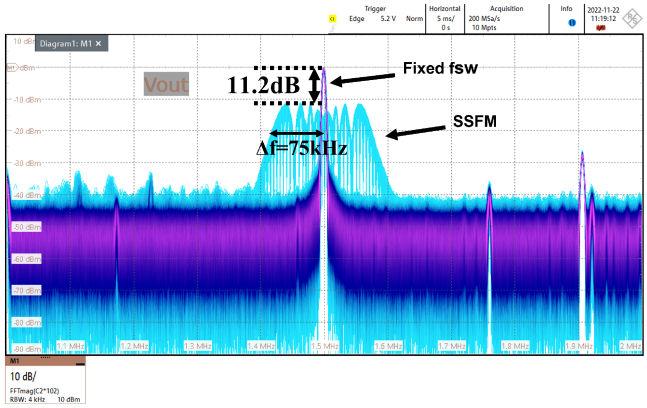

Fig. 6. Measured output voltage spectrum of the buck converter is compared when the SSFM is active or not active.

the output voltage of the converter, obtained before and after the application of the SSFM signal $\xi(t)$, are compared in Fig. 5. The spectrum values are normalized to the amplitude of the reference frequency tone when no SSFM is applied. The simulation shows a peak amplitude reduction of the main tone of about 11.6 dB.

The output voltage spectrum of the prototype converter was measured under the same input voltage $\xi(t)$ and it is shown in Fig. 6. As for the simulated case, the amplitudes are normalized to the amplitude of the reference tone when no SSFM is applied. The measured results are in close agreement with the simulated one. In Fig. 7, the peak EMI reduction is measured over the entire input voltage and load current range, showing only a marginal variation. In Fig. 8, the converter output voltage ripples before and after a triangular modulation with peak-to-peak amplitude of 0.2 V and $f_m = 5$ kHz are presented. Fig. 9 shows the measured efficiency of the converter. Being the current consumption of the

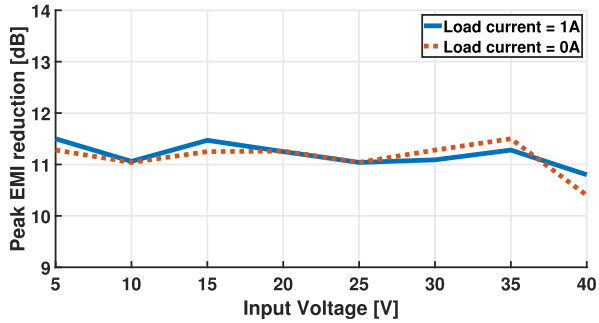

Fig. 7. Measured peak EMI reduction at different input voltages with a load current of 1 A (solid line) and 0 A (dotted line).

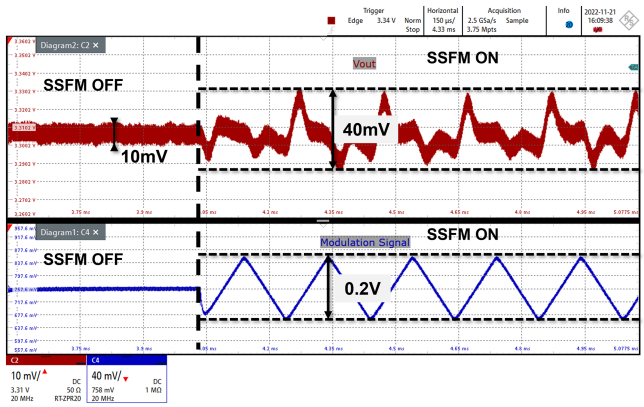

Fig. 8. Measured output voltage ripple of the converter. The modulation signal is a trianglular waveform with peak-to-peak amplitude of 0.2 V and $f_m = 5$ kHz. The converter operating condition is $V_{in} = 15$ V and $I_{\text{Load}} = 0$ A.

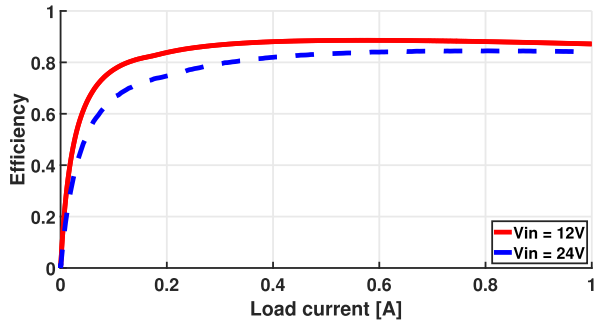

Fig. 9. Measured converter efficiency of the converter when the input voltage is 12 V (solid line) and 24 V (dashed line).

additional transconductor $G_{m,\text{SSFM}}$ only few μA, the efficiency curves are the same also when the SSFM is active. In Table II, the SSFM in time-based control is compared with the state-of-the-art. The proposed technique favorably compares with the existing solutions in terms of EMI reduction, when similar modulation factors are used. Moreover, since the time-based control integrates CCOs to perform the controller's integral gain, the SSFM modulation circuit only requires an additional transconductor, with minimum impact on the converter area and power consumption.

TABLE II
STATE-OF-THE-ART COMPARISON

	This work	[16]	[17]	[18]	[19]
Modulation Method	**FM of CCO in Time-Based Control**	Analog FM in Digital Core	All-Digital Delay-Lines	FM in Current-Mode Ripple-Based Converter	Multistep Piecewise Linear Modulator
Process	**0.18μm BCD**	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS
FM integrated in Converter	**yes**	no	no	yes	yes
Input Voltage	**5-40V**	n.a.	n.a.	2.8–4.2V	2.2–3.3V
Output Voltage	**3.3V**	n.a.	n.a	1.3–2.2V	1.7V
Modulation profile	**Triangular**	Chaotic	Arbitrary	Triangular	Onion Wave
Modulation Parameters	$\mathbf{f_0 = 1.5MHz}$ $\mathbf{\Delta f = 75kHz}$ $\mathbf{f_m = 5kHz}$ $\mathbf{RBW = 4kHz}$	$f_0 = 1$MHz $\Delta f = 100$kHz $f_m = 35$kHz $RBW = 9$kHz	$f_0 = 10$MHz $\Delta f = 900$kHz $f_m = 10$kHz $RBW = 9$kHz	$f_0 = 8 - 11$MHz $\Delta f = 1.5$MHz $f_m = 10$kHz $RBW = 3$kHz	$f_0 = 2 - 2.4$MHz $\Delta f = 400$kHz $f_m = n.a.$ $RBW = 10$kHz
EMI Reduction	**11.2dB**	10.1dB	17.6 dB	19 dB	12 dB
Area [mm^2]	**0.032***	0.096	0.182	n.a.	0.103**

* Triangular voltage waveform external.
** Sum of the modulator and oscillator area extrapoled from the die microphotograph.

V. CONCLUSION

SSFM is a commonly used technique to reduce the EMI produced by dc/dc converters. In this article, a novel SSFM technique has been introduced and applied to a buck converter with time-based control, by adding a simple transconductor to the integral control stage. As a result, the area occupation of the solution is only 0.032 mm^2 is lower compared to existing solutions. This article has also presented an analysis providing a link between the circuit parameters and the modulation factor. The proposed solution has been experimentally verified comparing the measured output voltage spectrum of the prototype buck converter with the simulated one.

REFERENCES

[1] Code of Federal Regulations 47 (47CFR), Part 15, "Subpart B: Unintentional radiators." Accessed: Dec. 1, 2022. [Online]. Available: http://www.ecfr.gov/

[2] K. K. Tse, H. S. Chung, S. Y. Huo, and H. C. So, "Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 399–410, Mar. 2000.

[3] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI reduction in switched power converters using frequency modulation techniques," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 569–576, Aug. 2005.

[4] D. Gonzalez et al., "Conducted EMI reduction in power converters by means of periodic switching frequency modulation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2271–2281, Nov. 2007.

[5] F. Pareschi, R. Rovatti, and G. Setti, "EMI reduction via spread spectrum in DC/DC converters: State of the art, optimization, and tradeoffs," *IEEE Access*, vol. 3, pp. 2857–2874, 2015.

[6] S. Johnson and R. Zane, "Custom spectral shaping for EMI reduction in high-frequency inverters and ballasts," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1499–1505, Nov. 2005.

[7] K. K. Tse, R.W.M. Ng, H. S.-H. Chung, and S. Y. R. Hui, "An evaluation of the spectral characteristics of switching converters with chaotic carrier-frequency modulation," *IEEE Trans. Ind. Electron.*, vol. 50, no. 1, pp. 171–182, Feb. 2003.

[8] Z. Yang, H. Li, Y. Ding, and J. Wang, "Continuous multi-scroll chaotic PWM and its chaotic signal selection method for EMI suppression of power converters," *IEEE Access*, vol. 8, pp. 168910–168922, 2020.

[9] H. S. Black, *Modulation Theory*, New York, NY, USA: Van Nostrand, 1953.

[10] M. Kokubo et al., "Spread-spectrum clock generator for serial ATA using fractional PLL controlled by/spl delta//spl Sigma/modulator with level shifter," in *Proc. IEEE Int. Dig. Tech. Papers. Solid-State Circuits Conf.*, 2005, vol. 1, pp. 160–590.

[11] S. J. Kim et al., "High frequency buck converter design using time-based control techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 990–1001, Apr. 2015.

[12] J. G. Kang, J. Park, M. G. Jeong, and C. Yoo, "A time-domain-controlled current-mode buck converter with wide output voltage range," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 865–873, Mar. 2019.

[13] M. Leoncini, A. Bertolini, A. Gasparini, S. Levantino, and M. Ghioni, "An 800-mA time-based boost converter in 0.18um BCD with right-half-plane zero elimination and 96% power efficiency," in *Proc. IEEE Eur. Solid State Circuits Conf.*, 2021, pp. 223–226.

[14] T. Rosa, M. Leoncini, and S. L. M. Ghioni, "A novel start-up technique for time-based boost converters with seamless PFM/PWM transition," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5.

[15] G. Z. K. Scott, "Spread spectrum frequency modulation reduces EMI," Analog Devices Inc., 2019. [Online]. Available: https://www.analog.com/media/en/technical-documentation/tech-articles/Spread-Spectrum-Frequency-Modulation-Reduces-EMI.pdf

[16] F. Pareschi, G. Setti, R. Rovatti, and G. Frattini, "Short-term optimized spread spectrum clock generator for EMI reduction in switching DC/DC converters," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 61, no. 10, pp. 3044–3053, Oct. 2014.

[17] M. De Martino, D. De Caro, D. Esposito, E. Napoli, N. Petra, and A. G. M. Strollo, "A standard-cell-based all-digital PWM modulator with high resolution and spread- spectrum capability," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 65, no. 11, pp. 3885–3896, Nov. 2018.

[18] S. H. Pakala, P. R. Surkanti, and P. M. Furth, "A spread-spectrum mode enabled ripple-based buck converter using a clockless frequency control," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 66, no. 3, pp. 382–386, Mar. 2019.

[19] H.-Y. Huang, H. M. Villaruz, and N. M. Mapula, "High-efficiency Low-EMI buck converter using multistep PWL and PVT insensitive oscillator," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9325–9332, Aug. 2022.