Nondifferential AC Choppers Based Identical Bipolar Buck–Boost AC–AC Converter Without Commutation Issue

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***Abstract*—This article proposes a new H-bridge structured bipolar pulsewidth modulation (PWM) buck–boost ac–ac converter based on the nondifferential ac choppers. The proposed converter can generate simple identical noninverting and inverting buck–boost voltage outputs by modulating one phase leg with single control duty ratio (d_1 or d_2). It can also provide flexible identical noninverting and inverting buck–boost operations by modulating both phase legs with two control duty ratios (d_1 and d_2). In the proposed topology, the use of nondifferential ac choppers eliminates the complementary switching of ac switches and related inductor open-circuit issue. Moreover, half the switching devices are configured as switching-cell units to avoid shoot-through occurrence due to accidental turn-ON of complementary switches. Therefore, the proposed topology is free from commutation issue and can abolish PWM deadtimes to produce high-quality output with improved utilization of switch duty ratios. It also provides continuous input current and can perform normally with reactive loads. It has the potential to mitigate both voltage sags and swells (due to bipolar operation) when used as series voltage compensator; and unlike the existing nondifferential bipolar ac–ac converters, it can provide compensation for more intense voltage sags (of above 50%) as well. In-depth analysis of the proposed topology and hardware verifications are provided in this article.**

***Index Terms*—AC–AC power converter, buck–boost operation, commutation issue, identical noninverting/inverting process, voltage sag and swell.**

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I. Introduction

With growing load condition diversity, various sources of interference, and continuous integration of distributed renewable energy sources to the grid, the grid voltage supplied to the consumer is at increasing risk of power quality problems [1]. Among other power quality issues, voltage sags, swells, and transients can damage the voltage sensitive equipment's and interrupt the industrial processes. This can result in financial penalties, loss of production, missing of important data, and increase in line losses [2].

The most common topologies for ac–ac power conversion are back-to-back H-bridge-based indirect ac–dc–ac converters with an intermediate dc link [3]. Thanks to the use of dc-link capacitor bank, the front-end rectifier and rear-end inverter stages are decoupled to a great extent, providing more flexibility over control of output voltage magnitude, frequency, and phase. Also, constant input voltage exists for inverter stage irrespective of line-frequency variations in supply voltage that increases its power utilization. However, dc-link capacitors have large volume that significantly contributes to the overall size of the converter. Moreover, electrolytic capacitors are usually employed to fulfill large capacitance demand at dc link, which have relatively smaller life period due to their wear out characteristics [4]. Therefore, the direct ac–ac converters are widely developed with stage–stage power conversion and without necessity of dc-link capacitor bank, in an effort to reduce power conversion stages, control complexity, and size of power converter. Despite their limited control over frequency and phase of produced voltage, direct ac–ac converters can find various useable applications aimed at grid voltage regulation.

To ensure the supply of smooth ac voltage during grid power quality events, especially voltage sags and swells, various devices have been developed [5], [6], [7], [8], [9], [10]. These devices are termed as ac voltage regulators [5], [6], ac voltage stabilizers [7], ac sag supporters [6], and dynamic voltage restorers (DVRs) [8], [9]. Among them, the series voltage injection devices (ac sag supporters [7] and DVRs [9], [10]) are more preferred due to their ability to process only difference of supply and load power, reducing the size and cost of the system compared with full-power rated ac regulators [5], [6], [7]. The direct ac–ac converter-based compensators can save external energy source and dc-link capacitor and, thus, improve the performance, size,

and cost of the system. Therefore, to regulate the grid voltage without concerning the phase shift and harmonics, the direct ac–ac converters are more preferred and continuously researched for voltage regulation [11], [12].

The fundamental buck, boost, and buck–boost ac–ac converters are simplest single-stage topologies [13]. However, buck and boost converters have narrow voltage gains that decrease the voltage sag mitigation range. The buck–boost converter is prone to higher device voltage/current stresses and poor input and output power quality. Moreover, these converters are unipolar and, therefore, cannot mitigate voltage swell unless assisted with oversized and overpriced tapped-winding transformer [14].

Z-source ac–ac converters are developed [15], [16] that can provide bipolar output by adding a unique impedance network. Nevertheless, they use many inductors and capacitors. Also, the unavailability of noninverting buck operation and sharp gain curve in inverting buck–boost operation decreases their practical operation range. A current-fed inverting and noninverting buck–boost ac–ac converter is proposed in [17] that can minimize the number of passive elements. However, it has complex modulation, large number of semiconductor devices in power loop, and does not work with nonunity power factor loads. A unified inverting and noninverting buck–boost ac–ac converter is proposed [18] with minimum number of passive elements, simple switch modulation and operation, and support for reactive loads. However, it has discontinuous input and output currents and its components are exposed to higher stresses. A bipolar buck–boost ac–ac converter is proposed with continuous input and output currents [19]. However, it has complicated modulation strategy and circuit operation due to its composite configuration. Moreover, all these ac–ac converters [13], [14], [15], [16], [17], [18], [19] are susceptible to commutation issues where slight overlap- or deadtime between complementary switches (which is inevitable to occur due to delays in gate driving signals and limited speed of switching devices [20]) would cause short circuit of voltage source (switch current spikes) and/or open circuit of inductor (switch voltage spikes), respectively. Therefore, pulsewidth modulation (PWM) deadtimes are intentionally added in conjunction with *RC* snubbers [21] or complex commutation techniques [22] to get rid of commutation issues. Nevertheless, these approaches have some drawbacks such that the deadtimes cause switch duty cycle reduction and degrades output power quality; *RC* snubbers result in power dissipation and do not address short-circuit issues under fault conditions; soft-commutation techniques bring control complexity, require voltage/current sensing, and may not work well for distortion in input voltage (especially across zero crossing).

The switching-cell (SC) configuration-based ac–ac converters [20], [23] are immune from dead and overlap time and can inherently solve the commutation issue. However, the basic buck, boost, and buck–boost SC ac–ac converters [20], [23] have the same limitations as their non-SC counterparts [13]. A noninverting buck–boost SC ac–ac converter is proposed [24] with discrete buck and boost voltage operations and applied as DVR. However, due to its unipolar operation, it uses a line-frequency tapped-winding transformer (to also provide compensation for voltage swell) that would make the system uneconomical. An inverting and noninverting SC buck–boost ac–ac converter is proposed [25] that can address voltage sag and swell without using tapped-winding transformer. However, it has discontinuous input and output currents and cannot regulate voltage sags with depth of more than 50%. An SC bipolar buck–boost ac–ac converter is proposed [26] with continuous input and output currents. However, it needs large number of inductors with complex modulation. Moreover, these SC ac–ac converters [20], [23], [24], [25], [26] are required to implement SC structure for each switching device (to avoid short circuit) by adding one additional diode for each switch. This greatly increases the number of external diodes, their cost, and footprint. Recently, an improved bipolar-type buck ac–ac converter with nondifferential ac coppers is proposed [27] by applying partial SC configuration on original topology in [28]. It can eliminate commutation issue by adding fewer external diodes than the existing SC converters [20], [23], [24], [25], [26]. Nevertheless, the converter can only provide buck operation that restricts its voltage regulation range, i.e., it can mitigate only shallow voltage sags (below 50%). Also, the input current is discontinuous that increases the THD of input line current and, thus, requires additional input *LC* filter.

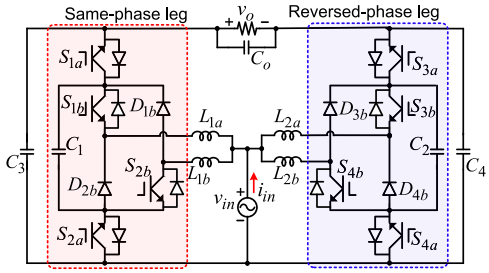

Fig. 1. Proposed bipolar SC buck–boost ac–ac converter.

In this article, a new nondifferential PWM ac choppers based bipolar buck–boost ac–ac converter is proposed. It can solve the commutation issue by incorporating a partial SC structure in which the added number of external diodes is only half of the active switches. The proposed converter has identical noninverting and inverting buck–boost processes (with single or two duty ratio controls) that would greatly simplify the circuit operation, parameter optimization, and control (unlike exiting bipolar ac–ac converters [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]). It can draw continuous sinusoidal input current without needing extra *LC* filter. Also, if used as DVR, the bipolar buck–boost operation would make it able to mitigate wide magnitudes of both voltage sags (below and above 50%, unlike [27] and [28]) and swells without using a tapped-winding transformer.

II. Proposed Converter and Its Operation

Fig. 1 shows the proposed bipolar-type SC buck–boost ac–ac converter. It has an ac H-bridge structure consisting of two nondifferential ac choppers based same-phase and reversed-phase legs (SP-Leg and RP-Leg).

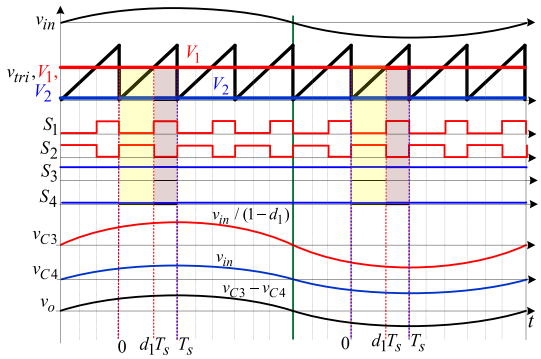

Fig. 2. PWM switching signals for SDRC-NIBB operation.

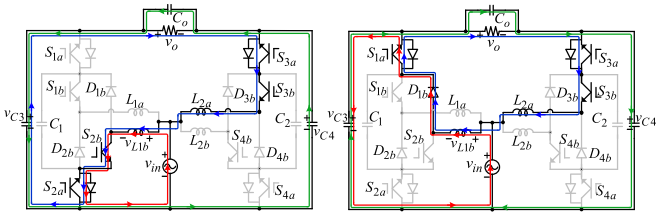

Fig. 3. Equivalent circuits for SDRC-NIBB operation. (a) Interval d_1T_s. (b) Interval $(1-d_1)T_s$.

Each phase leg consists of four IGBTs. The middle two IGBTs in each phase leg (S_{1b}, S_{2b} for SP-Leg, and S_{3b}, S_{4b} for RP-Leg) are arranged in SC configuration by adding two extra fast recovery diodes (D_{1b}, D_{2b} for SP-Leg, and D_{3b}, D_{4b} for RP-Leg) and separation inductors (L_{1a}, L_{1b} for SP-Leg, and L_{2a}, L_{2b} for RP-Leg). Capacitors C_1 and C_2 are connected across SCs of SP-Leg and RP-Leg for providing an inductor current path during deadtime. Input source v_{in} shares common ground point with SP-Leg and RP-Leg and its positive (reference) terminal is connected to separation inductors. Capacitors C_3 and C_4 are connected across SP-Leg and RP-Leg, respectively, and load is differentially connected across their output terminals.

A. *Single Duty Ratio-Controlled Noninverting Buck–Boost (SDRC-NIBB) Operation*

Fig. 2 shows the PWM control signals. The control reference signal V_2 for modulation of RP-Leg is set to zero, and $d_2 = 0$. Switch S_3 of RP-Leg is completely ON and S_4 is OFF. SP-Leg is modulated at high frequency through control reference signal V_1. S_2 is ON for time interval d_1T_s and its complementary switch S_1 is ON for interval $(1-d_1)T_s$. The equivalent circuits are shown in Fig. 3. Body diodes of switches $S_{1b} - S_{4b}$ do not conduct due to the use of external diodes and, therefore, omitted in equivalent circuit diagrams. L_{2a} and C_4 form permanent *LC* filter across v_{in}, and $v_{C4} = v_{\text{in}}$. Circuit operation for $v_{\text{in}} > 0$ is explained as follows.

Interval [0∼d_1T_s]: The equivalent circuit is shown in Fig. 3(a). S_2 and S_3 are ON and S_1 and S_4 are OFF. L_{1b} stores energy from v_{in}. L_{2a} keeps freewheeling load current i_o. The

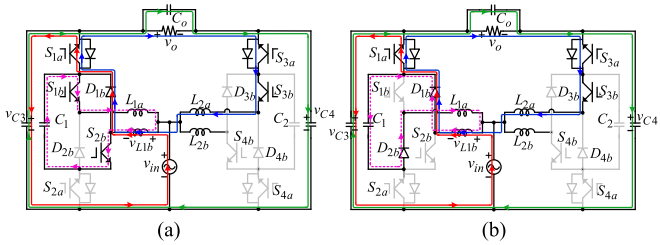

Fig. 4. Equivalent circuits showing commutation study of the proposed converter for SDRC-NIBB operation ($v_{\text{in}} > 0$). (a) Overlap time: S_{1b} and S_{2b} are turned ON. (b) Deadtime: S_{1b} and S_{2b} are turned OFF.

circuit voltage/current relation is given by

$$\frac{di_{L1b}}{dt} = \frac{v_{\text{in}}}{L_{1b}}. \tag{1}$$

Interval [d_1T_s∼T_s]: This is shown in Fig. 3(b). S_1 and S_3 are ON and S_2 and S_4 are OFF. v_{in} and L_{1b} together charge C_3. L_{2a} keeps freewheeling load current i_o. Therefore, i_o current remains continuous. Circuit voltage/current relation is given by

$$\frac{di_{L1b}}{dt} = \frac{v_{\text{in}} - v_{C3}}{L_{1b}}. \tag{2}$$

The circuit operation remains same for $v_{\text{in}} < 0$. Only difference is that the circuit voltage and current are reversed. Capacitor C_3 voltage [by applying voltage-second balance condition on L_{1b} from (1) and (2)] and C_4 voltage are given by

$$v_{C3} = \frac{v_{\text{in}}}{1-d_1}, \quad v_{C4} = v_{\text{in}}. \tag{3}$$

The output voltage v_o and voltage gain G_1 (v_o/v_{in}) are given by

$$v_o = v_{C3} - v_{C4} = v_{\text{in}} \frac{d_1}{1-d_1} \tag{4}$$

$$G_1 = \frac{v_o}{v_{\text{in}}} = \frac{d_1}{1-d_1}. \tag{5}$$

In practice, there exists a small dead or overlap time between high-frequency complementary switches due to finite response time of switching devices and nonidentical time delays of gate driving circuits [20]. To understand the natural safe commutation ability of the proposed converter, small overlap time and deadtime are inserted in high-frequency complementary switches S_{1b} and S_{2b} for SDRC-NIBB operation, and equivalent circuits are shown in Fig. 4.

The equivalent circuit of the proposed converter for switch overlap time is shown in Fig. 4(a), when S_{1b} and S_{2b} are both turned ON. As observed, shoot through of capacitor C_1 is avoided by inductors L_{1a} and L_{1b}, which limit C_1 current by providing high-impedance path. Fig. 4(b) shows the equivalent circuit for deadtime when S_{1b} and S_{2b} are both turned OFF. Capacitor C_1 and external diodes of switches S_{1b} and S_{2b} provide continuous path to inductor L_{1a} and L_{1b} currents.

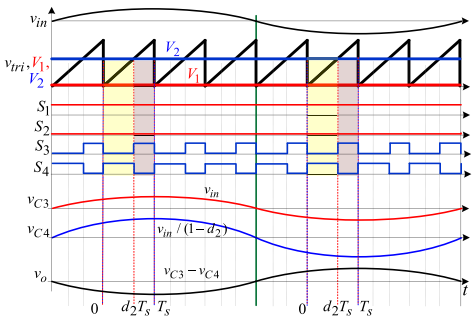

Fig. 5. PWM switching signals for SDRC-IBB operation.

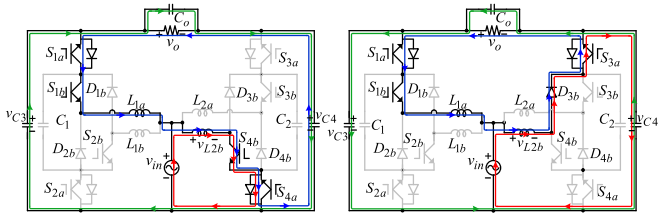

Fig. 6. Equivalent circuits for SDRC-IBB operation. (a) Interval d_2T_s. (b) Interval $(1-d_2)T_s$.

B. Single Duty Control-Controlled Inverting Buck–Boost (SDRC-IBB) Operation

Fig. 5 shows the PWM control signals. RP-Leg now operates at high frequency by modulating control reference signal V_2. The ON-time of S_4 makes up the time interval d_2T_s and the conduction time of its complementary switch S_3 makes up the time interval $(1-d_2)T_s$. Control reference signal V_1 for SP-Leg is set to zero (i.e., $d_1 = 0$). Switch S_1 is completely ON and S_2 is OFF. The equivalent circuits are depicted in Fig. 6 (for $v_{\text{in}} > 0$). L_{1a} and C_3 create an *LC* filter across v_{in} such that $v_{C3} = v_{\text{in}}$. Circuit operation is given as follows.

Interval [0∼d_2T_s]: The circuit is shown in Fig. 6(a). S_1 and S_4 are ON and S_2 and S_3 are OFF. v_{in} energizes L_{2b}. Load current i_o freewheels through L_{1a}

$$\frac{di_{L2b}}{dt} = \frac{v_{\text{in}}}{L_{2b}}. \tag{6}$$

Interval [$d_2T_s \sim T_s$]: The circuit is depicted in Fig. 6(b). S_1 and S_3 now conduct circuit current and S_2 and S_4 are in cutoff state. C_4 is charged from v_{in} and L_{2b}. L_{1a} keeps providing freewheeling path to i_o

$$\frac{di_{L2b}}{dt} = \frac{v_{\text{in}} - v_{C4}}{L_{2b}}. \tag{7}$$

Circuit voltages and currents are reversed for $v_{\text{in}} < 0$ but the operation remains same. Capacitor C_3 voltage (through voltage-balance condition on L_{2b}) and capacitor C_4 voltage are determined as follows:

$$v_{C3} = v_{\text{in}} \text{ and } v_{C4} = \frac{v_{\text{in}}}{1-d_2}. \tag{8}$$

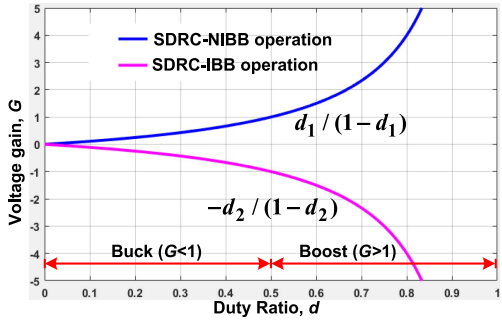

Fig. 7. Voltage gain versus duty ratio plots for the proposed SDRC-NIBB and SDRC-IBB operations.

The output voltage v_o and voltage gain G_2 (v_o/v_{in}) are given by

$$v_o = v_{C3} - v_{C4} = -v_{\text{in}}\frac{d_2}{1-d_2} \tag{9}$$

$$G_2 = \frac{v_o}{v_{\text{in}}} = -\frac{d_2}{1-d_2}. \tag{10}$$

As observed, voltage gain G_2 for inverting buck–boost operation is same as G_1 for noninverting operation. However, the voltage v_o polarity across load is reversed as indicated by negative sign. These voltage gains are plotted in Fig. 7 against switch duty ratio.

C. Two Duty Ratio-Controlled Noninverting and Inverting Buck–Boost (TDRC-NIBB/IBB) Operations

Fig. 8(a) and (b) shows the switch control signals for TDRC-NIBB and TDRC-IBB operations, respectively. Both duty ratios d_1 and d_2 are now tuned together to provide maximum control degree of freedom. The ON-time of complementary switches S_2 and S_1 in SP-Leg constitute time intervals d_1T_s and $(1-d_1)T_s$, respectively. However, the conduction times of S_4 and S_3 in RP-Leg make up the time intervals d_2T_s and $(1-d_2)T_s$, respectively. Noninverting and inverting outputs are obtained for $d_1 > d_2$ and $d_2 > d_1$, respectively.

1) Noninverting Buck–Boost (TDRC-NIBB) Operation ($d_1 > d_2$): Fig. 8(a) shows the control signals and Figs. 9(a)–(c) show the equivalent circuits. The circuit operation is as follows.

Interval [0∼d_2T_s]: S_2 and S_4 are ON and S_1 and S_3 are OFF [see Fig. 9(a)]. L_{1b} stores energy from v_{in} and conducts a current $i_{\text{in}} + i_o$. L_{2a} releases energy while conducting a current i_o. The circuit equations are given by

$$\frac{di_{L1b}}{dt} = \frac{v_{\text{in}}}{L_{1b}}, \quad \frac{di_{L2a}}{dt} = -\frac{v_{\text{in}}}{L_{2a}}. \tag{11}$$

Interval [d_2T_s∼d_1T_s]: The equivalent circuit is shown in Fig. 9(b). For SP-Leg, S_2 remains ON and S_1 remains OFF as in the previous interval. For RP-Leg, S_4 is now turned OFF and S_3 is turned ON. L_{1b} and L_{2a} store energy. Circuit equations become

$$\frac{di_{L1b}}{dt} = \frac{v_{\text{in}}}{L_{1a}}, \quad \frac{di_{L2a}}{dt} = \frac{-v_{\text{in}} + v_{C4}}{L_{2a}}. \tag{12}$$

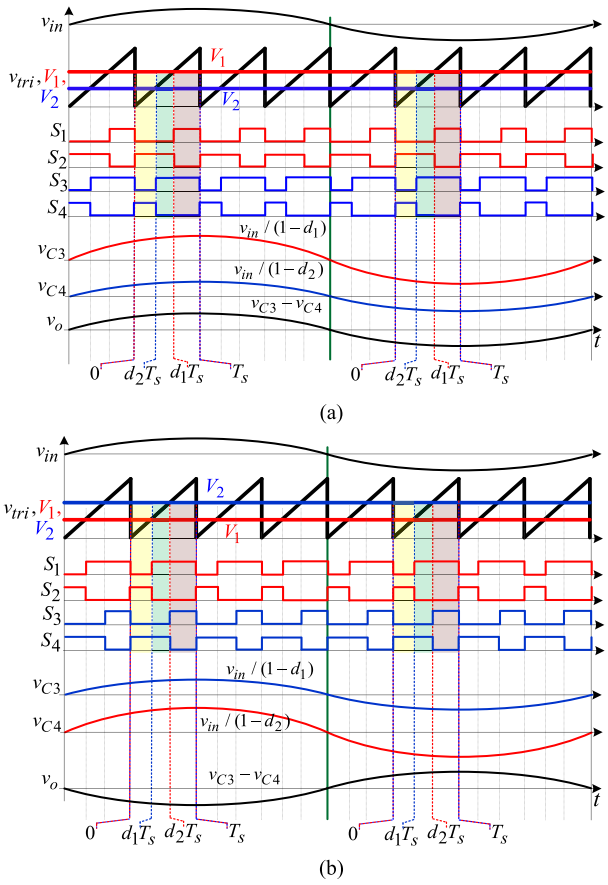

Fig. 8. PWM switching signals for (a) TDRC-NIBB operation and (b) TDRC-IBB operation.

Interval $[d_1T_s \sim T_s]$*:* The equivalent circuit is shown in Fig. 9(c). S_2 is turned OFF and S_1 is turned ON for SP-Leg. RP-Leg retains the switching states of the previous interval. v_{in} and L_{1b} charge capacitor C_3. L_{2a} stores energy. Circuit equations become

$$\frac{di_{L1b}}{dt} = \frac{v_{\text{in}}}{L_{1b}}, \quad \frac{di_{L2a}}{dt} = \frac{-v_{\text{in}} + v_{C4}}{L_{2a}}. \tag{13}$$

2) Inverting Buck–Boost (TDRC-IBB) Operation $(d_1 < d_2)$*:* Switching signals are given in Fig. 8(b). Fig. 9(d)–(f) provides the equivalent circuits.

Interval $[0 \sim d_1T_s]$*:* S_2 and S_4 are ON. S_1 and S_3 are OFF. v_{in} provides energy to L_{2b}. L_{1a} releases energy.

Interval $[d_1T_s \sim d_2T_s]$*:* S_1 and S_4 are ON. S_2 and S_3 are OFF. L_{1a} and L_{2b} both store energy.

Interval $[d_2T_s \sim T_s]$*:* S_1 and S_3 are ON. S_2 and S_4 are OFF. v_{in} and L_{2b} charge C_4. L_{1a} stores energy.

Circuit equations for TDRC-IBB operation are same as (11)–(13) for TDRC-NIBB operation. Only difference is now being that the duration of interval d_2T_s is greater than the interval d_1T_s. Capacitors C_3 and C_4 voltages from (11)–(13) can be obtained as follows:

$$v_{C3} = \frac{v_{\text{in}}}{1-d_1}, \quad v_{C4} = \frac{v_{\text{in}}}{1-d_2}. \tag{14}$$

The output voltage v_o and voltage gain G_{12} are given by

$$v_o = v_{C3} - v_{C4} = \frac{v_{\text{in}}}{1-d_1} - \frac{v_{\text{in}}}{1-d_2} \tag{15}$$

$$G_{12} = \frac{v_o}{v_{\text{in}}} = \frac{1}{1-d_1} - \frac{1}{1-d_2}. \tag{16}$$

From (16), when $d_1 > d_2$, v_{C3} is greater than v_{C4} and voltage gain G_{12} is positive. When $d_1 < d_2$, v_{C3} will be lower than v_{C3} and G_{12} is negative. By putting $d_2 = 0$ in (16), the voltage gain G_{12} for SDRC-NIBB operation is achieved. Similarly, putting $d_1 = 0$, voltage gain G_{12} becomes same as in SDRC-IBB operation. The voltage gain G_{12} for TDRC-NIBB and TDRC-IBB operations is plotted in Fig. 10 for variations in d_1 and d_2. A three-dimensional (3-D) gain plot is obtained, which provides infinite possible values of d_1 and d_2 to achieve a specific voltage gain G_{12}. Gain curve line G_1 on graph is same as for SDRC-NIBB operation, which is special case when $d_2 = 0$. However, gain line G_2 is for SDRC-IBB operation, which is special case when $d_1 = 0$.

III. Component Voltage/Current Stresses and Ripples and Design Discussion

Table I provides the component voltage/stresses and ripples of the proposed converter for all operating modes. In this section, analysis of the component voltage and current stresses and ripples is performed. Also, the guidelines are provided for parameter design/selection of the components.

A. Switch Voltage Stresses

The switch voltage stresses v_S for SDRC-NIBB and SDRC-IBB operations are given by

$$\begin{cases} v_{S1,S2} = v_{\text{in}} + v_o = \left(1 + \frac{1}{G_1}\right) v_o, \text{ NIBB} \\ v_{S3,S4} = v_{\text{in}} = \frac{v_o}{G_1}, \text{ NIBB} \\ v_{S1,S2} = v_{\text{in}} = \frac{v_o}{G_2}, \text{ IBB} \\ v_{S3,S4} = v_{\text{in}} + v_o = \left(1 + \frac{1}{G_2}\right) v_o, \text{ IBB}. \end{cases} \tag{17}$$

From (17), normalized switch voltage stresses v_s/v_o are plotted in Fig. 11(a) for NIBB/IBB operations. As observed, S_1 and S_2 have higher stresses for NIBB operation and S_3 and S_4 have higher (and identical) stresses for IBB operation. The maximum switch voltage stresses occur as the gain reduces to zero (buck operation when v_{in} is minimum). Therefore, switch voltage ratings are decided corresponding to minimum v_{in}.

The switch voltage stresses v_S for TDRC-NIBB and TDRC-IBB operations are given by

$$\begin{cases} v_{S1,S2} = v_{\text{in}} \frac{1}{1-d_2} + v_o = \frac{1+G_1+G_{12}}{G_{12}} v_o, \text{NIBB} \\ v_{S3,S4} = v_{\text{in}} \frac{1}{1-d_2} = \frac{1+G_1}{G_{12}} v_o, \text{NIBB} \\ v_{S1,S2} = v_{\text{in}} \frac{1}{1-d_1} = \frac{1+G_2+G_{12}}{G_{12}} v_o, \text{ IBB} \\ v_{S3,S4} = v_{\text{in}} \frac{1}{1-d_1} + v_o = \frac{1+G_2+G_{12}}{G_{12}} v_o, \text{ IBB}. \end{cases} \tag{18}$$

Switches S_1 and S_2 have higher voltage stresses for noninverting operation. S_3 and S_4 have the same higher voltage stresses for inverting operation. The normalized switch S_1, S_2 voltage stresses (v_s/v_o) for noninverting operation, and S_3, S_4

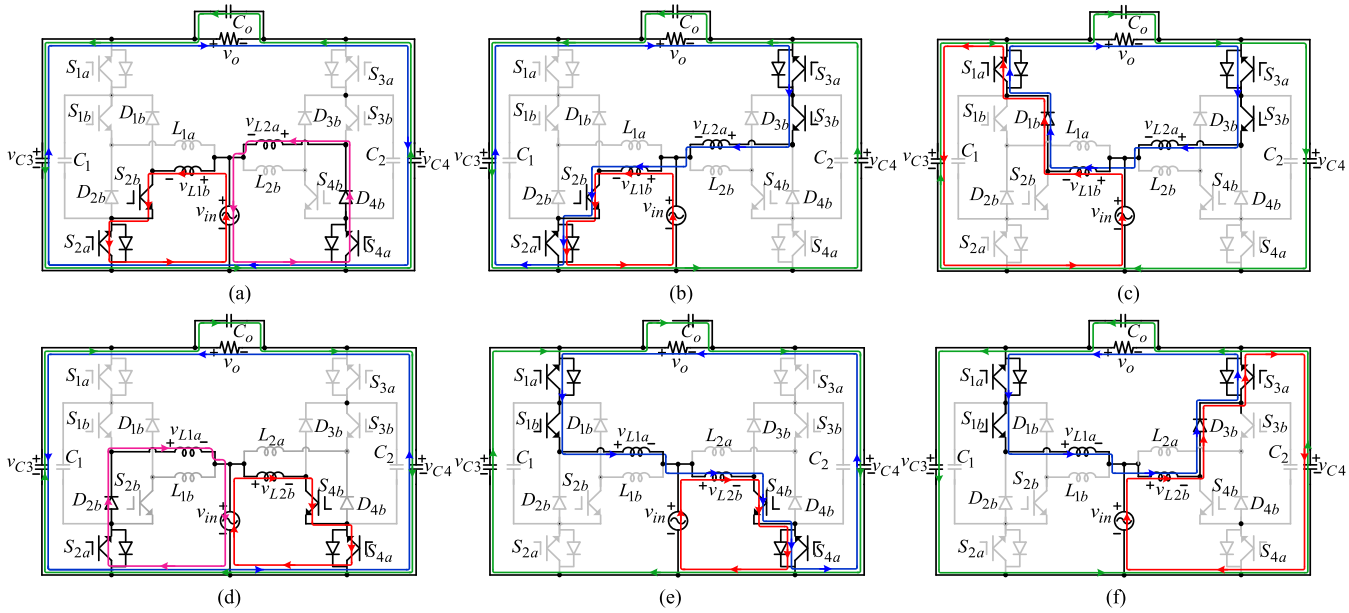

Fig. 9. Equivalent circuits of the proposed converter for TDRC-NIBB and TDRC-IBB operations. (a)–(c) are for TDRC-NIBB operation. (a) $0 \sim d_2\, T_s$. (b) $d_2\, T_s \sim d_1\, T_s$. (c) $d_1\, T_s \sim T_s$. (d)–(f) are for TDRC-IBB operation. (d) $0 \sim d_1\, T_s$. (e) $d_1\, T_s \sim d_2\, T_s$. (f) $d_2\, T_s \sim T_s$.

TABLE I
COMPONENT VOLTAGE/CURRENT STRESSES AND RIPPLES FOR THE PROPOSED CONVERTER

Parameters	Duty ratio D as a function of gain G	Switch voltage and current stresses		Inductor current stresses and ripples		Capacitor voltage stresses and ripples	
		v_s	i_s	i_L	Δi_L	v_C	Δv_C
Noninverting buck–boost operation	$d_1 = \frac{G_1}{1+G_1}$ $G_1 > 0$	$v_{S1,2} = v_{in} + v_o$ $v_{S3,4} = v_{in}$	$i_{S1a,3a,2,4} = i_{in} + i_o$ $i_{S1b,3b} = i_o$	$i_{L1} = i_{in} + i_o$ $i_{L2} = i_o$	$\Delta i_{L1} = \frac{v_o(1-d_1)T_s}{L_1}$ $\Delta i_{L2} = 0$	$v_{C1,3} = v_{in} + v_o$ $v_{C2,4} = v_{in}$	$\Delta v_{C1-C4} = \frac{i_o d_1 T_s}{C_{1-4}}$
Inverting buck–boost operation	$d_2 = \frac{G_2}{1-G_2}$ $G_2 < 0$	$v_{S1,2} = v_{in}$ $v_{S3,4} = v_{in} + v_o$	$i_{S1a,3a,2,4} = i_{in} + i_o$ $i_{S1b,3b} = i_o$	$i_{L1} = i_o$ $i_{L2} = i_{in} + i_o$	$\Delta i_{L1} = 0$ $\Delta i_{L2} = \frac{v_o(1-d_2)T_s}{L_2}$	$v_{C1,3} = v_{in}$ $v_{C2,4} = v_{in} + v_o$	$\Delta v_{C1-C4} = \frac{i_o d_2 T_s}{C_{1-4}}$
Noninverting buck–boost operation	$d_1 = \frac{G_2+G_{12}}{1+G_2+G_{12}}$ $d_2 = \frac{G_1-G_{12}}{1+G_1-G_{12}}$	$v_{S1,2} = \frac{v_{in}}{1-d_b} + v_o$ $v_{S3,4} = \frac{v_{in}}{1-d_b}$	$i_{S1a,3a,2,4} = i_{in} + i_o$ $i_{S1b,3b} = i_o$	$i_{L1} = i_{in} + i_o$ $i_{L2} = i_o$	$\Delta i_{L1} = \frac{v_{in} d_1 T_s}{L_1}$ $\Delta i_{L2} = \frac{v_{in} d_2 T_s}{L_2}$	$v_{C1,3} = \frac{v_{in}}{1-d_2} + v_o$ $v_{C3,4} = \frac{v_{in}}{1-d_2}$	$\Delta v_{C1-C4} = \frac{i_o d_1 T_s}{C_{1-4}}$
Inverting buck–boost operation	$d_a = \frac{G_2+G_{12}}{1+G_2+G_{12}}$ $d_b = \frac{G_1-G_{12}}{1+G_1-G_{12}}$	$v_{S1,2} = \frac{v_{in}}{1-d_b}$ $v_{S3,4} = \frac{v_{in}}{1-d_b} + v_o$	$i_{S1a,3a,2,4} = i_{in} + i_o$ $i_{S1b,3b} = i_o$	$i_{L1} = i_o$ $i_{L2} = i_{in} + i_o$	$\Delta i_{L1} = \frac{v_{in} d_1 T_s}{L_1}$ $\Delta i_{L2} = \frac{v_{in} d_2 T_s}{L_2}$	$v_{C1,3} = \frac{v_{in}}{1-d_1}$ $v_{C2,4} = \frac{v_{in}}{1-d_1} + v_o$	$\Delta v_{C1-C4} = \frac{i_o d_2 T_s}{C_{1-4}}$

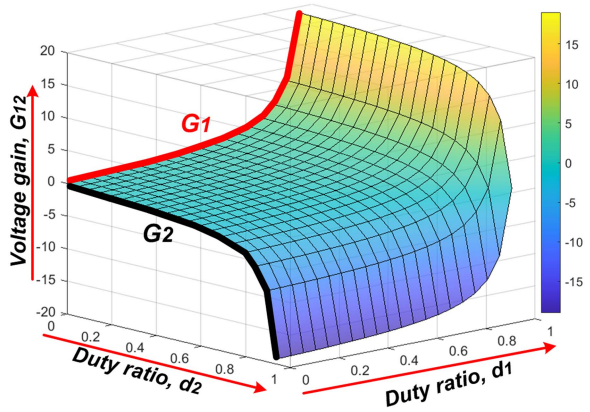

Fig. 10. Voltage gains versus duty ratios for TDRC-NIBB/IBB operations.

voltage stresses for inverting operation are plotted in Fig. 12 in terms of voltage gains G_{12} and G_1 or G_2. From the resultant 3-D graph, switch voltage stresses for the same gain G_{12} increase as the G_1 or G_2 increases. The maximum stresses occur for minimum gain G_{12} when input voltage v_{in} is maximum.

B. Switch Current Stresses

The switch current stresses i_S for noninverting and inverting operations are given by

$$\begin{cases} i_{S1a,S3a,S2,S4} = i_{\text{in}} + i_o = (1 + G_{1,2})\, i_o \\ i_{S1b,S3b} = i_o. \end{cases} \tag{19}$$

From (19), normalized switch current stresses i_s/i_o are plotted in Fig. 11(b). As observed, the current stresses of switches S_{1a}, S_{3a}, S_2, and S_4 increase with voltage gain $G_{1,2}$.

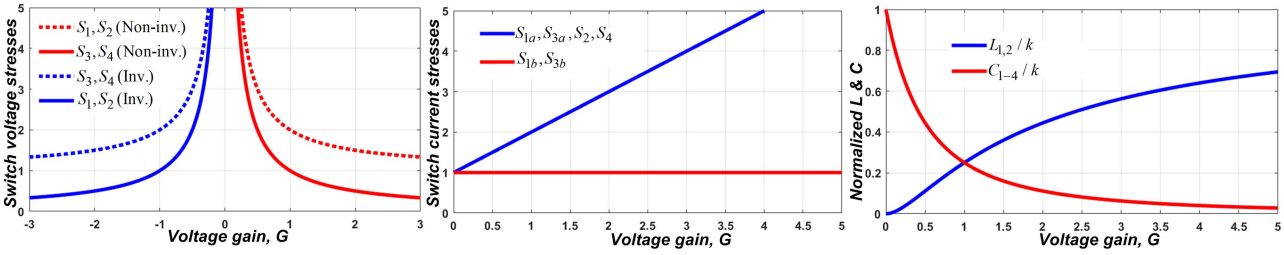

Fig. 11. Component voltage and current stress and passive component requirements. (a) Switch voltage stresses. (b) Switch current stresses. (c) Inductance and capacitance requirement.

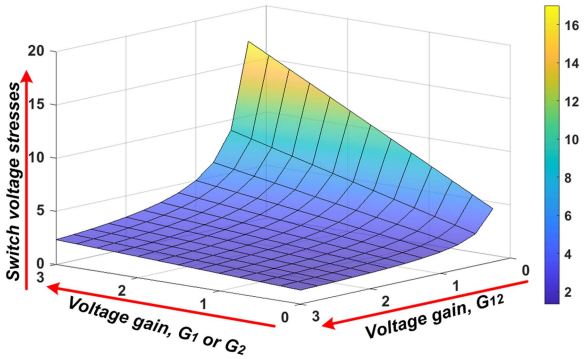

Fig. 12. Switch voltage stresses for TDRC-NIBB/IBB operation.

Maximum current stresses occur for maximum gain $G_{1,2}$ (when v_{in} is minimum) and switch current ratings can be determined accordingly. The current stresses of switches S_{1b} and S_{3b} are independent of voltage gain $G_{1,2}$ and decided by the load current i_o.

C. Inductor Design

Inductors are designed based on their maximum current stresses i_L(without getting the core into saturation) and allowable current ripple Δi_L. Inductors L_1 and L_2 have a current stress of $(1+G_{1,2})i_o$ (as plotted in Fig. 11(b) for switches S_{1a}, S_{3a}, S_2, and S_4), which is highest for the maximum value of gain G.

The values of inductors L_1 and L_2 to limit the maximum current ripple to $\Delta\, i_L = x \cdot i_L$, where $x = (10-30)\%$, can be found as follows:

$$L_{1,2} = \frac{v_o\,(1-d_{1,2})\,T_s}{x \cdot i_L} \tag{20}$$

where $d_{1,2} = G_{1,2}\,/(1+G_{1,2})$ and $i_L = (1+G_{1,2})\,i_o$. Therefore, (20) becomes

$$L_{1,2} = \frac{v_o T_s}{x \cdot i_o} \cdot \frac{1}{(1+G_{1,2})^2} = \frac{k}{(1+G_{1,2})^2}. \tag{21}$$

In (21), the term $v_o T_s/x i_o$ is constant and represented by k. From (21), the required normalized inductance values $L_{1,2}/k$ are plotted in Fig. 11(c). The required inductance $L_{1,2}$ increases with decrease in gain $G_{1,2}$. $L_{1,2}$ is determined for minimum gain (maximum v_{in}).

D. Capacitors $C_1 - C_4$

Capacitors $C_1 - C_4$ are selected based on their maximum voltage stresses v_C and to maintain the voltage ripple Δv_C within the desired limits. The capacitors have voltage stresses of $(1+G_{1,2})/G_{1,2}\ v_o$ (as plotted in Fig. 11(a) for switches S_1 and S_2 for noninverting operation), which are highest for minimum gain G.

The values of capacitors $C_1 - C_4$ are selected to restrict the maximum voltage ripple to $\Delta\ v_C = \ y \cdot v_C$, where v_C is the maximum capacitor voltage stress, and $y\ = (5-10)\%$. To maintain the Δv_C within the desired limits, minimum required capacitor $C_1 - C_4$ values can be determined as follows:

$$C_{1-4} = \frac{i_o d_{1,2} T_s}{y \cdot v_C}. \tag{22}$$

Putting $d_{1,2} = G_{1,2}\ /(1+G_{1,2})$ and $v_C = (1+G_{1,2})/G_{1,2}\ v_o$ in (22), we obtain

$$C_{1-4} = \frac{i_o T_s}{y \cdot v_C}\ \frac{G_{1,2}^2}{(1+G_{1,2})^2} = k \cdot \frac{G_{1,2}^2}{(1+G_{1,2})^2}. \tag{23}$$

From (23), the required capacitance values C_{1-4}/k (normalized with respect to k) are plotted in Fig. 11(c) against variations in $G_{1,2}$. The required capacitance value increases with gain. Therefore, capacitors are selected for large value of $G_{1,2}$.

IV. Comparison With the Existing Bipolar AC–AC Converters

Table II provides a comparison of the key features, operating conditions, and measured efficiency of the proposed and state-of-the-art bipolar ac–ac converters [15], [18], [25], [26], [27]. The impedance-source (Z-source) converter in [15] is widely known as bipolar buck–boost ac–ac converter with few switching devices. However, it uses various passive components and does not provide noninverting step-down voltage. Unified bipolar buck–boost ac–ac converter [18] can reduce the number of passive components. However, it cannot operate as noninverting boost converter and provides discontinuous input/output currents. These bipolar buck–boost ac–ac converters are also susceptible to commutation issue as switch dead and overlap times would result in their inductor open circuit or voltage-source short circuit.

TABLE II
COMPARISON OF SALIENT FEATURES OF THE PROPOSED AND CONVENTIONAL SC BIPOLAR AC–AC CONVERTERS

Parameters	Z-source bipolar buck–boost ac–ac [15]	Unified inv./noninv. converter [18]	SC inv./noninv. converter [25]	SC inv./noninv. converter [26]	Bipolar SC converter [27]	Proposed bipolar SC converter
Buck-boost voltage gain	$\frac{1-d}{1-2d}$	$\frac{d_1-d_3}{1-d_3}$	$\frac{d}{1-d}, \frac{2d-1}{d}$	$d, \frac{1}{1-d}, -\frac{d}{1-d}$,	$d_1 - d_2$ (Only buck)	$\frac{1}{1-d_1} - \frac{1}{1-d_2}$
No. of switching devices	Four switches	Eight switches, eight diodes	Eight switches, Eight diodes	Six switches, six diodes	Eight switches, four diodes	Eight switches, four diodes
No. of passive components	Three inductors, four capacitors	Four inductors, four capacitors	Four inductors, four capacitors	Five inductors, two capacitors	Four inductors, four capacitors	Four inductors, four capacitors
Continuity of input current	Discontinuous	Discontinuous	Discontinuous	Continuous	Discontinuous	Continuous
Need input LC filter	No	Yes	Yes	No	Yes	No
Bipolar operation	Yes	Yes	Yes	Yes	Yes	Yes
Buck–boost operation	Yes	Yes	Yes	Yes	No	Yes
Identical/symmetric bipolar buck–boost process	No	No	No	No	No	Yes
Control degree of freedom	One (d)	One (d)	One (d)	One (d)	Two (d_1 and d_2)	Two (d_1 and d_2)
Commutation issue	Yes	Yes	No	No	No	No commutation issue
Control complexity	High	High	High	High	Low	Low
Switching type	Hard switching	Hard switching	Hard switching	Hard switching	Hard switching	Hard switching
Operating conditions and peak efficiency η for bipolar buck–boost operation	$f_{sw} = 20\,kHz$ $P_o = 650\,W$ $V_{in} = 86\,V_{rms}$ $V_o = 114\,V_{rms}$ $\eta = 86.6\,\%$	$f_{sw} = 25\,kHz$ $P_o = 260\,W$ $V_{in} = 106\,V_{rms}$ $V_o = 84\sim106\,V_{rms}$ $\eta = 94.1\,\%$	$f_{sw} = 30\,kHz$ $P_o = 400\,W$ $V_{in} = 78\sim141\,V_{rms}$ $V_o = 110\,V_{rms}$ $\eta = 94$	$f_{sw} = 30\,kHz$ $P_o = 400\,W$ $V_{in} = 70\sim150\,V_{rms}$ $V_o = 110\,V_{rms}$ $\eta = 94.2\,\%$	$f_{sw} = 18\,kHz$ $P_o = 400\,W$ $V_{in} = 141\,V_{rms}$ (buck) $V_o = 98\,V_{rms}$ $\eta = 95\,\%$	$f_{sw} = 30\,kHz$ $P_o = 400\,W$ $V_{in} = 70\sim150\,V_{rms}$ $V_o = 110\,V_{rms}$ $\eta = 95.1\,\%$

The SC bipolar buck–boost ac–ac converters in [25] and [26] can provide protection from commutation issue. However, they require dedicated external diodes corresponding to each active switch, increasing their semiconductor devices requirement. Moreover, the former provides discontinuous input/output currents with no provision of noninverting boost operation, and the latter needs five inductors. More importantly, these SC bipolar ac–ac converters have asymmetric circuit topologies with nonidentical noninverting and inverting buck–boost operations. Therefore, the noninverting and inverting operations of these converters have different switch modulation strategies, different circuit operations, different component voltage and current stresses and ripples, different switching devices rating and losses, different value requirement of inductor and capacitors, and different control. This would create challenges in optimizing the circuit parameters, losses, efficiency, and control for both noninverting and inverting operations. For instance, the component selected for worst-case conditions in one polarity operation would be underutilized in the opposite polarity operation.

The nondifferential SC ac chopper-based bipolar buck converter in [27] and proposed buck–boost converter can reduce the requirement of external diodes to only half of the active switches. Moreover, these converters have symmetric circuit topologies with identical noninverting and inverting operations that simplify the PWM switching strategies, circuit operations, component design optimization and selection, circuit losses, and control. In addition, the identical bipolar operations are same as in single-phase matrix converters [29], [30], which are capable of producing step-changed output frequency, enabling these converters for various new applications (high-gain ac–dc rectifier with low output ripple [29], traction converter [30], etc.) that are not supported by SC bipolar buck–boost ac–ac converters in [25] and [26]. In comparison to counterpart nondifferential ac choppers based converter in [27] with only step-down bipolar operation, the proposed converter can provide both step-up and step-down bipolar voltages while using the same number of circuit components as in [27]. Moreover, converter in [27] has discontinuous input current (and related issues of increased devices current stresses, current ratings, power losses, and poor input power quality) and requires an external input *LC* filter.

The proposed converter can provide continuous input current without needing an external *LC* filter. To summarize it, the main standout characteristics of the proposed converter is that it can provide identical noninverting and inverting output voltages with step-up and step-down voltage gains, a feature not exhibited by the existing SC bipolar ac–ac converters.

V. EXPERIMENTAL RESULTS

A hardware prototype is developed and the experiments are performed based on the component specifications and operating conditions given in Table III. The PWM switching signals are implemented using a TMS320F28335 DSP microcontroller kit. To implement the closed-loop control for voltage sag and swell

TABLE III
EXPERIMENTAL SPECIFICATIONS

Input voltage range ($v_{in,min} \sim v_{in,max}$)	100 V_{peak}~ 200 V_{peak}
Output voltage v_o	155.5 V_{peak}
Rated output power (P_o)	400 VA
Load (RL)	30 Ω + 10 mH
PWM frequency (f_s)	30 kHz
Capacitors ($C_1 - C_4, C_{in}, C_o$)	3 μF, 3 μF, 3 μF
Inductors ($L_{1a,1b}, L_{2a,2b}$)	(1 mH, 1 mH)
Diodes ($D_{1b} - D_{4b}$)	RHRG3060
IGBTs ($S_1 - S_4$)	FGH40N60SFDTU

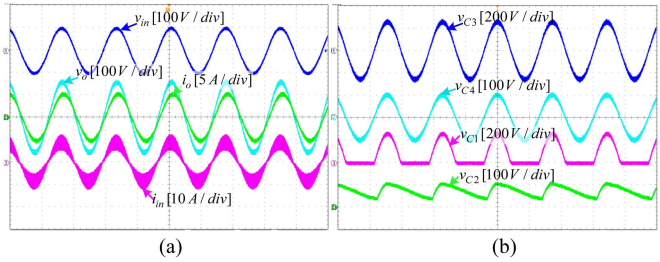

Fig. 13. Experimental results for noninverting boost operation. (a) Input/output voltages/currents. (b) Capacitor voltages.

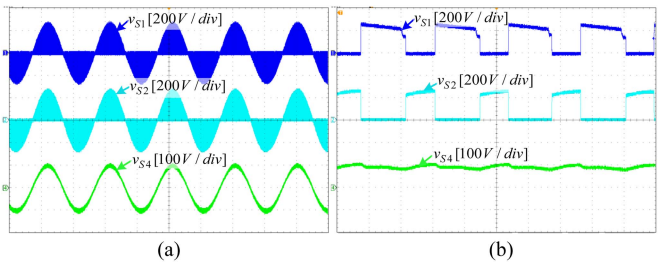

Fig. 14. (a) Switch voltage stresses for noninverting boost operation. (b) Enlarged waveforms of (a).

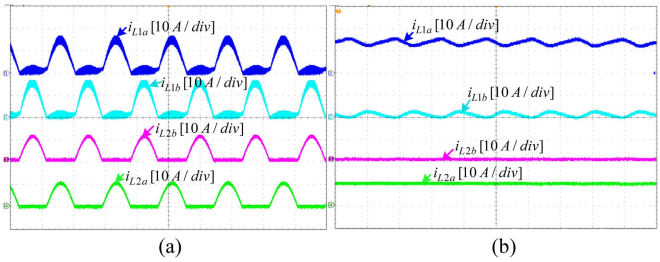

Fig. 15. (a) Inductor currents for noninverting boost operation with a small overlap time. (b) Enlarged waveforms of (a).

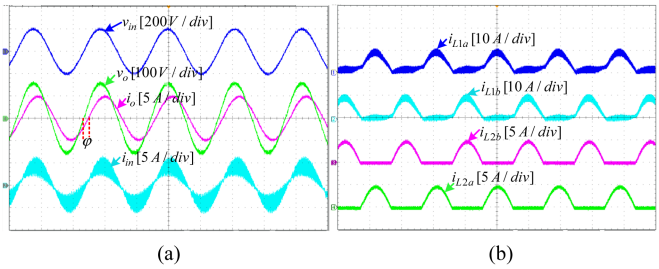

Fig. 16. Experimental results for noninverting buck operation with partial inductive load. (a) Input and output voltages/currents. (b) Inductor currents.

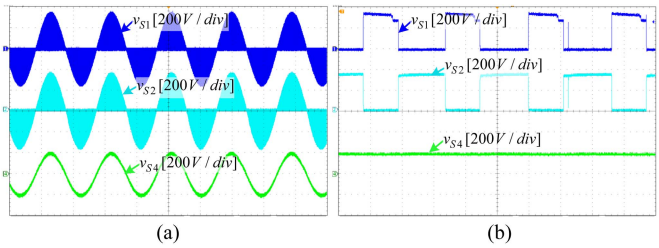

Fig. 17. (a) Switch voltage stresses for noninverting buck operation. (b) Enlarged waveforms of (a).

compensation in application of the proposed converter as DVR, a voltage transducer of model number LV25-P is connected across load and the sensed signal is sent to DSP kit through built-in 12 bit analog-to-digital converter. The peak value of this sensed load voltage v_l is determined based on the formula given in [31]. This peak load voltage v_l value is compared with predefined reference value $V_{l,\text{ref}}$ to generate the error signal *e(t)*. This error signal is used to generate the dynamically adjustable control reference signals V_1 and V_2 through a PI controller to generate the PWM control signals.

Figs. 13–15 show the experimental results for noninverting boost operation to produce output voltage v_o of 155.5 V_{peak} from input voltage v_{in} of 100 V_{peak}. The switch duty ratio d_1 is adjusted to 0.62 to provide a gain G_1 of 1.55. Fig. 13(a) shows the waveforms of input voltage v_{in} , input current i_{in}, output voltage v_o, and output current i_o. Fig. 13(b) shows the capacitor $C_1 - C_4$ voltage stresses. Capacitors C_1 and C_3 voltages peak at around 255.5 V, and capacitors C_2 and C_4 have peak voltage stresses of around 100 V. Fig. 14(a) shows the switches S_1, S_2, and S_4 voltage stresses. Fig. 14(b) shows the enlarged waveforms of Fig. 14(a). Fig. 15 shows the current waveforms of inductors L_{1a} and L_{1b} for a small switch overlap time of 0.2 μS between switches S_{1b} and S_{2b}. As observed, there are no overshoots in inductors L_{1a} and L_{1b} currents, which are the same as switches S_{1b} and S_{2b} shoot-through currents [in Fig. 4(a)], validating that the proposed converter has no shoot-through issue.

Figs. 16 and 17 show the experimental results for noninverting buck operation ($v_{in} = 200\ V_{peak}$ and $v_o = 155.5\ V_{peak}$) with a partial inductive load *RL* of 30 Ω + 40 mH. Switch control duty ratio is 0.42 and voltage gain is 0.73. Fig. 16(a) shows the waveforms of v_{in}, i_{in}, v_o, and i_o. As observed, the output current lags the output voltage by an angle φ. Fig. 16(b) shows the inductors L_1 and L_2 current. Fig. 17(a) and (b) shows the line-frequency and high-frequency measured waveforms of switch S_1, S_2, and S_4 voltage stresses, respectively. Figs. 18 and 19 show the experimental results for inverting boost operation ($v_{in} = 100\ V_{peak}$ and $v_o = 155.5\ V_{peak}$) with a partial inductive load *RL* of 30 Ω + 40 mH. The same duty ratio d_2 of 0.62 is selected to provide the required voltage gain (G_2= 1.55) as in noninverting operation. Fig. 18(a) shows the measured waveforms of v_{in},

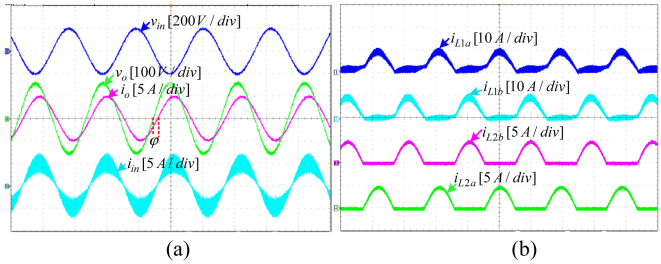

Fig. 18. Experimental results for inverting boost operation with partial inductive load. (a) Input and output voltages/currents. (b) Inductor currents.

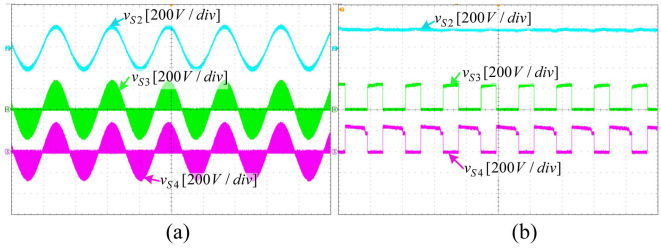

Fig. 19. (a) Switch voltage stresses for inverting boost operation. (b) Enlarged waveforms of (a).

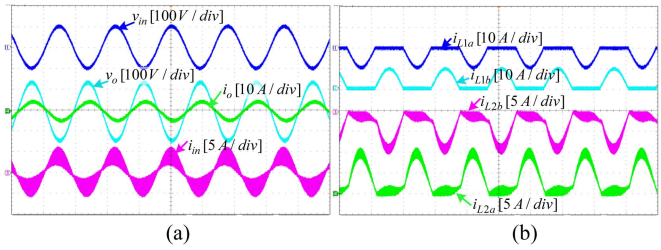

Fig. 20. Experimental results for inverting buck operation. (a) Input and output voltages/currents. (b) Inductor currents.

i_{in}, v_o, and i_o. Fig. 18(b) shows the measured waveforms of inductors L_1 and L_2 currents. L_2 acts as energy storing and filtering inductor and L_1 freewheels the load currents. Fig. 19 shows the measured waveforms of switches S_2, S_3, and S_4 voltage stress. Switch S_2 now withstands a peak voltage stress of 100 V ($= v_{\text{in}}$) and switches S_3 and S_4 block peak voltage of 255.5 V. Fig. 20 shows the measured waveforms of inverting buck operation when $v_{\text{in}} = 200\,\text{V}_{\text{peak}}$ and $v_o = 155.5\,\text{V}_{\text{peak}}$. Fig. 20(a) shows the experimental results of v_{in}, i_{in}, v_o, and i_o. Fig. 20(b) shows the waveforms of inductors L_1 and L_2 currents.

Fig. 21 shows the configuration of the proposed DVR. Fig. 22 shows the dynamic response of the proposed ac–ac converter-based DVR against grid voltage sags and swells under closed-loop control. Fig. 22(a) shows the measured waveforms of input line voltage v_{in}, load voltage v_l, series injected converter voltage v_{conv}, and control duty ratio D for voltage sag condition when v_{in} is decreased from optimal value of $110\,\text{V}_{\text{rms}}$ to $65\,\text{V}_{\text{rms}}$. The

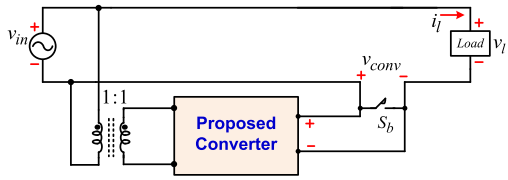

Fig. 21. Configuration of the proposed DVR.

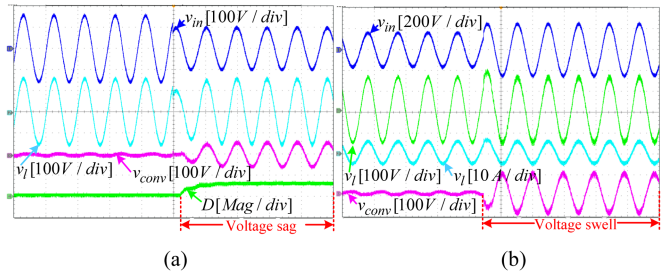

Fig. 22. Measured waveforms of dynamic response of the proposed ac–ac converter-based DVR. (a) Voltage sag mitigation. (b) Voltage swell mitigation.

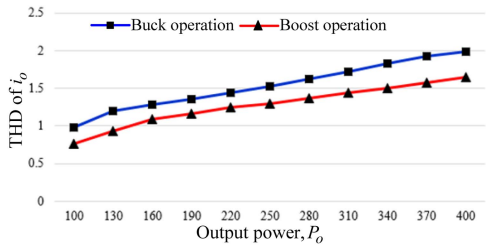

Fig. 23. THD of output current versus output power.

proposed converter operates with noninverting buck–boost operation and injects the desired value of positive series voltage v_{conv} (through dynamically controlled duty ratio D) and load voltage v_l is regulated. Fig. 22(b) shows the measured waveforms of v_{in}, v_l, v_{conv}, and load current i_l for voltage swell occurrence when v_{in} is increased to $150\,\text{V}_{\text{rms}}$. The proposed inverting buck–boost function is now activated, generating negative series voltage ($-v_{\text{conv}}$) and load voltage v_l is again regulated to its nominal value.

Fig. 23 shows the measured total harmonic distortion THD of output current i_o of the proposed converter for buck ($v_{\text{in}} = 150\,\text{V}_{\text{rms}}$) and boost ($v_{\text{in}} = 70\,\text{V}_{\text{rms}}$) operations for varying values of load power P_o. As observed, the THD of output current i_o is higher for boost operation for the same value of output power. This is due to the large current flowing through passive components, increasing their ripple components. Moreover, for both buck and boost operations, the output current THD increases with output power, again due to the higher circuit currents. Overall, the measured THD values are below 2% for the entire operation range. Fig. 24 shows the practical power conversion efficiency of the proposed converter for a wide variation in input voltage. The practical results completely back up the theoretical analysis.

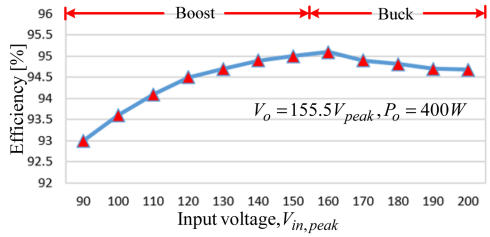

Fig. 24. Measured efficiency of the proposed converter.

VI. Conclusion

A novel bipolar-type buck–boost ac–ac converter is proposed based on the partial dual-buck structured nondifferential ac choppers. The proposed converter is able to produce identical noninverting and inverting operations with single duty ratio control and simplified operations. It is also able to produce same operations with two duty ratio controls, giving more degree of freedom to adjust the voltage gain. The proposed converter is resistant to short circuit of voltage source and interruption of inductor current for switch overlap and dead-time, respectively, solving the commutation issue without using the PWM deadtimes and snubber circuit or control burden. It also provides low ripple (continuous) input current and supports the inductive loads. The proposed converter is a potential candidate for application as DVR with its bipolar buck–boost operations providing a wide range mitigation of both grid voltage sag and swell. A comprehensive analysis of the proposed converter is provided and backed up by the experimental results.

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