Influence of the Uneven Temperature Distribution on the Electrode Warpage of PP IGBTs

Yiming Zhang, Erping Deng, Jiaqi Guo, Zhibin Zhao, Yan Zhong, Lei Zhang, Xinling Tang, and Xiang Cui

***Abstract*—The pressure and junction temperature distribution within press-pack insulated gated bipolar transistors had been proven uneven due to the thermomechanical coupling effect caused by electrode warpage. However, the root reason for the electrode warpage remains unclear, and therefore leads to confusion in optimization. In this article, the influence of vertical and lateral temperature difference on the electrode warpage is first separated and analyzed through the proper combination of boundary conditions in finite element simulation. The lateral temperature difference is found to be the main reason for the electrode warpage, which is different from the perception state of the art and provides the possibility to suppress the electrode warpage directly. Furthermore, the role of the lateral temperature difference is analyzed by a simplified model and it is found that the lateral temperature difference could be decreased by only pure thermal design rather than thermomechanical design. The electrode size and pedestal layout are discussed to alleviate the lateral temperature difference of the electrode and the simulation results also show great improvement in pressure and junction temperature distribution. Finally, the junction temperature distribution is measured by the sequential $V_{CE}(T)$ method to verify the root reason and also the effectiveness of the improvement.**

***Index Terms*—Electrode warpage, influence factors, lateral temperature difference, press pack IGBTs, thermomechanical coupling.**

I. Introduction

PRESS pack insulated gate bipolar transistors (PP IGBTs) have been applied to high voltage and high-power applications such as high voltage direct current (HVDC) successfully [1], [2], for their advantages of high-power density, easy series connection, and failure short-circuit mode [3], [4], [5], [6]. Multiple chips are parallel connected within PP IGBTs to obtain a higher current rating, as shown in Fig. 1 [7]. The uniform distribution of pressure, temperature and current among parallelled chips is important, but difficult to realize on account of the multiphysics coupling effect. On the one hand, the pressure distribution could be significantly changed due to the thermal expansion and is very different from the even pressure distribution designed without heating [8], [9]. On the other hand, the junction temperature and current distribution in PP IGBTs are also worsened in turn as the result of the uneven pressure distribution because the thermal and electrical connection is ensured by direct contact without soldering [9], which is different from the bond wire power modules. Hence, partial chips could suffer a higher temperature or larger pressure and cause damage or reliability problems [10]. It is a crucial task to realize the even distribution of the pressure, temperature, and current.

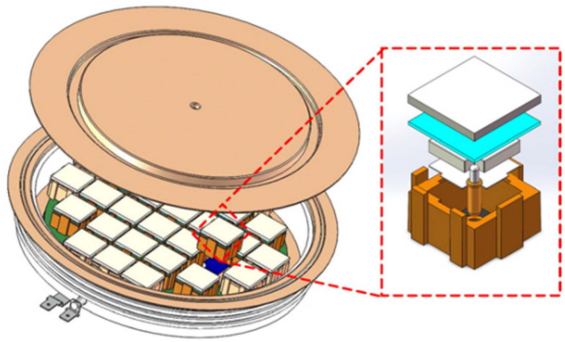

Fig. 1. Structure diagram of a PP IGBTs from [8].

Some research has been carried out from different perspectives to understand the multiphysics behavior within PP IGBTs. Some decoupled model has been proposed firstly to investigate the distribution characteristics [11], [12], [13]. In 2012 and 2013, Poller et al. [14], [15] developed a fully coupled model to obtain the pressure, temperature, and current distribution within PP IGBTs. It is revealed that the central chips suffer higher pressure than the edge chips during the heating phase. The electrode warpage induced by thermal expansion (thermomechanical coupling effect) was first proposed to explain the uneven distribution. In 2013, Deng et al. [16] established a more refined multiphysics model and Deng et al. [17] improve the model accuracy, by measuring the coupling relationships such as thermal contact resistance and thermal electrical resistance. In 2019, Lai et al. [18] proposed a structure containing two parallel single-chip devices which are mechanically

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decoupled but thermally and electrically coupled. The current and junction temperature distribution characteristics under uneven clamping force are measured and the electro-thermal part of the multi-physics model is verified. Furthermore, the influence of thermomechanical coupling is verified through the junction temperature measurement by Zhang et al. [19] and the thermal resistance measurement by Chen et al. [20]. Experimental results confirm that the thermomechanical coupling is intensified with the increase of flowing current. In 2022, Cao et al. [21], [22] also point out that the uneven distribution could worsen with the increase of roughness caused by the fretting wear.

Based on the above perception, certain approaches were proposed to decrease the effect of the electrode warpage and also the thermomechanical coupling. One approach is to reduce the thermal contact resistance directly through the nanosilver paste sintering technology [23] or liquid metal thermal interface material [24]. With this approach, the junction temperature distribution could be improved but not the pressure distribution because the warpage still exists. Another approach is to suppress the electrode warpage through some structural design. In 2021, Dai et al. [25] considered the series-connection stack application and analyzed the influence of the clamping area on the electrode warpage. A stamp with a larger clamping area was advised to compensate for the electrode warpage due to the thermal expansion and realize even pressure distribution. In 2021, Chang et al. [26] utilize the elastic half-space theory to describe the uneven pressure distribution and Chang et al. [27], [28] proposed a distributed press-pack packaging technology to improve the pressure distribution uniformity. Nevertheless, these approaches are indirect and may face other limits.

Overall, the electrode warpage is proposed as a limitation of device rating, and some indirect suppression approaches are proposed. However, it is only known that the electrode warpage could be more severe as heating power increases, but without a clear explanation of the intrinsic mechanism. This leads to confusion about whether there is a direct approach to eliminate the electrode warpage from its beginning. Hence, this article is a good supplement to existing work by finding out that the lateral temperature difference is the dominant factor and establishing the relationship between warpage and lateral temperature difference, which also exhibits the possibility of eliminating the warpage directly.

The rest of this article is organized as follows. The thermomechanical coupling finite element model is established and the pressure and temperature distribution under different heating power is obtained in Section II. Then, the lateral temperature distribution on the electrode is proposed and the influence of uneven electrode temperature distribution on the electrode warpage is investigated in Section III. A simplified model is established to illustrate the role of electrode lateral temperature difference in the PP IGBTs. Some approaches are proposed to improve pressure and temperature uniformity accordingly. In Section IV, two layouts are compared experimentally through the junction temperature distribution measurement by the sequential $V_{CE}(T)$ method to verify the analysis above. Finally, Section V concludes this article.

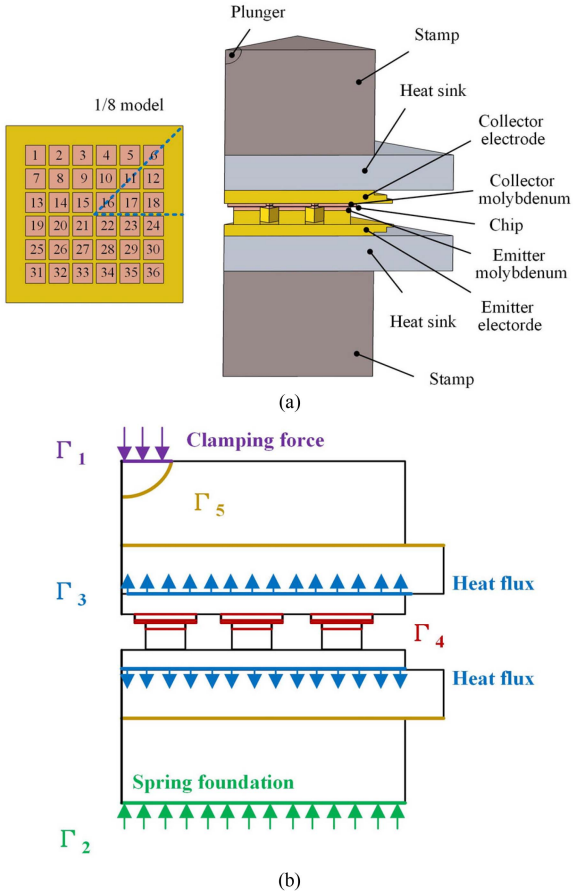

Fig. 2. Finite-element model and boundary conditions. (a) Geometry structure of finite element model. (b) Boundary conditions.

II. Thermomechanical Coupling Effect

A. Finite-Element Model

The existing finite element model considering multiphysics coupling for PP IGBTs is gradually maturing and being used to explore its physics behavior [15], [16], [17]. However, there are still a lot of details about the model and boundary conditions that should be careful, such as the contact boundary for interfaces significantly affecting the pressure distribution within PP IGBTs. A finite element model is established in this section to reproduce the thermomechanical coupling effect and investigate the root reason for the electrode warpage within PP IGBTs. A device with a rectangular electrode is chosen for the convenience of the grouped layouts, which will be illustrated in Section III. It should be pointed out that the tendency of pressure and junction temperature distribution under electrodes with a different geometry is the same and the root reason for thermomechanical coupling is also not affected. The heat sink and clamping fixtures such as the plunger and stamp are considered to ensure accuracy. Only 1/8 of the model is calculated for the reduction of the calculated amount utilizing the symmetry of the structure. The simulation model and boundary conditions are summarized in Fig. 2. The influence of the silver layer on the pressure distribution is limited [29] and therefore removed to avoid small faces in the meshing process.

The current field is not included here for simplification because the electro-thermal coupling is relatively weak compared to thermomechanical coupling [16] and only the latter is the main concern in this article.

For the elastic stress field, the governing equation and the boundary conditions [30] considering thermal coupling could be summarized as

$$(\lambda+\mu)\nabla(\nabla\cdot\boldsymbol{u})+\mu\nabla^2\boldsymbol{u}+\boldsymbol{f}-\beta\nabla T=0 \tag{1}$$

$$t_N=f_N, \qquad \forall \boldsymbol{x}\in\Gamma_1 \tag{2}$$

$$t_N=-k(u-u_0), \qquad \forall \boldsymbol{x}\in\Gamma_2 \tag{3}$$

$$\begin{cases} d_N^{(i)}\geq 0, t_N^{(i)}\leq 0, d_N^{(i)}\cdot t_N^{(i)}=0 \\ \Phi^{(i)}=\left\|t_T^{(i)}\right\|-\mu\left\|t_N^{(i)}\right\|\leq 0 \\ v_T^{(i)}+\xi^{(i)}t_T^{(i)}=0, \xi^{(i)}\geq 0 \\ \Phi^{(i)}\cdot\xi^{(i)}=0 \end{cases} \quad \forall \boldsymbol{x}\in\Gamma_3\cup\Gamma_4\cup\Gamma_5 \tag{4}$$

where $\boldsymbol{u}$ is the displacement vector, $\boldsymbol{f}$ is the volume force, λ and μ are the Lame constants, and β is the thermal stress coefficient, f_N and k are applied force and the spring constant. t_N and t_T are the normal and tangential traction force, d_N and v_T are the contact gap and slip velocity. The superscript $i=1,2$ denotes the different boundaries. Φ is the slip function and ξ is the friction multiplier. Γ_1 to Γ_5 denote different boundaries.

A total clamping force of 45 kN (36 chips paralleled) is applied on the plunger surface Γ_1. The spring foundation of 5×10^6 N/m is set on the bottom of the stamp Γ_2 to simulate the disc spring, which is corresponding to spring travel of 9 mm at 45 kN). All of the contact boundaries (Γ_3, Γ_4, and Γ_5) are described as friction contact. The frictional coefficient of the surface between the chip and molybdenum is set as 0.2 and the frictional coefficient of the surface between molybdenum and copper is given as 0.5 [9]. The frictional coefficient among copper and aluminum is supposed to be 0.3 considering the coating process of the heat sink. The temperature of the heat sink and clamping fixture is supposed as 20 °C with an extra cooling system.

For the thermal field, the governing equation and the boundary conditions [31] are given as

$$-\nabla\cdot(k\nabla T)-\Phi=0 \tag{5}$$

$$q_N=h(T-T_a), \qquad \forall \boldsymbol{x}\in\Gamma_3 \tag{6}$$

$$T_2-T_1=h_{\mathrm{th,c}}(t_N)\cdot q_N^{(i)}, q_N^{(1)}=q_N^{(2)} \ \forall \boldsymbol{x}\in\Gamma_4 \tag{7}$$

where k is the thermal conductivity, and Φ is the body heat source. q_{N} is the normal heat flux. h and T_{a} are the heat transfer coefficient and the water temperature. $h_{\mathrm{th,c}}(F)$ is the relationship between the thermal contact conductance and pressure. The superscript $i=1,2$ denotes the different boundaries. Γ_1 to Γ_5 denote different boundaries.

All IGBT chips are set as the body heat source in the active area and different power density is applied to investigate the thermomechanical coupling effect. The heat sink is simulated as the convective heat transfer boundary condition applied on the device surface Γ_3. The equivalent convective heat transfer coefficient h is 5000 W/(m$^2\cdot$K) [32] and the ambient temperature

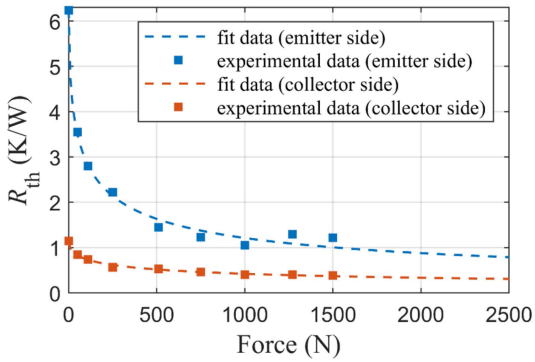

Fig. 3. Relationship between thermal resistance and clamping force of a single IGBT chip submodule.

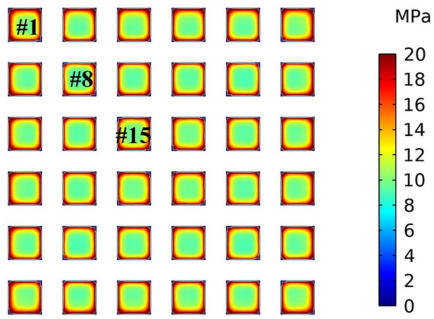

Fig. 4. Pressure distribution within PP IGBTs(zero heating power, room temperature).

T_{a} is 20 °C. The heat transfer behavior at the contact surface Γ_4 within the device is described as thermal contact resistance for the connection between the thermal and mechanical fields. The relationship between the junction to water thermal resistance and the clamping force is measured and fitted through a single chip module similarly to [17] as shown in Fig. 3. Then, the relationship between the thermal contact resistance and the clamping force is obtained and transferred to the relationship between the thermal contact conductance and the pressure. After that, position-dependent thermal contact conductance is applied on each chip to simulate a more realistic temperature distribution.

B. Unbalanced Pressure and Junction Temperature Distribution With Heating Power

The pressure and junction temperature distribution under different heating power is obtained by the finite-element model established. The pressure distribution with no heating power at room temperature is given in Fig. 4. Simulation results indicate that the pressure distribution is relatively uniform without heating power. The force on the edge chips is slightly larger than that of the center chips. The reason for the force deviation is the electrode warpage [29] because of the area discrepancy between the face of force applied and the face that bears force. The pressure and temperature distribution under the heating power of 175 W per IGBT chip are given in Fig. 5. Simulation results indicate that the central chips suffer higher mechanical stress and lower temperature, but the edge chips suffer lower mechanical

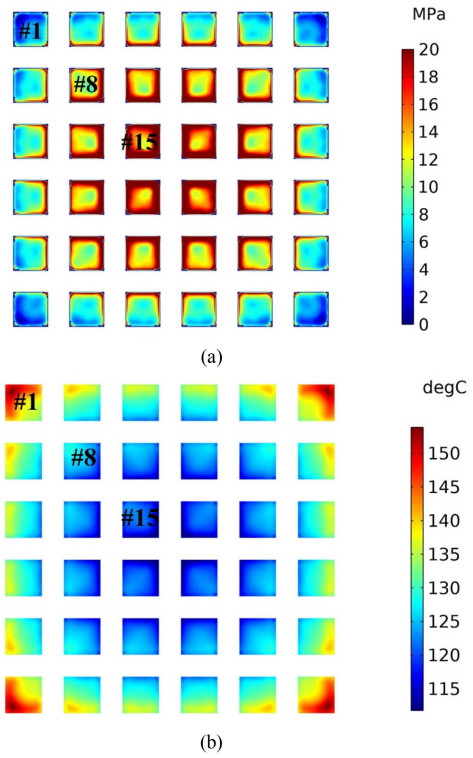

Fig. 5. Pressure and junction temperature distribution within PP IGBTs (175 W per IGBT chip). (a) Pressure distribution. (b) Junction temperature distribution.

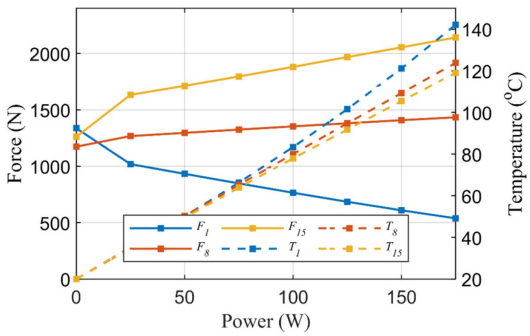

Fig. 6. Clamping force and junction temperature distribution within PP IGBTs under different heating power.

stress and higher temperature, which is significantly different from the room temperature simulation. This temperature distribution exhibit the same trend as the experimental results in [19]. Hence the model established is reasonable and could be used to investigate the root reason for the thermomechanical coupling effect and the electrode warpage.

The marked chips (#1, #8, and #15) in the diagonal line are selected to explain more phenomena. The clamping force (integration of the chip surface pressure) and the junction temperature (chip surface average temperature) of each IGBT chip under different heating powers per chip are given in Fig. 6. The deviation of the clamping force and junction temperature, which corresponds to the $|F_1\text{-}F_{15}|$ and $|T_1\text{-}T_{15}|$, are also shown in Fig. 7. As can be seen, the deviation of clamping force among

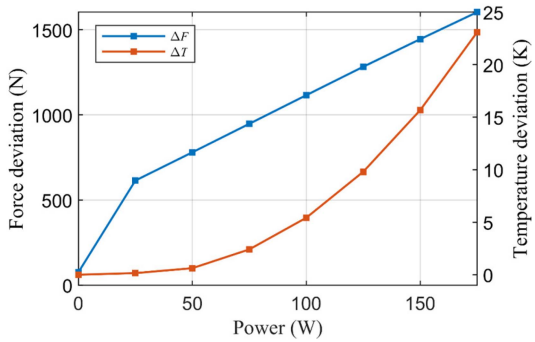

Fig. 7. Deviation of the clamping force and junction temperature within PP IGBTs under different heating power.

different chips increases from 76 to 1604 N as the heating power increases from 0 to 175 W. The heating power of 0 W indicates the initial condition that only total clamping force is applied but no current flowing through. The relationship between the deviation of clamping force and heating power is not linear in the range of 0 to 25 W. This is the result that the friction force between the heat sink and electrode induced by the different lateral thermal expansion. The influence of this friction force is not considered in the later analysis because it is relatively minor and indicate the effect of external condition but not within PP IGBTs. The deviation of the junction temperature increases up to 23.1 °C at the heating power of 175 W. The deviation of junction temperature rises slowly at the initial stage but sharply after the deviation of clamping force reaches about 800 N. The reason is that the thermal contact resistance changes more distinctly at small clamping force but slightly at large clamping force as shown before in Fig. 3. Generally, the pressure and temperature distribution become more uneven with the increase of heating power, which could become more severe within the device at a higher current rating.

The thermal strain distribution of different materials along the cut line is also given in Fig. 8. Calculation results show that the thermal strain of copper is the largest and the value of silicon and molybdenum is relatively low. The deformation of the z-axis along the cut line is illustrated in Fig. 8(b). The deformation of copper material accounts for about 91.3% of the total deformation at a heating power of 175 W, which is caused by a larger thermal strain and a higher thickness. The deformation of silicon and molybdenum keeps a low value at different heating power. Hence, the deformation of the copper electrode is the main reason for thermal stress and should be paid more attention to.

III. Root Reason for the Thermomechanical Coupling Effect

A. Influence of Vertical and Lateral Temperature Difference

According to the analysis above, the deformation of the copper electrode induced by the heating power is the dominant factor of thermomechanical coupling. This deformation is decided by the temperature distribution within the electrode and is generally referred to as warpage. The temperature distribution of the

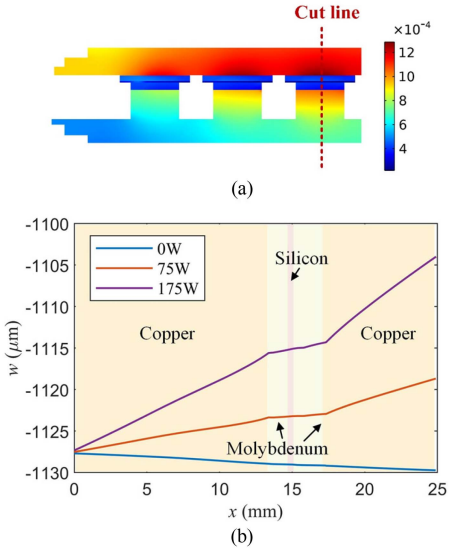

Fig. 8. Thermal strain and the deformation of different materials. (a) Thermal strain distribution (175 W per IGBT chip). (b) Deformation of different materials at different power.

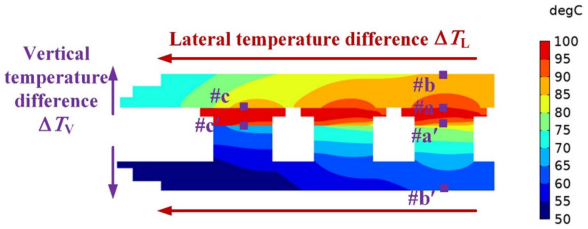

Fig. 9. Temperature distribution of the cut plane (175 W per IGBT chip).

electrode at the heating power of 175 W is given in Fig. 9. As can be seen, the temperature is uneven both in the vertical direction and the lateral direction. The vertical temperature difference ΔT_V is caused by the heat flow across the electrode and this difference corresponds to its thermal resistance. The lateral temperature difference ΔT_L is the result of the thermal coupling caused by the layout and the central position of the electrode has a higher temperature than the edge position. Both vertical and lateral temperature differences result in electrode warpage. The schematic diagram of the electrode warpage under vertical and lateral temperature differences is given in Fig. 10. The vertical temperature difference could lead to the electrode bending outward, which has been explained in [15] and [16] and is supposed to be the main reason for the uneven pressure distribution before, as shown in Fig. 10(a). However, the lateral temperature difference could result in uneven electrode thickness at different positions in the lateral direction and induce pressure unevenness, which is not considered in previous literature, as illustrated in Fig. 10(b). For the sake of description, these two factors are also defined quantitatively. The ΔT_V is defined as the average value of T_a-T_b and T_a'-T_b'. The ΔT_L is defined as the average value of T_a-T_c and T_a'-T_c'. The average value is chosen considering the different heat dissipation structures of both sides. The electrode warpage at different heating power is

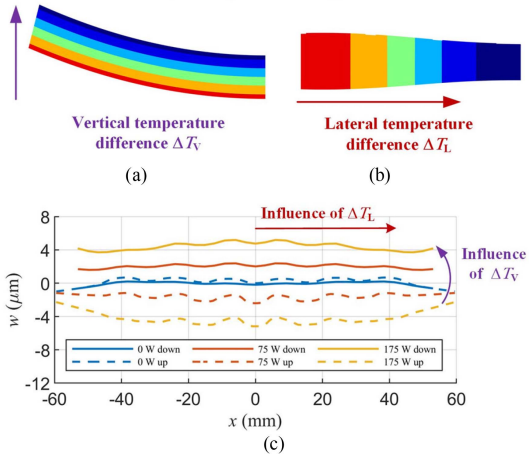

Fig. 10. Example of the electrode warpage under uneven temperature distribution. (a) Warpage is induced by vertical temperature difference. (b) Warpage is induced by lateral temperature difference. (c) Actual electrode warpage.

given in Fig. 10(c) as an example with real constraints. As can be seen, the realistic warpage seems to be the result of both ΔT_L and ΔT_V induced by the heating power. It is necessary to make a further distinction between the effect of the ΔT_L and ΔT_V on the electrode warpage.

However, it is not an easy task to decouple the influence of these two factors because the increase in heating power increases both ΔT_L and ΔT_V. To address this problem, the heat transfer coefficient is adjusted because it mainly affects the lateral heat conduction within the electrode [32], but has little influence on the vertical heat conduction. Then, different ΔT_V and ΔT_L combinations could be realized through the combination of heating power and heat transfer coefficient. The range of heating power per IGBT chip is from 0 to 175 W and the range of heat transfer coefficient is from 2500 to 50000 W/(m^2·K). The relationship between force and junction temperature deviation with ΔT_V and ΔT_L is given in Fig. 11. The scatter point is the original data obtained by finite-element calculation. The surface is the fitted data through the cubic spline and the contour line is also shown. As can be seen, the contour line of the force deviation is almost parallel to the ΔT_V axis, which indicated that the force deviation is mainly influenced by the ΔT_L rather than ΔT_V. In the case of small ΔT_L, force deviation is relatively low even if the ΔT_V is relatively large. An example is point A in Fig. 11, which corresponds to a heat power per IGBT chip of 175 W and a heat transfer coefficient of 50 000 W/(m^2·K). The pressure distribution at point A is given in Fig. 12. Calculation results confirm that the uniform pressure distribution could be obtained even at a high heating power under the condition of low ΔT_L, which is different from the existing knowledge. The junction temperature deviation also exhibits similar behavior to force deviation and the peak value of junction temperature deviation is located at a high ΔT_L.

B. *Simplified Model for the Lateral Temperature Difference*

A simplified model is built for further understanding the influence of the electrode lateral temperature difference on the

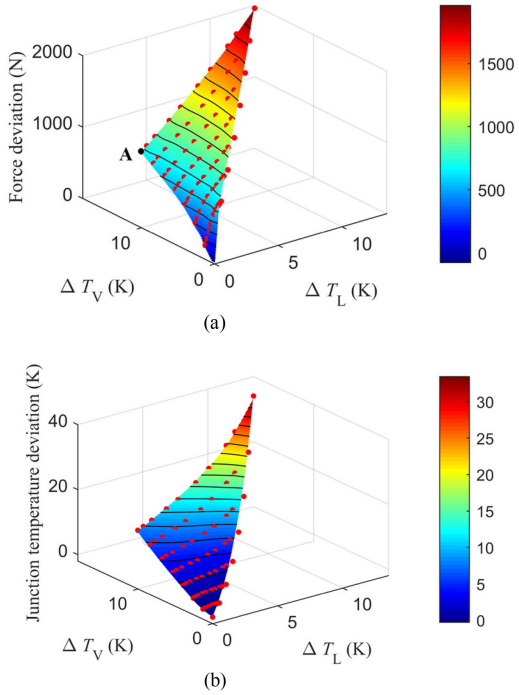

Fig. 11. Force and junction temperature deviation under different ΔT_V and ΔT_L.

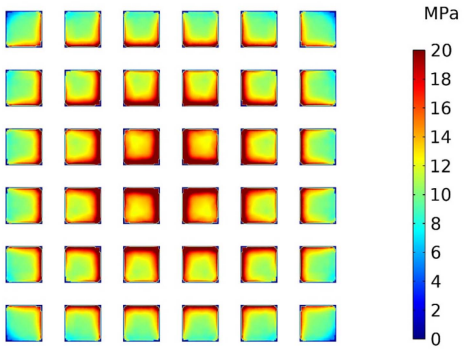

Fig. 12. Pressure distribution at point A ($\Delta T_L = 2.9$ K and $\Delta T_V = 15.1$ K, heat power per IGBT chip is 175 W, heat transfer coefficient is 50 000 W/(m^2·K)).

pressure and junction temperature distribution. The simplified geometry is shown in Fig. 13(a). Only one side heat flow path is investigated and two fixed displacement constraints are applied to the electrode for the convenience of description. The circuit model for the thermal field and mechanical field are given respectively in Fig. 13(b) and (c). The bidirectional thermomechanical coupling is realized through the parameters marked blue such as F_m, F_n, $T_{up,n}$, etc.

For the thermal circuit model, the thermal contact resistance is described as a function of force and the thermal coupling effect is considered by mutual resistance in (8) [32]. The heating power of every chip is supposed to be the same. Then, the junction temperature for chip m could be obtained as (9). The electrode

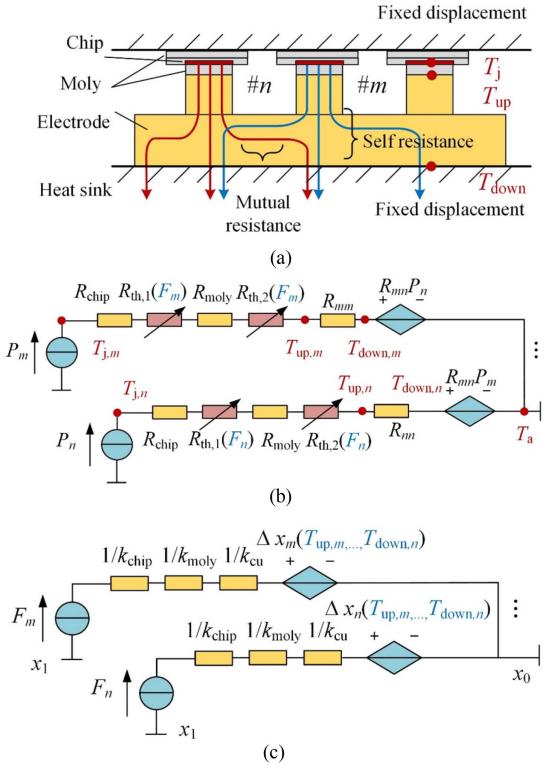

Fig. 13. Simplified thermomechanical coupling model considering lateral temperature difference. (a) Simplified geometry. (b) Thermal circuit model. (c) Force circuit model.

lateral temperature difference and junction temperature deviation of chip m and n could be derived as (10) and (11)

$$T_{\mathrm{up},m} = T_a + \sum_p R_{mp} P \tag{8}$$

$$T_{j,m} = T_{\mathrm{up},m} + (R_b + R_{\mathrm{th}}(F_m))P \tag{9}$$

$$\Delta T_L = T_{\mathrm{up},m} - T_{\mathrm{up},n} = \left(\sum_p R_{mp} - \sum_p R_{np}\right) P \tag{10}$$

$$\begin{aligned}\Delta T_j &= T_{j,m} - T_{j,n} \\ &= \Delta T_L + (R_{\mathrm{th}}(F_m) - R_{\mathrm{th}}(F_n))P\end{aligned} \tag{11}$$

where $T_{\mathrm{up},m}$ is the upper side temperature of the electrode at the location of chip m, $T_{j,m}$ is the junction temperature for chip m, and T_a is the ambient temperature. $R_b = R_{\mathrm{chip}} + R_{\mathrm{moly}}$ is the bulk thermal resistance, $R_{\mathrm{th}}(F_m) = R_{\mathrm{th},1}(F_m) + R_{\mathrm{th},2}(F_m)$ is the thermal contact resistance, and R_{mp} is the thermal resistance matrix for the electrode. The diagonal term represents self thermal resistance and the off-diagonal term represents mutual thermal resistance. F_m is the clamping force for chip m.

For the force circuit model, the electrode warpage is expressed as the thermal deformation deviation of parallel submodules Δx. Then, the quantitative relationship between Δx and ΔT_L could be derived as given in (12), which indicates the electrode warpage increases linearly as the increase of ΔT_L. Then, the force deviation caused by the electrode warpage could be further

obtained as (13). Furthermore, the junction temperature deviation in (11) could be estimated using first-order Taylor expansion and lead to (14)

$$\begin{aligned}\Delta x &= \Delta x_m - \Delta x_n \\ &= \alpha\left[\frac{1}{2}\left(T_{\mathrm{up},m}+T_{\mathrm{down},m}\right)-\frac{1}{2}\left(T_{\mathrm{up},n}+T_{\mathrm{down},n}\right)\right]L \\ &= \alpha PL\left(\sum_p R_{mp}-\sum_p R_{mp}\right)=\alpha L\Delta T_L \qquad (12)\end{aligned}$$

$$\Delta F = F_m - F_n = k\Delta x = k\alpha L\Delta T_L \qquad (13)$$

$$\Delta T_j \approx \Delta T_L + \frac{\mathrm{d}R_{\mathrm{th},c}}{\mathrm{d}F}\Delta F = (1+\frac{\mathrm{d}R_{\mathrm{th},c}}{\mathrm{d}F}k\alpha L)\Delta T_L \qquad (14)$$

where Δx is the thermal deformation deviation of parallel submodules, L is the thickness of the copper electrode, α is the coefficient of thermal expansion of copper, and k is the equivalent spring coefficient, which satisfies $1/k = 1/k_{\mathrm{chip}}+1/k_{\mathrm{moly}}+1/k_{\mathrm{cu}}$.

As shown in (14), the junction temperature deviation ΔT_j consists of two terms. The first term ΔT_L represents the thermal coupling effect and the second term represents the influence of thermal contact resistance deviation caused by ΔT_L. It should be pointed out that only the first term exists in the traditional module and the second term is unique in PP IGBTs. The second term induces the opposite temperature distribution trend compared to the traditional module because the $dR_{\mathrm{th},c}/dF$ is negative and could be a dominant factor within PP IGBTs.

In general, the ΔT_L is the root reason for the uneven pressure and junction temperature distribution ΔF, ΔT_j within PP IGBTs. A small ΔT_L should be expected in the packaging design of PP IGBTs. As shown in (10), the value of ΔT_L depends on the difference of the row sum of the electrode thermal resistance matrix $S_m = \sum_p R_{mp}$. A typical thermal resistance matrix for the electrode in Section II is extracted and shown in Fig. 14(a). The thermal resistance matrix is obtained by imposing the heat source on each chip in sequence as shown in [32]. The row sum S_m of the thermal resistance matrix is given in Fig. 14(b). The R_{mm} denotes the self thermal resistance and the $C_m = \sum_{p\neq m} R_{mp}$ denotes the sum of mutual thermal resistance. As can be seen, the S_m of central chips such as #15 is larger than edge chips such as #1. The reason is that central chips are surrounded by more chips than edge chips and the sum of mutual thermal resistance C_m is larger. Hence, two improvements could be proposed to reduce the row sum difference ΔS_m and also the ΔT_L. One is to increase the self and mutual thermal resistance of edge chips, which corresponds to the adjustment of electrode diameter. Another is to decrease the mutual thermal resistance of all chips, which corresponds to the grouped layout. These improvements will be discussed in Section III-C. The relationship between the key variables mentioned above is summarized in Fig. 15 for a better understanding of the role of lateral temperature difference.

The analyses above lay the foundation of the optimization under high heating power without the change of packaging material or adaption of the disc spring. Besides, the object of

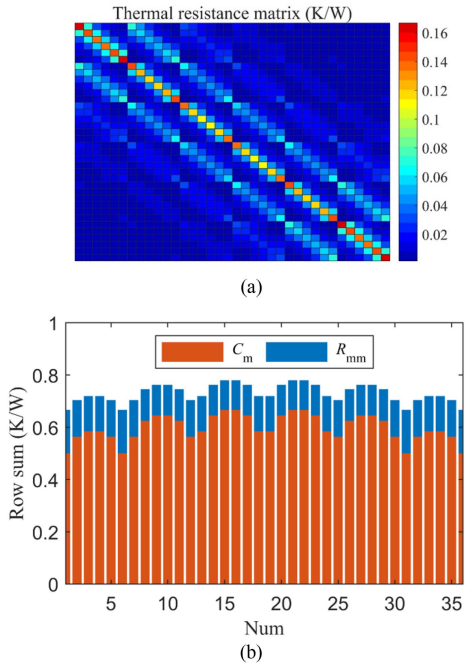

Fig. 14. Thermal resistance matrix and row sum for the electrode in Section II. (a) Thermal resistance matrix. (b) Row sum S_m for every chip m. R_{mm} and C_m denote the self thermal resistance and sum of mutual thermal resistance for chip m respectively.

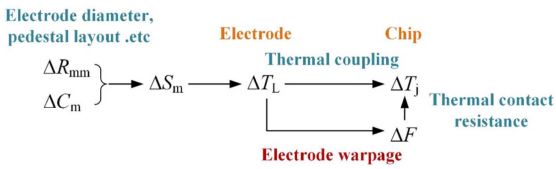

Fig. 15. Relationship among key variables.

thermomechanical optimization could also be realized approximately through pure thermal design which restricts the ΔT_L by holding the row sum S_m of the thermal resistance matrix to be the same. The thermal contact resistance during pure thermal design is supposed to be the const value with rating clamping force. This assumption has a small influence on the calculation result of the ΔT_L because the thermal contact resistance mainly influenced the temperature of the molybdenum plate and chip, but not the electrode. Furthermore, a simplified optimization procedure is proposed to replace the traditional thermomechanical optimization procedure as shown in Fig. 16. Pure thermal optimization is performed but not thermomechanical optimization to find out the optimum layout. Hence, the optimization target becomes more clear and the calculation amount in every iteration could also be reduced such as from 3780 s (thermomechanical coupling calculation) to 26 s (pure thermal calculation).

C. Proposed Improvements

1) Electrode Design: Both self and mutual thermal resistance terms of the edge chip increase significantly as the decrease of electrode diameter because of the worsened heat dissipation conditions [32]. Hence, the row sum difference ΔS_m between

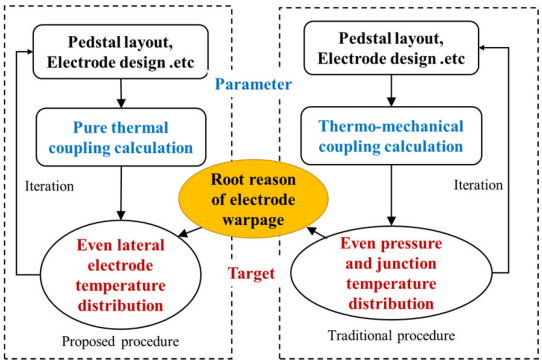

Fig. 16. Optimization procedure.

edge chips and central chips, and also the ΔT_L, ΔT_j, and ΔF could be reduced through the proper adjustment of electrode diameter.

The electrode diameter d_E is selected as a parameter from the range of 85 to 120 mm. The pure thermal calculation is performed firstly to investigate the influence of electrode diameter d_E. The row sum S_m, self thermal resistance R_{mm} and sum of mutual thermal resistance C_m for edge chip #1 and central chip #15 are illustrated in Fig. 17(b). As can be seen, the R_{mm} and C_m of edge chip #1 have a larger change rate than central chip #15 as the variation of electrode diameter. Therefore, both the row sum difference $|\Delta S_m|$ and the lateral electrode temperature difference $|\Delta T_L|$ could be reduced through adjustment of d_E for this change rate difference. The relationship between the $|\Delta S_m|$, $|\Delta T_L|$ and d_E is given in Fig. 17(c). As can be seen, both the $|\Delta S_m|$ and $|\Delta T_L|$ reaches about zero at the $d_E = 95$ mm. This suppression of lateral temperature difference could be illustrated more clearly by the temperature distribution along cut lines 2 and 3 as shown in Fig. 17(d). According to the (13) and (14) proposed in Section III-B, the ΔT_j, ΔF could also be suppressed as soon as the ΔT_L is reduced.

The pressure and junction temperature distribution are then obtained by thermomechanical calculation for validation and given in Fig. 18. The relationship between the force and junction temperature deviation to the d_E is illustrated in Fig. 19. As can be seen, the junction temperature deviation ΔT_j meets the minimum value and the force deviation ΔF also decreases to a low value at the $d_E = 95$ mm, which indicates the effectiveness of the reduction of ΔT_L. It should be pointed out that the ΔT_j and ΔF are not zero as the prediction of (13) and (14). This is the result of friction force between the device and the heat sink as discussed in Section II. This force deviation could be reduced further as the decrease of d_E for the reverse ΔT_L could compensate for the force deviation caused by friction force. However, it is not recommended because the pressure distribution on the edge chip could be worsened at a too-small d_E although better force deviation among different chips. In conclusion, relatively uniform pressure and temperature distribution could be realized through the electrode design (force deviation of 683 N and temperature deviation of 14.3 K for the model in this article).

2) Pedestals Layout Design: The mutual thermal resistance decreases dramatically as the increase of distance between

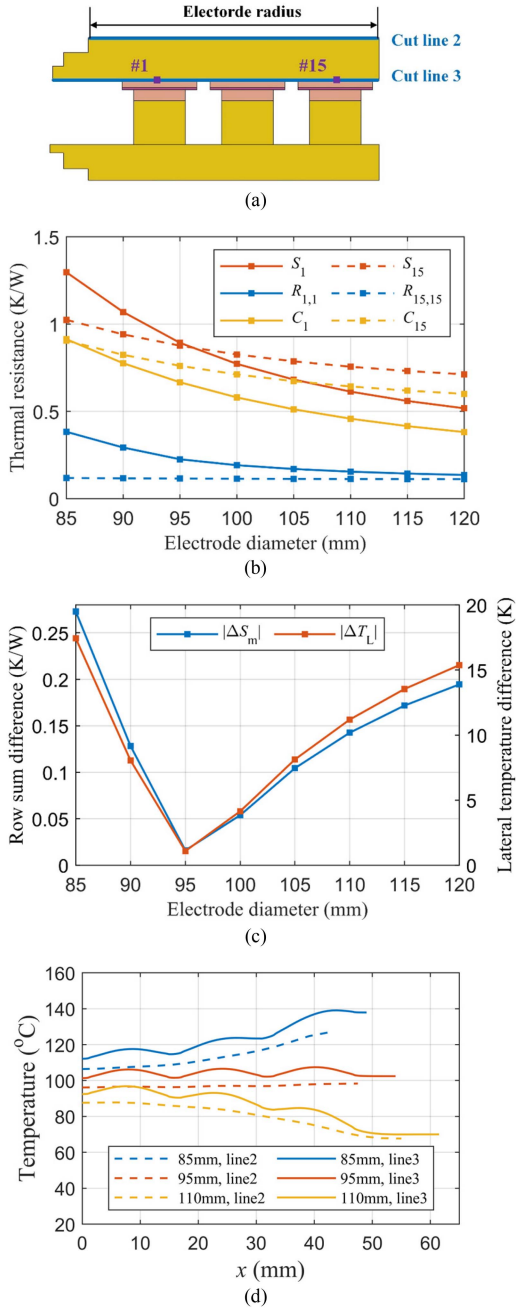

Fig. 17. Pure thermal calculation results under different electrode diameters d_E. (a) Section view of PP IGBTs. (b) Row sum S_m, self thermal resistance R_{mm}, and mutual thermal resistance C_m for edge chip #1 and central chip #15. (c) Row sum difference and lateral temperature difference. (d) Temperature distribution along cut line 2 and cut line 3.

pedestals [32]. Therefore, the row sum difference ΔS_m between edge chips and central chips caused by the mutual thermal resistance could be suppressed through the increase of the pedestal distance. However, the increase in the pedestal distance leads to a rise in the size and cost of the whole device. A better way is to adapt the grouped layout and only alleviate the thermal coupling effect among different groups. All paralleled chips are divided into several parts and the increased distance between the adjacent chips from different groups is defined as group distance

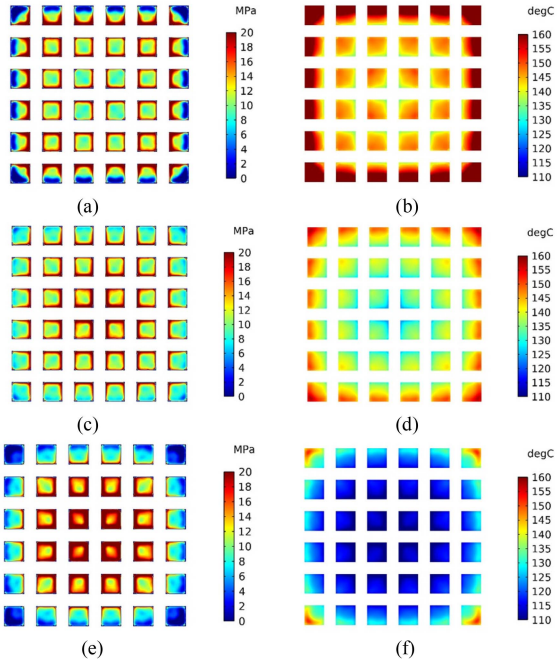

Fig. 18. Pressure and junction temperature distribution with different electrode diameter d_E. (a) Pressure distribution, $d_E = 85$ mm. (b) Junction temperature distribution, $d_E = 85$ mm. (c) Pressure distribution, $d_E = 95$ mm. (d) Junction temperature distribution, $d_E = 95$ mm. (e) Pressure distribution, $d_E = 110$ mm. (f) Junction temperature distribution, $d_E = 110$ mm.

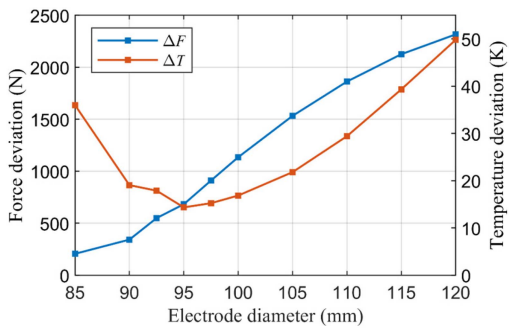

Fig. 19. Force and junction temperature deviation with different electrode diameter d_E.

d_g, as given in Fig. 20(a). The 0 mm of group distance is exactly the initial layout without grouping. The group distance d_g is increased from 0 to 16 mm. The margin between the electrode and edge submodule holds the same at different group distances to avoid the influence of the electrode diameter.

The row sum S_m, self thermal resistance R_{mm} and sum of mutual thermal resistance C_m under different d_g for edge chip #1 and central chip #15 are extracted by pure thermal calculation and given in Fig. 20(b). The difference in the C_m between #1 and #15 decreases as the increase of group distance, which indicates the suppressed thermal coupling effect. The row sum difference $|\Delta S_m|$ and the lateral electrode temperature difference $|\Delta T_L|$ were reduced because of the decrease of $|\Delta C_m|$ as shown in Fig. 20(c) and (d). Then, the ΔT_j, ΔF should also decrease for the reduction of ΔT_L according to the (13) and (14).

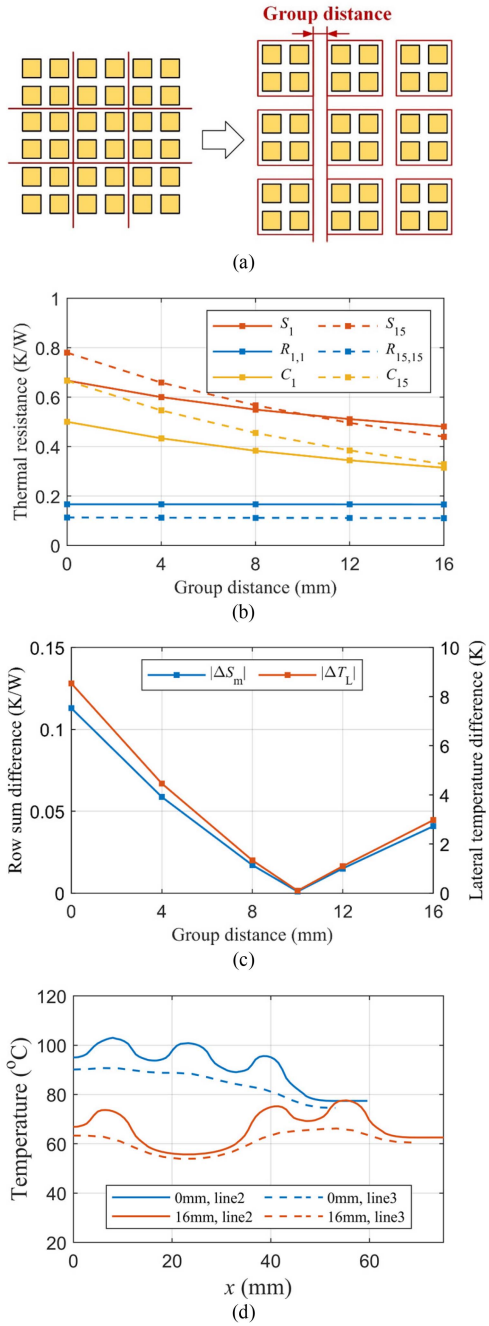

Fig. 20. Pure thermal calculation results under different group distance d_g. (a) Grouped layout. (b) Row sum S_m, self thermal resistance R_{mm}, and mutual thermal resistance C_m for edge chip #1 and central chip #15. (c) Row sum difference and lateral temperature difference. (d) Temperature distribution along cut line 2 and cut line 3.

The pressure and junction temperature distribution with 0 and 16 mm group distance are obtained by thermomechanical calculation and given in Fig. 21. The relationship between the force deviation and temperature deviation and group distances is shown in Fig. 22. As can be seen, both the force deviation and junction temperature deviation decrease with the increase of group distance. The force deviation is reduced from about 1554.0 to 346.3 N and the junction temperature deviation is decreased from about 21.9 K to about 9.8 K at $d_g = 16$ mm. The non-zero

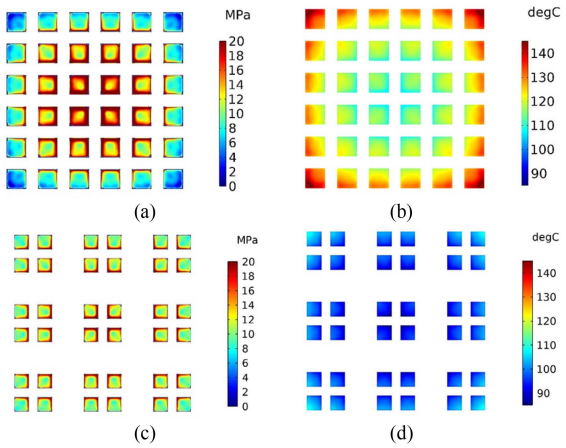

Fig. 21. Pressure and junction temperature distribution with different group distance d_g. (a) Pressure distribution, $d_g = 0$ mm. (b) Junction temperature distribution, $d_g = 0$ mm. (c) Pressure distribution, $d_g = 16$ mm. (d) Junction temperature distribution, $d_g = 16$ mm.

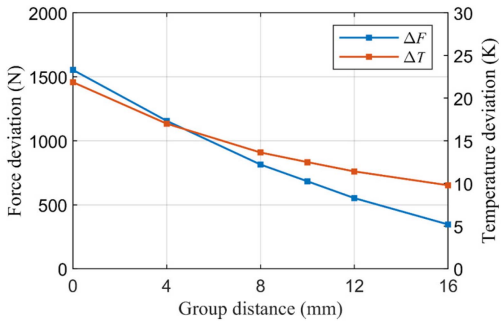

Fig. 22. Force and junction temperature deviation with different group distance d_g.

TABLE I
COMPARISION OF DIFFERENT GROUPING SCHEMES

Group number	Group distance	Temperature deviation	Force deviation	Device dimension
1	0	21.9 K	1554.0 N	106 mm
9	8 mm	13.6 K	814.3 N	122 mm
9	16 mm	9.8 K	346.3 N	138 mm
4	8 mm	4.9 K	689.0 N	114 mm
4	16 mm	5.3 K	290.8 N	122 mm

force and junction temperature deviation are also the results of the friction force illustrated in Section II. This deviation could be reduced further through a larger grouped distance but with the increase in the size and cost. A comprehensive comparison of different group schemes including force deviation, junction temperature deviation and device dimension is given in Table I. A scheme that contains more chips in each group (such as four groups and nine chips in each group) seems to alleviate the negative effects of increasing distance, which could be a choice in the trade-off process.

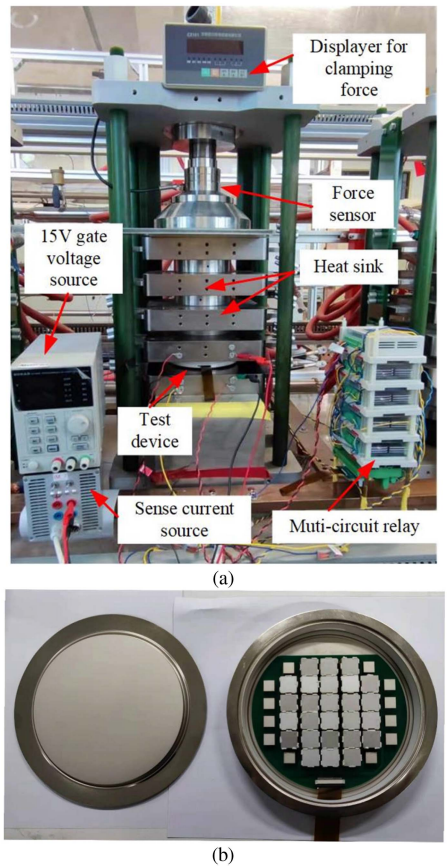

Fig. 23. Test setup of the temperature distribution measurement experiments [19]. (a) Test platform. (b) Test device.

IV. EXPERIMENTAL VERIFICATION

Based on the theoretical analyses and calculation results above, the lateral temperature difference of the electrode ΔT_L is the dominant factor affecting the thermomechanical coupling effect. Relative uniform pressure and junction temperature distribution among the parallel chips could be realized through the reduction of ΔT_L, such as electrode design or pedestal layout design. An experiment is performed in this section to confirm the effectiveness of the ΔT_L reduction. Different ΔT_L is realized through the modification of pedestal layouts but not electrode diameter. The reason is that the modification of the pedestal layout could be easily achieved through the adjustment of the submodule location for press-pack packaging. But the modification of electrode diameter is not so convenient because of the requirement for customized housing. As for the verification means, the direct measurement of pressure distribution under heating conditions within PP IGBTs is impossible because the FUJI pressure film is insulated. Only the junction temperature distribution could be obtained by the gate voltage control through the sequential $V_{ce}(T)$ method proposed in [19].

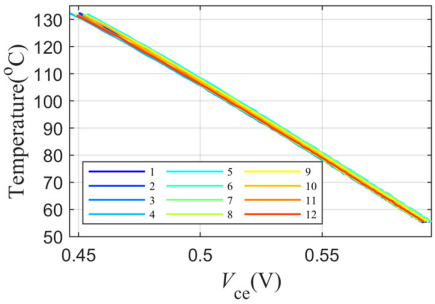

Fig. 24. Calibration curves of different IGBT chips.

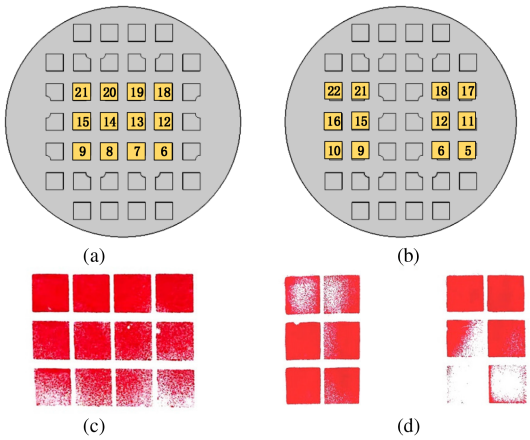

Fig. 25. Two layouts of submodules and pressure distribution. (a) Layout I. (b) Layout II. (c) Pressure distribution of layout I. (d) Pressure distribution of layout II.

The test PP IGBT device is shown in Fig. 23(b) and 12 IGBT chips are chosen in parallel in this experiment to measure the junction temperature distribution. The printed circuit board with individual gate wiring is specially designed according to the requirement of the sequential $V_{\rm ce}(T)$ method. The test setup of the junction temperature distribution measurement experiment is given in Fig. 23(a). All calibration curves of 12 IGBT chips are sequentially measured via the platform at a sense current of 100 mA. The calibration results of all IGBT chips are given in Fig. 24 and the $V_{\rm ce}$ and T exhibit a great linear relationship.

To investigate the influence of the lateral temperature difference of the electrode, two layouts of submodules are adapted. In the layout I, 12 IGBT chips are closely placed in the center with a larger lateral temperature difference. In the layout II, 12 IGBT chips are divided into two groups and a smaller lateral temperature difference is realized through the reduction of the thermal coupling among submodules as discussed in Fig. 20. The height of all submodules is controlled within the tolerance of 15 μm and the pressure distribution is measured by prescale film in the clamping phase. The layout of submodules and pressure distribution is shown in Fig. 25. The pressure distribution in the layout I is relatively uniform and layout II is not very uniform. The reason is that the height of the pedestal is changed after the experiment of the layout I. However, this difference is not so big and can also be reflected by the junction temperature.

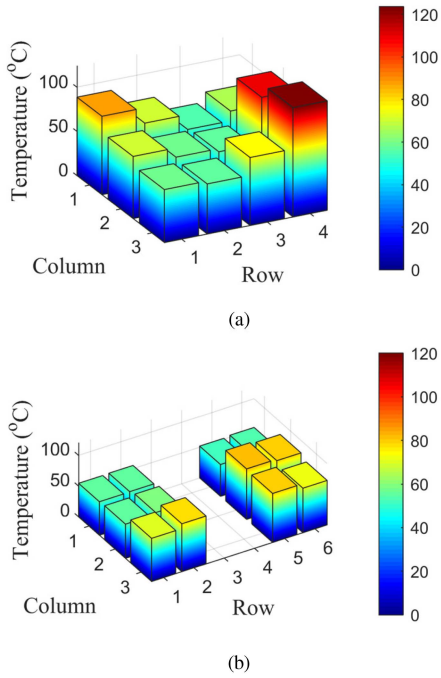

Fig. 26. Temperature distribution of the two layouts ($I_{\rm heating} = 360$ A, $t_{\rm on} = 5$s, $F_{\rm total} = 15$ kN, and $T_{\rm inlet} = 20$ °C). (a) Layout I. (b) Layout II.

A dc power cycling test at $I_{\rm heating} = 360$ A (30 A per IGBT chip), $t_{\rm on} = 5$s, $F_{\rm total} = 15$ kN(1.25 kN per IGBT chip), and $T_{\rm inlet} = 20$ °C is performed to obtain the junction temperature distribution within PP IGBTs. The experimental results under the two layouts are shown in Fig. 26. The temperature of the outmost chip (#6, #18, and #21) is higher than that of the inner chip (#13, #14) within the layout I, which is the outcome of the thermomechanical coupling effect. However, the temperature distribution within the layout II is relatively uniform and the IGBT chips which have a higher temperature are located in the submodules which have a lower height (#5, #6, and #12) but not the submodules at the edge. This indicates that the thermomechanical coupling effect is weakened through the grouping and validates the conclusion above.

V. Results and Discussion

The influence of the heating power on the electrode warpage is investigated above and explained by the lateral temperature difference ΔT_L through a device with 36 IGBT chips. In some commercial devices, many of the chips are diode chips and have a different power loss profile from IGBT chips. Moreover, the device operates under the rectifier or inverter operating condition rather than dc operating condition. In this section, the influence of uneven heating power is analyzed and the pressure distribution under more realistic operating conditions is given as an example.

The 12 chips on the edge are treated as diode chips to investigate the influence of uneven heating power. The heating power applied to these chips sweeps from 0 to 300 W and other chips are considered IGBT chips with a constant 150 W heating power. The thickness difference between diode and IGBT chips is not considered here because this difference could be suppressed

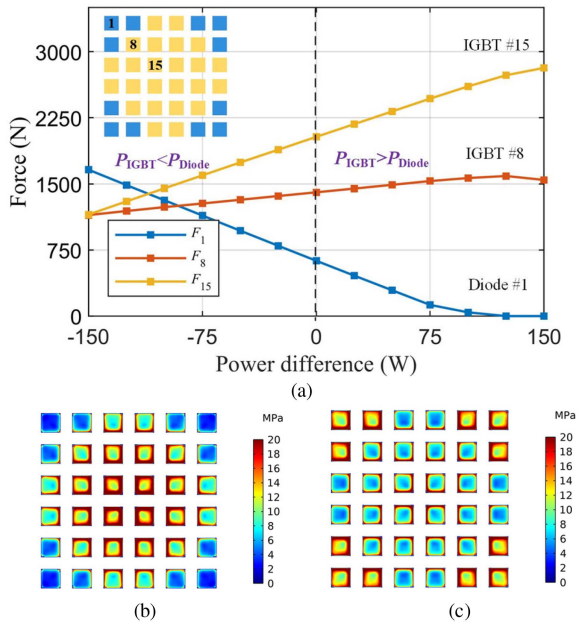

Fig. 27. Influence of the uneven power profile on pressure distribution. (a) Clamping force distribution under different power differences $\Delta P = P_{\mathrm{IGBT}}$-$P_{\mathrm{Diode}}$; (b) Pressure distribution under rectifier operation mode ($P_{\mathrm{IGBT}} =$ 115.4 W and $P_{\mathrm{Diode}} = 69.2$ W) (c) Pressure distribution under inverter operation mode ($P_{\mathrm{IGBT}} = 66.7$ W and $P_{\mathrm{Diode}} = 166.7$ W).

through tolerance matching [2] or a prestressed process [33] and the pressure distribution is guaranteed to be uniform before heating up [17]. The clamping force distribution under different heating power differences $\Delta P = P_{\mathrm{IGBT}}$-$P_{\mathrm{Diode}}$ is illustrated in Fig. 27(a). Simulation results indicate that the chips with larger heating power have a larger clamping force. The reason is that the part of the electrode at these locations suffers a higher temperature, which results in a larger thickness. This phenomenon agrees with the conclusion above that the electrode lateral temperature difference ΔT_L is the main reason for electrode warpage. In practical applications, the power losses of IGBT chips and diode chips could be different under various operating conditions. Take the high side IGBT and diode in [4] ($\pm$800kV/5GW converter, $f_{\mathrm{sw}} = 100$ Hz, and $V_{\mathrm{dc}} = 2200$ V) as an example, the power loss ratio is about 10: 3 in rectifier operation mode but 4: 5 in inverter operation mode. Assuming a total power loss of 3600 W, the pressure distribution is calculated and shown in Fig. 27(b) and (c). As can be seen, the position of the chip with the highest clamping force changes significantly in these two modes. Therefore, for the devices containing anti-parallel diodes, the electrode lateral temperature difference ΔT_L should be maintained as a small value as possible in all operation modes. An interleaved arrangement for IGBT and diode chips could be a suitable solution that utilizes the thermal coupling between IGBT and diode chips.

VI. Conclusion

In this article, the understanding of the root reason for electrode warpage and thermomechanical coupling within PP IGBTs is put forward. Some improvement approaches are proposed to suppress the electrode warpage and improve the pressure and junction temperature distribution. The conclusion could be drawn as follows.

1) Both vertical and lateral temperature differences exist within the electrode of PP IGBTs. The influence of these two factors on the electrode warpage could be distinguished through the combination of boundary conditions in simulation, which is beneficial for further study of the root reason.
2) The lateral temperature difference of the electrode is the main reason for the electrode warpage, but not the vertical temperature difference. This is different from existing knowledge and indicates the possibility of even pressure and junction temperature distribution under large heating power.
3) The lateral temperature difference is related to the thermal coupling effect. Hence, the electrode warpage could be suppressed approximately only through the pure thermal design rather than the thermomechanical design.
4) The modification of the electrode diameter and the grouped layout could both decrease the lateral temperature difference and improve the uniformity of the pressure and temperature distribution. The influence of the lateral temperature difference and the effectiveness of improvement are verified by experiment.

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