IGBT Junction Temperature Estimation Using a Dynamic TSEP Independent of Wire Bonding Faults

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***Abstract*—Despite that many temperature-sensitive electrical parameters (TSEPs) have been discovered for the online estimation of the junction temperature of IGBT devices, their wide adoption in the field is yet to come. This is because they are most susceptible to both the aging status and operating points of IGBTs, which can result in inaccurate results if not attended. In this study, a novel dynamic TSEP, the gate voltage undershoot $V_{\mathrm{GE(np)}}$ of the complementary IGBT switch, is proposed. It is based on the crosstalk effect and measured during the turn-OFF switching transition of the controlled IGBT switch for its temperature estimation. Its monotonic temperature dependence has been identified with implications for the changing load current and bus voltage, which are experimentally verified using a 1200 V/450 A IGBT module. The theoretical analysis and experimental results also show that $V_{\mathrm{GE(np)}}$ is independent of bond wire failures while providing comparatively high relative sensitivity. The MMC power equivalent experimental results are given to verify the feasibility of the proposed method in commercial engineering applications. Finally, the multivariate linear regression method is used to improve the ability to estimate the IGBT's temperature by accounting for the operating point.**

***Index Terms*—Crosstalk effect, insulated gate bipolar transistor (IGBT), junction temperature monitoring, temperature-sensitive electrical parameter (TSPE).**

I. Introduction

OFFSHORE wind power has become one of the popular renewable energy resources with comparably more stable wind speed and larger capacity for power generation. The flexible dc transmission technology based on modular multilevel converters (MMCs) has become the most attractive technical solution for long-distance offshore wind power transmission and grid connection due to its advantages of good scalability, low loss, and independent adjustment of active and reactive power [1], [2], [3]. IGBT power modules are fundamental to MMC operations and exposed to harsh environments (e.g., the complex temperature, humidity, dust, and vibration conditions) as being deployed on offshore platforms. Several wear-out failures are frequently reported, including the bond wire lift-off and solder fatigue, which are mainly driven by cyclic temperature swings appearing in the multilayered package, coupled with different thermal expansion coefficients for the constituents [4], [5]. Numerous physics-of-failure life models have been introduced based on the accelerated life tests which allow the remaining useful lifetime of IGBT modules to be predicted, which is influenced by the maximum, average, and the fluctuation range of the junction temperature [6], [7], [8].

Consequently, the junction temperature is a prerequisite for *in situ* status awareness so that adjudicated health management functions such as active thermal management, over-temperature protection, and adaptive derating can be implemented to enhance the field robustness of IGBT modules. Meanwhile, IGBT current turn-OFF capability decreases with increasing junction temperature [9]. The temperature acquisition can help to optimize the performance, maximize the potential, and enable the health management for IGBTs.

However, to measure the junction temperature online is not a trivial task when considering the operating MMCs. Currently, the junction temperature monitoring methods can be divided into three categories: direct measurement [10], [11], [12], [13], thermal model-based calculation, and temperature-sensitive electrical parameters (TSEPs). The direct measurement method leverages either the negative temperature coefficient (NTC) thermistor or the p-n diode for temperature measurement [12]. Given that the NTC thermistor is mounted on a direct bonded copper (DBC) substrate isolated from the chip, a delayed response relative to the junction temperature is inevitable during thermal transients [13]. Although the integrated p-n diode is in a close proximity to the chip, this will reduce the active area of the chip and thus only adopted by some chip manufacturers. The thermal network-based junction temperature estimation method is computationally intensive, has a slow response time, and requires the accurate calculation of the IGBT module losses. In addition, the aging state of the solder layer needs to be monitored to update the thermal network. Therefore, the thermal

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TABLE I
COMPARISON OF THE METHOD PROPOSED IN THIS ARTICLE WITH OTHER TSEPS

Parametric loop	TSEP	$RS_p = \frac{\left\lvert V_{TESP(25°C)} - V_{TESP(T_j)} \right\rvert}{V_{TESP(25°C)} \cdot (T_j - 25)} \times 100\%$	Wire bonding fault immunity	Measure load current	Measure capacitor voltage	Difficulty of online monitoring
Power loop	$V_{ce(low\ current)}$	0.2882%/°C (2.396)	√	×	×	difficult
	$V_{ce(load\ current)}$	0.1212%/°C (1.007)	×	√	×	medium
	$I_{C(short)}$	0.0168%/°C (0.140)	×	√	√	difficult
	$V_{ce(peak)}$	0.0440%/°C (0.366)	√	√	√	medium
Gate loop	V_{th}	0.1056%/°C (0.878)	×	√	×	easy
	$V_{GE(Miller)}$	0.1154%/°C (0.959)	×	√	√	medium
	t_{Miller}	0.0495%/°C (0.411)	×	√	√	difficult
	$V_{GE(np)}$ in this paper	0.1203%/°C (1.000)	√	√	√	easy

network-based junction temperature estimation method is not suitable for online applications in MMCs containing a large number of IGBT modules [14], [15], [16].

TSEPs have recently attracted many endeavors and they leverage junction temperature-dependent attributes for the virtual temperature estimation by correlating appropriate electrical measurands or deductive parameters to the chip temperature. A multitude of TSEPs has been widely studied in the literature. From a measurement-window perspective, they can be divided into static and dynamic parameters depending on the IGBT operating status. When considering the source of excitations for the intended TSEPs, typical external stimulus sources include the gate voltage (or the gate current), dc-link voltage, load current, or any of their combinations.

For comparison, an overview of nine candidate TSEPs including our newly proposed one is given in Table I. The relative sensitivity of the TSEP, $V_{\mathrm{GE(np)}}$, proposed in this article is chosen as a benchmark 1.00. Other TSEPs include the collector voltage under both low (sensing) and high (load) current, respectively, that are $V_{\mathrm{CE(sat)L}}$ [17], [18], [19], and $V_{\mathrm{CE(sat)H}}$ [20], [21], the collector voltage edge rate [22], the current edge rate [23], and short-circuit current [24], etc. Both $V_{\mathrm{CE(sat)L}}$ and $V_{\mathrm{CE(sat)H}}$ are static measurements. The former is widely used for junction temperature estimation in accelerated aging tests [25] due to high repeatability. However, its online measurement necessitates additional circuits to provide an external low-current excitation. On the other hand, the load current satisfies the $V_{\mathrm{CE(sat)H}}$ measurement and thus additional excitation is unnecessary. In addition, due to the mid-point voltage changes between both positive and negative dc rails, both methods require specific protection from the dc-link voltage while enabling high resolution [17].

The TSEPs of the gate loop include the threshold voltage [14], [26], gate Miller plateau (magnitude and width) [27], [28], gate current [29], [30], turn-ON delay time [31], [32], and turn-OFF delay time [33], etc. They are usually noted as dynamic TSEPs as being coupled with the transient stimulus sources and enabled by the gate driver step output voltage. Typical responses to the gate circuit excitation from such TSEPs are normally weak, so are their temperature dependency, e.g., only several tens of millivolts per Celsius degree for the threshold voltage at the best. Since measurements take place during fast transients of the gate loop, which may be complicated by coupling due to spurious variations of the power loop signals, they are easily interfering with measurement noise, resulting in inaccuracy.

By considering a robust TSEP for the through-life junction temperature measurement, parametric drifts due to the degradation of module packaging materials also produce noise and measurement error. The bond wire failure is a common failure mode and their stray inductance and resistance may increase substantially as it intensifies, which also affects external electrical parameters. This has been observed as a noise factor due to aging for many TSEPs, such as $V_{\mathrm{CE(sat)H}}$, short-circuit current, threshold voltage, and Miller platform voltage.

In this article, a novel TSEP is proposed based on the gate voltage undershoot, $V_{\mathrm{GE(np)}}$, during the turn-OFF transition of the complementary IGBT switch in typical half-bridge configurations. This method is immune from the bonding wire failures and can maintain its efficacy for a severely degrading IGBT switch with wire bonding faults [34]. The TSEP proposed in this article is presented and monitored at the gate loop, whilst maintaining a high relative sensitivity of monitoring.

The rest of this article is organized as follows. In Section II, the internal structure and equivalent circuit of the IGBT module are given. The analytical model and temperature dependence of gate voltage undershoot $V_{\mathrm{GE(np)}}$ are analyzed in detail. In Section III, a commercial IGBT module is tested at different load currents, capacitor voltages, and junction temperatures to verify the effectiveness of the proposed method. The MMC power equivalent experimental results are given to verify the feasibility of the proposed method in commercial engineering applications. In Section IV, the calibration and calculation method for junction

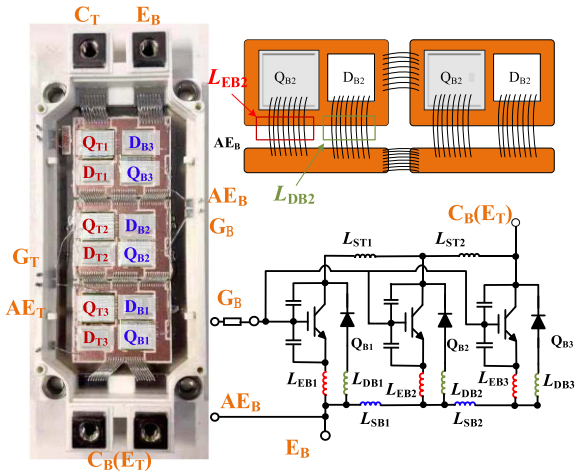


Fig. 1. Internal structure of a multichip IGBT module and its bottom switch equivalent circuit.

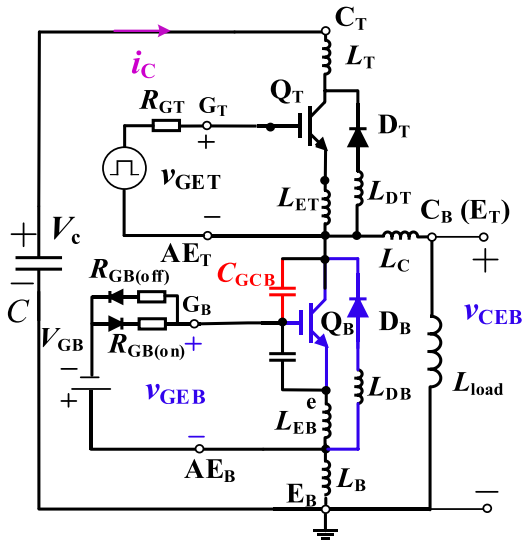


Fig. 2. Circuit diagram of the double pulse test.

temperature is also given. Finally, Section V concludes this article.

II. Analysis of Crosstalk Effect and the Gate Voltage Undershoot

A. Crosstalk Effect in the Half-Bridge Configuration

A 1200 V/450 A open IGBT module (TXFF450R120MC1) produced by TANXI Company is used to carry out the theoretical and experimental analysis. The internal structure of the module and the equivalent circuit of its bottom switch are shown in Fig. 1. The module consists of two switches, forming a half-bridge structure, and each switch includes three paralleled IGBT-diode branches. The emitter of the IGBT chip and the anode of the diode chip are both connected to the copper-clad substrate by bonding wires. L_{ETi} and L_{EBi} (i = 1, 2, 3) are the stray inductance of the IGBT chip emitter bonding wires; L_{DTi} and L_{DBi} (i = 1, 2, 3) are the stray inductance of the diode chip's anode bonding wires. L_{DTi} and L_{DBi} (i = 1, 2, 3) are the stray inductances between the chip branches. L_{SBi} contains the inductance of the DBC and the inductance of the bonding wires between the DBC and the DBC. L_{SBi} is also the coupling inductor of the gate loop and power loop, its value is about 20 nH. Due to the change of load current, the induced voltage on L_{SB} will be coupled to the gate loop, generating a large gate voltage drop. The subscripts T and B refer to the top and bottom switches, respectively. Compared with the diode chip, the IGBT chip has a more complex structure and bears the greater stress in the turn-ON and turn-OFF process, which leads to lower reliability. IGBT chip bonding wire fracture becomes one of the main failure modes of the module.

The double-pulse test circuit is established as shown in Fig. 2. The top IGBT Q_{T} is used as the actively controlled switch, whilst the bottom IGBT Q_{B} remains in the OFF-state under a negative gate bias voltage. The load inductance L_{load} is connected in parallel with the bottom IGBT Q_{B}. Key waveform trajectories including the Q_{B} collector voltage, Q_{T} collector current, and the gate voltages of both Q_{B} and Q_{T} during the Q_{T} turn-OFF

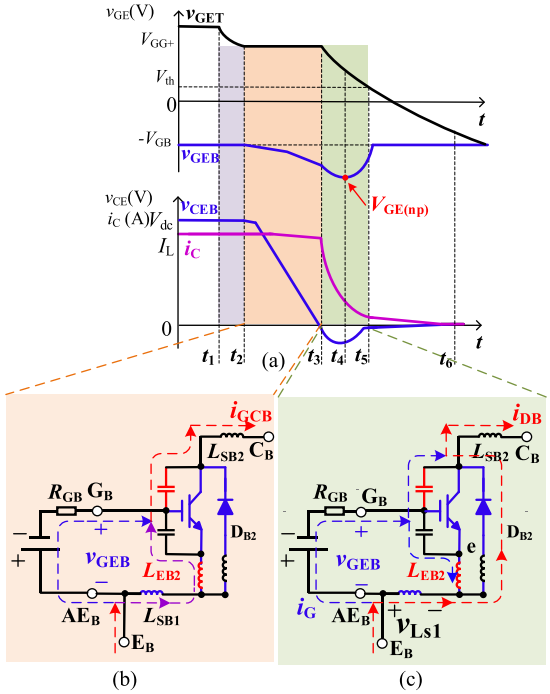


Fig. 3. (a) Waveforms of the v_{GET}, v_{GEB}, v_{CEB}, and i_{C} during the Q_{T} turn-OFF. (b) Distribution of Miller capacitor discharge current i_{GCB} in t_2-t_3 stage. (c) Distribution of diode current i_{DB} in t_3-t_5 stage.

are shown in Fig. 3(a). During the t_2-t_5 stage, the Q_{B} gate voltage v_{GEB} has a voltage undershoot due to the crosstalk phenomenon [35], [36], which can be analyzed in two stages: 1) t_2-t_3 stage, the Q_{B} collector voltage rise stage; 2) t_3-t_5 stage, the Q_{T} collector current drop stage. In the half-bridge structure, the gate voltage undershoot caused by the crosstalk phenomenon is common under normal operation irrespective of the type of the IGBT devices used. No matter what type of IGBT device, the crosstalk voltage undershoot will occur due to the charging and discharging process of the Miller capacitor in the (1) stage. Different types of IGBT devices have different internal

stray inductances, which will affect the induced voltage in the commutation process in (2) stage, and then affect the peak value of crosstalk voltage undershoot. The method proposed in this article does not increase the peak value of the crosstalk voltage, and does not change the control method of the existing converter. The proposed monitoring method utilizes the crosstalk voltage of the converter in normal operation and within safe limits for monitoring.

B. Analysis of Crosstalk Phenomenon in t_2-t_3 Stage

During the t_2-t_3 stage, the collector voltage v_{CET} of the top IGBT $\mathrm{Q_T}$ gradually rises. The antiparallel diode $\mathrm{D_B}$ is still in the cutoff state under negative pressure. During this process, the collector current i_{c} decreases slightly and its rate of change is small. The induced voltage on the stray inductor in the experimental loop is correspondingly small, so the collector current change in this process can be neglected, and v_{CEB} and v_{CET} are considered to satisfy

$$\frac{\mathrm{d}v_{\mathrm{CEB}}}{\mathrm{d}t} = -\frac{\mathrm{d}v_{\mathrm{CET}}}{\mathrm{d}t}. \tag{1}$$

As the collector voltage v_{CEB} gradually decreases, the Miller capacitor C_{GCB} is discharged, and the capacitor discharge current i_{GCB} distribution is shown in Fig. 3(b). The equivalent inductance of the IGBT chip bond wires has the capacitive current flowing through. However, the capacitive current is small, and the induced voltage change caused by the bond wire faults has a small coupling effect on the gate loop. The influence of gate stray inductance on the crosstalk process can be ignored.

Take the chip $\mathrm{Q_{B2}}$ branch as an example, t_2 is the time zero, and the gate voltage satisfies

$$v_{\mathrm{GEB}} = -R_{\mathrm{GB(on)}}C_{\mathrm{GCB2}}\frac{\mathrm{d}v_{\mathrm{CET}}}{\mathrm{d}t}\left(1-\mathrm{e}^{-t/\tau}\right) - V_{\mathrm{GB}} \tag{2}$$

$$\tau = R_{\mathrm{GB2(on)}}\left(C_{\mathrm{GEB2}}+C_{\mathrm{GCB2}}\right). \tag{3}$$

It can be seen that the time constant τ is affected by the input capacitance $C_{\mathrm{GCB2}}+C_{\mathrm{GEB2}}$. Before all the bonding wires of a single chip lift-off, the input capacitance remains unchanged. Some of the bond wire lift-off has a negligible impact on v_{GEB}. The duration of the t_2-t_3 stage is $t_{\mathrm{v.off}}$. v_{CEB} at time t_3 is

$$V_{\mathrm{GE(t3)}} = -R_{\mathrm{GB(on)}}C_{\mathrm{GCB2}}\frac{\mathrm{d}v_{\mathrm{CET}}}{\mathrm{d}t}\left(1-\mathrm{e}^{-t_{\mathrm{v.off}}/\tau}\right) - V_{\mathrm{GB}}. \tag{4}$$

C. Analysis of Crosstalk Phenomenon in t_3-t_5 Stage

At t_3, v_{CET} reaches the bus voltage, v_{CEB} of $\mathrm{Q_B}$ drops to zero. The diode $\mathrm{D_B}$ starts to conduct, and the load current I_{L} commutates from $\mathrm{Q_T}$ to $\mathrm{D_B}$. The $\mathrm{Q_T}$ collector current i_{CT} and the diode $\mathrm{D_B}$ current i_{DB} follow the relationship:

$$-\frac{\mathrm{d}i_{\mathrm{CT}}}{\mathrm{d}t} = \frac{\mathrm{d}i_{\mathrm{DB}}}{\mathrm{d}t}. \tag{5}$$

The distribution of the diode current i_{DB} is shown in Fig. 3(c), i_{DB} does not flow through the stray inductance L_{EBi}, before and after the IGBT chip emitter bond wire lift-off, the circuit parameters flowing through the i_{DB} remain unchanged, and the bonding wire fault does not affect the crosstalk voltage at this stage. Take the IGBT $\mathrm{Q_{B2}}$ branch as an example, t_3 is the time zero. The voltage v_{ge} of the input capacitor at the initial moment is

$$v_{\mathrm{Ge}}|_{t=t_0} = V_{\mathrm{GE(t3)}}. \tag{6}$$

The i_{DB} flowing through the diode generates an induced voltage at the anode equivalent inductance L_{EB2}, which causes the collector voltage v_{CEB} to produce an undershoot, and the input capacitor continues to discharge.

The i_{DB} flows through the stray inductance L_{SB1} between the branches to generate an induced voltage, which is coupled to the gate loop, making v_{GEB} continue to drop. The KVL equation of the gate loop is given

$$R_{\mathrm{GB(on)}}\left(C_{\mathrm{GCB2}}+C_{\mathrm{GEB2}}\right)\frac{\mathrm{d}v_{\mathrm{Ge}}}{\mathrm{d}t} + v_{\mathrm{Ge}} = v_{\mathrm{LS1}} - V_{\mathrm{GB}}. \tag{7}$$

Combined with the initial conditions (6), v_{Ge} can be obtained by solving

$$v_{\mathrm{Ge}} = \left(V_{\mathrm{GE(t3)}} - v_{\mathrm{LS1}} - V_{\mathrm{GB}}\right)\mathrm{e}^{-t/\tau} + v_{\mathrm{LS1}} - V_{\mathrm{GB}}. \tag{8}$$

The gate voltage v_{GEB} during t_3-t_5 stage is

$$\begin{aligned} v_{\mathrm{GEB}} &= v_{\mathrm{Ge}} - v_{\mathrm{LS1}} \\ &= \left(V_{\mathrm{GE(t3)}} - v_{\mathrm{LS1}} + V_{\mathrm{GB}}\right)e^{-t/\tau} - V_{\mathrm{GB}} \end{aligned} \tag{9}$$

v_{LS1} is

$$v_{\mathrm{LS1}} = L_{\mathrm{SB1}}\frac{\mathrm{d}i_{\mathrm{DB2}}}{\mathrm{d}t}. \tag{10}$$

At t_4, the current rate of change $\mathrm{d}i_{\mathrm{DB2}}/\mathrm{d}t$ reaches the maximum, and v_{GEB} reaches the negative peak value $V_{\mathrm{GE(np)}}$, which is

$$\begin{aligned} V_{\mathrm{GE(np)}} = &\left[V_{\mathrm{GE(t3)}} - L_{\mathrm{SB1}}\max\left(\frac{\mathrm{d}i_{\mathrm{DB2}}}{\mathrm{d}t}\right) + V_{\mathrm{GB}}\right]\mathrm{e}^{-(t_4-t_3)/\tau} \\ &- V_{\mathrm{GB}}. \end{aligned} \tag{11}$$

D. Effect of Junction Temperature in t_2-t_3 Stage

At the t_2-t_3 stage, the voltage change rate $\mathrm{d}v_{\mathrm{CET}}/\mathrm{d}t$ is [37]

$$\frac{\mathrm{d}v_{\mathrm{CET}}}{\mathrm{d}t} = \frac{W_{\mathrm{N}}J_{\mathrm{C.ON}}\left(N_{\mathrm{D}} + J_{\mathrm{C,ON}}/qv_{\mathrm{sat.p}}\right)}{\varepsilon_{\mathrm{s}}p_0}. \tag{12}$$

The duration of the t_2-t_3 phase, $t_{\mathrm{v.off}}$ is

$$t_{\mathrm{v.off}} = \frac{\varepsilon_{\mathrm{s}}p_0V_{\mathrm{c}}}{W_{\mathrm{N}}J_{\mathrm{C.ON}}\left(N_{\mathrm{D}} + J_{\mathrm{C,ON}}/qv_{\mathrm{sat.p}}\right)}. \tag{13}$$

Among them, the saturated drift speed $v_{\mathrm{sat.p}}$ is less affected by temperature. p_0 is greatly affected by temperature, p_0 is [22]

$$p_0 \approx \sqrt{\frac{\mu_{\mathrm{n}}I_{\mathrm{L}}}{qAh_{\mathrm{p}}(\mu_{\mathrm{n}}+\mu_{\mathrm{p}})}}. \tag{14}$$

μ_{n}, $\mu_{\mathrm{p,}}$ and h_{p} are all affected by temperature, and can be expressed as

$$\mu_{\mathrm{n}} = 1360\left(\frac{T+273.15}{300}\right)^{-2.42} \tag{15}$$

TABLE II
KEY PARAMETERS TRENDS AGAINST OPERATION CONDITIONS CHANGE

Operation condition	dv_{CET}/dt	$\max(\lvert di_c/dt\rvert)$	$V_{GE(t3)}$	$V_{GE(np)}$
$T_j\uparrow$	$\downarrow$	$\downarrow$	$\uparrow$	$\uparrow$
$V_C\uparrow$	–	$\uparrow$	$\downarrow$	$\downarrow$
$I_L\uparrow$	$\uparrow$	$\uparrow$	$\downarrow$	$\downarrow$

$$\mu_p = 495\left(\frac{T+273.15}{300}\right)^{-2.20} \tag{16}$$

$\mu_n/(\mu_n+\mu_p)$ is approximately unaffected by temperature $h_p \propto T^{-0.5}$. Therefore, as the temperature increases, h_p decreases p_0 increases, dv_{CET}/dt decreases, and $t_{v.off}$ increases correspondingly.

According to (4), the influencing factors of $V_{GE(t3)}$ are R_{GB}, input capacitance $C_{GEB}+C_{GCB}$, dv_{CET}/dt, and $t_{v.off}$. The input capacitance is temperature-independent. The internal resistance of the IGBT module $R_{GB(in)}$ is less affected by temperature, $R_{GB(on)}$ is greater than $R_{GB(in)}$, and the gate resistance R_{GB} is affected by temperature and can be ignored. As the junction temperature increases, dv_{CET}/dt decreases, which causes $V_{GE(t3)}$ to increase. $t_{v.off}$ increases, causing $V_{GE(t3)}$ to decrease. $V_{GE(t3)}$ mainly depends on the temperature characteristics of dv_{CET}/dt, and the exponential function will weaken the influence of temperature. Therefore, as the temperature T_j increases, $V_{GE(t3)}$ increases.

In addition, with the influence of the operating point, the load current I_L increases, p_0 decreases, dv_{CET}/dt increases, and then $V_{GE(t3)}$ decreases. As the capacitor voltage V_c increases, dv_{CET}/dt remains unchanged, and $t_{v.off}$ increases, causing $V_{GE(t3)}$ to decrease. The summary of the influence of I_L, V_C, and T_j on $V_{GE(t3)}$ is shown in Table II.

E. Effect of Junction Temperature in t_3-t_5 Stage

The decrease in collector current of the IGBT Q_T is determined by the recombination of excess holes. The rising process of the current of the diode Q_B is mainly determined by the diffusion process of electrons. In the same Si-based device, the diffusion rate of electrons is faster than the recombination rate of holes in the temperature range of 25 °C to 150 °C. Therefore, the commutation process in the t_3-t_5 stage mainly depends on the change rate of the collector current of the IGBT.

The relationship between collector current density and time is [37]

$$J_C(t) = \frac{qD_{nE}N_{D,NB}p_0}{L_{nE}N_{AE}}e^{-t/\tau_{p0,NB}} = J_{C,ON}e^{-t/\tau_{p0,NB}}. \tag{17}$$

The max current rate of change is

$$\max\left(\left|\frac{dJ_C}{dt}\right|\right) = \frac{J_{C,ON}}{\tau_{p0,NB}}. \tag{18}$$

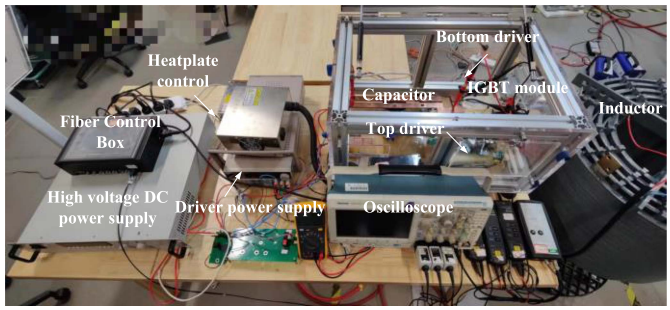


Fig. 4. Photograph of experimental platform.

$\tau_{p0,NB}$ is the hole life of the N-type base area

$$\tau_{p0,NB} = \frac{1}{\sigma_{cp}N_rE_{NB}\mu_p}. \tag{19}$$

Substitute (19) into (18) to get

$$\max\left(\left|\frac{dJ_C}{dt}\right|\right) = J_{C,ON}\sigma_{cp}N_rE_{NB}\mu_p. \tag{20}$$

According to (11), $V_{GE(np)}$ depends on $V_{GE(t3)}$ and di_{DB2}/dt. As the junction temperature T_j increases, μ_p decreases, and then $\max(|dJ_C/dt|)$ decreases. In addition, $V_{GE(t3)}$ increases, so $V_{GE(np)}$ increases. Furthermore, as the load current I_L increases, $V_{GE(t3)}$ decreases, and $J_{c,on}$ increases, causing $\max(|dJ_C/dt|)$ to increase. The combined effect makes $V_{GE(np)}$ decrease with I_L increasing. As the capacitor voltage V_C increases, $V_{GE(t3)}$ decreases, and electric field strength E_{NB} increases, causing $\max(|dJ_C/dt|)$ to increase. The combined effect makes $V_{GE(np)}$ decrease with V_C increasing. The summary of the influence of I_L, V_C, and T_j on $V_{GE(np)}$ is shown in Table II.

III. EXPERIMENTAL VALIDATION

The experimental platform is displayed in Fig. 4, which has the electrical connection coinciding with the circuit in Fig. 2. The test rig has a 1.2 mF dc capacitor C, and a 0.3 mH load inductance L_{load}. The gate resistor on the top driving circuit is 1.8 Ω, while the bottom driving circuit has separated turn-ON and turn-OFF resistors $R_{GB(on)}$ and $R_{GB(off)}$, which are 18 and 2.2Ω, respectively. Moreover, the negative gate turn-OFF voltage V_{GB} applied has 6.45 V amplitude. The experimental platform uses a heatplate to control the junction temperature of IGBTs. In order to heat up the devices evenly and thoroughly, they are closely mounted onto the heatplate and heated for sufficient time to reach thermal equilibrium. In the meanwhile, the ambient temperature is kept steady.

IGBT Module TXFF450R120MC1 is tested when the capacitor voltage is 500 V, the load current is 125 A, and the junction temperature T_j is set to 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C, respectively. The experimental results are shown in Fig. 5. The experimental results show that as the junction temperature increases, the gate voltage $V_{GE(np)}$ gradually increases. As the junction temperature T_j increases from 25 °C to 125 °C, the peak gate voltage $V_{GE(np)}$ increases from −11.22 to −9.94 V,

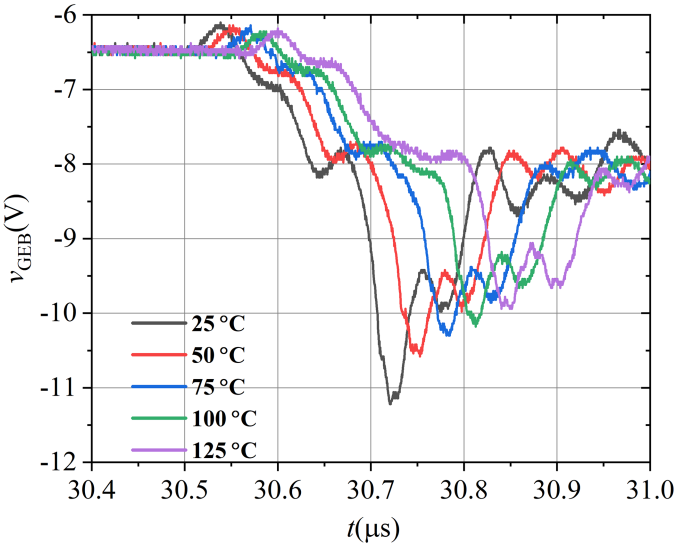


Fig. 5. Relationship of v_{GEB} with junction temperature $T_{\mathrm{j.}}$ of the TXFF450R120MC1.

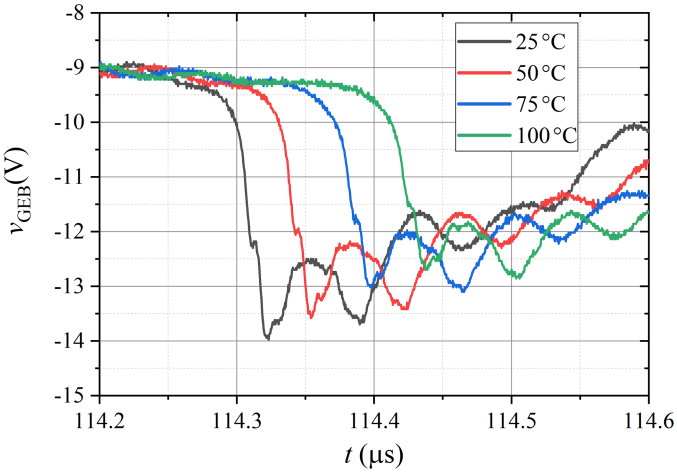


Fig. 6. Relationship of v_{GEB} with junction temperature $T_{\mathrm{j.}}$ of the FF600R17ME4.

with a relative change of 11.41%. The resultant sensitivity is 0.1203%/°C.

To further illustrate the effectiveness of the method proposed in this article, IGBT module (FF600R17ME4) of 1700 V and 800 A from Infineon have also been tested. The gate voltage v_{GEB} waveform during the turn-OFF process is shown in Fig. 6. During the experiment, the capacitor voltage is 800 V, the load current is 300 A, and the junction temperature is changed to 25 °C, 50 °C, 75 °C, and 100 °C. The gate voltage undershoot peaks $V_{\mathrm{GE(np)}}$ are −13.98, −13.58, −13.02, and −12.70 V, which are still large. The sensitivity of the calculated junction temperature monitoring is 0.1221%/°C.

A. In Suit Monitoring Circuit Discussion

The schematic diagram of gate voltage undershoot peak $V_{\mathrm{GE\ (np)}}$ measurement is shown in Fig. 7(a) and the photo of

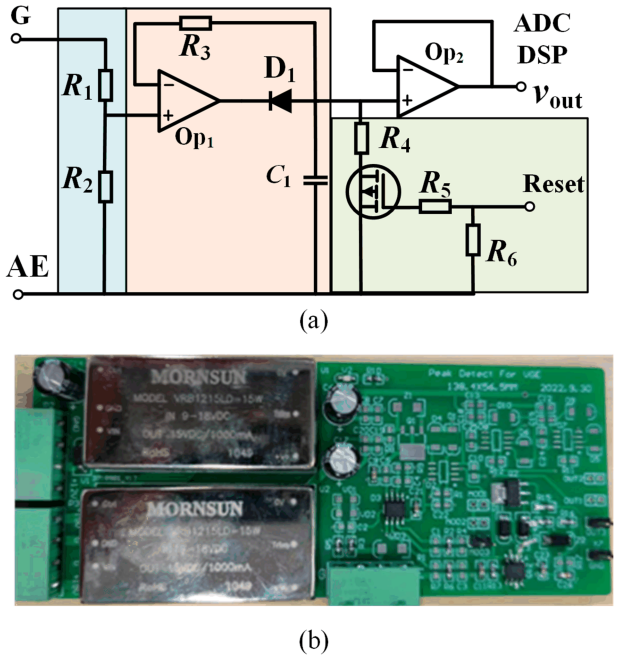


Fig. 7. (a) Schematic of the $V_{\mathrm{GE(np)}}$ measurement circuit. (b) Photo of peak detection circuit.

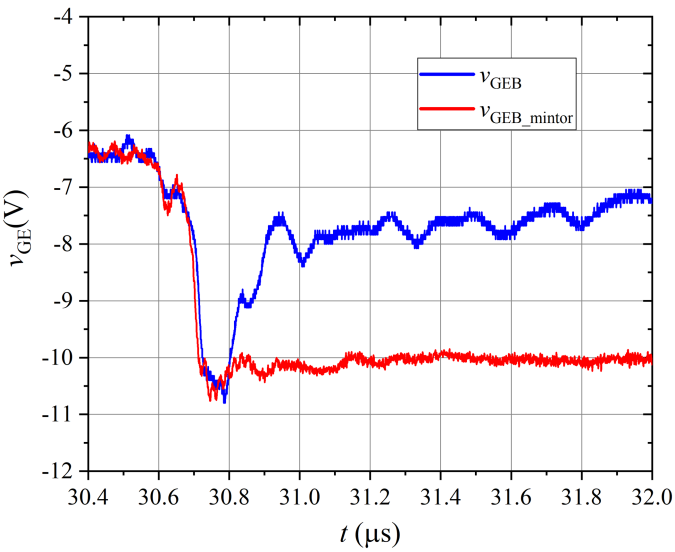


Fig. 8. Experimental results of gate voltage via the peak detection circuit.

peak detection circuit is shown in Fig. 7(b). The sampling circuit samples the peak voltage held by the capacitor without requiring a high sampling frequency, thereby reducing the hardware cost of the measurement circuit. In addition, only the operational amplifier Op_1 in the measurement circuit needs a higher bandwidth. The experimental results are shown in Fig. 8, where the blue line v_{GEB} is the experimental waveform sampled directly using the probe and oscilloscope, and the red line $v_{\mathrm{GEB\cdot mintor}}$ is the experimental waveform after the peak detection circuit. The experimental results show that the peak detection circuit can follow the rapidly changing gate voltage well and the peak is

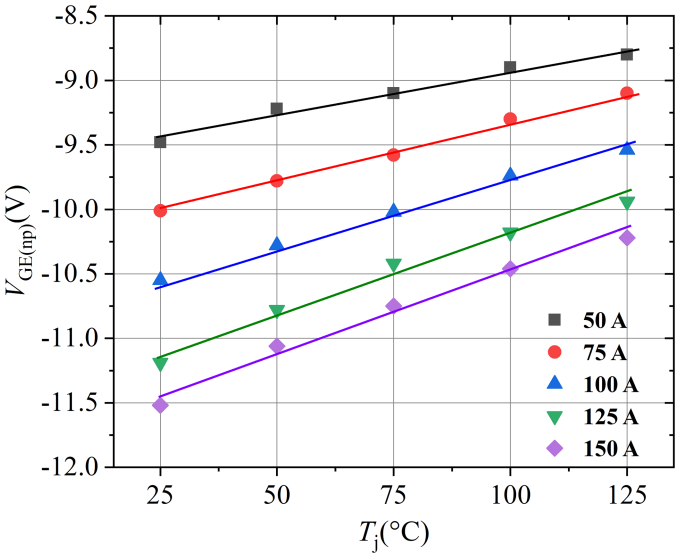


Fig. 9. Relationship of $V_{GE(np)}$ with junction temperature T_j at different load current I_L.

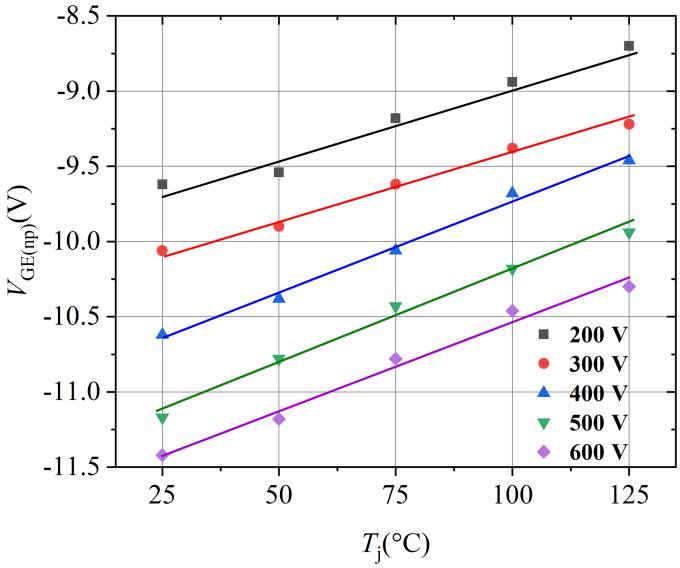


Fig. 10. Relationship of $V_{GE(np)}$ with junction temperature T_j at different capacitor voltage V_C.

well maintained. The capacitor voltage and load current can be considered constant and their measurement is in the steady-state phase (as opposed to the transient process of IGBT turn-OFF). The gate voltage undershoot peak is held by the peak detection circuit. It can be seen that none of the monitoring quantities required for junction temperature estimation need to be measured during the IGBT module turn-OFF process, avoiding the challenge of short-time window measurements.

B. Influence of the Load Current

The load current I_L is one of the important factors affecting crosstalk. With the load current I_L increasing, the collector voltage change rate dv_{GEB}/dt increases, and the current change rate di_c/dt increases, resulting in the decrease of gate voltage v_{GEB} and peak voltage $V_{GE(np)}$.

The experimental results at different junction temperatures when the load current is 50, 75, 100, 125, and 150 A are shown in Fig. 9. The capacitor voltage is 500 V, the load current is 125 A, and the junction temperature increases from 25 °C to 125 °C. As the load current increases, $V_{GE(np)}$ decreases. In the process of increasing the load current from 50 to 150 A, when the junction temperature is 25 °C, $V_{GE(np)}$ decreases from −9.48 to −11.52 V. However, when the load current is 150 A, with the T_j increasing from 25 °C to 150 °C, $V_{GE(np)}$ increases from −11.52 to −10.22 V. Therefore, in order to meet the accuracy of the junction temperature monitoring, it is necessary to measure the load current during the turn-OFF process.

In the range of junction temperature from 25 °C to 125 °C, the $V_{GE(np)}$ changes under different load currents are different. When the load current I_L is 50 A, the increase of $V_{GE(np)}$ is 0.68 V, and the temperature sensitivity is 0.0068 V/°C. When the load current I_L is 150 A, and the temperature sensitivity is 0.0130 V/°C. As the load current increases, the temperature sensitivity of $V_{GE(np)}$ increases.

C. Influence of the Capacitor Voltage

The capacitor voltage V_C is another factor that directly affects the crosstalk. As the capacitor voltage V_C increases, the dv_{GEB}/dt increases, causing the gate voltage v_{GEB} to decrease, and the negative peak voltage $V_{GE(np)}$ decreases accordingly.

At different junction temperatures T_j, the experimental results of capacitor voltages V_C of 200, 300, 400, 500, and 600 V are shown in Fig. 10. The junction temperature is gradually increased from 25 °C to 125 °C, and the load current is 125 A. As the capacitor voltage increases, $V_{GE(np)}$ increases.

In the process of increasing the capacitor voltage from 200 to 600 V, when the junction temperature is 25 °C, $V_{GE(np)}$ decreases from −9.62 to −11.53 V. However, when the capacitor voltage is 600V, with the T_j increases from 25 °C to

150 °C, $V_{GE(np)}$ increases from −11.53 to −10.30 V. A large range of capacitor voltage fluctuations will cause errors in junction temperature monitoring.

In the range of junction temperature between 25 °C and 125 °C, the $V_{GE(np)}$ variations under different capacitor voltages are different. When the capacitor voltage V_C is 200 V, the temperature sensitivity is 0.0092 V/°C. When the capacitor voltage V_C is 600 V, and the temperature sensitivity is 0.0112 V/°C. As the capacitor voltage increases, the temperature sensitivity of $V_{GE(np)}$ increases.

D. Influence of the Bond Wire Fault

The crosstalk phenomenon is a joint result of the top and bottom IGBT devices in the half-bridge circuit, which is affected by the collector voltage and current change rates of the top (i.e., active) switch and the gate loop parameters of the bottom (i.e., OFF-state) switch. The top one affects the excitation source of the equivalent circuit, while the bottom one determines circuit parameters.

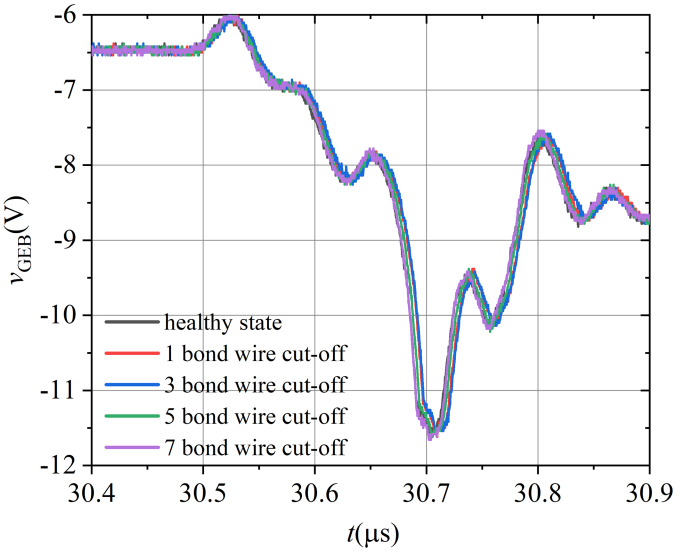


Fig. 11. Waveforms of v_{GEB} under different bond wire cutoff of the bottom IGBT switch.

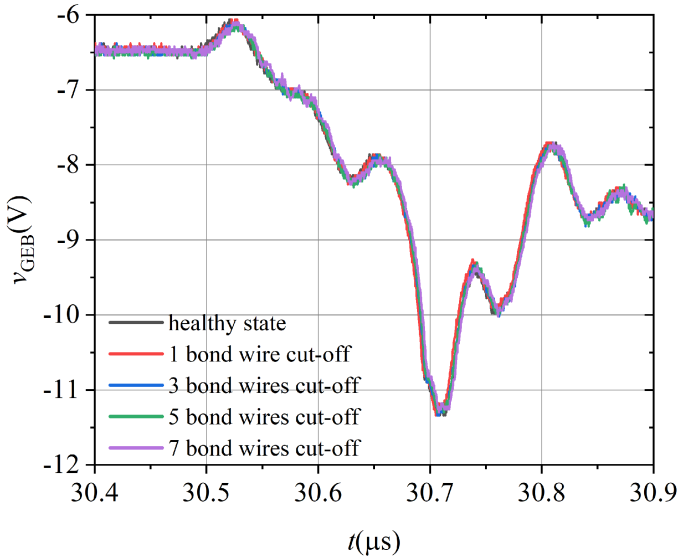


Fig. 12. Waveforms of v_{GEB} under different bond wire cutoff of the top IGBT switch.

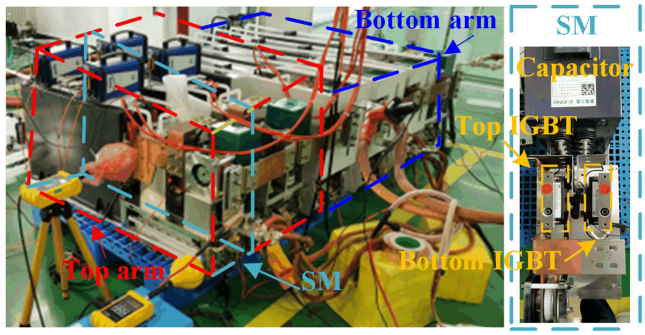
Due to the fracture of the emitter bonding wires on the IGBT chip of the bottom switch, the stray inductance of the gate loop increases. During the crosstalk, as only the charge and discharge current of the Miller capacitor flows through the IGBT chip bonding wires with a small slew rate, the increased gate loop inductance has a weak influence on the gate voltage. The experimental results of v_{GEB} at the various number bond wires cutoff on the bottom IGBT chip are shown in Fig. 11. For test conditions, the capacitor voltage is 500 V, the load current is 150 A, and the junction temperature is 25 °C. In the process of bond wires cutoff number increasing from 0 to 7, the value of $V_{\mathrm{GE(np)}}$ fluctuates less than 0.04V. The results show that the bond wire failure of the bottom IGBT has little effect on v_{GEB}.

The experimental results of the v_{GEB} at the number of top IGBT chip bonding wires cutoff is shown in Fig. 12. In the experiment, the capacitor voltage is 500 V, the load current is 125 A, and the junction temperature is 25 °C. In the process of the number of bond wire breaks from 0 to 7, the gate voltage overshoot peak value $V_{\mathrm{GE(np)}}$ fluctuates less than 0.03 V and there is no regularity in peak voltage changes.

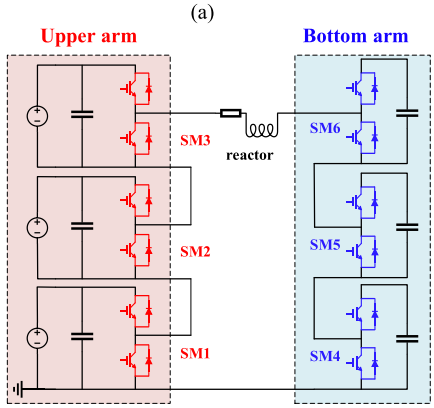
E. MMC Power Equivalent Experiment

In order to verify the proposed TSEP in the real-time operation of the MMC, experimental results are obtained from a single-phase MMC experimental platform as shown in Fig. 13. The power equivalent experiment includes the upper and lower arms of a single-phase MMC, and power is transmitted between the arms through outdoor reactors. Each bridge arm has three half-bridge SMs. The six SMs and their drive units are all dismantled from the commercial MMC of Xiamen flexible dc transmission project. Therefore, the experimental results can effectively reflect the applicability of commercial MMCs.

The voltage sources are connected in parallel with the capacitors of the upper bridge arm SMs to supplement the active power loss during the experiment. At the beginning of the experiment, the capacitors of the upper and lower bridge arm SMs are pre-charged with the same voltage through the parallel voltage source. IGBT modules are controlled with the phase-shifted carrier PWM mode, and the current is adjusted by changing the



(a)



(b)

Fig. 13. (a) Single-phase MMC experimental platform. (b) Experimental circuit schematic.

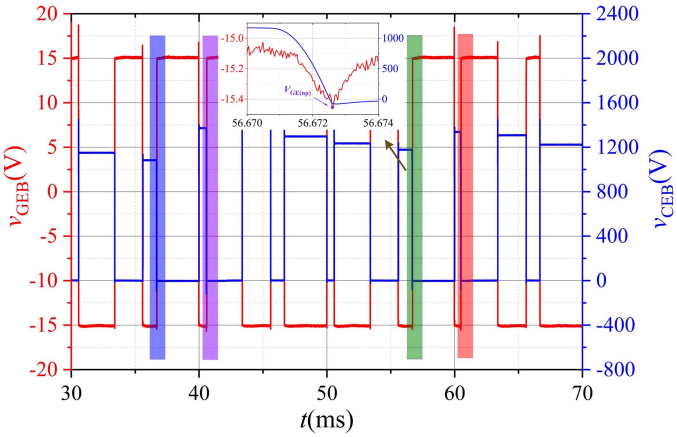


Fig. 14. Experimental results of driving signal and output voltage of SM in a single-phase MMC.

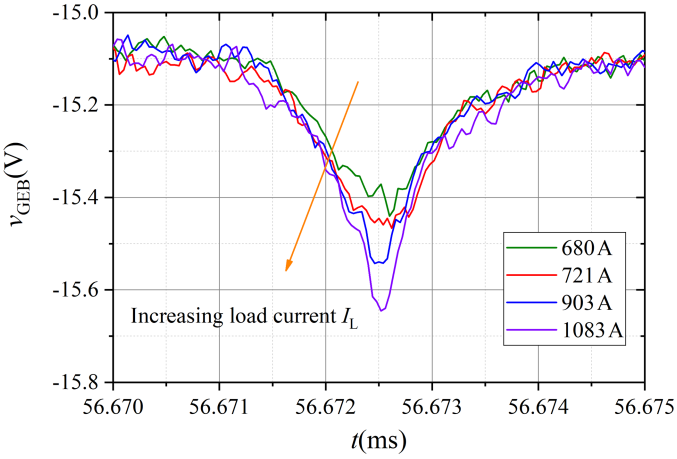


Fig. 15. Measured v_{GEB} waveforms of SM during operation of the single-phase MMC.

initial angular frequency of the triangular carrier in the PWM modulation.

The single-phase MMC power with a SM capacitor voltage of 1200 V and load current of 800 A operates at the phase-shifted carrier PWM control. The MMC submodule output voltage and its driving control are shown in Fig. 14. The V_{GEB} waveforms during the IGBT turn-OFF transitions and corresponding $V_{GE(np)}$ values are sequentially extracted from four consecutive measurement windows which are indicated by four colored boxes in Fig. 14, respectively. Since the load currents are different, $V_{GE(np)}$ values also vary, which conforms to the experimental results in Part B. All 4 consecutive turn-OFF processes are time-aligned with reference to their initial rise of gate voltages for meaningful comparison. The experimental results are shown in Fig. 15. The results show a decreasing $V_{GE(np)}$ (or a negative increase) corresponding to the increasing load current in the pulsewidth-modulation (PWM) operation, which is consistent with the double-pulse test results shown in previous sections.

The junction temperature estimation result of the IGBT module during the single-phase MMC power equivalence experiment

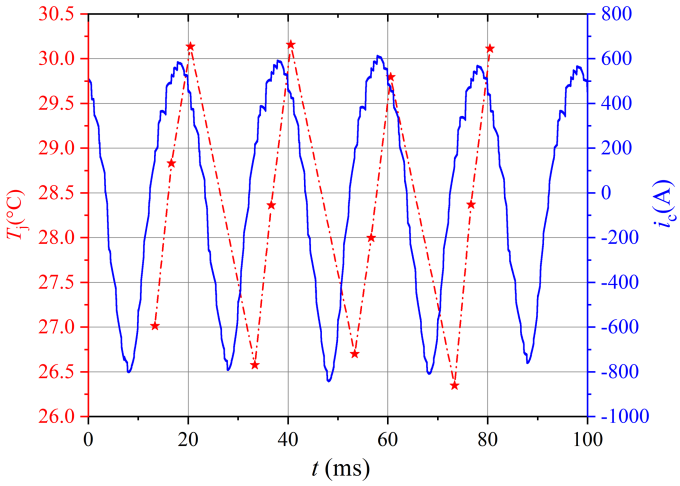


Fig. 16. Junction temperature estimation result of IGBT module in MMC power equivalence experiment.

is shown in Fig. 16. The experimental device is equipped with a water-cooling heatsink. The bottom IGBT module only conducts during the positive half-cycle of the current, so the IGBT junction temperature will cool down to about the cooling water temperature during the negative half-cycle of the current. During the equivalent power operation, the junction temperature shows a regular variation.

IV. Calibration Method for Monitoring

Like most other TSEPs, the proposed gate voltage undershoot peak value $V_{GE(np)}$ is also affected by load current, capacitor voltage, and junction temperature. In practical power electronic converter applications, the variation in operating conditions is inevitable and must be considered before applying temperature monitoring. During converters' operation, the load current changes in two timescales. 1) Due to the change of the transmission power, the effective value of the load current changes, which is a long-term change. 2) The load current follows the change of the AC side current, which is approximately in a sinusoidal curve, the IGBT device is turned OFF at different times in a cycle according to the modulation strategy, resulting in different collector currents in the turn-OFF process, which is a short-time scale change. The relationship of $V_{GE(np)}$ with different load current I_L at junction temperature T_j is shown in Fig. 17. The change of $V_{GE(np)}$ with load current can be fitted into a linear curve.

Actually, the power electronic converters usually have the capacitor voltage balance control strategies implemented in operation. For example, the modular multilevel converter (MMC) realizes the internal capacitor voltage balance by controlling the submodules to alternately conduct. The fluctuation range of capacitor voltage is usually less than 5%. The relationship of $V_{GE(np)}$ with different capacitor voltage V_C at junction temperature T_j is shown in Fig. 18. The change of $V_{GE(np)}$ with capacitor voltage V_C can be fitted into a linear curve. When the load current is 125 A and the junction temperature is 25 °C, the

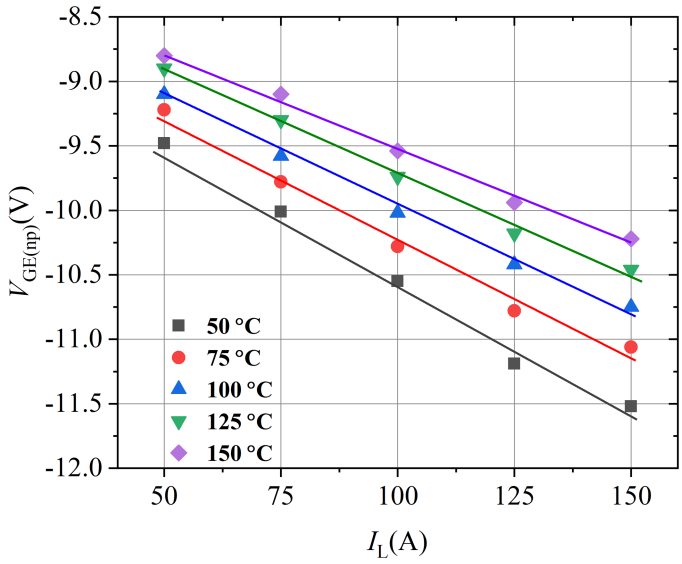


Fig. 17. Relationship of $V_{GE(np)}$ with different load current I_L at junction temperature T_j.

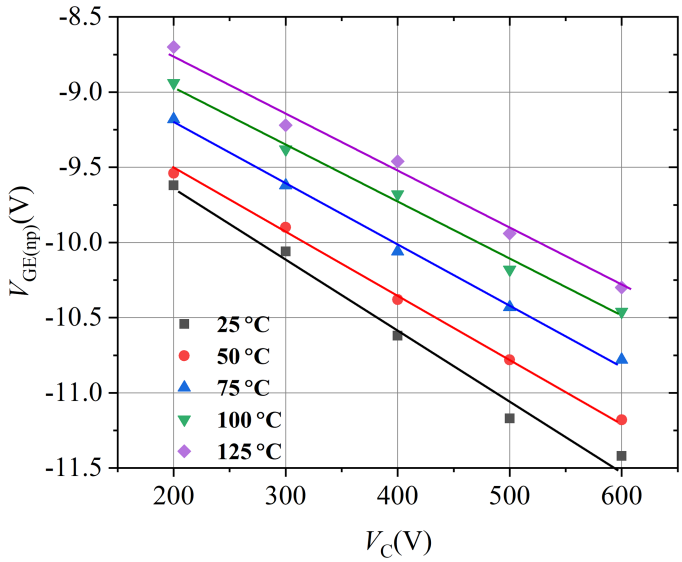


Fig. 18. Relationship of $V_{GE(np)}$ with different capacitor voltage V_C at junction temperature T_j.

capacitor voltage is reduced from 600 V by 5%. According to the calculation of the fitting result, it can be calculated that the junction temperature monitoring will interfere with 12.05 °C. In order to meet the monitoring accuracy requirements, the fluctuation of the capacitor voltage cannot be ignored.

The relationship between $V_{GE(np)}$ and load current I_L, capacitor voltage V_C, and junction temperature T_j can be fitted as a linear relationship

$$V_{GE(np)} = -0.0175I_L - 0.0041V_C + 0.0105T_j - 6.9976. \quad (21)$$

In practical applications, it is necessary to measure the $V_{GE(np)}$ of the complementary switch as well as the load current and the capacitor voltage at the same time and calculate the junction temperature using (21). At the same time, the junction temperature can also be obtained according to the method of looking up the table.

V. Conclusion

In this article, a new dynamic TSEP of $V_{GE(np)}$ for the IGBT module is proposed based on the crosstalk gate voltage v_{GEB} of the complementary IGBT switch in the half-bridge structure. It has the benefits of high sensibility, easy measuring accessibility, monotonic temperature dependence on load conditions, and independence on bond wire failures, which makes it promising for the online junction temperature estimation. Unlike some other TSEPs, the proposed TSEP is not affected by the bond wire lift-off unless the failure deteriorates to a chip open-circuit. Based on the theoretical analysis and experimental validation, the main conclusions appear as follows.

1) The proposed TSEP can effectively reflect the junction temperature. As the junction temperature increases, $V_{GE(np)}$ increases linearly. The temperature sensitivity is 0.0130 V/°C.
2) When the number of bond wire lift-off gradually rises from 1 to 7, either occurring on the top or bottom IGBT, $V_{GE(np)}$ is rarely influenced. Hence, the temperature estimation based on this method is not disturbed by the bond wire failure.
3) $V_{GE(np)}$ decreases linearly with the increase of load current and capacitor voltage. The calibration and calculation method of junction temperature is given in the article.

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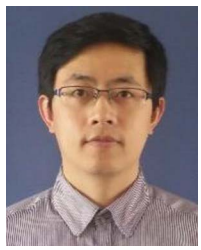

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