Design of PCB Rogowski Coil Current Sensor With Low Droop Distortion

Qianming Xu, *Member, IEEE*, Yuan Feng, *Student Member, IEEE*, Peng Guo, *Member, IEEE*, Nan Mo, Bailong Xu, Zhuo Qing, Yandong Chen, *Senior Member, IEEE*, and An Luo, *Senior Member, IEEE*

***Abstract*—Wide bandgap devices (SiC and GaN) bring the potential for a great increase in power density of power electronics, but also pose a challenge to the bandwidth of the current sensor because of the high operating frequency. Rogowski coil is suitable for high-frequency current measurement due to its characteristic of differential output, but the existing design is difficult to take into account the sensitivity and mutual inductance at the same time, and faces the inherent defect of droop distortion. This article proposes an optimal printed circuit board (PCB) Rogowski coil structure design method for SiC MOSFET power module and a novel sample-filter-hold (SFH) method to minimize droop distortion in integrators. First, the optimal parameters with multiobjective constrained optimization of the Rogowski coil current sensor for the SiC-MOSFET power module are obtained. Then, the influence factors of droop distortion of the sensor in buck converters and inverters are quantitatively analyzed for the first time and an SFH suppression method is proposed, which can eliminate the offset caused by droop distortion reliably and accurately. Finally, the experimental results demonstrate that the proposed Rogowski coil design method and the SFH method for lower droop distortion achieve better low-frequency performance compared to the commercial Rogowski coil.**

***Index Terms*—Current sensor, droop distortion, parameter optimization, printed circuit board (PCB) Rogowski coil, SiC-MOSFET.**

I. Introduction

THE wide bandgap power electronic device has been widely used in high-efficiency and high-power density applications [1], [2], [3] due to its high switching frequency and low on-state resistance. However, it also brings the following problems: the high-frequency switching characteristic of SiC-MOSFET poses a considerable challenge to the bandwidth of the current sensor. What is more serious is that the short-circuit withstand time of SiC-MOSFET is extremely low [4], and the short-circuit protection time is generally limited to be within 2 μs, which results in the faster response time requirement of the current sensor.

Traditional current measurement methods are often difficult to meet the above requirements. The shunt resistance method calculates the current by measuring the voltage of the resistor connected in series with the SiC-MOSFET, which has the advantages of simplicity, excellent linearity, and low cost [5]. However, the current needs to flow through the series resistance will inevitably generate additional losses. And since the external resistance is directly connected in series with the source of the MOSFET, effective galvanic isolation cannot be performed.

The current transformer generates a current signal proportional to the measured current on the secondary side through the coupling of the ferrite core, and then converts it into a voltage signal through the sampling resistance. Li et al. [6] proposed a silicon steel current transformer that shows a good transient performance for the current measurement of SiC-MOSFET. However, the use of magnetic cores increases the volume and weight of the sensor, and saturation can easily lead to nonlinear measurement results. The Hall current sensor can measure current of dc $\sim$ sub-MHz with good accuracy and galvanic isolation performance. Therefore, it has a wide range of applications in the current measurement of power devices [7], [8]. However, it has the disadvantages of insufficient high-frequency performance and considerable temperature drift effect [9], limiting its application for SiC-MOSFET current measurement.

In view of the high switching frequency of SiC-MOSFET and the fast rise of short-circuit current, the Rogowski coil, which is sensitive to rapidly changing current [10], has become a suitable choice for SiC-MOSFET fast switch current measurement. The sensor consists of two parts: coil and integrator. The design target of the former is mainly bandwidth, immunity, and sensitivity, whereas the latter is mainly bandwidth. Existing research on the coil focuses more on the design of high bandwidth and high immunity. Wang et al. [11] proposed a Rogowski coil current sensor with a bandwidth of up to 120 MHZ and high immunity against the adjacent conductor, but its mutual inductance is only 1.7 nH. Such low sensitivity requires the signal processing circuit to have a considerable gain. Zhang et al. [12] cleverly use the differential working state and self-integrating working

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Qianming Xu, Yandong Chen, and An Luo are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China, and also with the Zhejiang Magtron Intelligent Technology Co., Ltd., Jiaxing 314006, China (e-mail: xqm@hnu.edu.cn; yandong_chen@hnu.edu.cn; an_luo@hnu.edu.cn).

Yuan Feng, Peng Guo, Nan Mo, Bailong Xu, and Zhuo Qing are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: fengyuan@hnu.edu.cn; pengguo92@hnu.edu.cn; monan777@hnu.edu.cn; xubailong@hnu.edu.cn; zhuoqing@hnu.edu.cn).

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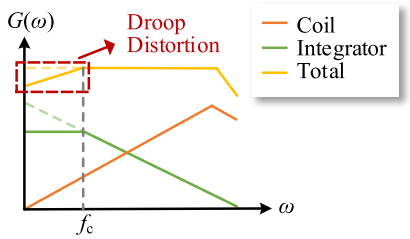

Fig. 1. Bode diagram for Rogowski coil, integrator, and total.

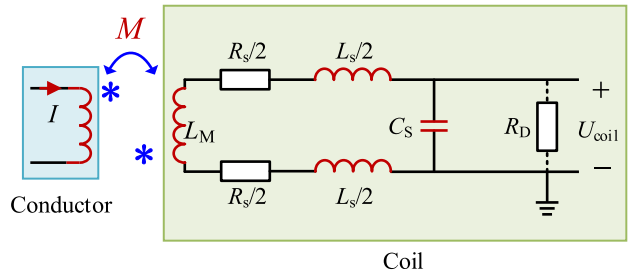

Fig. 2. Lumped stray parameter equivalent circuit of the coil.

state of the Rogowski coil simultaneously, successfully expand the bandwidth to more than 300 MHZ, and analyze the errors caused by conductor tilt and eccentricity. However, its mutual inductance is only 0.1 nH, which may reduce the signal-to-noise ratio (SNR), thus introducing larger noise. High bandwidth and high sensitivity are difficult to realize simultaneously because of the requirement of integration. Hence, the increase in bandwidth will lead to the reduction of mutual inductance, followed by the reduction of sensitivity and SNR. How to design a Rogowski coil for existing modules to achieve both the required measurement bandwidth and maximum mutual inductance is rarely studied.

On the other hand, the low gain characteristics of the coil at low-frequency conditions bring challenges to the bandwidth of the integrated circuit. To maintain high SNR and stability, the low-frequency gain of the opamp cannot be infinitely high. As is shown in Fig. 1, generally the integrator has a cutoff frequency f_c in low-frequency band, resulting in the difficulty to sense the dc component of the switch current, which is known as the "droop distortion" [13], [14]. The Bode diagram with the ideal opamp (dash line) and the practical one (solid line) is shown in Fig. 1.

To alleviate the droop distortion, the low-frequency gain of the signal process circuit for the coil must be large enough, but such a high gain will inevitably amplify the error caused by the nonideal factors (mainly the offset voltage) of the opamp. Generally, the offset voltage of precision opamps is less than 1 mV. Banik et al. [15] propose an opamp based on 90 nm process and the offset voltage is less than 50.8 μV. Furthermore, if compensation measures are taken, as described in the offset voltage can be reduced to 7.2 μV [16]. However, for the Rogowski signal process circuits with high gain, such errors are still not negligible, which will be explained in Section III-A. Therefore, the process circuit for the Rogowski coil requires a tradeoff [17] between less droop distortion and lower frequency gain. Some scholars have proposed a switch reset method [18] to avoid this tradeoff: Reset the integrator by discharging the integrating capacitor when the SiC-MOSFET is turned OFF. The principle of this method is to minimize the integration time by integrating in each switching cycle independently, thus the droop distortion is not so serious in such a short time. But this kind of forced reset must be performed when the SiC-MOSFET current completely turns to zero. In some power loops with large stray inductance or without a suitable snubber circuit, the time for turning OFF will be longer and thus the switching ringing may not be completely attenuated within one cycle, making it difficult to reliably reset [19]. Furthermore, Kim et al. [20] proposed a systematic approach to compensate for offset voltage by looking up a two-dimensional offset table when microcontroller unit (MCU) startups. However, the adoption of high-speed analog-to-digital converters (ADCs) and field-programmable gate array adds complexity to sensor design. To accurately obtain offset at arbitrary duty cycle and switching frequency, a large amount of computing and storage space is unavoidable.

The rest of the article is structured as follows. Section II first establishes the mathematical model of the mutual inductance of the Rogowski coil differentiator based on the law of electromagnetic induction, so as to choose a suitable structure of the coil and finally figure out the optimal parameters of the coil. Then, in Section III, the signal process circuit is designed by following steps: first, a noninverting integrating circuit is used to integrate the output by the coil. Then, the novel sample-filter-hold (SFH) method is used to provide a reliable reset regardless of whether the switching ringing ends, which not only effectively suppresses the droop distortion but also reduces the error caused by the nonideal factor of the opamp. Eventually, the rebuild of the fast switch current waveform with low distortion and low delay is finally realized. In Section IV, the prototype based on a SiC power module is built and the effectiveness of the proposed printed circuit board (PCB) Rogowski coil current sensor is proved by experiments. Finally, Section V concludes the article.

II. Design of the PCB Rogowski Coil

A. Basic Concept

As is illustrated in Fig. 2, the lumped stray parameter equivalent circuit [21] of Rogowski coil consists of the coil magnetic inductance L_M, coil leakage inductance L_S, coil resistance R_S, and terminal capacitance C_S. In order to eliminate the spikes of gain when resonates, a damping resistor R_D is often added to the terminal. In order to sense the high-frequency ringing current of SiC-MOSFET, stray parameters (including R_s, L_s, and C_s) of the coil are supposed to be small enough, so the number of turns and size of the coil should not be too large. In addition, in some cases, the coil is supposed to be embedded in the power module. Under size limits, the gain of a PCB coil is usually less than 10 nH [20], [22], [23], [24], so the larger M is, the larger sensitivity it has and the smaller gain of integrator it needs, which can bring larger SNR. Meanwhile, the bandwidth of the sensor is also an important design objective. Neglecting the trivial coil resistance R_S, the bandwidth of the coil is determined by

$$f_{BW} = \frac{1}{2\pi\sqrt{L_2 C_s}} \tag{1}$$

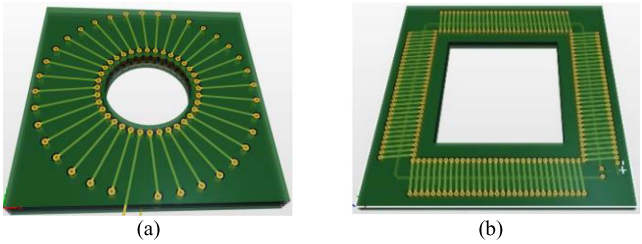

Fig. 3. Structure of (a) circular coil and (b) rectangular coil.

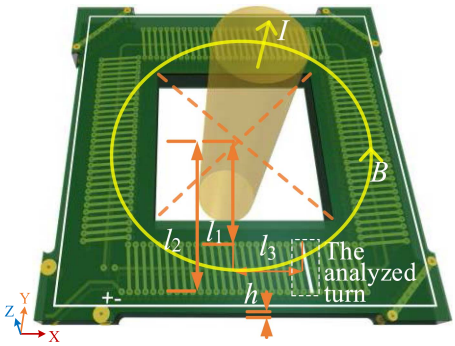

Fig. 4. Magnetic flux of one turn at a certain position.

$$L_2 = L_{\mathrm{M}} + L_{\mathrm{S}} \tag{2}$$

where L_2 and f_{BW} are the secondary inductance and the upper frequency limit of the coil, respectively. It should be pointed out that the terminal capacitance C_{S} and the secondary inductance L_2 are stray parameters that cannot be calculated easily when designed, so the design flow should be divided into two steps: 1) find the factors affecting mutual inductance and determine the structure parameters preliminarily, including inner diameter, outer diameter, height, etc.; 2) figure out the bandwidth using finite-element method (FEM) software to adjust the structure parameters eventually.

B. Structure Parameter Optimization Design

The switching ringing frequency of SiC-MOSFET f_{ringing} is mainly effected by the switching loop inductance L_{loop}, gate–drain capacitance C_{GD}, and equivalent resistance R_{eq} [19]. In most conditions, f_{ringing} ranges from 1 to 30 MHz [10], [11], [12], [13], [14]. Assuming the designed bandwidth $BW_{\mathrm{goal}} =$ 30 MHz. The design procedure is shown as follows. Generally, there are two kinds of structure of Rogowski coils: rectangle and circular (shown in Fig. 3). For both structures, the heights of the coil are much smaller than the heights of the current carrying conductor passing through it, so is reasonable to consider the conductor to be of infinite length. Moreover, because the PCB coils are tightly arranged, each turn can be approximately considered a rectangle. As is shown in Fig. 4, take the rectangle coil as an example and take a turn at a certain position to analyze, the magnetic flux of which (noted as ϕ_1) can be expressed as

$$\phi_1 = \int_{l_1}^{l_2} d\phi = \int_{l_1}^{l_2} \frac{\mu_0 h I}{2\pi} \times \frac{ldl}{l^2 + l_3^2} = \frac{\mu_0 h I}{4\pi} \ln \frac{l_2^2 + l_3^2}{l_1^2 + l_3^2} \tag{3}$$

where l_1 is the y distance from conductor center to turn inside (also denoted as the inner radius of the coil), l_2 is the y distance from conductor center to line turn outside (also denoted as the outer radius of the coil), l_3 is the x distance from conductor center to line turn, and h is the height of the coil.

In order to achieve the goal of maximum sensitivity, the mutual inductance of these two structures within the same space limit is compared in the following. Mutual inductance of circular coils M_{cir} can be expressed as

$$M_{\mathrm{cir}}(l_1) = \frac{u_0}{2\pi} n_{\mathrm{cir}} h \ln\left(\frac{l_2}{l_1}\right) \tag{4}$$

$$n_{\mathrm{cir}} = \mathrm{floor}\left[\pi / \arcsin\left(\frac{c}{2l_1}\right)\right] \tag{5}$$

where n_{cir} is the number of turns, c is the clearance of turns, and floor is the round down function. It is not difficult to find that mutual inductance M will reach the maximum when the outer radius l_2 and the height h reach their maximum and c reaches its minimum. The number of turns n and the inner radius l_1 are mutually dependent according to (5). Therefore, the key is to find the optimal value of the inner radius l_1.

Relatively, the mutual inductance of the rectangular coil M_{rect} can be expressed as follows:

$$M_{\mathrm{rect}}(l_1) = \frac{\psi}{I} = 4 \sum_{i=0}^{n_{\mathrm{rect}}/4} \frac{\mu_0 h}{4\pi} \ln \frac{l_2^2 + (-l_1 + ci)^2}{l_1^2 + (-l_1 + ci)^2} \tag{6}$$

$$n_{\mathrm{rect}} = \mathrm{floor}\left(\frac{2l}{c}\right). \tag{7}$$

Limited by space size, assuming that $l_{1.\min} = 7.5$ mm, $c_{\min} = 0.254$ mm, and $h_{\max} = 1.6$ mm, the multiobjective optimal problem turns to be

$$\begin{aligned} \max: & \begin{cases} M(l_1) \\ BW(l_1) \end{cases} \\ \text{s.t.} \quad & l_1 > l_{1.\min}, BW(l_1) > BW_{\mathrm{goal}}, l_2 = l_{2.\max} \\ & c = c_{\min}, h = h_{\max}. \end{aligned} \tag{8}$$

Due to the number of turns N must be an integer, both functions $M_{\mathrm{cir}}(l_1)$ and $M_{\mathrm{rect}}(l_1)$ are rough. This means it is hard to find the maximum of M by using the derivation method. More importantly, the bandwidth of the coil must be obtained through FEA because the stray parameters are hard to be mathematically modeled, so it is difficult to find an analytical solution but a numerical solution. Fig. 5 shows the functions $M(l_1)$ with different l_2 and different shapes of coil (rectangular or circular). It can be seen that without constraints of bandwidth and l_1, the maximal M is achieved when $l_1 = 2.8$ mm ($0.35l_2$), 3.4 mm ($0.33l_2$), and 4.6 mm ($0.33l_2$) with $l_2 = 8$, 10.4, and 12 mm, respectively. In this article, l_2 is set to 10.4 mm according to the power module on which the coil is installed.

It can be seen that the mutual inductances of the rectangular coil are larger than those of the circular coil under the same limiting factors, so finally the coil shape is chosen to be rectangular. Meanwhile, for mutual inductance, when $l_1 > l_{1.\,\mathrm{turn}}$, M increases for more turns can be arranged in the coil. On

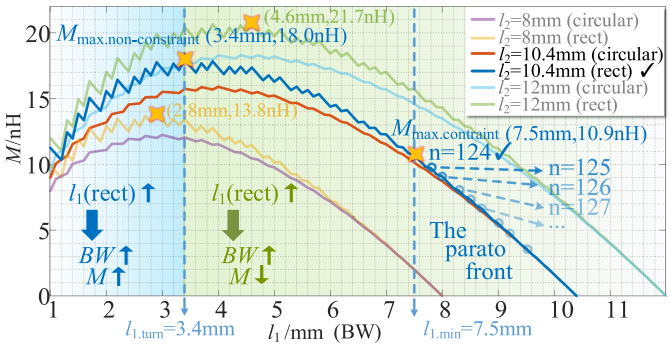

Fig. 5. Numerical sweeping result of mutual inductance.

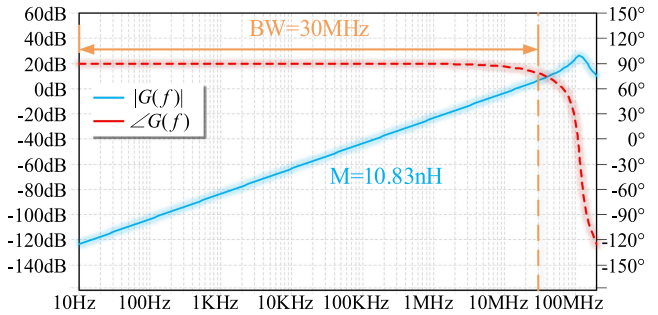

Fig. 6. Bode diagram of the designed Rogowski coil.

TABLE I
STRUCTURE PARAMETERS OF THE DESIGNED ROGOWSKI COIL

n (turns)	l_1 (mm)	l_2 (mm)	*h* (mm)	*c* (mm)
124	7.5	10.4	1.6	0.254

the contrary, when $l_1 < l_{1.\,\mathrm{turn}}$, M decreases for the increasing distance between conductor and coil, which decreases the flux. For bandwidth, it is always positively associated with l_1 in that shorter winding brings lower R_s, L_s, and C_s in Fig. 2. To achieve the maximum M, l_1, and M are set to 7.5 mm and 10.9 nH, respectively. Then, the bandwidth of the coil is figured out by FEA to check whether it meets the requirement.

In order to calculate the bandwidth, the stray parameters were extracted by using the FEM software Ansys Q3D. The results showed that $L_2 = 1808$ nH, $C_S = 44$ pF and $M = 10.83$ nH, which verifies the mutual inductance calculated by (6) within an error of 1%. To alleviate the peak caused by *LC* resonance, a damping resistance R_D (shown in Fig. 2) of 2 kΩ is added to the terminal of the coil. Finally, the Bode diagram is figured out using LTspice simulation, which illustrated that the coil has good frequency response at frequencies below 30 MHz, which meets the design requirement. Finally, to improve the noise immunity of the coil, two returning wires [25] are added to the coil. Fig. 6 and Table I show the frequency responses and the structure parameters of the designed coil, respectively.

In some conditions where the ringing frequency or low current is low, the mutual induction is supposed to be as large as possible,

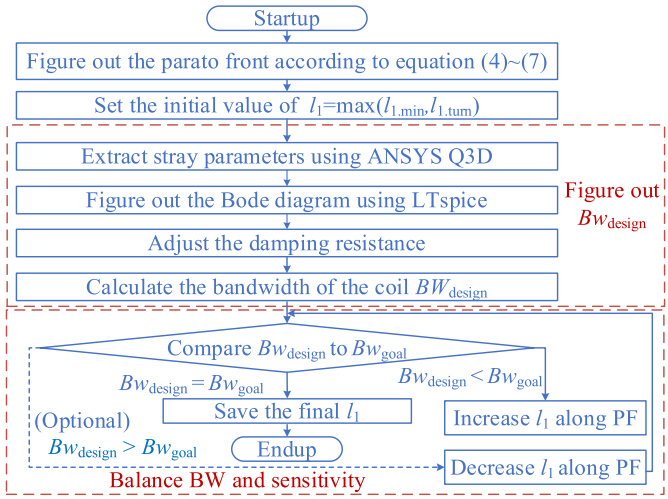

Fig. 7. General steps to maximize the *M* value.

whereas the bandwidth is less important. To achieve a larger mutual inductance, the general optimization steps are shown in Fig. 7, where BW_{design} is the bandwidth of the designed coil. Due to l_1 always having a positive correlation with the bandwidth, the Pareto front can be easily found in Fig. 5, so only few times of FEA simulations need to be performed. Eventually, surplus bandwidth will be converted to sensitivity through the multiobjective optimization.

III. DESIGN OF THE SIGNAL PROCESS CIRCUIT

Section II introduces the design process of high sensitivity coil, then a signal process circuit is required to rebuild the current waveform. In this section, the common problem existing in the Rogowski coil integral circuit: droop distortion is analyzed mathematically. Then, an SFH offset calibrating method is proposed, which is proven to have a good effect against droop distortion in various working conditions.

A. Droop Distortion Characteristic Analysis

Section II suggests that the Rogowski coil serves as an ideal differential circuit at low frequencies whose transfer function is $G_{\mathrm{coil}}(s) = sM$, resulting in the gain being extremely low in low frequencies. Therefore, the gain characteristic of the Rogowski coil makes the following requirement for the integrator: in order to rebuild the current completely, the transfer function of integrator is supposed to be $G_{\mathrm{int}}(s) = K/s$, where K is the gain factor. Limited by the size of the sensor, M is usually less than 10 nH, so K is supposed to be large or the sensitivity of the sensor will be too low. A large K means the gain of G_{int} is extremely large at frequencies approaching zero. For instance, to achieve a sensitivity of 1 mV/A for a coil with the mutual inductance of 10 nH, the integrator needs to achieve a gain of 10 000 at 10 Hz, which will bring a poor SNR ratio and even the saturation of the opamp. In fact, for purpose of limiting the error caused by a too high gain in low frequency, poles are often added to the transfer function to limit its low-frequency gain as it is shown in Fig. 1, leading to the droop distortion and making it more difficult to

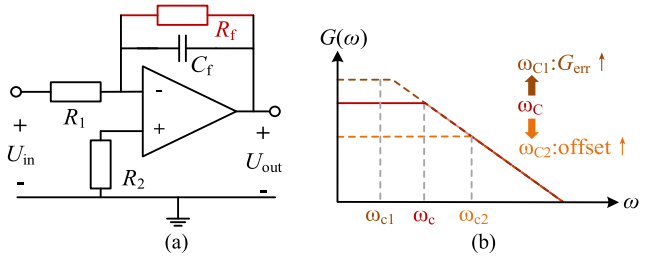

Fig. 8. Typical integrating circuit for (a) Rogowski coil and (b) its Bode diagram.

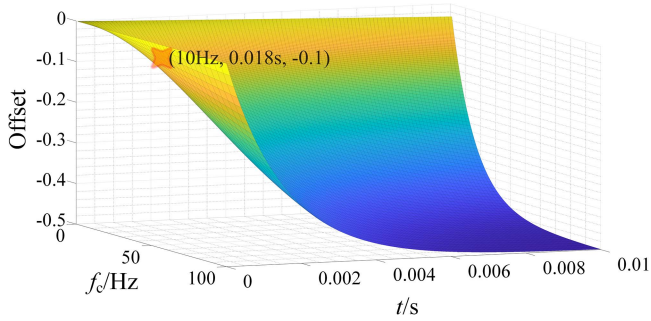

Fig. 9. Offset waveform for different f_c of buck converters.

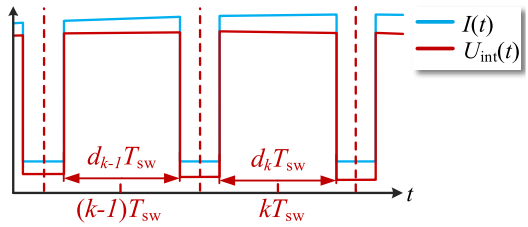

Fig. 10. Current measured and integrator output in the kth switching periods.

rebuild the signal. A typical simple practical integrating circuit [26] and its Bode diagram (solid line) are shown in Fig. 8.

Obviously, the transfer function of output voltage $U_{\rm int}$ and input voltage $U_{\rm in}$ can be expressed as

$$G_{\rm int}(s) = -\frac{1}{R_1C_{\rm f}}\frac{1}{s+1/R_{\rm f}C_{\rm f}} = \frac{K}{s+2\pi f_{\rm c}}. \tag{9}$$

The gain factor K can be adjusted by R_1, $C_{\rm f}$, and the cutoff frequency $f_{\rm c}$ by $R_{\rm f}$. Among them, $R_{\rm f}$ is the most critical because the pole $2\pi f_{\rm C}$ determines the severity of droop distortion caused by the absence of low-frequency components, which has a bad influence on switching current measurement in buck converter and inverter. The influence is quantitatively analyzed as follows. First, for buck converter, assuming a normalized pulsewidth modulation (PWM) current waveform (range from 0 to 1) whose period and duty cycle are T and d, respectively. It is reasonable to neglect high-frequency components (switch ringing) of the current waveform in that Rogowski transducer is very sensitive to them. Then, the s-domain expression of the switching current is

$$I(s) = \frac{1}{s}\frac{e^{-dTs}-1}{e^{-Ts}-1}. \tag{10}$$

Furthermore, the output of the integrator is given by

$$U_{\rm int}(s) = G_{\rm coil}(s)G_{\rm int}(s)I(s) = sM\frac{K}{s+2\pi f_{\rm c}}\frac{1}{s}\frac{e^{-dTs}-1}{e^{-Ts}-1}$$
$$= \frac{KM\left(e^{-dTs}-1\right)}{(s+2\pi f)\left(e^{-Ts}-1\right)}. \tag{11}$$

In order to quantify the droop distortion, the time-domain expression of the output of the integrator when SiC-MOSFET turned OFF (ideally equals to 0) is obtained by (11), which is given by

$$u_{\rm int}(t) = L^{-1}\left[U_{\rm int}(s)\right] = \frac{1-e^{\omega_{\rm c}dT}}{1-e^{\omega_{\rm c}T}}\left[e^{-\omega_{\rm c}t} - e^{-\omega_{\rm c}(t-kT)}\right] \tag{12}$$

with

$$(t-kT > dT).$$

It is noted that the cutoff angular frequency $\omega_{\rm c} = 2\pi f_{\rm c}$ and $k = \text{floor}(t/T)$. To transduce switching harmonic, $\omega_{\rm c} \ll (1/T)$ is always the case. Hence, (12) can be simplified as

$$u_{\rm int}(t) = d\left(e^{-\omega_{\rm c}t}-1\right) \qquad (t-kT > dT). \tag{13}$$

From (13), it can be seen that offset will accumulate over time. Fig. 9 shows the offset waveform for different $f_{\rm c}$. It is apparent that $f_{\rm c}$ cannot be too large in that the offset will rapidly increase to 0.5 meaning that the dc component has a completely lost for a normalized square wave. When $f_{\rm c}$ >10 Hz, it only takes 1.8 ms or less for the offset to accumulate to 10%.

Second, the similar problem also exists in inverters. Assuming the output current is a normalized sinusoidal wave whose fundamental frequency and phase are $f_{\rm fund}$ and φ, respectively, with the switching frequency and modulation ratio are $f_{\rm sw}$ and a, respectively. The output of the integrator $U_{\rm int}$ can be expressed as (13), where $d_{\rm k}$ is the duty in the kth switching period (as shown in Fig. 10)

$$U_{\rm int}(t) = \begin{cases} U_{\rm int}\left[(k-0.5d_k)T_{\rm sw}\right]e_k(t) + \frac{dI(t)}{dt}T_{\rm c}\left[1-e_k(t)\right] \\ \text{when} \quad (k-0.5d_k)T_{\rm sw} < t < (k+0.5d_k)T_{\rm sw} \\ U_{\rm int}\left[(k+0.5d_k)T_{\rm sw}\right]e_k(t) \\ \text{when} \quad (k+0.5d_k)T_{\rm sw} < t < (k+1.5d_k)T_{\rm sw} \end{cases} \tag{14}$$

with

$$e_k(t) = e^{-\frac{t-(k-1)T_{\rm sw}}{T_{\rm c}}}, d_k = \frac{(1+a)\sin\left(2\pi f_{\rm fund}kT_{\rm sw}\right)}{2}$$
$$k \in Z, 1 \le k \le \frac{f_{\rm sw}}{f_{\rm fund}}.$$

Due to $f_{\rm sw} \gg f_{\rm fund}$, it is reasonable to linearize the current in one switching period, so when $f_{\rm c}$ varies, the offset waveform is shown as Fig. 11. Compared to the buck converter, the offset of inverters is not a constant in steady state, which suggests that not only the droop distortion will bring to overall waveform, distortion in each fundamental period will also appear, causing harmonic components. More seriously, the offset is also

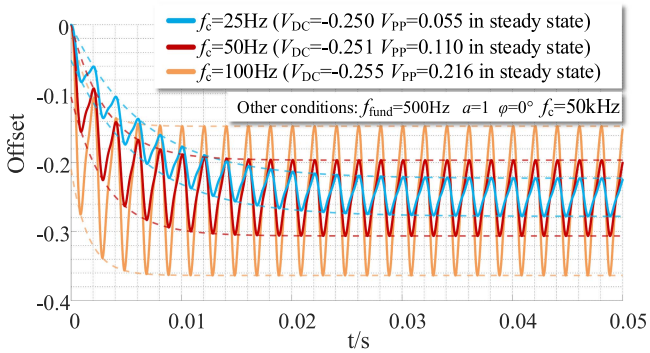

Fig. 11. Offset waveform for different f_C of inverters.

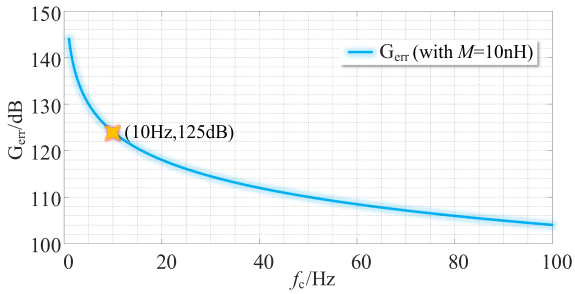

Fig. 12. Gain of error caused by the offset voltage.

impacted by f_{fund}, f_{sw}, a, and φ, making it hard to compensate for the offset accurately in real time, but it can be estimated using numerical methods. Note as the peak-to-peak value average value to offset waveform in steady state, respectively. Then, $V_{\text{pp.offset}}$ and $V_{\text{dc.offset}}$ can be approximately expressed as follows when $f_c << f_{\text{fund}}$, which is necessary and can be satisfied when designing:

$$V_{\text{pp.offset}} = \frac{11 f_c}{f_{\text{fund}}} \tag{15}$$

$$V_{\text{DC.offset}} = \frac{m_a \cos\varphi}{4}. \tag{16}$$

According to the analysis above, it is complex to calculate the offset waveform, the only way to reduce the droop distortion is to reduce f_c. However, the decrease of f_c enlarges the low-frequency gain, which increases the error caused by the nonideal factors of the opamp, and also leads to a decrease in stability. The reason is as follows.

In the practical integrating circuit [27], the influence of the opamp's offset voltage and offset current is equivalent to adding an equivalent input voltage V'_1 at the noninverting input end, which can be expressed as

$$V'_1(s) = V_{\text{IO}}(s) + I_{\text{IO}}(s)R. \tag{17}$$

After amplification by the circuit, the error voltage V'_{O} at the output can be expressed as

$$V'_{\text{O}}(s) = \frac{KV'_1(s)}{s + \omega_c}. \tag{18}$$

Since the offset current is often very small and its influence can be limited by adjusting R_2, the output error V'_{O} can be simplified to

$$V'_{\text{O}} = \frac{KV_{\text{IO}}}{\omega_c}. \tag{19}$$

Converting this to a measurement of current, the absolute error of the current I_o' can be expressed as

$$V'_{\text{O}} = \frac{V'_{\text{O}}}{KM} = \frac{V_{\text{IO}}}{M\omega_c}. \tag{20}$$

Equation (20) illustrated that the error caused by the offset voltage of the opamp is amplified $1/(M\omega_c)$ times (noted as G_{err}). Due to the size limitation of the SiC-MOSFET power module and the requirements of the bandwidth, the mutual inductance of the coil should not be too large. Assuming that $M = 10$ nH, then the function relationship between the gain of error and the cutoff frequency f_c is shown in Fig. 12.

Similarly, taking 10 Hz as the boundary, it can be seen that when fc <10 Hz, the dc gain will exceed 125 dB, suggesting that even if the V_O' is as small as 1 μV, it will bring a considerable current error of 1.78 A. More importantly, the integrator shown in Fig. 8 represents a general case, suggesting that it is difficult to improve the integrating circuit to reduce offset and G_{err} simultaneously, which is reflected in the Bode diagram in Fig. 8(b) (dash line). The dilemma that droop distortion and noise of the opamp cannot be suppressed to an acceptable level simultaneously makes it hard to determine f_c. Hence, it is necessary to adopt an additional distortion suppressing circuit, which is proposed as follows.

B. Proposed SFH Method to Reduce Droop Distortion

From the analysis of Section III-A, it can be seen that the effect of droop distortion only causes loss of the low frequency component, which refers to the dc component in a switching period. Hence, it is not necessary to reset the output completely during the off time, but only to reset the lost dc component. Meanwhile, the dc components of the current drop rapidly to zero after the SiC-MOSFET is turned OFF, thus ensuring that the reset can be performed right after turned OFF, rather than after the fully attenuation of the turn-OFF ringing.

Therefore, the problem turns to how to quickly and accurately extract and reset the dc component. Before that, it is necessary to choose a suitable integrator. Since the droop distortion can be compensated, an integrator with strong low-frequency gain suppression should be selected to improve the accuracy. Ray and Davis [28] propose an integrator circuit using T-type filtering as shown in Fig. 13(a). The Bode diagram is shown in Fig. 13(b), indicating that the circuit has excellent performance for low-frequency gain G_{LF} and is more difficult to saturate, so this circuit is adopted. The gain factor K and dc gain are set to 4×10^6 and 35 dB, respectively, to limit G_{err}.

Even though the decrease of G_{err} brings the increase of G_{LF}, suggesting this circuit has more serious distortion problems, it can be compensated by the proposed SFH method, whose schematic diagram is shown in Fig. 14.

The whole processing circuit is divided into following three parts.

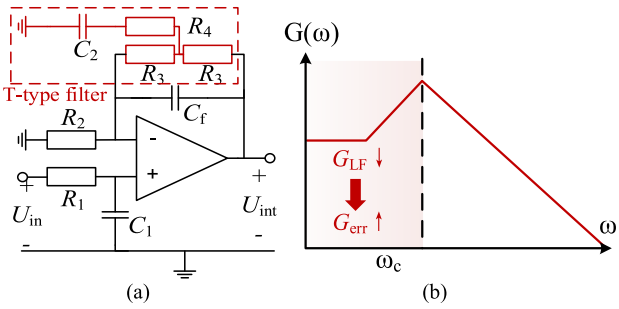

Fig. 13. (a) Integrating circuit with T-type filter and (b) its Bode diagram.

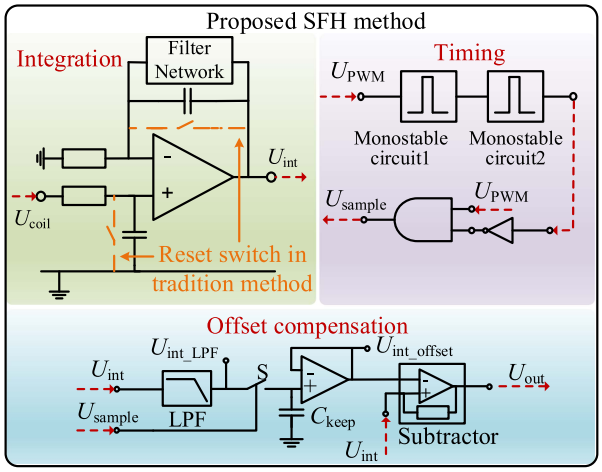

Fig. 14. Proposed SFH circuit.

1) The integrator shown in Fig. 14.
2) The offset compensation circuit to calculate, save, and eventually compensate for the output offset.
3) The timing circuit to activate the offset compensation circuit at an appropriate time.

How it works is explained in the following.

First, in the offset compensation circuit, the original integrating output $U_{\rm int}$ is connected to a low-pass filter (LPF). The filter circuit adopts a Butterworth type active LPF circuit, which has a balance of amplitude-frequency characteristics and transient response performance. In order to make a tradeoff of the damping factor of the switching current ringing and the delay of the filter, set

$$f_{\rm c} = \left(\frac{1}{6} \sim \frac{1}{5}\right) f_{\rm ringing} \tag{21}$$

where $f_{\rm ringing}$ and $f_{\rm c}$ are the switching ringing frequency of the current and the cutoff frequency of the filter, respectively. In order to save the dc component, the output of the filter is connected to a ceramic capacitor with a small leakage current through a high-speed analog S switch, and then a follower with high input impedance is used to output the offset voltage kept in the capacitor $U_{\rm int\_offset}$. Finally, a subtract circuit is applied to compensate for the offset. In order to ensure the correct reset occasion, the timing circuit in Fig. 14 is used to activate the above offset compensation circuit. How it works is explained in the following.

According to Section III, the offset compensation must be performed when the MOSFET is completely turned OFF, so the period of monostable circuit 1 (noted as Δt_1) is set equal to the delay time from the falling edge of the PWM to the time when the SiC-MOSFET is completely turn-OFF, which can be looked up in the datasheet. Then, the period of monostable circuit 2 (noted as Δt_2) is set equal to the time of several current ringing period. When the falling edge of the MOSFET driving signal $U_{\rm PWM}$ is detected, the monostable circuit 1 is triggered to wait for the SiC-MOSFET completely turned OFF. After Δt_1, the monostable circuit 2 is triggered and $U_{\rm sample}$ turns high. Then, the offset compensation circuit is activated so $U_{\rm int\_offset}$ updates and is kept in the capacitor $C_{\rm keep}$. The or gate ensures that the offset compensation circuit is enabled only when $U_{\rm PWM}$ is low, which ensures that the sampling of $U_{\rm int}$ is only performed when SiC-MOSFET is turned OFF so as to keep the correct $U_{\rm int\_offset}$ of this switch cycle until the next switch cycle.

In summary, the overall workflow is as follows.

1) Filtering: Filter the high-frequency ringing in $U_{\rm int}$ through the LPF thus to track the offset in $U_{\rm int}$ in real time.
2) Sampling: Sample $U_{\rm int\_LPF}$ for Δt_2 by turning on the analog switches S Δt_1 after the SiC-MOSFET turned OFF to obtain $U_{\rm int\_offset}$. Δt_1 and Δt_2 are set by the timing circuit in Fig. 14.
3) Holding: After sampling, turn OFF the analog switches S, so $U_{\rm int\_offset}$ is held in the capacitor $C_{\rm keep}$.
4) Compensation: Subtract $U_{\rm int\_offset}$ from $U_{\rm int}$ through the subtraction circuit in real time, and finally compensate for the offset.

Compared to the traditional switch reset [21], offset can be compensated through the LPF before the end of ringing. When the off time is extremely short, the increment of $U_{\rm int\_offset}$ can still be added to $C_{\rm keep}$ quickly due to the low delay of the LPF. However, the traditional switch reset method needs to reset the integrator after the end of ringing, which is difficult to be implemented during a short off time period. The reset during the ringing will cause inevitable distortion. Hence, the supposed SFH method can compensate for the offset more reliably than the traditional method. A comparison of the waveforms of the proposed SFH method, the traditional switching reset method, and the output of the integrator in a short off time period is shown in Fig. 15, where $U_{\rm int\_LPF}$ is the output of the LPF, $U_{\rm sample}$ is the control signal for sampling, $U_{\rm reset}$ is the control signal for resetting, and $U_{\rm out(reset)}$ is the output of the integrator with the reset switch.

In addition, although the dc component is subtracted from the integrator, not removed, it does not mean the integrator will saturate over time in that the SFH circuit compensates for the offset so as to compensate for the dc component of the integrator $U_{\rm int\_DC}$, which attenuates overtime, not accumulates. Therefore, dc component in $U_{\rm out}$ is always larger than $U_{\rm int\_DC}$. Within the measuring range, $U_{\rm out}$ does not saturate, so does not $U_{\rm int}$. Moreover, the offset only updates in a short time after turned OFF, so it has no limitation for the purposed compensation

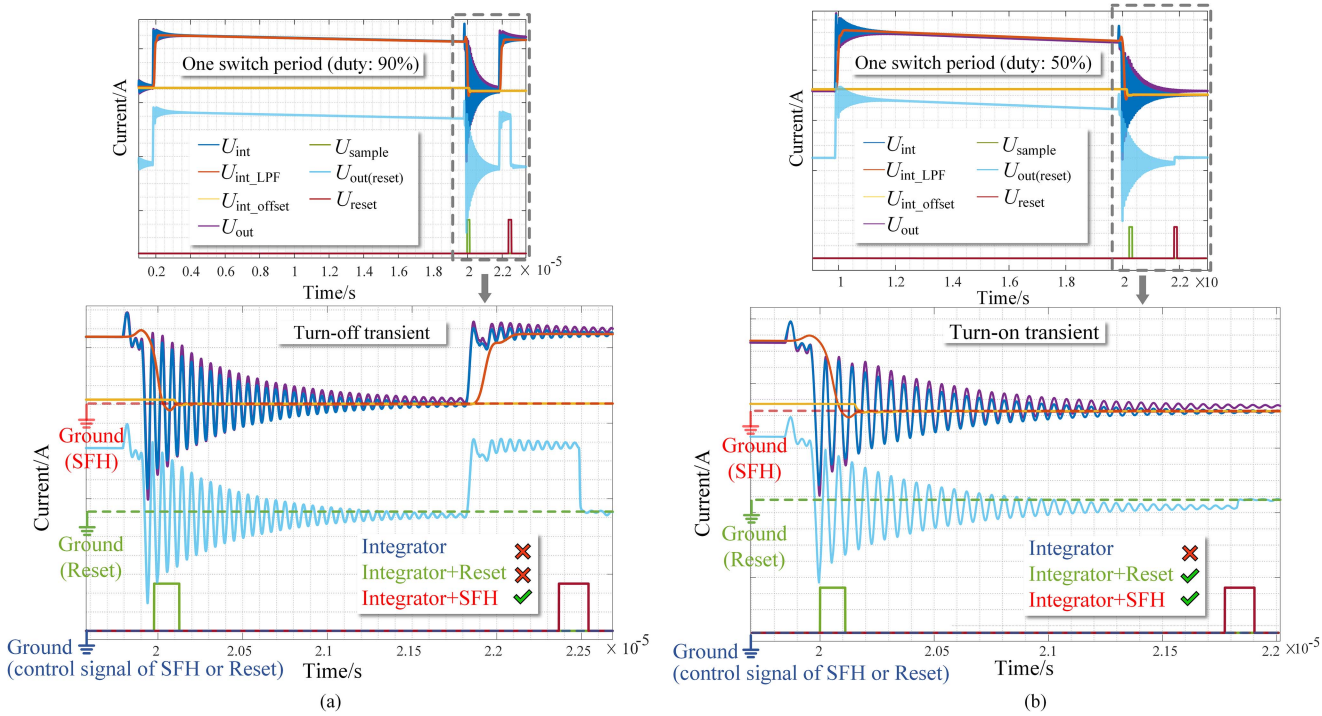

Fig. 15. Comparison of the proposed SFH method and the traditional switching reset method in a (a) short off time period and (b) long off time period.

TABLE II
MAIN PARAMETERS OF ROGOWSKI COIL SENSOR TESTING PLATFORM

Parameters	Value
DC-link voltage U_{dc}	300 V
DC-link capacitance C_{dc}	470μF
Filter inductance L_f	2 mH
Filter capacitance C_f	20 μF
Load resistance R_l	5 Ω
Switching frequency f	50 kHz

method during faults, which must occur during on time of the MOSFET.

IV. EXPERIMENT

To test the proposed Rogowski coil current sensor designed for the SiC-MOSFET power module, a buck converter and an inverter based on the Cree CCS050M12CM2 power module are built. The whole experimental platform and the parameters of the circuit are shown in Fig. 16 and Table II, respectively. The commercial Rogowski coil Tektronix TRCP0300 is used to compare with the Rogowski coil proposed. The former has the bandwidth of 30 MHz, whereas the latter of 30 MHz. The oscilloscope adopts Keysight DSOX3024T with the bandwidth of 200 MHz and the sampling rate of 2 GSa/s, which can ensure the accuracy of the experimental results.

The current waveform of the buck converter is a PWM wave with a fixed duty cycle, which has a constant dc component,

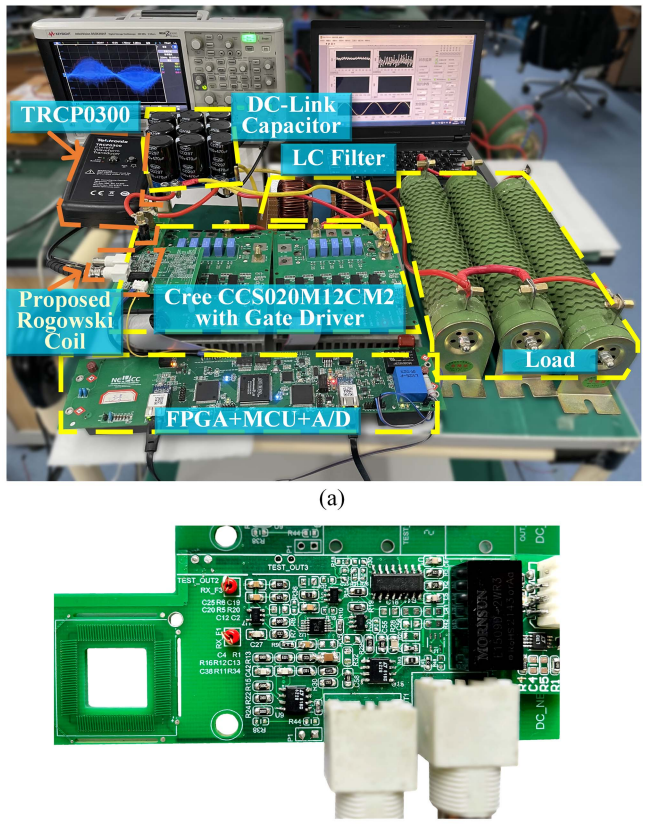

Fig. 16. Rogowski coil current sensor experimental platform. (a) Overall. (b) Proposed Rogowski sensor.

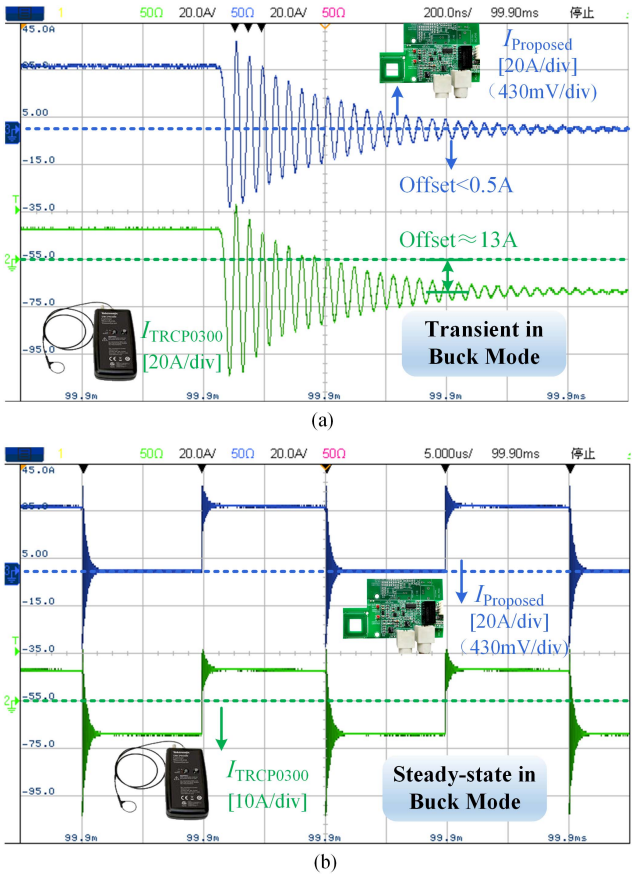

Fig. 17. Switching current of the buck converter measured by the proposed Rogowski coil and commercial Rogowski coil in (a) one period and (b) multiple periods.

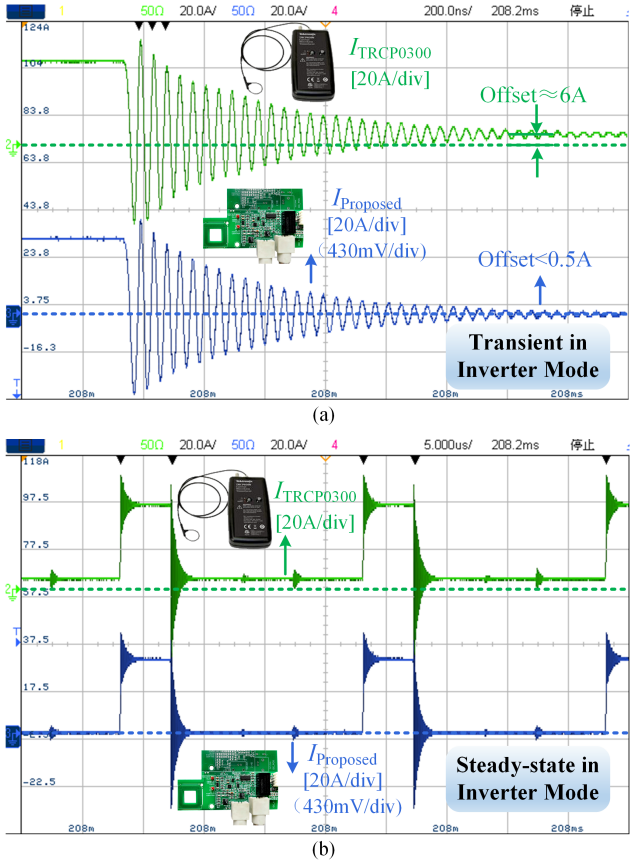

Fig. 18. Switching current of the inverter measured by the proposed Rogowski coil and commercial Rogowski coil in (a) one period and (b) multiple periods.

so it is suitable to test the drooping distortion suppressing capability of the Rogowski coil. The experiment results of the buck converter are shown in Fig. 17. It can be seen that the maximum current is around 26 A, and the ringing frequency is around 23 MHz, which indicates that both current sensors are of sufficient bandwidth after the SiC-MOSFET is turned OFF. The result shows the validity of both optimal design for the coil and the SFH method. On the one hand, the proposed sensor shows the sensitivity of 430 mV/A, so the mutual inductance is 10.8 nH with $K = 4\times10^6$ of the integrator, indicating a 1% error of (6). One the other hand, TRCP0300 coil has an offset of about 13 A. It can be seen in Fig. 17 that the dc component almost completely losses, which is consistent with the analysis results in Section III-A. On the contrary, the current measured by the proposed Rogowski sensor has an offset of less than 0.5 A, which reflects the good low frequency performance of the Rogowski coil proposed.

The experimental results of the inverter are shown in Fig. 18. It can be seen that the proposed Rogowski coil and TRCP0300 have an offset less than 0.5 and about 6 A, respectively, indicating that the proposed Rogowski sensor also has a better performance for inverters. Different from the buck converter, duties vary in each switching period. Hence, in a period of high duty, the high-frequency ringing after turned OFF cannot completely attenuate before the next period, which makes it difficult to perform a switch reset [21]. More importantly, the SPWM wave means different dc component in different switching cycles. The loss of them brings distortion of the fundamental wave, which is in line with Section III-A. The distortion is bad for the calibration of the overcurrent protection threshold, the restoration of the output current, and the control of the power module [29]. Therefore, for inverters, the Rogowski coil proposed also has considerable advantages.

V. Conclusion

The widespread application of the wide bandgap device SiC-MOSFET has created a demand for current sensors with high bandwidth, low delay, and small size, which are difficult to satisfy simultaneously with traditional current sensors. Therefore, this article proposes an improved design scheme of Rogowski coil. First, the parameters of the Rogowski coil are optimized to achieve the maximum mutual inductance while ensuring the measurement bandwidth, and then the sampling-filtering-hold circuit is used to calibrate the integrator reliably. The proposed design method not only maintains the inherent advantages of high bandwidth in ordinary Rogowski coils but also minimizes the droop distortion of Rogowski coils, so it is especially suitable for the measurement of SiC-MOSFET switching current. The experimental results verified the effectiveness of the proposed optimal PCB Rogowski coil structure design method and the SFH offset calibrating method.

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Qianming Xu (Member, IEEE) was born in Henan, China, in 1989. He received the B.S. degree in electrical engineering and automation and Ph.D. degree in electrical engineering from Hunan University, Changsha, China, in 2012 and 2017, respectively.

Since 2019, he has been an Associate Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include a multilevel converter, power electronic reliability monitoring, and power quality control.

Yuan Feng (Student Member, IEEE) was born in Guangdong, China, in 1998. He received the B.S. degree in electrical engineering from Changsha University of Science and Technology, Changsha, China, in 2021. He is currently working toward the M.S. degree in electrical engineering with Hunan University, Changsha, China.

His research interests include an electromagnetic sensor, multiobjective optimization, and embedded SiC-MOSFET driver.

Peng Guo (Member, IEEE) was born in Hunan, China, in 1992. He received the B.S. degree in electrical engineering from Wuhan University of Technology, Wuhan, China, in 2015, and the Ph.D. degree in electrical engineering from Hunan University, Changsha, China, in 2020.

He is currently a Postdoctoral Fellow with Hunan University. His research interests include a modular multilevel converter, switch-mode power amplifier, and model predictive control.

Nan Mo was born in Henan, China, in 1998. He received the B.S. degree in electrical engineering and automation, in 2020, from Hunan University, Changsha, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include high-frequency link inverter and modulation strategy.

Bailong Xu was born in Anhui, China, in 1992. He received the B.S. degree in electrical engineering from Harbin Engineering University, Harbin, China, in 2014, and the M.S. degree in electrical engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2017. He is currently working toward the Ph.D. degree in electrical engineering with Hunan University, Changsha, China.

In the field of electric vehicles, he was a Hardware Engineer from 2017 to 2021. His research interests include high power density dc/dc converters, multiport converter and its control technology, and planar transformers.

Zhuo Qing was born in Hunan, China, in 1997. He received the B.S. degree from Xiangtan University, Xiangtan, China, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with Hunan University, Changsha, China.

His research interests include control of power converters and electromagnetic interference of power electronics system.

Yandong Chen (Senior Member, IEEE) was born in Hunan, China, in 1979. He received the B.S. and M.S. degrees in instrument science and technology and Ph.D. degree in electrical engineering from Hunan University, Changsha, China, in 2003, 2006, and 2014, respectively.

He was a Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include power electronics for microgrid, distributed generation, power quality, and energy storage.

Dr. Chen was the recipient of the 2014 National Technological Invention Awards of China and the 2014 WIPO-SIPO Award for Chinese Outstanding Patented Invention. He is a member of the IEEE Power Electronics Society.

An Luo (Senior Member, IEEE) was born in Changsha, China, in 1957. He received the B.S. and M.S. degrees in industrial automation from Hunan University, Changsha, in 1982 and 1986, respectively, and the Ph.D. degree in fluid power transmission and control from Zhejiang University, Hangzhou, China, in 1993.

From 1996 to 2002, he was a Professor with the Central South University. Since 2003, he has been a Professor with the College of Electrical and Information Engineering, Hunan University, where he is also the Chief of the National Electric Power Conversion and Control Engineering Technology Research Center. His research interests include distributed generation, microgrid, and power quality.

Dr. Luo was elected to the Chinese National Academy of Engineering in 2015, the highest honor for scientists and engineers and scientists in China. He has won the highly prestigious China National Science and Technology Awards three times (2014, 2010, and 2006).