# An Extendable Interleaved Quasi Z-Source High Step-Up DC–DC Converter

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***Abstract*—A quasi z-source high step-up dc–dc converter is proposed here by integrating a coupled-inductor and a quadruple voltage rectifier technique. This converter can be used for high-voltage gain applications, without using extreme duty cycle and transformer high turns ratio values. Furthermore, low-voltage rating MOSFETs, which have small ON-resistances, can be used to reduce conduction losses and improve the converter efficiency. Also, single-core coupled inductors with multiwindings are used to reduce the magnetic components count. Using the interleaved technique at the converter input stage reduces the current stresses of the power MOSFETs as well as the current stresses of the primary side windings of the coupled inductor. For high power applications, number of the input stage interleaved legs can be properly chosen to reduce the input current and output voltage ripples values, which reduce the input and output filters volumes. Leakage inductances energy recovery is another benefit of the given converter. To confirm performance of the proposed converter and its operating principles, as well as the given simulation results and mathematical analyses, a two-leg topology of the introduced converter has been implemented and tested by applying both interleaved and noninterleaved gate-drive signals at different conditions.**

***Index Terms*—Coupled inductor, high step-up dc–dc converter, interleaved, quasi-z-source, voltage multiplier (VM).**

## I. Introduction

HIGH step-up dc–dc converters are generally implemented in different ways. The most important methods are using the magnetic-coupling technique, switched capacitor cells (SCCs), switched inductor cells (SICs), voltage lift, voltage multiplier cells (VMCs), cascading methods, and interleaving the converters. In the past, researchers have also tried to combine the abovementioned approaches to introduce new high step-up dc–dc converters [1]. One of the common approaches to increase the output voltage of the dc–dc converters is using the magnetic coupling technique, which is used in both isolated and nonisolated topologies to reduce number of the magnetic cores that typically form bulky parts of the circuits. Despite the ability of this method to achieve high-voltage gain, employing the magnetic coupling technique is associated with some problems, especially increasing the voltage stresses across the power switches. Therefore, researchers have tried to eliminate these voltage spikes by adding active and passive clamp circuits that increase the complexity and bulkiness of the converters [1], [2]. Although, high-voltage gains are obtained by utilizing the magnetic coupling technique, but using the extreme duty cycle values, high turns ratio of the coupled inductors, and high-voltage stresses on the output stage diodes are the main drawbacks of these converters [2].

Also, using the charge pump-based SCCs is one of the best approaches to increase power density of the dc–dc converters. In recent years, many converters have been proposed based on this approach to improve their performance, solve some problems such as current and voltage stresses of their components, and overcome some of their practical limitations to achieve high-voltage gains [3], [4].

Voltage multiplier (VM) blocks, a combination of diodes and capacitors, can be considered as subsets of the SCCs, which are efficient and inexpensive circuits with simple topologies for obtaining high dc voltage values. One of the main problems with these converters is the generated high inrush currents, which charge or discharge the capacitors. Combining the VM parts with coupled inductors is a solution for this issue [1], [5].

Structurally, VMs can be divided into following two general categories:

1) VMs are usually implemented in middle stage of the converters after their power switches to reduce voltage stresses and increase voltage gains of the converters.
2) VM rectifiers are composed only capacitors and diodes and they are considered as output stage of the converters [1], [6].

It should be mentioned that high-voltage gains are achieving by combining the VM techniques and the dc–dc converters [7], [8], [9]. Achieving high-voltage gains even at low duty cycle values and reducing voltage stresses on the power components are the two main advantages of these converters.

SICs are another method, which are widely used in high step-up dc–dc converters. In an SIC converter, the inductors are charged in parallel and discharged in series [10]. Low-voltage gain is one of the main weaknesses of the proposed converter in [11], which in fact combines both active and inactive SICs. Actually, some of the proposed high step-up dc–dc converters are combinations of the aforementioned techniques to obtain desired voltage gains, for instance, a coupled-inductor and a VM cell are combined in [12]. Also, a high-voltage gain is obtained by interleaving at the input side and using a VM cell at the converter output stage in [13].

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Also, voltage gain can be increased by combining the SCC and VMC [14], the VMC and cascading techniques [15], the SIC, SCC, and VMC [16], the SCC, coupled inductor, and interleaved techniques [17], [18]. Also, impedance source networks (ISNs) based converters are other new approaches to achieving high-voltage gains. Although these topologies provide higher voltage gains than the boost converters, but they also have higher conduction losses due to their lower operating duty cycle values. Of course, their diodes reverse recovery problems are less than the other converters. Achieving high-voltage gain, clamping the voltage of the switches to certain values, and eliminating the voltage spikes on the power switches are other advantages of these topologies [5], [19], [20]. By combining ISNs with other techniques, many high step-up converters with isolated and nonisolated topologies can be introduced. For example, one of the first proposed converters by using ISN technique has been introduced in [21], which cannot achieve a high-voltage gain. Also, a cascaded converter with coupled inductor and SCC has been introduced in [22], which its discontinuous input current is one of its main disadvantages. Also, three other different topologies have been proposed in [23] to achieve high-voltage gain.

High-voltage gains can be achieved by adding the VMCs, SCCs, and coupled inductors to the conventional Z-source dc–dc converters [24], [29]. Besides, combinations of the SCC and SIC with a the conventional ISN dc–dc converter have been introduced in [30], which have low-voltage gains, but continuous input currents. Other two dc–dc converters with an input–output common-ground are given in [31] and [32], and a zero-voltage switch configuration can also be found in [33]. Furthermore, an ISN-based isolated converter was introduced in [34], by combining a coupled inductor and a VM circuit.

Here, an interleaved quasi z-source based high step-up dc–dc converter is proposed, which has some good features such as isolated input–output ports and achieving high-voltage gain without applying extreme duty cycle and transformer high turns ratio values. Low current and voltage stresses on its power components make it possible to use low price and low ON-resistance power switches to improve the converter efficiency and cost. Also, using coupled inductors on a single magnetic core reduces the magnetic components count and cost, and its low input current ripple value effectively reduces the converter input filter volume as well as its cost. Voltage spikes on the power switches, which are mainly due to the leakage inductances, are also effectively eliminated.

The rest of this article is organized as follows. The general topology of the proposed converter and its operating principles are introduced in Section II. Then, the converter steady-state key waveforms and their various operational states are given in Section III. Then, the converter is analyzed under the steady-state condition in Section IV. Next, the voltage and current stresses of the different semiconductor power devices of the converter and a design procedure are given in Sections V and VI, respectively. Also, a power loss analysis is given in Section VII. Then, the proposed converter is compared with some other topologies in Section VIII, in detail. The experimental results are given in Section IX. Finally, Section X concludes this article.

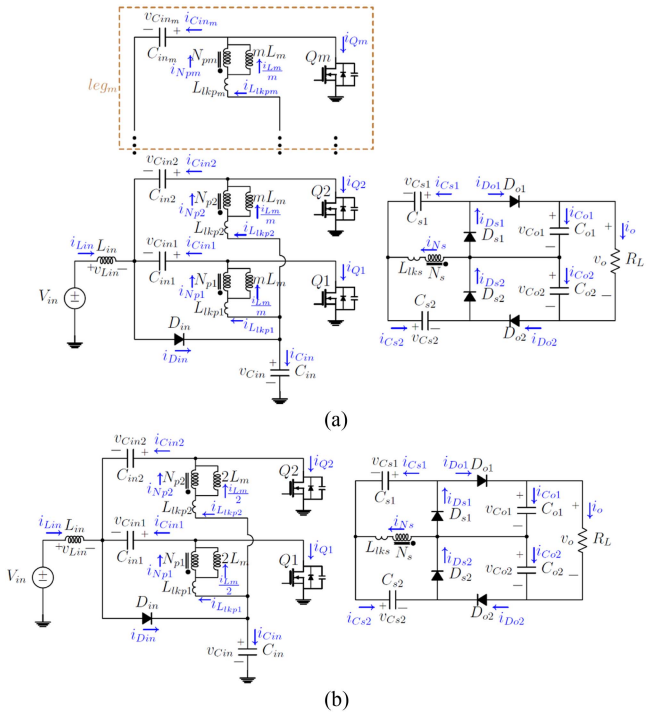


Fig. 1. Proposed DC-DC converter: (a) general configuration and (b) a two-branch configuration.

## II. Proposed Converter General Topology and Its Operating Principles

The general configuration of the proposed converter, which consists of two stages, is shown in Fig. 1(a). The input stage includes a quasi z-source network and some interleaved branches to reduce the input current ripple value, as well as the components current stresses. Also, its output stage includes a quadruple voltage cell to achieve high-voltage gain. These two stages are combined through a single-core coupled inductor. Here, each coupled inductor is modeled by a magnetizing inductor, $L_m$, a leakage inductor, $L_{\rm lk}$, and an ideal transformer with secondary to primary windings turns ratio equal to $n$. Also, a common winding is considered on the secondary side, as shown in Fig. 1(a). Each switch can be turned ON and OFF like the interleaved converters, taking into account the proper constant phase shift in between the gate drive signals. More branches on the input side can be used to reduce the input current ripple and the current stresses values on each branch. However, each switch requires a separate PWM gate drive signal. Although the same signals can also be applied to the switches to simplify the gate-drive circuit, but the input current ripple value is increased, as compared to the interleaved control method. To simplify the mathematical analyses and implementation of the prototype converter, only a configuration of the converter with two parallel branches is considered here, as shown in Fig. 1(b). Its two switches gate-drive pulses have a phase difference of 180°. Also, $N_{p1}$ and $N_{p2}$ are exactly the same in both windings and the turns ratio is $n = N_s/N_{p1}$. The converter operating principles under the continuous conduction mode (CCM) are discussed, too.

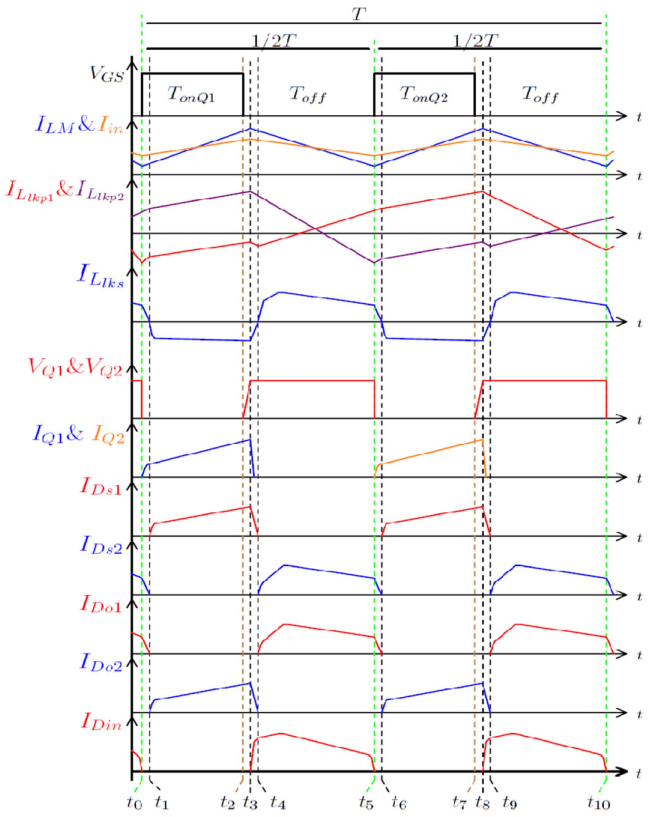


Fig. 2. Key waveforms of the proposed converter.

The following assumptions are made to simplify the analyses:

1) All components are considered ideal.
2) The magnetizing inductor and all capacitors are large enough to keep the inductor current and capacitors voltages constant during a switching period.
3) Each coupled inductor turns ratio is equal to $n = N_s/N_{p1}$ and $k = mL_m/(mL_m + L_{\rm lkp})$ parameter is also defined here to simplify the equations.

## III. Converter Key Waveforms and Its Different Operational States

The converter key waveforms are shown in Fig. 2 under the CCM operation mode. Using these waveforms, different operational states are discussed. As shown in Fig. 2, this converter has ten different main operating states over a switching period, including six short transient states and four main states. In state II, switch $Q_1$ conducts current. States II and VII are exactly the same, but $Q_2$ conducts the current instead of $Q_1$ during state VII. Also, states V and X are exactly the same.

*State I* [$t_0$–$t_1$]: During this subinterval, MOSFET $Q_1$ is conducting the current, and $D_{s2}$ and $D_{o1}$ are ON, while diodes $D_{\rm in}$, $D_{s1}$, and $D_{o2}$ are OFF, as shown in Fig. 3(a). The magnetizing inductor and the primary leakage inductor are being charged by capacitor $C_{\rm in}$. The input inductor, $L_{\rm in}$, is charged by voltage $V_s$+$V_{\rm cin1}$. On the secondary side, the stored energy in leakage inductor $L_{\rm lks}$ is discharged on $C_{s2}$, $C_{o1}$, and output. Also, the stored energy in $C_{s1}$ is transferred to the load and the output capacitors. This state ends when $D_{s2}$ and $D_{o1}$ are both OFF.

*State II* [$t_1$–$t_2$]: During this state, MOSFET $Q_1$ is still conducting the current. Diodes $D_{s1}$ and $D_{o2}$ start to conduct, while diodes $D_{\rm in}$, $D_{s2}$, and $D_{o1}$ are OFF, as shown in Fig. 3(b). Energy is transferred to the secondary side through the magnetizing inductor $L_m$. On the secondary side, the coupled inductor transfers its energy along with the energy stored in the capacitor $C_{s2}$ to the output capacitors. In addition, $C_{s1}$ is charged by the coupled inductor energy to be used in the next state. The input inductor $L_{\rm in}$ is still charged with voltage $V_s$+$V_{C\rm in1}$. This state ends when MOSFET $Q_1$ is turned OFF by the control circuit.

*State III* [$t_2$–$t_3$]: By turning MOSFET $Q_1$ OFF, its drain-source paralleled equivalent capacitor is rapidly charged during this short time and its drain-source voltage reaches to $V_{C\rm in}$+$V_{C\rm in1}$. This state is finished when the input diode $D_{\rm in}$ starts to conduct the current. To simplify the converter analyses, this short operational state is ignored here.

*State IV* [$t_3$–$t_4$]: During this operational state, both $Q_1$ and $Q_2$ are OFF and diodes $D_{\rm in}$, $D_{s1}$, and $D_{o2}$ are conducting the current, but diodes $D_{s2}$ and $D_{o1}$ are OFF, as shown in Fig. 3(c). Some part of the stored energy in the magnetizing inductor and the primary leakage inductors is transferred to $C_{\rm in1}$ and $C_{\rm in2}$. When diodes $D_{s1}$ and $D_{o2}$ currents reach to zero, this state is finished.

*State V* [$t_4$–$t_5$]: During this subinterval, both MOSFETs $Q_1$ and $Q_2$ are OFF and diodes $D_{\rm in}$, $D_{s2}$, and $D_{o1}$ are conducting the current, but diodes $D_{s1}$ and $D_{o2}$ are OFF, as shown in Fig. 3(d). The energy is transferred to the secondary side and load through the coupled inductor during this operational state, which is finished by turning ON MOSFET $Q_2$ through the control circuit.

*State VI* [$t_5$–$t_6$]: This state is similar to the first state, but $Q_2$ is conducting the current instead of $Q_1$, as shown in Fig. 3(e). The input inductor current is linearly increasing by applying $V_s$+$V_{C\rm in2}$ on it. This state ends when $D_{s2}$ and $D_{o1}$ are turned OFF.

*State VII* [$t_6$–$t_7$]: MOSFET $Q_2$ is still conducting the current during this operational state, as shown in Fig. 3(f). Energy is transferred to the secondary side through the coupled inductor and the input inductor current is still increasing due to the applied $V_s$+$V_{C\rm in2}$ voltage. This operational state is ended when MOSFET $Q_2$ is turned OFF by the control circuit.

*State VIII* [$t_7$–$t_8$]: By turning MOSFET $Q_2$ OFF, its drain-source paralleled equivalent capacitor is rapidly charged during this short subinterval and its drain-source voltage reaches to $V_{C\rm in}$+$V_{C\rm in2}$. This state is finished when the input diode $D_{\rm in}$ starts to conduct the current. To simplify the converter analyses, this short operational state is also ignored here.

*State IX* [$t_8$–$t_9$]. This operational state is similar to the state IV, as shown in Fig. 3(g).

*State X* [$t_9$–$t_{10}$]: Both MOSFETs $Q_1$ and $Q_2$ are OFF during this operational state and the input diode $D_{\rm in}$ is conducting the current. Diodes $D_{s2}$ and $D_{o1}$ are still ON and diodes $D_{s1}$ and $D_{o2}$ are OFF, as shown in Fig. 3(h). Some part of the stored energy in the magnetizing inductor and the primary leakage inductors is transferred to the capacitors $C_{\rm in1}$ and $C_{\rm in2}$, but some part is

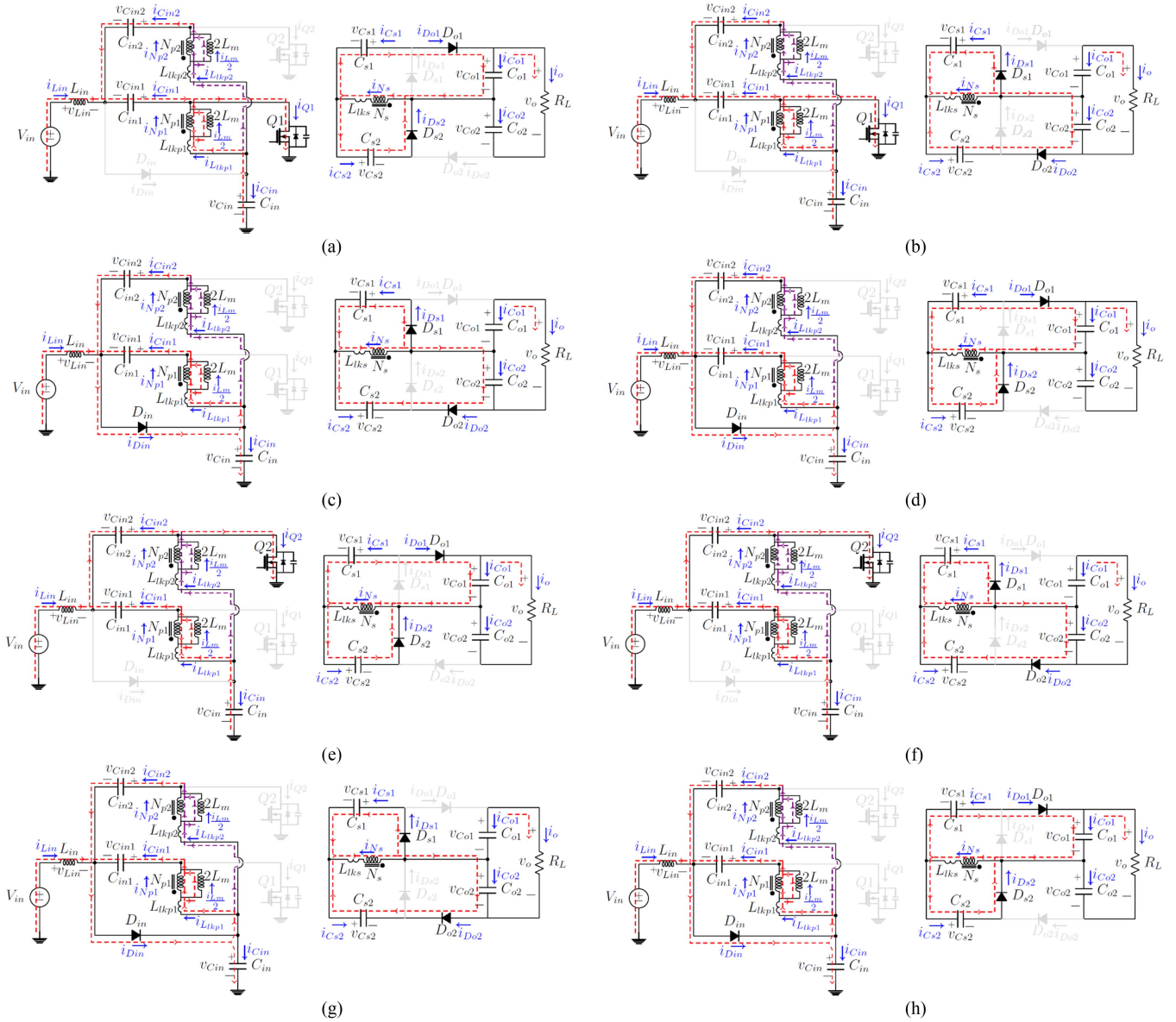


Fig. 3. Operational states over a switching period: (a) state I, (b) state II, (c) state IV, (d) state V, (e) state VI, (f) state VII, (g) state IX, and (h) state X.

transferred to the secondary side through the coupled inductors. This state is finished when the control circuit turns $Q_1$ ON.

## IV. Steady-State Analysis of the Converter

As previously discussed, states II, V, VII, and X are the four main operational states of the converter. Other operating states do not have significant effects on the converter characteristics because they are too short. Therefore, these nondominant states are ignored to simplify the converter analyses, and only the abovementioned four main operational states are considered here. Also, states V and X are exactly the same, as mentioned before, and $N_{p1}$ is equal to $N_{p2}$. Due to the converter primary stage symmetrical configuration, capacitors $C_{\text{in1}}$ and $C_{\text{in2}}$ and MOSFETs $Q_1$ and $Q_2$ drain-sources voltages are also the same. MOSFET $Q_1$ is ON during state II, as shown in Fig. 3(b). By considering this equivalent circuit, we can write

$$v_{L_{\text{in}}} = V_{in} + V_{C_{\text{in1}}} \tag{1}$$

$$v_{L_{Np1}} = V_{C_{\text{in}}} \tag{2}$$

$$v_{L_m} = \frac{mL_m}{mL_m + l_{\text{lkp}}} V_{C_{\text{in}}} = kV_{C_{\text{in}}} \tag{3}$$

$$v_{L_{\text{lkp1}}} = V_{C_{\text{in}}} + v_{L_m} = (1-k)\, V_{C_{\text{in}}} \tag{4}$$

$$v_{L_{Ns}} = nv_{L_m} = nkV_{C_{\text{in}}} = V_{C_{s1}} \tag{5}$$

$$V_{c_{o2}} = v_{L_{Ns}} + V_{c_{s2}} = V_{c_{s1}} + V_{c_{s2}} \tag{6}$$

Also, from Fig 3(b), we can write

$$I_{\text{in}} = I_{L_{\text{in}}} = -i_{C_{\text{in1}}} - i_{C_{\text{in2}}} \tag{7}$$

$$i_{Q1} = I_{\text{in}} - i_{C_{\text{in}}} \tag{8}$$

$$i_{L_{\text{lkp1}}} + i_{L_{\text{lkp2}}} = -i_{C_{\text{in}}}. \tag{9}$$

Applying KCL to Fig. 3(b) and considering (9), a relationship between the primary windings currents is obtained as follows:

$$i_{L_{Np1}} + i_{L_{Np2}} = -i_{C_{\text{in}}} - I_{L_m} = -ni_{L_{Ns}} = -ni_{L_{\text{lks}}}. \tag{10}$$

On the secondary side of the converter, we can write

$$i_{L_{Ns}} = i_{L_{\text{lks}}} = i_{C_{s2}} - i_{C_{s1}} \tag{11}$$

$$i_{D_{s1}} = i_{C_{s1}} \tag{12}$$

$$i_{D_{o2}} = -i_{C_{s2}} = i_{C_{o2}} + I_o \tag{13}$$

$$i_{C_{o1}} = -I_o. \tag{14}$$

Also, during state VII, MOSFET $Q_2$ is ON, as shown in Fig. 3(f), and the converter describing equations are exactly the same, as derived in state II, except for few minor changes as follows:

$$v_{L_{\text{in}}} = V_{\text{in}} + V_{C_{\text{in2}}} \tag{15}$$

$$v_{L_{Np2}} = V_{C_{\text{in}}} = v_{L_{Np1}} \tag{16}$$

$$i_{Q2} = I_{\text{in}} - i_{C_{\text{in}}}. \tag{17}$$

The converter secondary side diodes states are the same during states II and VII. Therefore, (3)–(7) and (9)–(14) are established during this time interval too. Also, all MOSFETs are OFF during states V and X, as shown in Fig. 3(d) and (h), and the converter main relationships are given as follows:

$$v_{L_{\text{in}}} = V_{\text{in}} - V_{C_{\text{in}}} \tag{18}$$

$$v_{L_{Np1}} = -V_{C_{\text{in1}}}, v_{L_{Np2}} = -V_{C_{\text{in2}}}. \tag{19}$$

Using (3) and (5), we can write

$$v_{L_{Ns}} = -nkV_{C_{\text{in1}}} = -nkV_{C_{\text{in2}}} = -V_{C_{s2}} \tag{20}$$

$$V_{C_{o1}} = V_{C_{s1}} - v_{L_{Ns}} = V_{C_{s1}} + V_{C_{s2}}. \tag{21}$$

Also, when all MOSFETs are OFF, relationships between the currents of some components are given as follows:

$$I_{\text{in}} = I_{L_{\text{in}}} = i_{C_{\text{in}}} \tag{22}$$

$$i_{D_{\text{in}}} \simeq I_{\text{in}} + 2i_{C_{\text{in1}}} \tag{23}$$

$$i_{L_{\text{lkp1}}} = i_{C_{\text{in1}}} \simeq i_{L_{\text{lkp2}}} = i_{C_{\text{in2}}}. \tag{24}$$

Applying KCL on currents of the windings of the coupled inductors and using (24), we can write

$$i_{L_{Np1}} + i_{L_{Np2}} = i_{C_{\text{in1}}} + i_{C_{\text{in2}}} - I_{L_m} = -ni_{L_{Ns}} = -ni_{L_{\text{lks}}}. \tag{25}$$

Also, the following relationships are easily given for the converter secondary side by considering Fig. 3(d) and (h):

$$i_{L_{Ns}} = i_{L_{\text{lks}}} = i_{C_{s2}} - i_{C_{s1}} \tag{26}$$

$$i_{D_{s2}} = i_{C_{s2}} \tag{27}$$

$$i_{D_{o1}} = -i_{C_{s1}} = i_{C_{o1}} + I_o \tag{28}$$

$$i_{C_{o2}} = -I_o. \tag{29}$$

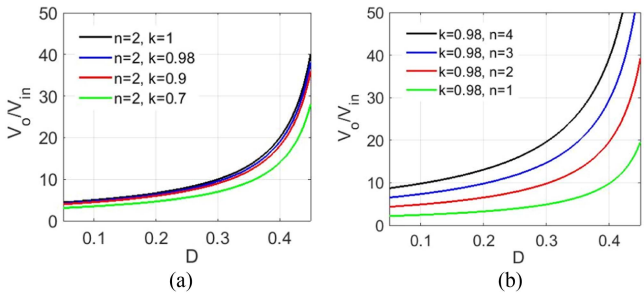


Fig. 4. Converter voltage gain versus duty cycle: (a) $n = 2$ and different coupling coefficients and (b) $k = 0.98$ and different turns ratio.

A relationship between the voltages of the input capacitors is also obtained by applying the volt–second balance principle law to the coupled inductors primary windings

$$V_{C_{\text{in}}} = \frac{1 - 2D_{Q_1}}{2D_{Q_1}} V_{C_{\text{in1}}} = \frac{1 - 2D_{Q_2}}{2D_{Q_2}} V_{C_{\text{in2}}}. \tag{30}$$

Applying the same duty cycles to both power switches, i.e., $D_{Q1} = D_{Q2}$, and using enough large capacitors, the same voltages are applied on both capacitors $C_{\text{in1}}$ and $C_{\text{in1}}$, in practice. By applying the volt–second balance principle to $L_{\text{in}}$ and using (1), (18), and (30), the applied dc voltages on the input capacitors are also identified easily

$$V_{C_{\text{in}}} = \frac{1 - D}{1 - 2D} V_{\text{in}},\ V_{C_{\text{in1}}} = V_{C_{\text{in2}}} = \frac{D}{1 - 2D} V_{\text{in}} \tag{31}$$

where $D = D_{Q_1} + D_{Q_2}$. By using this definition, the converter duty cycle maximum value is equal to 0.5 and each MOSFET duty cycle can vary between 0 and 0.25. Combining the converter secondary side relations and (31), the voltage gain is calculated

$$G = \frac{V_o}{V_{\text{in}}} = \frac{2nk}{1 - 2D}. \tag{32}$$

Fig. 4 shows the converter voltage gain for different values of the turns ratio of the transformer and coils coupling coefficient. As clearly shown, the voltage gain is not too sensitive to the coils coupling coefficients, but increasing the turns ratio of the transformer increases the voltage gain value.

## V. Voltage and Current Stresses of the Power Semiconductor Devices

Here, voltage and current stresses of the power MOSFETs and diodes are given in detail. Both MOSFETs have the same drain-source voltage stresses, which are given as follows:

$$V_{\text{DS}_{Q_{1,2}}} = \frac{1}{2nk} V_o. \tag{33}$$

Also, these devices currents values, which are the same, can be approximated by considering (8), (17), (22), (32), and applying the charge–balance principle law to the capacitor $C_{\text{in}}$

$$I_{Q_{1,2}} \simeq \frac{2nkP_o}{D\,(1 - 2D)\,V_o}. \tag{34}$$

When $n = 2, k = 0.99, D = 0.33, P_o = 200\,W$, and $V_o = 300\,V$, the voltage and current stresses of these MOSFETs are approximately equal to $75\,V$ and $24\,A$, respectively.

Considering (31), (32), and equivalent circuits of the converter during states I, II, V, and VI, as shown in Fig. 3(a), (b), (e), and (f), diode $D_{\text{in}}$ peak inverse voltage is given by

$$\text{PIV}_{D_{\text{in}}} = \frac{1}{2nk}\,V_o. \tag{35}$$

Considering (7), (23), (32), and applying the charge-balance law to $C_{\text{in}1}$ and $C_{\text{in}2}$, the $D_{\text{in}}$ current can be approximated as

$$I_{D_{\text{in}}} \simeq \frac{2nkP_o}{(1-D)(1-2D)V_o}. \tag{36}$$

If $n = 2$, $k = 0.99$, $D = 0.33$, $P_o = 200\ W$, and $V_o = 300\ V$, then $\text{PIV}_{D_{\text{in}}} = 75\ V$ and $i_{D_{\text{in}}} \simeq 12\ A$.

Also, by considering the converter equivalent circuits during states II and V, the same voltage stresses, equal to half of the output voltage, are applied on the output stage diodes

$$\text{PIV}_{D_{s1}} = \text{PIV}_{D_{s2}} = \text{PIV}_{D_{o1}} = \text{PIV}_{D_{o2}} = 0.5V_o. \tag{37}$$

Thus, $150\ V$ is applied to these diodes here. Also, from (12), (13), (27), (28), and the output capacitor average currents values during states II and V, the output diodes currents are given as follows:

$$I_{D_{s1}} = I_{D_{o2}} \simeq \frac{P_o}{DV_o},\ I_{D_{s2}} = I_{D_{o1}} \simeq \frac{P_o}{(1-D)V_o}. \tag{38}$$

For the given values of $D = 0.33$ , $P_o = 200\ W$, and $V_o = 300\ V$, $i_{D_{s1}} = i_{D_{o2}} \simeq 2\ A$ and $i_{D_{s2}} = i_{D_{o1}} \simeq 1\ A$.

## VI. Passive Components Design Procedure

Here, an exemplified design approach is given for calculating values of the capacitors and inductors, as well as their voltage and current stresses in detail. From (31) and (32), the primary stage capacitors voltages are easily identified as follows:

$$V_{C_{\text{in}}} = \frac{1-D}{2nk}\,V_o,\ V_{C_{\text{in}1}} = V_{C_{\text{in}2}} = \frac{D}{2nk}\,V_o. \tag{39}$$

In the same manner, from (5), (20), and (39), the second stage capacitors voltage stresses are also determined

$$V_{C_{s1}} = 0.5(1-D)V_o,\ V_{C_{s2}} = 0.5DV_o,\ V_{C_{o1,\,o2}} = 0.5V_o. \tag{40}$$

By ignoring the leakage inductance or equally by considering the unity coupling coefficient, the voltage gain is ideally obtained as $V_o/V_{\text{in}} = I_{\text{in}}/I_o = 2n/1-2D$ . By considering $I_C = C\Delta V/\Delta T$, (22), and voltage gain with unit coupling factor, capacitor $C_{\text{in}}$ value is calculated. Where $\Delta T = (1-D)T_s$. In the same manner, the converter different capacitors capacitances values can also be calculated as follows:

$$\begin{cases} C_{\text{in}} = \frac{2n(1-D)P_o}{(1-2D)f_s\Delta V_{C_{\text{in}}}V_o} \\ C_{\text{in}1} = C_{\text{in}2} = \frac{nDP_o}{(1-2D)f_s\Delta V_{C_{\text{in}1}}V_o} \\ C_{s1} = \frac{P_o}{f_s\Delta V_{C_{s1}}V_o}\ ,\quad C_{s2} = \frac{P_o}{f_s\Delta V_{C_{s2}}V_o} \\ C_{o1} = \frac{DP_o}{f_s\Delta V_{C_{o1}}V_o}\ ,\quad C_{o2} = \frac{(1-D)P_o}{f_s\Delta V_{C_{o2}}V_o}. \end{cases} \tag{41}$$

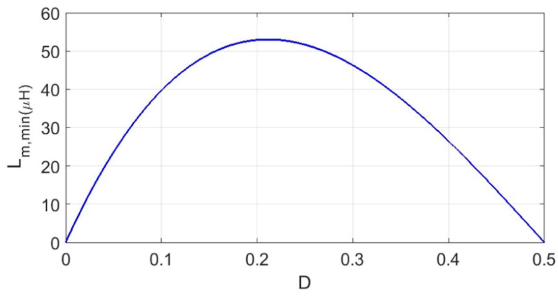


Fig. 5. Minimum value of the magnetizing inductance of the converter to guarantee its CCM operation mode.

If voltages ripples values smaller than 1% and 0.1% for the input and output capacitors are, respectively, desired, then from (39) and (40), $\Delta V_{C_x}/V_o$ is equal to, 0.5, 0.24, 0.1, 0.05, and 0.15 for $C_{\text{in}}$, $C_{\text{in}1,2}$, $C_{s1}$, $C_{s2}$, $C_{o1,2}$, and $C_{o1,2}$, respectively. When $n = 2$, $D$ =0.33, $P_o = 200$ W, $V_o = 300$ V, and $f_s = 50$ kHz parameters values are considered, then $C_{\text{in}} \approx 213\ \mu F$, $C_{\text{in}1} = C_{\text{in}2} \approx 106.5\ \mu F$, $C_{s1} \approx 133\ \mu F$, $C_{s2} \approx 266\ \mu F$, and $C_{o1} = C_{o2} \approx 30\ \mu F$ are approximately obtained.

Also, by considering the converter primary stage symmetrical configuration and using (9) and (11), we can write

$$\begin{cases} N_1\ i_{L_m} = N_1 i_1\ + N_2 i_2 + N_3 i_3 + \ldots \\ I_{L_m} = -I_{C_{\text{in}}} - nI_{C_{s1}} + nI_{C_{s2}}\ . \end{cases} \tag{42}$$

Considering the output capacitors zero dc currents, applying the charge-balance principle law on the capacitor $C_{\text{in}}$, and using (32), dc value of the magnetizing current of the transformer is simply obtained as follows:

$$I_{L_m} = I_{\text{in}}. \tag{43}$$

Considering (3), (31), and taking into account the inductor general relationship, i.e., $V_L = L\Delta I/\Delta T$, current ripple value of the magnetizing inductor is obtained during the second state

$$\Delta i_{L_m} = \frac{kD(1-D)V_{\text{in}}}{2(1-2D)L_m f_s}. \tag{44}$$

To guarantee CCM operation mode of the converter, $I_{L_m} > \Delta i_{L_m}/2$, which identifies minimum value of the magnetizing inductance, must be satisfied. Therefore, from (32), (43), and (44), minimum value of the magnetizing inductance for CCM operation mode of the converter is simply identified as follows:

$$L_{m\,\min} = \frac{kR_L}{16n^2 f_s}\,D(1-D)(1-2D). \tag{45}$$

This minimum value can be plotted versus the converter duty cycle value under the light load conditions, as shown in Fig. 5, where $R_L = 1800\ \Omega$, $f_s = 50$ kHz, $n = 2$, and $k = 0.99$. Therefore, choosing $L_m$ equal to 60 $\mu$H leads to the CCM operation of the converter. Also, from (18) and (31), the input inductor value is easily calculated by considering the equivalent circuit of the converter during its second state as follows:

$$L_{\text{in}} = \frac{D(1-D)V_{\text{in}}}{2(1-2D)f_s\Delta I_{\text{in}}} \tag{46}$$

## VII. Power Loss Analysis of the Converter

The dominant power losses, which commonly occur in power MOSFETs, diodes, and ESRs of the capacitors and coupled inductors, are analyzed here in detail. Conduction losses of both power MOSFETs depend on their ON-resistances as well as their rms currents values. From (34), the rms currents and conduction losses values of the power MOSFETs are, respectively, obtained as follows:

$$I_{Q_1\,\mathrm{RMS}} = I_{Q_2\,\mathrm{RMS}} = \frac{nkP_o\sqrt{2D}}{D\,(1-2D)\,V_o} \tag{47}$$

$$P_{Q_1(\mathrm{con})} = P_{Q_2(\mathrm{con})} \simeq \frac{2n^2k^2P_o^2R_{\mathrm{DS(on)}}}{D(1-2D)^2V_o^2}. \tag{48}$$

The power MOSFETs ON-resistances values are approximately equal to 20 mΩ, which lead to $P_{Q_1(\mathrm{con})} = P_{Q_2(\mathrm{con})} \simeq 1.86\ W$.

Switching losses are caused by the power MOSFETs currents and voltages overlapping during their ON and OFF transient events. Here, turn-OFF switching losses of the power MOSFETs are calculated by using (33) and (34) as follows:

$$P_{Q_1(\mathrm{off})} = P_{Q_2(\mathrm{off})} = f_s \int^{t_{\mathrm{off}}} v_{DS_Q}(t)\, i_Q(t)\, dt \simeq \frac{P_o f_s t_{\mathrm{off}}}{D\,(1-2D)} \tag{49}$$

where $t_{\mathrm{off}} \simeq 20\ ns$. So $P_{Q_1(\mathrm{off})} = P_{Q_2(\mathrm{off})} \simeq 1.78\ W$. Also, these MOSFETs switching-ON losses, due to their drain-sources equivalent parasitic capacitances, are given as follows:

$$P_{Q_1(\mathrm{on})} = P_{Q_2(\mathrm{on})} \simeq \frac{1}{2}C_{\mathrm{DS}}f_s\,V_{\mathrm{DS}}^2 = \frac{C_{\mathrm{DS}}f_sV_o^2}{8n^2k^2}. \tag{50}$$

Here, $C_{\mathrm{DS}} \simeq 200$ pF. So $P_{Q_1(\mathrm{on})} = P_{Q_2(\mathrm{on})} \simeq 0.02$W.

By considering the given analyses in Section V, diodes losses, mainly due to their conduction losses, are calculated too

$$P_{D_{\mathrm{in}}} \simeq \frac{2n}{1-2D}\,\frac{V_{F(D_{\mathrm{in}})}}{V_o}P_o,\ P_{D_{s1,\,s2}} = P_{D_{o1,\,o2}} \simeq \frac{V_F}{V_o}P_o. \tag{51}$$

If $V_{F(D_{\mathrm{in}})} = 0.5\ V$ and $V_F = 1\ V$, then $P_{D_{\mathrm{in}}} \simeq 3.92\ W$ and $P_{D_{s1}} = P_{D_{s2}} = P_{D_{o1}} = P_{D_{o2}} \simeq 0.66\ W$ are obtained.

Power losses of the capacitors are mainly due to their ESRs. Since the rms current values of the output capacitors are enough small, their power losses can be ignored to shorten the analyses. Also, according to (7), (22), and using the charge-balance principle law, power losses of the main capacitors can be calculated as follows:

$$\begin{cases} P_{C_{\mathrm{in}}} \simeq \frac{1-D}{D}I_{\mathrm{in}}^2\mathrm{ESR}_{C_{\mathrm{in}}} \\ P_{C_{\mathrm{in1}}} = P_{C_{\mathrm{in2}}} \simeq \frac{D}{4(1-D)}I_{\mathrm{in}}^2\mathrm{ESR}_{C_{\mathrm{in1,\,2}}}. \end{cases} \tag{52}$$

If $\mathrm{ESR}_{C_{\mathrm{in}}} = 5\ \mathrm{m\Omega}$ and $\mathrm{ESR}_{C_{\mathrm{in1,\,2}}} = 25\ \mathrm{m\Omega}$, then $P_{C_{\mathrm{in}}} \simeq 0.7\ W$ and $P_{C_{\mathrm{in1}}} = P_{C_{\mathrm{in2}}} \simeq 0.23\ W$ are obtained. Generally, windings and core losses are the inductors main components losses. Here, core losses are negligible due to the current ripple small value and using ferrite cores. Also, by considering (9) and (24), windings losses of the coupled inductor and input inductor can be approximated as follows, respectively:

$$\begin{cases} P_{\mathrm{CI}} \simeq r_{L_{\mathrm{lkp}}}I_{\mathrm{in}}^2\left(\frac{1}{D(1-D)} - 3\right) \\ P_{L_{\mathrm{in}}} = r_{L_{\mathrm{in}}}\,I_{\mathrm{in}}^2 \end{cases} \tag{53}$$

where $r_{L_{\mathrm{lkp}}}$ is the primary referred equivalent series resistance of the coupled inductor, $r_{L_{\mathrm{in}}} \simeq 5\ \mathrm{m\Omega}$, and $r_{L_{\mathrm{lkp}}} \simeq 25\ \mathrm{m\Omega}$. Therefore, $P_{L_{\mathrm{in}}} \simeq 0.3\ W$ and $P_{\mathrm{CI}} \simeq 2.7\ W$ are, respectively, achieved. So the converter total losses are identified as follows:

$$\begin{aligned} P_{\mathrm{Loss}} = {} & 2\left(P_{Q_1(\mathrm{con})} + P_{Q_1(\mathrm{on})} + P_{Q_1(\mathrm{off})}\right) + 2P_{C_{\mathrm{in1}}} \\ & + 2P_{\mathrm{CI}} + 4P_{D_{s1}} + P_{D_{\mathrm{in}}} + P_{C_{\mathrm{in}}} + P_{L_{\mathrm{in}}} = 20\ \mathrm{W}. \end{aligned} \tag{54}$$

Therefore, the converter efficiency value is determined under the abovementioned conditions

$$\eta = \frac{P_o}{P_o + P_{\mathrm{Loss}}} = \frac{200}{200+20} \approx 0.91\%. \tag{55}$$

## VIII. Comparison Between Different Topologies

Fig. 6 shows some different converters voltage-gains versus duty cycle as well as their active switches and diodes normalized voltage stresses versus their voltage gains, respectively. To do a better comparison, turns ratios of the used transformers of these converters are considered to be the same and equal to 2. As clearly shown in Fig. 6, higher voltage gains and lower voltage stresses on the components are achieved by using the proposed converter as compared to the others.

Although specifications of the proposed converter and the introduced one in [29] are the same, but lower voltage stresses are applied to the proposed converter diodes. Also, the proposed converter input current and output voltage ripples values are half of the given ones in [29] due to its interleaved structure. These ripples values can be more reduced by using more branches at the input stage, if it is necessary. Consequently, smaller input filter, input inductor, and input capacitor, as well as smaller output capacitors, can be used here as compared to [29] under the same conditions. Also, high-voltage gains are achieved in low duty cycle values by using the given converter in [28], but voltage stress on its MOSFET is higher than the voltages of the MOSFETs of the proposed converter clearly.

Finally, a comprehensive comparison between the proposed converter and some other converters have been done, as tabulated in Table I. It should be mentioned that the given converter can be used for higher output power values than the given one here. But, due to our laboratory equipment and limited measurement instruments, only a scaled-down prototype converter has been implemented and tested to show its good performance, as well as to verify the given mathematical analyses and simulation results. Some conclusions are given as follows by considering Table I and the given mathematical analyses and simulation results:

1) Lower current ripple value is achieving at the input port of the proposed converter, as compared to the other ones in Table I, when interleaved gate-drive signals are properly applied to the converter. This means that smaller and low-cost input inductor, as well as input filter, can be used to satisfy the necessary requirements, in practice. Also, using the interleaved operation reduces capacitances and prices of the input and output capacitors, i.e., $C_{\mathrm{in}}$, $C_{o1}$, and $C_{o2}$, and higher efficiency values are achieved, as compared to the noninterleaved control approach.

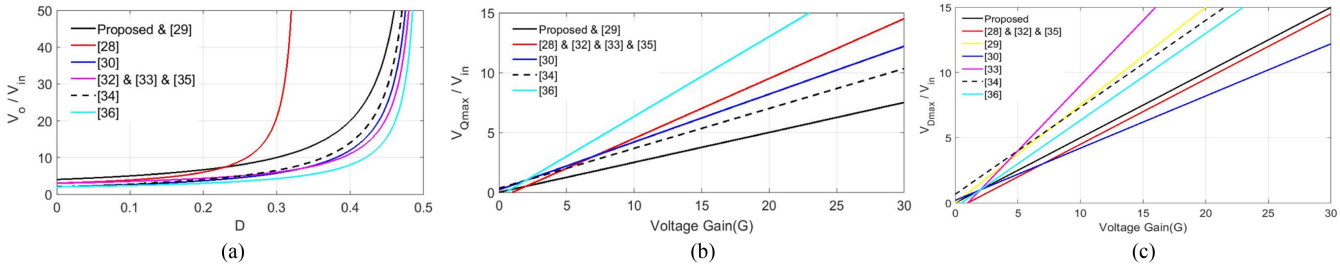


Fig. 6. Comparing different characteristics of some converters: (a) voltage gain, (b) active switches normalized voltage stresses, and (c) diodes normalized voltage stresses.

TABLE I
COMPARISON BETWEEN THE PROPOSED CONVERTER AND SOME OTHER RELATED DC–DC CONVERTERS

| | Voltage gain ($G$) | $V_{Q\,max}$ | $V_{D\,max}$ | Number of components | | | | Duty cycle range | $V_{in}$ (V) | $V_{out}$ (V) | $P_{out}$ (W) | $f_s$ (kHz) | $\eta$(%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Core | SW | D | C | | | | | | |
| [28] | $\frac{3(1-D)}{1-3D}$ | $\frac{G-1}{2}V_{in}$ | $\frac{G-1}{2}V_{in}$ | 2 | 2 | 5 | 5 | 0 < D < 0.3 | 40 | 240 | 144 | 100 | 96 |
| [29] | $\frac{n+2}{1-2D}$ | $\frac{GV_{in}}{n+2}$ | $\frac{G(n+1)}{n+2}V_{in}$ | 2 | 1 | 4 | 5 | 0 < D < 0.5 | 64 | 620 | 500 | 50 | 94 |
| [30] | $\frac{2+D}{1-2D}$ | $\frac{2G+1}{5}V_{in}$ | $\frac{2G+1}{5}V_{in}$ | 3 | 1 | 5 | 7 | 0 < D < 0.5 | 24 | 365 | 150 | 40 | 90 |
| [32] | $\frac{3-2D}{1-2D}$ | $\frac{G-1}{2}V_{in}$ | $\frac{G-1}{2}V_{in}$ | 2 | 1 | 4 | 5 | 0 < D < 0.5 | 30 | 180 | 125 | 25 | 95 |
| [33] | $\frac{1+n(1-D)}{1-2D}$ | $\frac{2G-n}{n+2}V_{in}$ | $\frac{n(2G-n)}{n+2}V_{in}$ | 2 | 2 | 2 | 4 | 0 < D < 0.5 | 48 | 350 | 100 | 100 | 94 |
| [34] | $\frac{n(1+D)}{1-2D}$ | $\frac{2G+n}{3n}V_{in}$ | $\frac{2G+n}{3}V_{in}$ | 2 | 1 | 4 | 5 | 0 < D < 0.5 | 25 | 400 | 300 | 50 | 92 |
| [35] | $\frac{3-2D}{1-2D}$ | $\frac{G-1}{2}V_{in}$ | $\frac{G-1}{2}V_{in}$ | 3 | 1 | 4 | 6 | 0 < D < 0.5 | 28 | 400 | 400 | 100 | 91 |
| [36] | $\frac{2-D}{1-2D}$ | $\frac{2G-1}{3}V_{in}$ | $\frac{2G-1}{3}V_{in}$ | 2 | 1 | 3 | 4 | 0 < D < 0.5 | 20 | 140 | 100 | 50 | 91 |
| Proposed converter | $\frac{2nk}{1-2D}$ | $\frac{GV_{in}}{2n}$ | $\frac{GV_{in}}{2}$ | 2 | 2 | 5 | 7 | 0 < D < 0.5 | 25 | 300 | 200 | 50 | 91 |
| | | | | | | | | | 30-60 | 600 | 240 | 100 | 94 |

2) Using more branches further improves the abovementioned parameters, when the interleaved approach is used.
3) However, the interleaved control approach, as widely used in the interleaved configurations, is more complex than the noninterleaved technique. Consequently, interleaved control approach is preferred for high power applications, in practice.
4) The proposed converter can achieve higher voltage gain, without using extreme duty cycle and transformer high turns ratio values, as compared to the other converters.
5) Generally, transformers and inductors are massive components that can strongly affect power density and price of each converter. However, this is a common issue in many dc–dc converters, even more the proposed converter is better than some other converters, as mentioned earlier and it can also be concluded from Table I easily.
6) Number of the active switches and their driver and control circuits are other issues. But, practically there is no problem in this point of view for high power applications. Because the proposed converter has lower voltage stresses on the semiconductor devices, as compared to the abovementioned converters under the same voltage gain and input voltage values. In addition, some other key parameters, such as output power to total cost ratio, determine complexity of the converters, in practice.
7) Using more diodes in the proposed converter, as also used in some other given converters in Table I, is not a significant issue. Because the proposed converter voltage gain and its output voltage are significantly higher than the other ones. So this issue cannot too affect the price and power density of the proposed converter, in practice.

As given in Table I, to deliver a specified wide output power variation range, 50 W$<P_{\rm out}<$240 W, the proposed converter has been tested by applying two different noninterleaved and interleaved gate-drive signals, respectively, as follows:

1) $V_{\rm out} = 600$ V and $f_s = 100$ kHz when 30 V$<V_{\rm in}<$60 V.
2) $V_{\rm out} = 300$ V and $f_s = 50$ kHz when $V_{\rm in} = 25$ V.

To verify the given analyses and simulation results, in the next section experimental results are given in more detail.

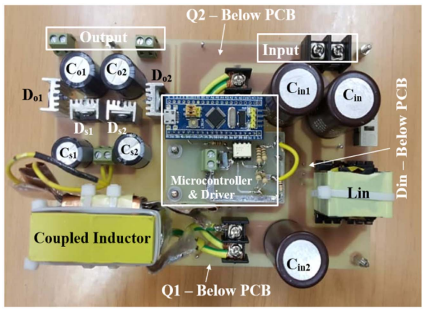


Fig. 7. Photograph of the prototype converter.

TABLE II
MAIN COMPONENTS SPECIFICATIONS OF THE PROTOTYPE CONVERTER

| Parameters/devices | Symbol | Specifications |
|---|---|---|
| Microcontroller | U1 | STM32F103C8T6 |
| Gate driver | HCPL 3120 | HCPL 3120 |
| MOSFETs | $Q_1$ and $Q_2$ | IRFP4227PBF (200 V–65 A–20 mΩ) |
| Input diode | $D_{in}$ | MUR3020 (200 V–30 A) |
| Output diodes | $D_{o1}$, $D_{o2}$, $D_{s1}$, and $D_{s2}$ | MUR860 |
| Input capacitors | $C_{in}$ | 220 μF |
| | $C_{in1}$ and $C_{in2}$ | 100 μF |
| Output capacitors | $C_{o1}$ and $C_{o2}$ | 47 μF |
| | $C_{s1}$ and $C_{s2}$ | 220 and 330 μF |
| Input inductor | $L_{in}$ | 200 μH (PQ32-30 core) |
| Coupled inductor | Coupled inductor | n = 2, $L_m$ = 60 μH, and $L_{lk}$ = 300 nH |

## IX. EXPERIMENTAL RESULTS

Fig. 7 and Table II, respectively, show a photograph of the prototype of the proposed converter and its main components specifications. Here, both power MOSFETs gate-drive signals can either be considered the same to simplify the circuit or a 180° phase shift in between them can be used to take advantages of the interleaved technique, in practice. The experimental results are given here, respectively, for both cases under the different conditions, as mentioned earlier and in the bottom row of the Table I for the proposed converter.

Figs. 8–10 show different experimental waveforms when $V_{\rm in}$ = 30 V, $P_o$ = 240 W, $V_o$ = 600 V, $f_s$ = 100 kHz, and the same gate-drive signals are applied to the prototype converter. Fig. 8 shows some experimental voltages and currents waveforms of the power semiconductor devices of the input stage of the prototype converter. Although the MOSFETs dominant switching losses occur during their transient turn-OFF times, as mentioned before, but they are switched ON with very low switching losses, as clearly shown in Fig. 8. It must be mentioned that some components, such as input inductor, input capacitor, and input diode, i.e., $L_{\rm in}$, $C_{\rm in}$, and $D_{\rm in}$,respectively, in the primary stage of the proposed converter are common here for all of its interleaved branches. Also, the input diode average current value is equal to the converter input dc current value. Therefore, for high output power and low input voltage applications, which leads to high input dc current values, some Schottky diodes can be connected properly in parallel instead of the input diode without any current sharing or thermal runaway issues, especially when they are assembled on a common heatsink. Also, using power MOSFETs as synchronous rectifier is another efficient approach to handle the high current values as well as to reduce the input diode power losses, in practice. Using more interleaved branches increases the frequencies of the input inductor current and input capacitor voltage. Consequently, smaller componnets can be used in practice to satisfy the necessary requirments. Also, the converter input dc current is equally divided between the main power MOSFETs or the primary coupled windings of the transformer.

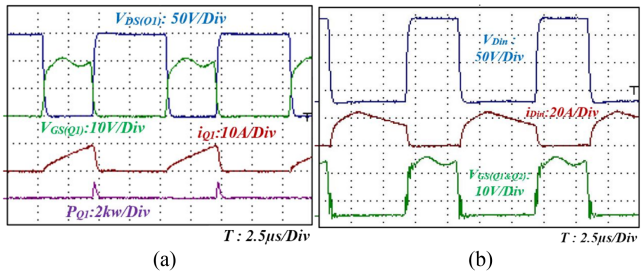


Fig. 8. Input stage key power semiconductor devices different voltages and currents waveforms: (a) MOSFET $Q_1$ gate-source and drain-source voltages, current, and power losses waveforms and (b) cathode–anode voltage waveform of the input diode $D_{\rm in}$, its current waveform, and $Q_1$ gate-source voltage signal, respectively.

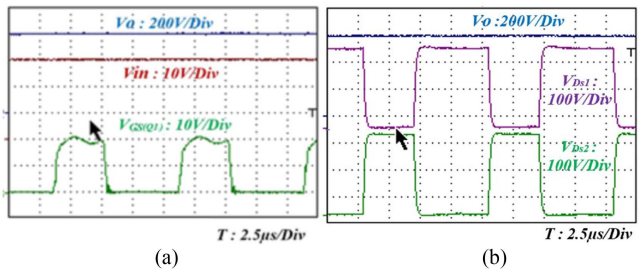


Fig. 9. (a) Prototype converter output and input voltages and MOSFET $Q_1$ gate-source voltage waveforms and (b) output voltage value and cathode–anode voltages waveforms of diodes $D_{s1}$ and $D_{s2}$, respectively.

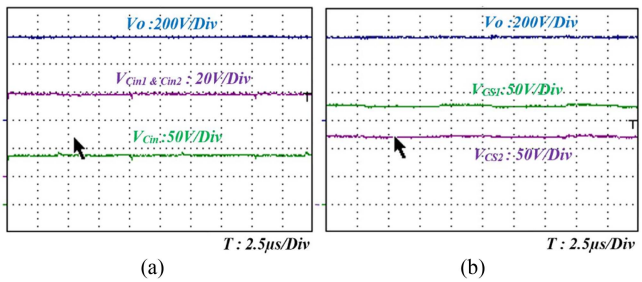


Fig. 10. Prototype converter input and output stages different capacitors voltages values: (a) output voltage and three different input capacitors voltages values, respectively and (b) output voltage and capacitors $C_{s1}$ and $C_{s2}$ voltages values, respectively.

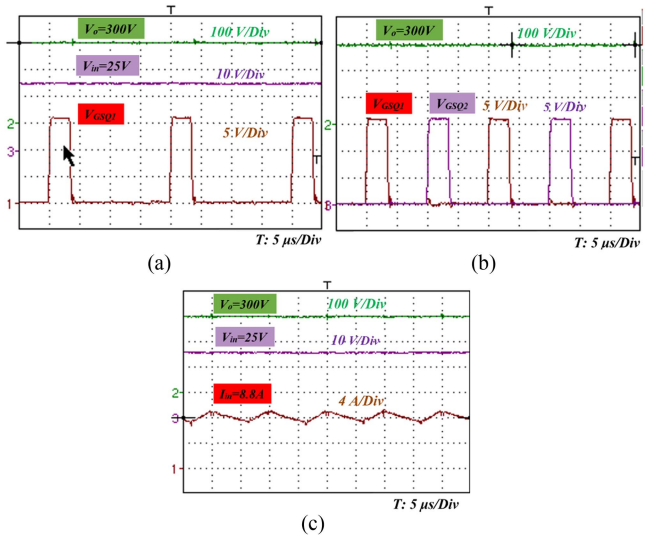


Fig. 11. (a) Output and input voltages values and MOSFET $Q_1$ gate-source voltage waveform, (b) output voltage value, MOSFETs $Q_1$ and $Q_2$ gate-sources voltages waveforms, and (c) output and input voltages values and the input current waveform, respectively.

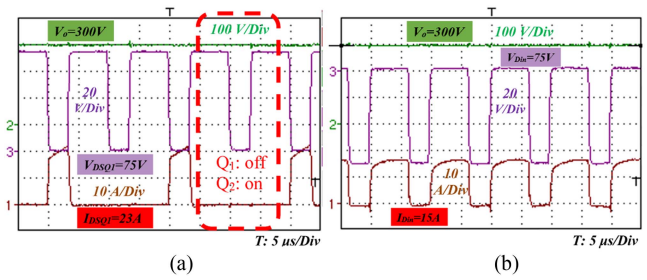


Fig. 12. Output voltage in addition of input stage key power semiconductor devices voltages and currents waveforms: (a) MOSFET $Q_1$ drain-source voltage and current waveforms and (b) input diode $D_{\text{in}}$ anode–cathode voltage and current waveforms, respectively.

Values of the converter input and output voltages as well as the MOSFET gate-source signal are also shown in Fig. 9(a). The cathode–anodes voltages waveforms of the output stage diodes of the prototype converter (i.e., $D_{s1}$ and $D_{s2}$) are also given in Fig. 9(b), in comparison with the output voltage. As clearly shown, low-voltage stresses are applied to these devices. Also, the prototype converter input and output stages different capacitors voltages values have been given in Fig. 10 in comparison with the output voltage.

Figs. 11–14 show different experimental waveforms when $V_{\text{in}} = 25$ V, $P_o = 200$ W, $V_o = 300$ V, $f_s = 50$ kHz, and a 180° phase shift in between the gate-drive signals is considered to apply to the prototype converter. Fig. 11 shows the values of the converter input and output voltages and input current waveform as well as the MOSFETs gate-source signals when $D = 0.333$. Using the interleaved technique effectively reduces the input current ripple value, as shown in Fig. 11(c).

Fig. 12 shows some experimental voltages and currents waveforms of the prototype converter, including its input stage power semiconductor devices voltages and currents waveforms, in addition of the converter output voltage value. As previously shown in Fig. 2, there is 180° phase shift in between the MOSFETs $Q_1$ and $Q_2$ gate-source voltages for a two-phase configuration of the converter under the interleaved control approach. When $Q_2$ is turned-ON by the control circuit, for instance, then both MOSFETs drain-source voltages are simultaneously equal to zero due to the coils mutual coupling effect. But, it should be mentioned that $Q_1$ cannot conduct the current during this subinterval without applying its gate-source voltage, as shown in Figs. 2 and 12(a). The same drain-source current waveform is achieved for $Q_2$ by considering 180° phase shift in between, which has not been shown here due to the absent of an extra current probe in our laboratory.

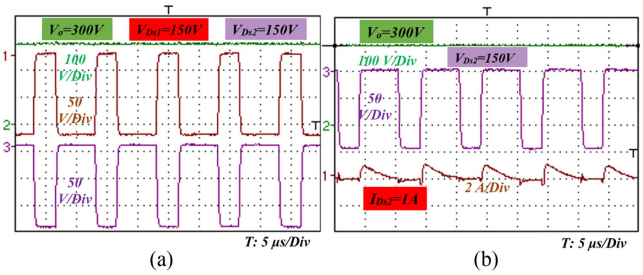


Fig. 13. Output voltage in addition of the output stage power diodes voltages and currents waveforms: (a) $D_{s1}$ and $D_{s2}$ anode–cathodes voltages and (b) output diode $D_{s2}$ anode–cathode voltage and current waveforms, respectively.

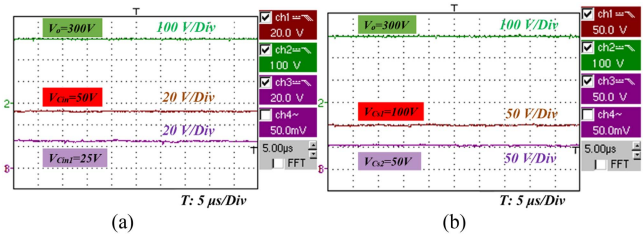


Fig. 14. Prototype converter output voltage and input and output stages different capacitors voltages values, $V_{\text{in}} = 25$ V, $P_o = 200$ W, and $f_s = 50$ kHz: (a) output voltage and input capacitors voltages values, and (b) output voltage and capacitors $C_{s1}$ and $C_{s2}$ voltages, respectively.

Fig. 13 shows voltages and currents waveforms of the two power diodes of the output stage of the prototype converter, in addition of the converter output voltage value. Furthermore, Fig. 13(b) shows the voltage and current waveforms of the output diode, $D_{s1}$. As clearly shown, low-voltage stresses are applied to these devices. Also, the prototype converter input and output stages different capacitors voltages values have been given and compared with the output voltage in Fig. 14.

The converter experimental efficiency curves have been plotted versus its output power in Fig. 15 for three different input voltage values, which clearly show that when the converter input voltage is increased currents amplitudes of the components of the circuit as well as their conduction losses, are decreased. Consequently, the converter efficiency is increased. To improve the converter efficiency, different components with low conduction losses can be used. In practice, a tradeoff between the converter cost and its efficiency can be done properly by choosing low-loss

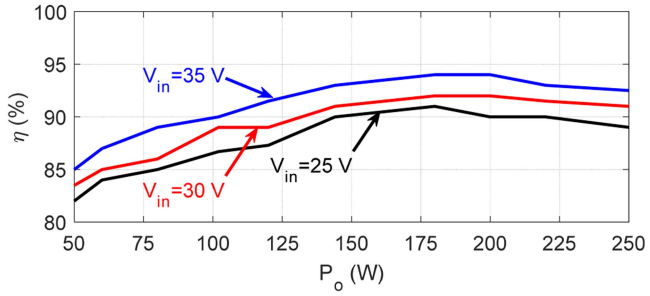


Fig. 15. Prototype converter experimental efficiency curves versus output power at three different input voltage values under the interleaved control approach when $V_o = 300$ V and $f_s = 50$ kHz.

inductors and transformers, low-ESR capacitors, as well as low $R_{ON}$ and low-drop voltage MOSFETs and diodes, to improve the converter efficiency by paying a reasonable cost.

## X. Conclusion

A quasi-z-source based high step-up converter has been introduced and mathematically analyzed here for high-voltage applications. High-voltage gain is achieved without using extreme duty cycle and high turns ratio values of the transformer. In addition, due to the low-voltage stresses on the components and the possibility of using multiple legs at the input stage of the given topology, low voltage, and current rating MOSFETs can be used. More legs in the primary stage can be used to reduce each MOSFET current stress and also to reduce the input current and output voltage ripples values to reduce the input inductor and filter and output capacitors volumes. Each switch can be switched ON and OFF like the interleaved converters, by taking into account proper phase shifts in between the gate-drive signals. It should be mentioned that the same gate-drive signals, without phase shift in between them, can also be applied to the switches to simplify the control circuit, but the input current and output voltage ripples values are increased, as compared to the interleaved control approach. Also, isolated input and output ports, recovery of the leakage inductances energies without using additional circuits, and reducing the reverse recovery problem of the output stage diodes are some other advantages of the given converter.

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