# A Three-Level *LLC* Converter With Flexible Variable-Mode Control for Wide Gain Range Application

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***Abstract*—Wide gain capability and full range efficiency are critical issues to *LLC* converters for wide-range applications. To address these issues, this article proposes a variable-mode controlled three-level *LLC* converter with two parallel diode-clamped legs. The proposed converter has four operation modes with different voltage gains, including the traditional frequency control mode and three new operation modes. With a deep analysis into the voltage gain and soft-switching characteristics of each operation mode, the designed flexible variable-mode control strategy can achieve soft switching and high efficiency over the wide gain range. Furthermore, it ensures smooth transitions among different modes and no surge current in the entire operating range. The effectiveness of the proposed method is investigated by a 400 V input, 8–65 V/1.5 kW output prototype. Experimental results show that the preliminary prototype achieves full zero-voltage-switching capability and maintains high efficiency over the whole output range.**

***Index Terms*—LLC converter, three-level, variable-mode control, wide gain range.**

## I. INTRODUCTION

IN RECENT years, the isolated dc–dc converter with high input voltage and wide gain range is required in many application fields, such as battery chargers for electrical vehicles [1], [2] and grid-connected systems in dc microgrids for photovoltaic and wind power generation [3], [4], [5]. At the same time, the converter is expected to meet the performance of high efficiency and high power density. The *LLC* resonant converter has attracted wide attention in academia and industry due to its simple topology and good soft-switching characteristics [6].

However, the gain adjustment capability of *LLC* resonant converter with conventional frequency control is limited, limiting its application in the wide gain range. First, the maximum voltage gain of the *LLC* converter is greatly affected by load, which is low under heavy load. Second, the gain adjustment capability of the *LLC* converter under light load is limited in the low voltage gain region, which leads to high switching frequency, high turn-OFF loss, and poor efficiency.

Many scholars have studied the gain range expansion of *LLC* converter, which can be divided into four categories: chopper topology transformation, resonant tank transformation, rectifier topology transformation, and variable-mode control.

*1) Chopper Topology Transformation:* The chopper gain is changed in these methods by modifying the full-bridge or half-bridge circuit on the primary side of the *LLC* converter. A bidirectional switch connecting the midpoint of input capacitors and the midpoint of a leg is added to the full-bridge *LLC* converter, which expands the gain range of the converter to the combination of a half-bridge and a full-bridge *LLC* converter [7]. The proposed converter in [8] is derived based on the switch integration technique, merging a buck–boost converter and a half-bridge *LLC* resonant converter. By adjusting the duty cycle of buck–boost, the input dc bus voltage of half-bridge *LLC* can be changed, and then the wide gain range can be realized. Similarly, the proposed converter in [9] is derived by integrating a two-phase interleaved boost converter and a full-bridge *LLC* converter by virtue of sharing the same full-bridge switching unit. The bus voltage can be changed by adjusting the duty cycle of the legs, so the gain characteristic is improved compared with the conventional full-bridge *LLC* converter.

*2) Resonant Tank Transformation:* These methods based on the strategy of resonant tank optimization enhance gain range by changing the structure of the resonant tank or the combination of multiple resonant branches. Hu et al. [10] proposed a modified *LLC* converter with two transformers in series, in which a bidirectional switch is paralleled with the primary winding of the second transformer. The turns ratio and the total magnetizing inductance of the resonant tank can be changed by controlling this switch to broaden the gain range. Sun et al. [11] proposed a novel *LLC* converter with two split resonant branches. The converter can operate in medium-gain mode or low-gain mode to regulate the input voltage in a wide range. Similarly, Khan et al. [12] proposed another *LLC* converter with dual resonant tanks. In [13], a resonant capacitor is connected in series with the magnetizing inductor of the *LLC* converter to be an *LCLC*

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resonant converter. As a result, the *LCLC* converter has a steeper gain curve and a wider gain range.

*3) Rectifier Topology Transformation:* The active switch is introduced in these methods to transform the original rectifier into a unit with gain adjustment capability to broaden the overall gain range. A hybrid rectifier in [14] connected on the secondary side of the transformer in an *LLC* converter can work in two operation modes. It operates as a voltage-doubler rectifier for rated output voltage and a bridge rectifier to achieve lower output voltage. A semiactive variable-structure rectifier is proposed in [15] for the *LLC* resonant converter to extend the output voltage range. The rectifier composed of two active switches and two diodes can operate as a voltage-doubler rectifier or voltage-quadrupler rectifier by changing the duty cycle of the active switches.

*4) Variable-Mode Control:* The variable-mode converters do not change the original topology structure but only switch the operation modes to achieve different gain ranges for different working environments. A novel *LLC* converter with multiple operation modes for wide voltage gain range application is proposed in [16]. The converter has three operation modes: dual full-bridge, full-bridge, and half-bridge operation modes, covering the high, medium, and low voltage gain range. Shi et al. [17] proposed a new hybrid control method that combines the burst-mode control and phase-shift control for the full-bridge *LLC* converter to realize a wide output voltage range. In [18] and [19], the variable-mode control strategy with three operation modes is adopted for the full-bridge *LLC* converter operating in a wide output range.

On the other hand, the conventional two-level *LLC* converter gradually cannot meet the input voltage requirements in the application fields due to the overvoltage limitation of the power devices. At present, multidevice series, multimodule series, or multilevel structure is commonly used to reduce the voltage stress of single power device. The topology control is relatively simple for the multidevice series structure, but the devices' static and dynamic voltage sharing should be considered. Similarly, the voltage sharing problem between modules exists in the multimodule series structure. The multilevel structure widely used has no voltage sharing problem despite more complicated control. Many scholars have studied the multilevel *LLC* converter applied in high input voltage and wide gain range. Jiang et al. [20] proposed a bidirectional three-level *LLC* resonant converter with the new pulse width and amplitude modulation control method. The converter can achieve a wide gain range as it has three operation modes with different voltage gains. Ren et al. [21] proposed a three-level dc–dc converter with dual outputs based on GaN devices to satisfy two standard dc bus voltage requirements in aircraft applications. It operates as an *LLC* converter in the low voltage mode and as a buck converter in the high voltage mode. In [22], a variable frequency multiplier technique is applied to a three-level *LLC* converter for wide input and output voltage ranges while preserving high efficiency. In [23] and [24], the analysis and design of a three-level *LLC* series resonant dc–dc converter for applications with high input voltage and wide gain range is presented. Haga and Kurokawa [25] proposed a modulation method for a full-bridge three-level *LLC* resonant converter to broaden the gain range of the converter. The topology can work in three-level and two-level modes to adapt to different voltage levels through the multimode hybrid modulation strategy.

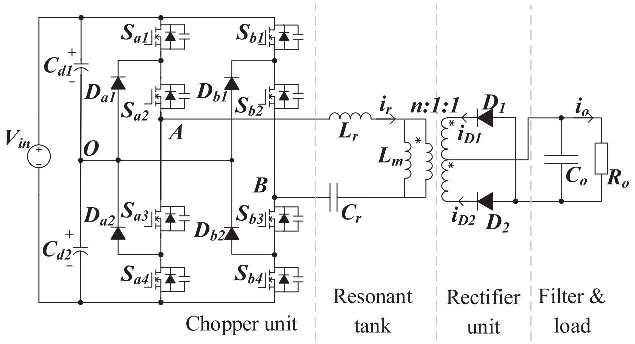


Fig. 1. *LLC* converter with two three-level diode-clamped legs in parallel.

This article proposes a variable-mode controlled three-level *LLC* resonant converter with two parallel diode-clamped legs for wide voltage gain range application. The converter can work in four operation modes with different voltage gains. Two flexible variable-mode control methods are designed to achieve a wide gain range while maintaining high efficiency. The advantages of the proposed converter can be summarized as follows:

1) wide voltage gain range to adapt to various applications;
2) reduced switching frequency range, which improves efficiency in the low voltage gain region;
3) half dc-bus voltage stress of switches and high power capacity brought by the three-level structure;
4) high operation efficiency, as zero voltage switching (ZVS) for all switches is guaranteed in the whole operation range;
5) smooth mode transitions in the proposed variable-mode control strategy.

The rest of this article is organized as follows. The operation principles of the proposed converter in each mode are analyzed in Section II. The performance analysis, including voltage gain, soft switching characteristic, current stress, and clamping diode, is presented in Section III. Two flexible variable-mode control strategies based on four operation modes are designed in Section IV, with the optimal mode transition method. The experimental results and evaluations from a 1.5-kW prototype are given in Section V to verify the feasibility of the proposed method. Finally, Section VI concludes this article.

## II. OPERATION PRINCIPLE

The proposed three-level *LLC* resonant converter is shown in Fig. 1, whose chopper unit is composed of two three-level diode-clamped legs in parallel. It can be considered that the voltages of input capacitors $C_{d1}$ and $C_{d2}$ are equal to half of the dc bus voltage when the capacitor voltage balance problem does not exist. In this case, there are five possible levels in the chopper output voltage $U_{AB}$: $V_{in}$, -$V_{in}$, $V_{in}$/2, -$V_{in}$/2, and 0. The withstand voltage of all single devices, including MOSFETs $S_{a1}$-$S_{b4}$ and diodes $D_{a1}$-$D_{b2}$, is half of the input dc bus. The topology can withstand 800 V dc bus input using the common

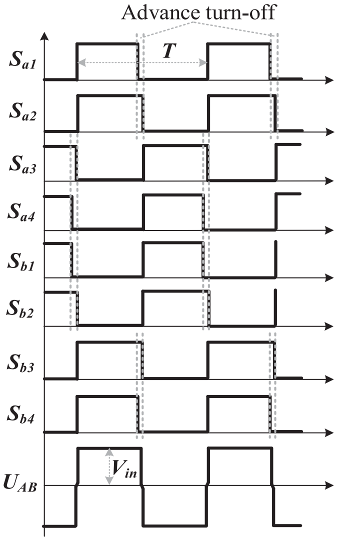


Fig. 2. Driving signals of switches and related waveforms in FBVF mode.

650 V silicon MOSFET, which matches the output bus voltage of common three-phase rectifiers.

It can be seen from the topology that its switching states are numerous, and it has the potential to realize a wide gain range through variable-mode control. However, introducing new operation modes may bring a series of adverse problems to the system. The adverse problems include the loss of soft-switching characteristics, capacitor voltage imbalance, and significant overshoot in the transient mode transition process, which will degrade the converter's performance and even make it unable to work. Therefore, the design of the variable-mode control scheme must be based on the analysis of gain range, soft switching characteristics, capacitor balance, mode transition, and other aspects. After detailed analysis and design, four operation modes introduced below are selected. Reasonable use of these operation modes can significantly expand the gain range of *LLC* converter while maintaining high efficiency.

### *A. Full-Bridge Variable Frequency Mode*

Full-bridge variable frequency (FBVF) mode is the most common operation mode, in which the system gain is adjusted by changing the switching frequency. As the operation mode is analyzed in detail in the literature [26], [27], [28], its specific working process and working waveform are no longer described. In this article, FBVF mode is chosen as the operation mode of the highest gain region. The converter remains in the mode before reaching the designed upper limit of the switching frequency.

As is shown in Fig. 2, the driving signals of the two switches in the same bridge arm, such as $S_{a1}$ and $S_{a2}$, are the same in FBVF mode. A minor adjustment, the advance turn-OFF of clamped switches, needs to be done to balance the static and dynamic voltage stress of the series switches with the same drive. Next, the specific process is illustrated, taking $S_{a1}$ and $S_{a2}$ as examples. When the switching state of $S_{a1}$ and $S_{a2}$ changes from ON-state to OFF-state, the voltage across $S_{a1}$ rises in advance due to its early turn-OFF. The voltage at the source of $S_{a1}$ is clamped by the midpoint of input capacitors due to the clamping diode $D_{a1}$ when the voltage across $S_{a1}$ rises to $V_{in}/2$. $S_{a2}$ is turned OFF after this process. Then the voltage across $S_{a2}$ rises from 0 to $V_{in}/2$, and the voltage at point A drops to 0, marking the end of the commutation process. Therefore, it is ensured that the voltages across $S_{a1}$ and $S_{a2}$ will not deviate much from $V_{in}/2$ in the static and dynamic states by turning off $S_{a1}$ in advance. This feature can also be realized for other switches using the same method.

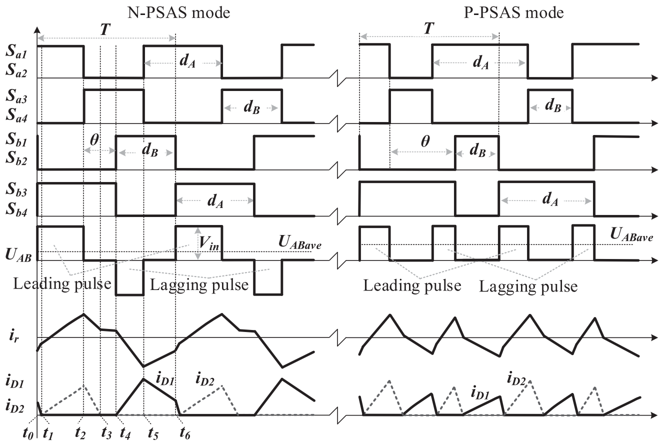


Fig. 3. Driving signals of switches and related waveforms in PSAS mode.

The output gain will be affected if the advance turn-OFF time $\Delta dt$ is too long, while the voltage stress of series switches may be unbalanced if too small. A reasonable value of $\Delta dt$ should be close to the voltage drop time of MOSFETs. The same method is used in the following operation modes, and the influence of $\Delta dt$ will be omitted in the following waveform and analysis as it is tiny.

### *B. Phase Shifted Asymmetry Mode*

Phase shifted asymmetry (PSAS) mode is proposed in this article, which combines phase shift control and asymmetric control that have been analyzed in detail in the literature [29], [30]. With the gain requirement decreasing continuously during operation in FBVF mode, the switching frequency will reach the upper limit. At this time, the converter enters PSAS mode to obtain a lower gain. Control schemes and related key waveforms of the converter in PSAS mode are shown in Fig. 3. The two switches in the same bridge arm also have the same driving signals in this mode, which means that there is no capacitor voltage balance problem as all switching states will not produce current to the neutral-point O in PSAS mode. A pair of complementary driving signals are applied to each leg's upper and lower bridge arms. The duty cycle of driving signals for $S_{a1}$ and $S_{a2}$ is $d_A$, while the duty cycle for $S_{a3}$ and $S_{a4}$ is $d_B$, equal to 1-$d_A$. The driving signals of $S_{b1}$ and $S_{b2}$ are obtained by backward phase-shifting $\theta$ from the driving signals of $S_{a3}$ and $S_{a4}$. PSAS mode proposed in the article has two control variables, namely phase shift angle $\theta$ and duty cycle $d_A$. The value range of $\theta$ is $[0, \pi]$. The value range of $d_A$ is [0.5, 0.75].

The chopper output voltage $U_{AB}$ is composed of two pulses: leading pulse and lagging pulse, within one switching cycle in

PSAS mode. According to the polarity of the lagging pulse, PSAS mode can be divided into N-PSAS mode and P-PSAS mode. The boundary condition is determined as the value of $d_A+\theta/(2\pi)$. When the value is less than 1, the lagging pulse is negative, and the converter is in N-PSAS mode. Otherwise, it is in P-PSAS mode. Therefore, the polarity of the lagging pulse changes from negative to positive and P-PSAS mode replaces N-PSAS mode with the increase of control variables $d_A$ and $\theta$.

There are six stages in one switching cycle for N-PSAS mode.

*Stage 1* ($t_0$-$t_1$)*:* Switches $S_{a1}$, $S_{a2}$, $S_{b3}$, and $S_{b4}$ on the primary side and diode $D_1$ on the secondary side are ON-state in the stage. The input voltage of resonant tank $U_{AB}$ is $V_{in}$, and the conduction current of $D_1$ decreases to 0.

*Stage 2* ($t_1$-$t_2$)*:* Diode $D_2$ starts conducting, while $D_1$ stops conducting at $t_1$. The resonant current $i_r$ becomes positive and continues to rise, as $U_{AB}$ is still $V_{in}$.

*Stage 3* ($t_2$-$t_3$)*:* $S_{a3}$ and $S_{a4}$ are turned ON, while $S_{a1}$ and $S_{a2}$ are turned OFF at $t_2$. Since the resonant current $i_r$ is above 0 at $t_2$, it will charge the junction capacitors of $S_{a1}$ and $S_{a2}$ first and then freewheels through the body diodes of $S_{a3}$ and $S_{a4}$ in dead time. Consequently, $S_{a3}$ and $S_{a4}$ can be turned ON with ZVS. As $U_{AB}$ is 0 in this stage, the resonant current $i_r$ drops, and the conduction current of $D_2$ decreases to 0.

*Stage 4* ($t_3$-$t_4$)*:* $D_2$ is turned OFF with ZCS at $t_3$. As $D_1$ and $D_2$ are OFF-state in this stage, the resonant current is equal to the excitation current and changes slowly.

*Stage 5* ($t_4$-$t_5$)*:* $S_{b1}$, $S_{b2}$, and $D_1$ are turned ON, while $S_{b3}$ and $S_{b4}$ are turned OFF at $t_4$. The value of resonant current at $t_4$ determines whether $S_{b1}$ and $S_{b2}$ can realize ZVS-ON. The ZVS-ON conditions can be satisfied by the good control parameter design in the next section. As $U_{AB}$ is -$V_{in}$ in this stage, the resonant current $i_r$ becomes positive and continues to rise, and the conduction current of $D_1$ rises.

*Stage 6* ($t_5$-$t_6$)*:* $S_{a1}$ and $S_{a2}$ are turned ON with ZVS, while $S_{a3}$ and $S_{a4}$ are turned OFF at $t_5$. The resonant current and the current of $D_1$ drop in this stage. $S_{b3}$ and $S_{b4}$ are turned ON with ZVS at $t_6$.

The control logic of N-PSAS mode and P-PSAS mode is the same, but the stages in one switching cycle are slightly different. The details of each stage in P-PSAS mode are not described here due to space limitations.

The average value of $U_{AB}$ will vary with the change of control variables, and its specific calculation expression is

$$U_{ABave} = V_{in}\left(d_A - d_B\right) = V_{in}\left(2d_A - 1\right). \tag{1}$$

It can be seen from (1) that the duty cycle $d_A$ directly determines the average output voltage $U_{AB\_ave}$, and the phase shift angle $\theta$ does not influence $U_{ABave}$.

By analyzing the control logic and waveforms of PSAS mode, we can obtain the following working characteristics.

1) The ZVS-ON characteristic of the leading-leg A is more accessible compared with the lagging-leg B.
2) For the switches $S_{b3}$ and $S_{b4}$ in the lower arm of lagging-leg B, the expansion of duty cycle $d_A$ makes up for the adverse effect of phase lag on ZVS-ON realization.
3) For the switches $S_{b1}$ and $S_{b2}$ in the upper arm of lagging-leg B, the increase of duty cycle $d_A$ and phase lag angle $\theta$ will reduce the freewheeling current before conduction, leading to the loss of ZVS-ON when the lagging pulse width is close to zero. However, with the further increase of $d_A$ and $\theta$, the lagging pulse width will expand positively after entering P-PSAS mode, making the freewheeling current before conduction rise again so that the ZVS-ON characteristic is restored.

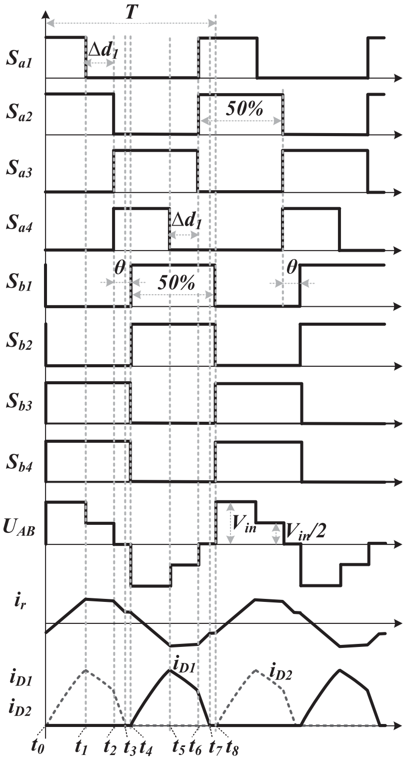


Fig. 4. Driving signals of switches and related waveforms in MPS mode.

In summary, PSAS mode reduces the chopper gain by introducing level 0 without the capacitor voltage balance problem. The switches $S_{b1}$ and $S_{b2}$ that is most difficult to realize ZVS-ON will lose ZVS-ON conditions when the lagging pulse width is close to zero, but this only occurs in a small area. In control, it is necessary to avoid entering the area where ZVS-ON is lost. The detailed calculation of soft-switching conditions will be given later.

### *C. Multilevel Phase Shift Mode*

The abovementioned two modes will not affect the neutral-point voltage but do not make full use of the multilevel characteristics of the circuit, as there is no level of $V_{in}$/2 in $U_{AB}$. Multilevel phase shift (MPS) mode is proposed, as is shown in Fig. 4. In order to balance the currents flowing into and out of the neutral-point O in one switching cycle, the symmetric multilevel mode must be used. Therefore, the asymmetric control is abandoned while the phase shift control is still adopted to expand the gain range. In MPS mode, the duty cycle of driving signals for all switches except $S_{a1}$ and $S_{a4}$ is 50%. $S_{a1}$ and $S_{a4}$

are turned on simultaneously with $S_{a2}$ and $S_{a3}$, respectively, but turned OFF in advance for some time. Multilevel duty cycle $\Delta d_1$ is defined as the ratio of the advance turn-OFF time to the switching period $T$, one of the control variables in MPS mode. The definition of phase shift angle $\theta$, another control variable in MPS mode, is almost the same as that in PSAS mode, i.e., the phase difference between the driving signals of $S_{a3}$ and $S_{b1}$. Three pairs of complementary driving signals are applied to $S_{a2}$ and $S_{a3}$, $S_{b1}$ and $S_{b3}$, and $S_{b2}$ and $S_{b4}$, respectively. At the same time, the driving signals of $S_{b1}$ and $S_{b2}$ are identical. The value range of $\theta$ is $[0, \pi]$. The value range of $\Delta d_1$ is [0, 0.5]. In order to ensure that the pulse width of level $V_{in}$ is greater than zero, the control variables need to satisfy the relational expression $\Delta d_1+\theta/(2\pi)<0.5$.

There are eight stages in one switching cycle for MPS mode.

*Stage 1* ($t_0$-$t_1$)*:* Switches $S_{a1}$, $S_{a2}$, $S_{b3}$, and $S_{b4}$ on the primary side and diode $D_2$ on the secondary side are ON-state in the stage. As the input voltage of resonant tank $U_{AB}$ is $V_{in}$, the resonant current and the conduction current of $D_2$ rise quickly.

*Stage 2* ($t_1$-$t_2$)*:* $S_{a1}$ is turned OFF at $t_1$. As the resonant current $i_r$ is positive, clamp diode $D_{a1}$ conducts, and the current flows out from the neutral-point O in this stage. $U_{AB}$ is $V_{in}$/2, and the resonant current $i_r$ decreases slowly.

*Stage 3* ($t_2$-$t_3$)*:* $S_{a3}$ and $S_{a4}$ are turned ON with ZVS, while $S_{a2}$ is turned OFF at $t_2$. The resonant current $i_r$ drops, and the conduction current of $D_2$ decreases quickly to 0 as $U_{AB}$ is 0 in this stage.

*Stage 4* ($t_3$-$t_4$)*:* $D_2$ stops conducting with ZCS at $t_3$. As $D_1$ and $D_2$ are both OFF-state in this stage, the primary side and secondary side of the transformer are separated, and the resonant current changes slowly. $S_{b1}$ and $S_{b2}$ are turned ON with ZVS at $t_4$.

Due to the symmetry, the operation principle of stages 5–8 in the next half switching cycle is similar to stages 1–4, except that the current direction differs. As a result, the details of stages 5–8 are not repeated here.

The waveform of $U_{AB}$ in MPS mode is symmetrical, and the average output voltage $U_{ABave}$ is 0. Therefore, the switches in MPS mode have more balanced current stress and better soft-switching characteristics. However, it is necessary to charge the resonant capacitor to establish the dc voltage component when MPS mode switches to other modes whose average output voltage is not 0.

The level $V_{in}$/2 is introduced in MPS mode, which reduces the rms of the fundamental component in $U_{AB}$. Compared with N-PSAS mode, MPS mode has a wider accessible gain range on the premise of ZVS-ON. In addition, MPS mode can realize ZCS-OFF of rectifier diodes by introducing the intermediate level, so the efficiency of the rectifier unit is relatively higher. Take stage 2 as an example. Due to the duty contraction of $S_{a1}$, the resonant current $i_r$ ends the rapid rise period in advance and starts to decrease slowly, which means that ZCS-OFF of rectifier diodes can be realized more easily. However, the conduction current will flow through the clamp diodes when the intermediate level is output. As a result, the conduction loss may be higher, which is a common disadvantage of the diode-clamped leg.

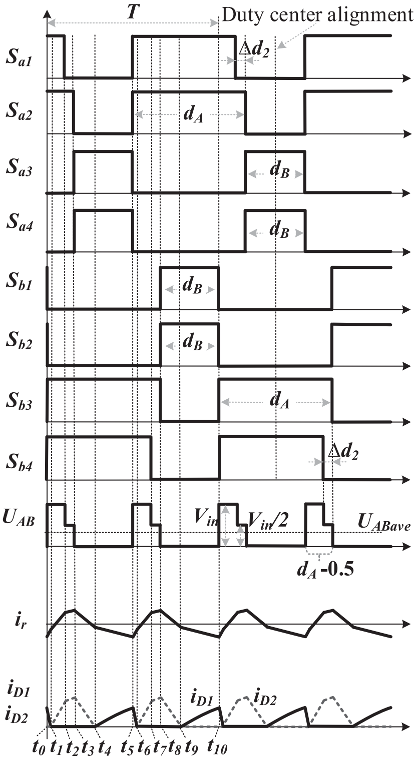


Fig. 5. Driving signals of switches and related waveforms in MFD mode.

The converter operating in MPS mode can realize the voltage balance of input capacitors $C_{d1}$ and $C_{d2}$. The current flows out from the neutral-point O in stage 2, while the current flows into the neutral-point in stage 6. Because the waveform is symmetrical and the duration of the two stages is the same, the total amount of current flowing into and out of the neutral-point O in one switching cycle is equal. Considering the slight potential shift caused by the actual circuit, the neutral-point potential can be stabilized by fine-tuning the multilevel duty cycle $\Delta d_1$ in a half-cycle.

### *D. Multilevel Frequency-Doubled Mode*

Multilevel frequency-doubled (MFD) mode is proposed as an operation mode in the low gain region under light and no-load conditions, as is shown in Fig. 5. When the PSAS mode reaches the endpoint, $\theta = \pi$, $d_A = 0.75$, it is equivalent to frequency-doubled control. At this time, keep the phase shift angle unchanged and reduce $d_A$. At the same time, the duty cycles of $S_{a1}$ and $S_{b4}$ are contracted from $d_A$ to $d_A$-$\Delta d_2$ to introduce the intermediate level. Multilevel duty cycle $\Delta d_2$ is defined as the ratio of the $V_{in}$/2 level time in half a switching cycle to the switching period $T$. The control variables in MFD mode are $d_A$ and $\Delta d_2$. The value range of $d_A$ is [0.5, 0.75]. The value range of $\Delta d_2$ is [0, 0.25]. Similarly, to ensure that the pulse width of level $V_{in}$ is greater than zero, the control variables need to satisfy the relational expression $d_A$ -$\Delta d_2$>0.5.

With the decrease of $d_A$ and increase of $\Delta d_2$, the average value and rms of $U_{AB}$ decrease so that the converter gain decreases. The formula in this mode for calculating the average value of

$U_{AB}$ is

$$U_{ABave} = V_{in}\left(2d_A - 1 - \Delta d_2\right). \tag{2}$$

There are ten stages in one switching cycle for MFD mode.

*Stage 1* ($t_0$-$t_1$)*:* Switches $S_{a1}$, $S_{a2}$, $S_{b3}$, and $S_{b4}$ on the primary side and diode $D_1$ on the secondary side are ON-state in the stage. The resonant current rises quickly.

*Stage 2* ($t_1$-$t_2$)*:* The current of diode $D_1$ decreases to 0, and $D_2$ conducts at $t_1$. The resonant current continues to rise as $U_{AB}$ is still $V_{in}$.

*Stage 3* ($t_2$-$t_3$)*:* $S_{a1}$ is turned OFF at $t_2$. Clamp diode $D_{a1}$ conducts, and the current flows out from the neutral-point O due to the positive resonant current, which means that the level of $V_{in}/2$ is output. The resonant current and current of $D_2$ rise slowly in this stage.

*Stage 4* ($t_3$-$t_4$)*:* $S_{a3}$ and $S_{a4}$ are turned ON with ZVS, while $S_{a2}$ is turned OFF at $t_3$. The resonant current and the current of $D_2$ decrease quickly.

*Stage 5* ($t_4$-$t_5$)*:* The current of $D_2$ decreases to 0, and $D_1$ conducts at $t_4$. The resonant current is reduced to negative and then continues to decrease. $S_{a1}$ and $S_{a2}$ are turned ON with ZVS at $t_5$.

The waveforms and operation principle of stages 6–10 in the next half switching cycle are the same as stages 1–5, which is not repeated here.

It is worth noting that switches $S_{a1}$, $S_{a2}$, $S_{b3}$, and $S_{b4}$ that are turned ON later in every half-cycle will lose ZVS-ON first as the control variables change. Therefore, the feasible range of control variables depends on the boundary of soft-switching characteristics, calculated in the following chapter. The operation mode that combines MFD and Burst control can be adopted if the low gain is needed under no-load conditions.

The converter in MFD mode can easily realize the voltage balance of input capacitors $C_{d1}$ and $C_{d2}$. The current flows out from the neutral-point O in stage 3, whereas the current flows into the neutral-point in stage 8. Due to the characteristic of frequency doubling, the two half-cycles in a switching cycle in MFD mode are the same, which means that the currents flowing in and out of the neutral-point O are equal. Similar to MPS mode, the method of fine-tuning duty cycle $\Delta d_2$ can be used to balance the input capacitor voltages in control.

## III. PERFORMANCE ANALYSIS

### A. Voltage Gain Analysis

The overall gain of the *LLC* resonant converter is obtained by multiplying chopper gain $M_C$, resonant tank gain $M_T$, and rectifier gain $M_R$. In the proposed wide-range flexible variable-mode technology, the structure of the rectifier unit does not change. Therefore, the gain expansion mainly comes from changing the resonant tank gain $M_T$ under frequency control and the chopper gain $M_C$ under variable-mode control.

First harmonic approximate (FHA) is a commonly used method for approximate analysis of gain expression in *LLC* converter. With the FHA method, the gain expression in FBVF mode can be derived as

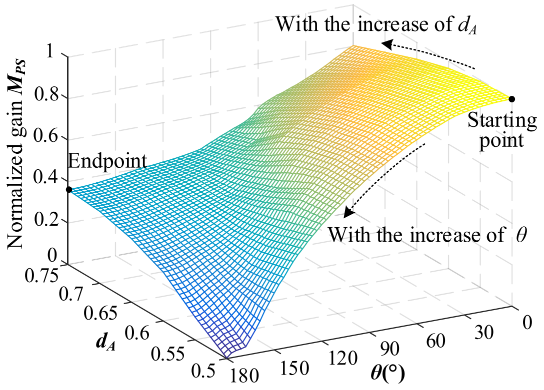


Fig. 6. Normalized chopper gain $M_{PS}$ in PSAS mode.

$$M_F = n\frac{V_o}{V_{in}} = \frac{L_n f_n^2}{\sqrt{\left[\left(L_n+1\right)f_n^2-1\right]^2+\left[\left(f_n^2-1\right)\frac{\sqrt{L_r/C_r}}{8n^2R_o}L_n f_n\right]^2}}. \tag{3}$$

$f_n = f_s(2\pi\sqrt{L_r C_r})$ is the normalized frequency; $f_s$ is the switching frequency; $L_n = L_m/L_r$ is the ratio of excitation inductance to resonance inductance. The meanings of other symbols are shown in Fig. 1.

Equation (3) is calculated when the chopper output is a symmetrical square wave, reflecting the relationship between the resonant tank gain $M_T$ and the switching frequency. When the converter is switched from FBVF mode to other operation modes, the chopper output waveform is no longer a symmetrical square wave. Therefore, it is necessary to use the Fourier decomposition method to calculate the ratio of the major harmonic rms in the chopper output waveform to that in the symmetrical square wave. This ratio can be called normalized chopper gain, which can characterize the gain expansion.

*1) PSAS Mode:* According to the abovementioned method and the waveform of $U_{AB}$ in Fig. 3, the normalized chopper gain of PSAS mode is calculated as

$$M_{PS} = \sqrt{\left(\sin\pi d_A\cos\frac{\theta}{2}\right)^2+\left(\frac{1}{2}\sin 2\pi d_A\cos\theta\right)^2}. \tag{4}$$

Since the starting point and ending point in PSAS mode are traditional frequency control and frequency-doubled control, respectively, the first and second harmonic components in PSAS mode are significant, so they are all considered in (4). As the influence of high order harmonic components is ignored, the voltage gain calculated by (4) has errors, which is suitable for preliminary analysis of gain design. The normalized chopper gain $M_{PS}$ can be obtained more accurately by simulation. The variation of chopper gain $M_{PS}$ with phase shift angle $\theta$ and duty $d_A$ is shown in Fig. 6. These data in the figure are collected from the simulation software PLECS. The control variables ($d_A$, $\theta$) change from starting point (0.5, 0) to the endpoint (0.75, $\pi$), and

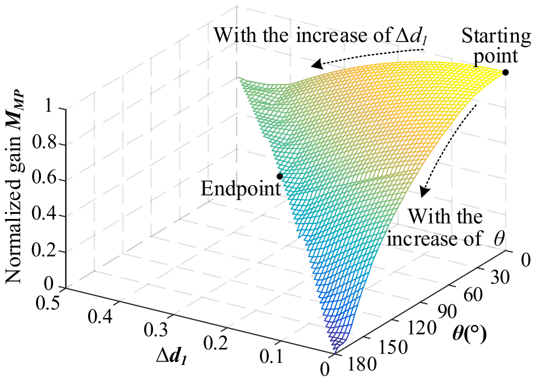


Fig. 7. Normalized chopper gain $M_{MP}$ in MPS mode.

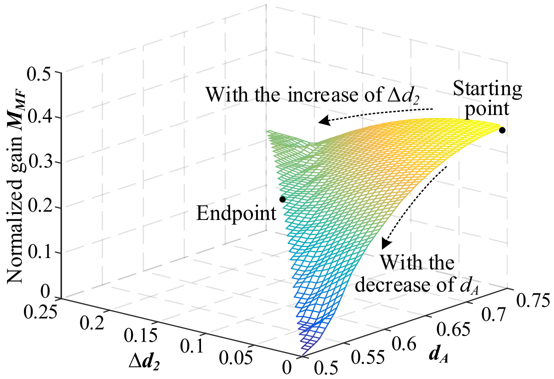


Fig. 8. Normalized chopper gain $M_{MF}$ in MFD mode.

the control path needs to be determined by combining gain and soft switching analysis.

*2) MPS Mode:* The first harmonic is the main component of the chopper output waveform in MPS mode. Therefore, considering only the first harmonic component, the normalized chopper gain of MPS mode is calculated as

$$M_{MP} = \frac{\sqrt{2}}{8}\sqrt{17 + 15\cos(2\pi\Delta d_1 + \theta)}. \tag{5}$$

Similarly, a more accurate voltage gain can be obtained by simulation, as shown in Fig. 7. The starting point for control variables $(\Delta d_2, \theta)$ is (0, 0), and the endpoint is determined below.

*3) MFD Mode:* Due to the frequency-doubled effect in MFD mode, the second harmonic is the main component of the chopper output waveform. Considering only the second harmonic component, the normalized chopper gain of MFD mode is calculated as

$$M_{MF} = \frac{1}{8}\sqrt{2 + 2\cos(8\pi d_A - 4\pi\Delta d_2)}. \tag{6}$$

The graph of voltage gain changing with control variables $d_A$ and $\Delta d_2$ obtained by simulation is shown in Fig. 8. The starting point for control variables ($\Delta d_2$, $d_A$) is (0, 0.75), and the endpoint is also determined below.

### *B. Soft Switching Analysis*

The control boundary of each mode for ZVS-ON needs to be determined considering the operation efficiency and stability of the converter, as soft switching conditions may be lost under some control variable values. Many papers have done the soft switching analysis of FBVF mode, so it is not repeated here, and the analysis of other modes is as follows.

*1) PSAS Mode:* As mentioned earlier, switches $S_{b1}$ and $S_{b2}$ are the most difficult to satisfy ZVS-ON conditions. All switches guarantee ZVS-ON conditions when $S_{b1}$ and $S_{b2}$ that are mainly analyzed next realize ZVS-ON. ZVS-ON is mainly related to these factors: the current at the switching time, equivalent DS capacitance of MOSFET, resonant capacitance, and dead time.

First, the N-PSAS mode is analyzed. According to the energy transfer relationship, to realize ZVS-ON, the turn-OFF current $I_{\mathrm{OFF}}$ must meet the following conditions:

$$2C_{ds}V_{in}^2 \le (L_r + L_m)I_{\mathrm{off}}^2 - I_{\mathrm{off}}U_{c0}\Delta t. \tag{7}$$

$C_{ds}$ is the equivalent DS junction capacitance of MOSFET; $U_{c0}$ is the resonant capacitor voltage at the switching time. Its value can be a simulation value or a computable conservative value, such as the peak value of resonant capacitor voltage at equal resonance; $\Delta t$ is the charge and discharge time of the equivalent DS junction capacitor. To calculate the minimum value of $I_{\mathrm{OFF}}$, the case that the current is zero at the end of charging and discharging is considered. At this time, the average charging current is $0.5I_{\mathrm{OFF}}$. Therefore, the calculated value of $\Delta t$ is $4C_{ds}V_{in}$ / $I_{\mathrm{OFF}}$.

A conservative condition of turn-OFF current $I_{\mathrm{OFF}}$ for realizing ZVS-ON in N-PSAS mode is

$$I_{\mathrm{off}} \ge \sqrt{\frac{2C_{ds}(V_{in}^2 + 2\pi V_o I_o\sqrt{L_r/C_r})}{L_r + L_m}}. \tag{8}$$

$V_o$ and $I_o$ are the output voltage and current in the *LLC* converter.

Similarly, the ZVS-ON condition in P-PSAS mode is

$$I_{\mathrm{off}} \ge \sqrt{\frac{2C_{ds}(3V_{in}^2 + 2\pi V_o I_o\sqrt{L_r/C_r})}{L_r}}. \tag{9}$$

Because the resonant current changes very slowly when the secondary current is zero, such as in stage 4 of N-PSAS mode, the current change is ignored to simplify the analysis. In the calculation, the output voltage is regarded as constant. A conservative value is selected for the resonant capacitor voltage in each stage, so the change of resonant inductor current is approximately linear. Under these approximate conditions, the relationship between turn-OFF current $I_{\mathrm{OFF}}$ and control variables can be obtained. Therefore, a set of sufficient conditions for realizing ZVS-ON are

$$\begin{cases} \frac{\frac{\theta}{2\pi}(1-d_A)(1-d_A-\frac{\theta}{2\pi})T_s V_{in}}{L_r} \ge \\ \sqrt{\frac{2C_{ds}(V_{in}^2+2\pi V_o I_o\sqrt{\frac{L_r}{C_r}})}{L_r+L_m}},\ d_A + \frac{\theta}{2\pi} < 1 \\ \frac{(d_A+\frac{nV_o}{\pi V_{in}})(1-d_A)(d_A+\frac{\theta}{2\pi}-1)T_s(V_{in}-\frac{nV_o}{2(1-d_A)})}{L_r} \ge \\ \sqrt{\frac{2C_{ds}(3V_{in}^2+2\pi V_o I_o\sqrt{\frac{L_r}{C_r}})}{L_r}},\ d_A + \frac{\theta}{2\pi} > 1 \end{cases}. \tag{10}$$

TABLE I
SUMMARY OF FOUR OPERATION MODES

| Operation Mode | Levels of $U_{AB}$ | Control Variables | Neutral-point Potential | Average value of $U_{AB}$ | ZVS-ON of MOSFETs | Suitable Gain Range | Output Voltage Range |
|---|---|---|---|---|---|---|---|
| FBVF | $V_{in}$, and $-V_{in}$ | $f_s$ [75, 200] | Noninfluence | 0 | Full range | High gain region | 65 V to 37 V |
| PSAS | $V_{in}$, $-V_{in}$, and 0 | $d_A$ [0.5,0.75]<br>$\theta$ [0, π] | Noninfluence | $V_{in}(2d_A-1)$ | Full range | Medium and low gain region | 37 V to 13.5 V |
| MPS | $V_{in}$, $-V_{in}$, $V_{in}/2$, $-V_{in}/2$, and 0 | $\Delta d_1$ [0,0.5]<br>$\theta$ [0, π] | Influence | 0 | Full range | Medium gain region | 37 V to 17.5 V |
| MFD | $V_{in}$, $V_{in}/2$, and 0 | $d_A$ [0.5,0.75]<br>$\Delta d_2$ [0,0.25] | Influence | $V_{in}(2d_A-1-\Delta d_2)$ | Full range | Low gain region | 13.5 V to 8 V |

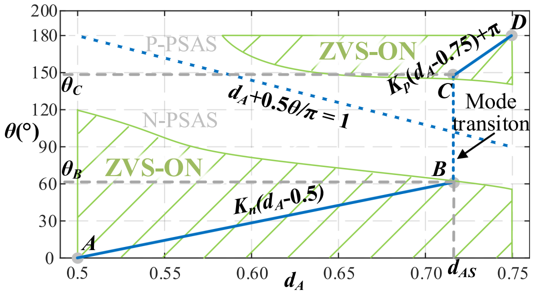


Fig. 9. ZVS-ON zone in PSAS mode.

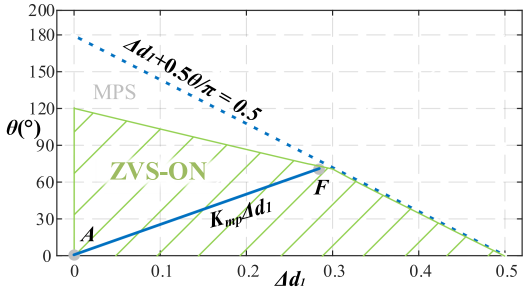


Fig. 10. ZVS-ON zone in MPS mode.

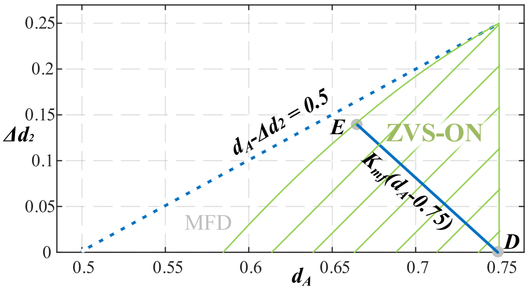


Fig. 11. ZVS-ON zone in MFD mode.

The preliminary design of converter parameters can use (10), and more accurate ZVS-ON conditions can be obtained by simulation based on these parameters. The ZVS-ON zone is drawn in Fig. 9, taking the parameters of the prototype introduced later as an example.

Considering the ZVS-ON condition, the control path in PSAS mode can adopt curve AB-CD, which determines the relationship between two control variables. Because the dc voltage of the resonant capacitor is only related to $d_A$ and has nothing to do with $\theta$, $d_A$ should change continuously in the control range, but $\theta$ can change suddenly. Therefore, the two control variables change continuously with a linear relationship in AB and CD, while there is a sudden change of $\theta$ between B and C. The transition process from B to C will be described in detail later. The boundary value $d_{AS}$ at the switching time from B to C needs to be determined, and then the slopes of $K_n$ and $K_p$ can be determined accordingly. The selection principle of $d_{AS}$ is to make the gain range of N-PSAS mode with high efficiency as large as possible and the gain difference before and after switching as small as possible. It can be determined by combining the gain graph with the ZVS-ON graph.

*2) MPS Mode:* Based on the soft switching analysis of PSAS mode and the consideration of the $V_{in}/2$ level stage, the sufficient condition for ZVS-ON in MPS mode can be obtained as

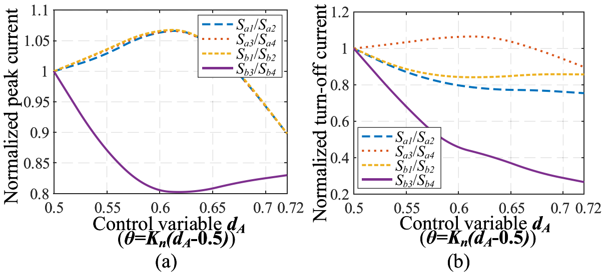
$$\frac{(\frac{\theta}{8\pi}-\frac{\Delta d_1}{2})(0.5-\frac{\theta}{2\pi})T_s V_{in}}{L_r} \geq \sqrt{\frac{2C_{ds}(V_{in}^2+2\pi V_o I_o\sqrt{\frac{L_r}{C_r}})}{L_r+L_m}}. \tag{11}$$

The ZVS-ON zone in MPS mode obtained by simulation is drawn in Fig. 10. Point F in the figure is the operating point with the lowest gain in the ZVS-ON zone, which is selected as the endpoint of MPS mode. Therefore, the control path in MPS mode can adopt curve AF, and the value of $K_{MP}$ can be determined accordingly.

*3) MFD Mode:* The same method as abovementioned is adopted in MFD mode. By approximately linearizing the inductor current, the sufficient condition for ZVS-ON can be obtained as

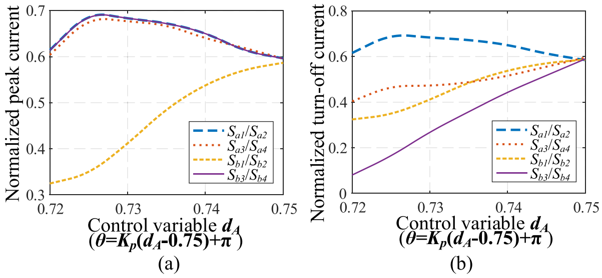
$$\frac{\left[nV_o - V_{in}(2d_A - 1 - \frac{\Delta d_2}{2})\right]^2 T_s}{L_r} \geq \sqrt{\frac{2C_{ds}(3V_{in}^2+2\pi V_o I_o\sqrt{\frac{L_r}{C_r}})}{L_r}}. \tag{12}$$

The ZVS-ON zone in MFD mode is drawn in Fig. 11. Similarly, the operating point with the lowest gain in the ZVS-ON zone is selected as the endpoint of MFD mode to obtain the widest gain range. The curve DE in the figure is the control path.



(a) (b)

Fig. 12. Normalized current stress in N-PSAS mode. (a) Peak current. (b) Turn-OFF current.



(a) (b)

Fig. 13. Normalized current stress in P-PSAS mode. (a) Peak current. (b) Turn-OFF current.

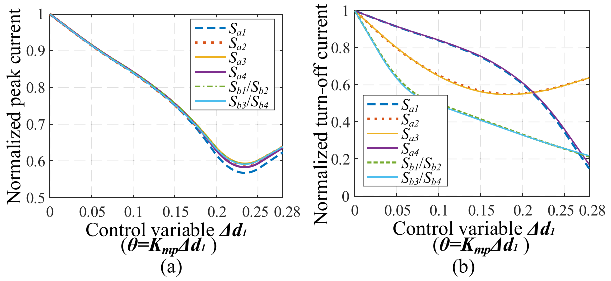
## C. Current Stress Analysis

The current stress of each switch is the same when the *LLC* converter is in FBVF mode, which is an advantage of traditional frequency control. However, besides FBVF mode, several new operation modes with different current stress characteristics are introduced to expand the gain range in this article. In these modes, the peak currents of switches may be different, which will lead to different ultimate stresses of the devices. Similarly, the switching currents may be unbalanced when the switches are turned OFF. The excessive turn-OFF current will cause a significant turn-OFF loss, and the small turn-OFF current may cause the loss of ZVS-ON condition for other switches in the same leg. Therefore, it is necessary to quantitatively analyze each switch's peak current and turn-OFF current in different operation modes.

In this section, a series of simulation work is done. In order to analyze the results more intuitively, the current values of each mode are normalized, and the selected reference value is the current value of FBVF mode at the same switching frequency. The load current is constant during changing control variables according to the designed path in each mode, and the output voltage changes with the gain.

*1) PSAS Mode:* Figs. 12 and 13 show the curves of peak current and turn-OFF current changing with control variables in N-PSAS mode and P-PSAS mode, respectively. The horizontal axis in the figures only shows the change of the control variable $d_A$, but in fact, another control variable $\theta$ also changes correspondingly according to the designed path. The same is true for the figures of other modes below.

The analysis shows that the N-PSAS mode has the characteristic of current imbalance. In Fig. 12(a), the peak currents of all switches except $S_{b3}$ and $S_{b4}$ first increase and then decrease, whose maximum values are about 1.06 times the peak current in FBVF mode at the same frequency. Therefore, the peak currents in N-PSAS mode do not increase significantly, and the current stress is in an acceptable range. In Fig. 12(b), the turn-OFF current of $S_{a3}$ and $S_{a4}$, whose maximum value is also about 1.06 times the reference value, is slightly higher than the reference value when $d_A$ is less than 0.67. The turn-OFF currents of other switches are always less than the reference value. Therefore, the turn-OFF currents and their corresponding turn-OFF loss in N-PSAS mode do not increase significantly. In addition, it is worth noting that the turn-OFF current of $S_{b3}$ and $S_{b4}$ is the lowest in the switches and decreases with the increase of the control variables, which means that the freewheeling current that can be used to complete ZVS-ON operations of $S_{b1}$ and $S_{b2}$ is small. The result proves the previous analysis conclusion: it is the most difficult to realize ZVS-ON conditions for MOSFETS $S_{b1}$ and $S_{b2}$.



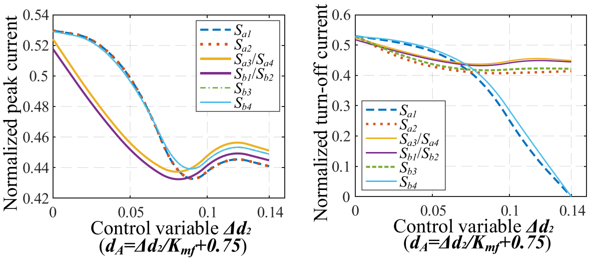
(a) (b)

Fig. 14. Normalized current stress in MPS mode. (a) Peak current. (b) Turn-OFF current.

As shown in Fig. 13, the peak currents and turn-OFF currents of MOSFETS in P-PSAS mode are always less than the reference value, which indicates that this mode has no higher requirement for the current stress of power devices. The endpoint of P-PSAS mode, frequency-doubled control, does not have the problem of device current imbalance, so the device currents gradually converge to equal value with control variables increasing. Similarly, it is concluded in P-PSAS mode that $S_{b1}$ and $S_{b2}$ are the most difficult to realize ZVS-ON.

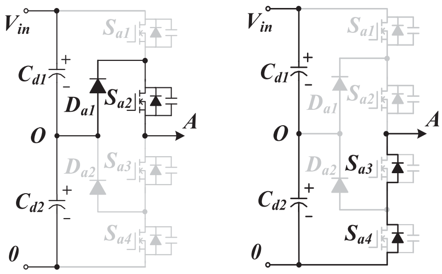
*2) MPS Mode:* Fig. 14 shows the peak current and turn-OFF current curves in MPS mode. The results show that the peak currents of each switch in MPS mode are almost the same and lower than the reference value. At the same time, compared with PSAS mode, the turn-OFF currents of each device in MPS mode are closer and will not exceed the reference value. The current stress performance in MPS mode is better than that in PSAS mode because the chopper output voltage and resonant tank current in MPS mode are positive and negative half-cycle symmetric.

*3) MFD Mode:* Fig. 15 shows the peak current and turn-OFF current curves in MFD mode. As the mode is in the low gain range, each switch's peak currents and turn-OFF currents are below half of the reference value in most cases. At the same time, the imbalance of device currents is not significant. It can be seen from Fig. 15(b) that the turn-OFF currents of $S_{a1}$ and $S_{b4}$ continuously decrease to 0. However, due to multilevel mode, $S_{a2}$ and $S_{b3}$ are still ON-state after $S_{a1}$ and $S_{b4}$ are turned OFF.



(a) (b)

Fig. 15. The normalized current stress in MFD mode. (a) Peak current. (b) Turn-OFF current.



(a) (b)

Fig. 16. Working state of input clamping diodes. (a) "0100" switching state. (b) "0000" switching state.

Therefore, the small turn-OFF currents of $S_{a1}$ and $S_{b4}$ do not affect the ZVS-ON of any other switches.

### D. Clamping Diode Analysis

There are clamping diodes $D_{a1}$, $D_{a2}$, $D_{b1}$, and $D_{b2}$ on the input side of the converter. It can be proved that clamping diodes can realize ZCS-OFF in the whole working process, which ensures the high efficiency of the converter. The following analysis takes $D_{a1}$ as an example.

Fig. 16 shows the commutation diagram of the input clamping diode $D_{a1}$. The positive current flows through $D_{a1}$ and $S_{a2}$ in the first stage when the switching state of $S_{a1}$ to $S_{a4}$ is "0100". $S_{a2}$ is turned OFF and enters the dead time in the next stage when the switching state is "0000". After $S_{a2}$ is turned OFF, body diodes of $S_{a3}$ and $S_{a4}$ start conducting due to the freewheeling effect. In this process, $D_{a1}$ will not withstand the reverse voltage, and its conduction current will drop to 0 with the turn-OFF of $S_{a2}$. Therefore, clamping diode $D_{a1}$ can realize ZCS-OFF. In the control logic of all operation modes used in this article, the following switching action after $D_{a1}$ conducts is the turn-OFF of $S_{a2}$. There is no case where the reverse voltage cuts off $D_{a1}$, so $D_{a1}$ always maintains ZCS-OFF characteristics. Similarly, other clamping diodes can also realize ZCS-OFF. Therefore, the switching loss of the input side clamping diodes is slight.

After the abovementioned introduction and analysis, the four operating modes and their suitable gain ranges are summarized in Table I.

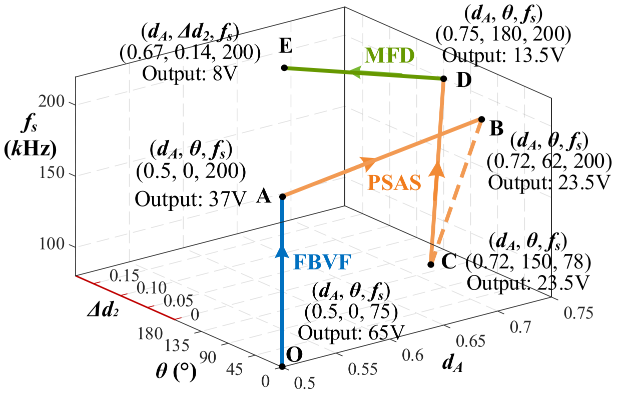


Fig. 17. First variable-mode control scheme. (Arrows in the figure represent the direction of gain decrease.).

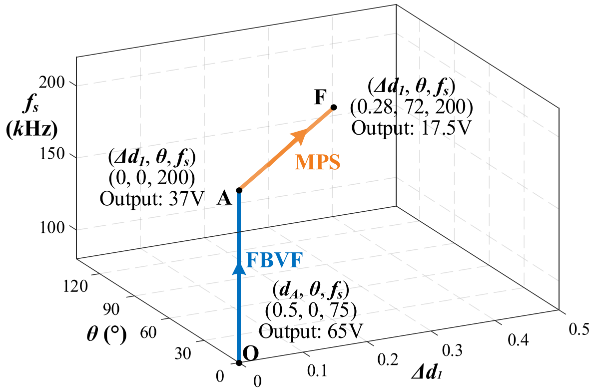


Fig. 18. Second variable-mode control scheme.

## IV. FLEXIBLE VARIABLE-MODE CONTROL

### A. Flexible Variable-Mode Control Method

Based on the abovementioned operation mode design and performance analysis, two flexible variable-mode control schemes in Figs. 17 and 18 are proposed in this article. Both control schemes can achieve a gain range far beyond traditional frequency control. Due to the different operation modes, the two control schemes have different characteristics. The first control scheme can be selected in the system with a tremendous demand for the gain range because it can achieve a wider gain range. The second control scheme has a smaller gain range than the first, but it has more straightforward control and better performance. The second control scheme can be preferred when its gain range can meet the system requirements.

The first control scheme combines FBVF, PSAS, and MFD operation modes. The conventional FBVF mode is used as the operation mode in the highest gain region, and the control variable is the switching frequency $f$. With the gain demand decreasing continuously, the switching frequency increases until it reaches the upper limit $f_{\max}$. Then, the converter enters PSAS mode. PSAS mode can be divided into two regions: N-PSAS and P-PSAS. The switching frequency is kept at the highest value while the phase shift angle $\theta$ and duty cycle $d_A$ gradually increase according to the designed path to reduce the gain in the N-PSAS region. After reaching the control boundary of

TABLE II
PARAMETERS AND COMPONENTS OF THE PROTOTYPE

| Parameters | Value | Parameter | Value |
|---|---|---|---|
| Input voltage $V_{in}$ | 400 V | Output capacitor $C_o$ | 84 uF |
| Output voltage $V_o$ | 65 V–8 V | Resonant capacitor $C_r$ | 80 nF |
| Maximum power | 1.5 kW | Resonant inductor $L_r$ | 31 uH |
| Rated current | 25 A | Magnetic inductor $L_m$ | 125 uH |
| Transformer turn ratio | 14:2:2 | Resonant frequency $f_r$ | 101 kHz |
| Dead time | 210 ns | Maximum frequency | 200 kHz |
| MOSFETs $S_{a1\text{-}b4}$ | IPP410N30N | Clamped Diodes $D_{a1\text{-}b2}$ | IDH20G65C5 |
| Secondary diodes $D_{1\text{-}2}$ | SBR40U200CTB | Digital signal processor | TMS320F280049 |
| Core of transformer | PQ40/40 | Core of inductor | PQ32/30 |

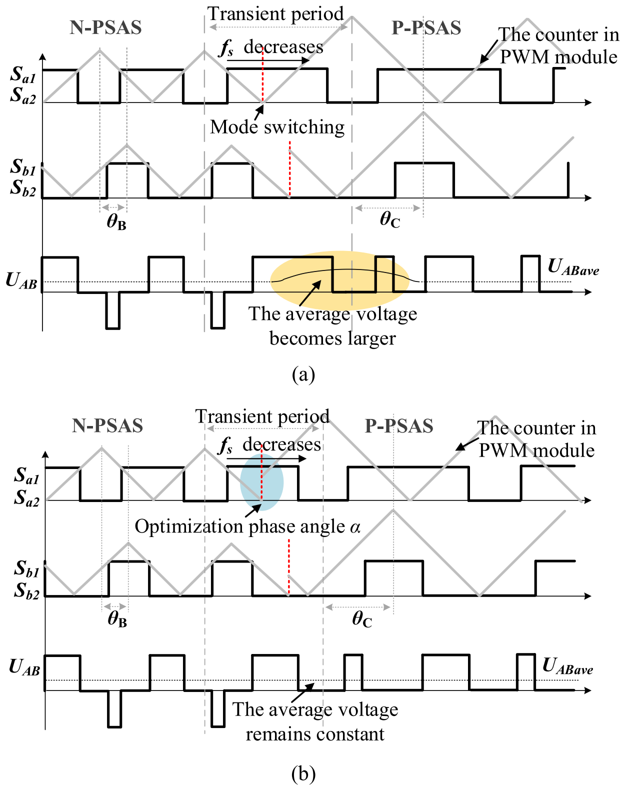
the N-PSAS region, $d_A$ still changes smoothly. However, $\theta$ transitions to the boundary value of the P-PSAS region, and the switching frequency decreases correspondingly to maintain the gain continuity. Then, $\theta$, $d_A$, and $f_s$ continue to increase in the P-PSAS region until $\theta = \pi$, $d_A = 0.75$, and $f_s = f_{\max}$, which is the endpoint of PSAS mode. Finally, the converter enters MFD mode to realize the lowest gain output. The control variables $d_A$ and $\Delta d_2$ in MDF mode increase until the ZVS-ON condition is no longer satisfied. The overall control logic and path for the first control scheme are shown in Fig. 17. The first variable-mode control scheme with the parameters in Table II can achieve a gain range from 65 V to 8 V under a resistor load, while the traditional frequency control can only achieve a gain range from 65 V to 37 V.

The second control scheme combines FBVF and MPS operation modes. The control path of the high gain region is the same as the first control scheme. The difference is that the converter will enter MPS mode when the switching frequency reaches the upper limit in FBVF mode. Then, the phase shift angle $\theta$ and multilevel duty cycle $\Delta d_1$ increase according to the designed path until reaching the boundary of the ZVS-ON zone. The overall control logic and path for the second control scheme are shown in Fig. 18. The second variable-mode control scheme with the parameters in Table II can achieve a gain range from 65 V to 17.5 V under a resistor load.

The designed variable-mode control schemes ensure gain continuity on the premise of ZVS-ON. Due to the continuous gain, the output voltage changes continuously without a sudden jump during mode transitions, which is the prerequisite of the variable mode control scheme.

## *B. Mode Transition*

In order to achieve a wide gain range under ZVS conditions, the converter needs to be switched between different operation modes. These mode transition processes are flexible in the proposed variable-mode control method, ensuring smooth transitions among different modes and no surge current in the entire operating range. It can be seen that the endpoint of FBVF mode is the starting point of PSAS mode and MPS mode (see Point A in Figs. 17 and 18). Similarly, the endpoint of PSAS mode is the starting point of MFD mode (see Point D in Fig. 17). For example, the driving signals of switches in PSAS mode when the control variables $d_A = 0.75$ and $\theta = 180°$ are exactly the same as those in MFD mode when the control variables $d_A = 0.75$ and $\Delta d_2 = 0$. Therefore, the variable-mode control schemes in the article have the continuity of control variables, which means seamless transitions for different operation modes. The only mode transition process to be considered is the switching from N-PSAS to P-PSAS in PSAS mode (see Point B to Point C in Fig. 17).



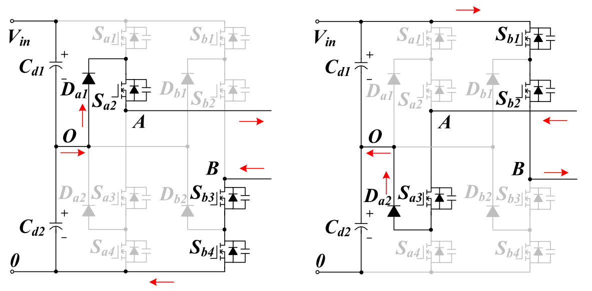
(a)

(b)

Fig. 19. Comparison of two mode switching methods. (a) Direct switching method. (b) Phase optimization switching method.

When the N-PSAS mode is switched to the P-PSAS mode, there will be a sudden change in the phase shift angle from $\theta_B$ to $\theta_C$, as shown by the dotted line in Fig. 9. Meanwhile, the switching frequency will decrease to make up for the gain gap. According to (1), in theory, the average values of $U_{AB}$ in one switching cycle before and after the mode transition are the same, so the dc voltage of the resonant capacitor is unchanged, and the direct switching without current overshoot can be realized. However, the modulation effect of the actual PWM module will cause the average value of $U_{AB}$ to change in the transient period, which will cause a terrible transient process and overshoot.

Fig. 19(a) shows the actual mode transition process in the digital PWM module. In practical application, the digital PWM module usually changes the values of Period Register and Compare Register at the zero-crossing point and the period point. The value of the Period Register increases since the switching frequency decreases after the mode transition. The duty cycle and modulation mode remain unchanged, so the high-level time after the transition is longer than before. In this case, the average value of $U_{AB}$ will increase in the transient period consisting of the last half-cycle before the mode transition and the first



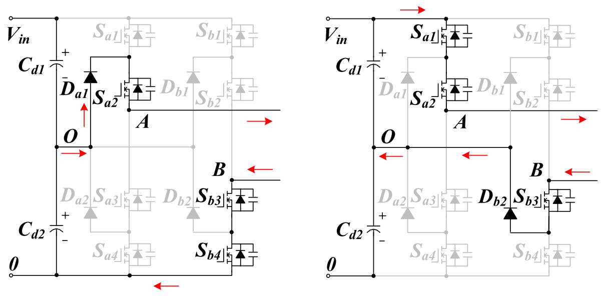
Current flows out of $O$

(a)

Current flows into $O$

(b)

Fig. 20. Current flow paths of stage 2 and stage 6 in MPS mode. (a) Stage 2 ($t_1$-$t_2$). (b) Stage 6 ($t_5$-$t_6$). (Red arrows in the figure represent the current direction.).



Current flows out of $O$

(a)

Current flows into $O$

(b)

Fig. 21. Current flow paths of stage 3 and stage 8 in MFD mode. (a) Stage 3 ($t_2$-$t_3$). (b) Stage 8 ($t_7$-$t_8$).

half-cycle after the mode transition, causing a severe influence on the system.

This article proposes a phase optimization switching method, as shown in Fig. 19(b). The average voltage in the transient period is consistent with the average before the mode transition by applying an advanced phase angle at the mode transition point. The value of the applied phase angle $\alpha$ is

$$\alpha = 2\pi d_{AS} - \theta_B - \theta_C. \tag{13}$$

As the action logic of the Action Register in the digital PWM module is unchanged, the phase optimization switching logic is consistent whether from N-PSAS mode to P-PSAS mode or vice versa. Due to the imperfect factors in practical application, antidisturbance hysteresis can be added to avoid the possible switching oscillation problem.

### C. Capacitor Voltage Balance

The voltage balance of input capacitors $C_{d1}$ and $C_{d2}$ is a prerequisite for the normal operation of the three-level *LLC* converter. The capacitor voltage balance will not be affected in FBVF and PSAS mode as no current flow into or out of the neutral-point O. MPS and MFD mode will affect the input capacitor voltages due to the introduction of the intermediate level. Next, the capacitor voltage balance in these two operating modes is analyzed in detail.

Fig. 20 shows the current flow paths of stage 2 ($t_1$-$t_2$) and stage 6 ($t_5$-$t_6$) in MPS mode. The current flows out from the neutral-point O in stage 2, while the current flows into the neutral-point in stage 6. It can be seen from Fig. 4 that the resonant currents of stage 2 and stage 6 have opposite directions and the same waveforms. Therefore, the sum of the currents contributed to the neutral-point in each switching cycle is naturally zero. Fig. 21 shows the current flow paths of stage 3 ($t_2$-$t_3$) and stage 8 ($t_7$-$t_8$) in MFD mode. The resonant currents of stage 3 and stage 8 in Fig. 5 have the same waveforms. The contribution current to neutral-point O in MFD mode is also naturally zero.

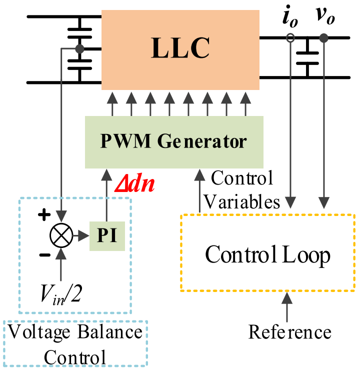


Fig. 22. Control scheme for the capacitor voltage balance.

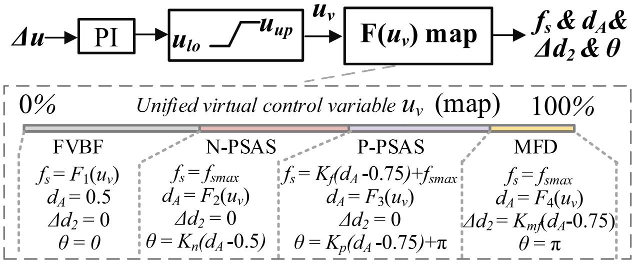


Fig. 23. Concept of unified virtual control variable.

In practice, there will be a slight deviation of neutral-point potential due to the symmetry deviation in the circuit, so the control scheme for the capacitor voltage balance in Fig. 22 is adopted. The output $\Delta dn$ of the capacitor balance control loop is used as the multilevel state's compensation. The compensation is minor in practice due to the slight deviation. In the PWM generator, $\Delta dn$ is added to the time when the current flows into the neutral-point, or $\Delta dn$ is subtracted from the time when the current flows out of the neutral-point.

### D. Unified Virtual Control Variable

The unified virtual control variable is proposed to manage multiple control variables in multiple operation modes in the flexible variable-mode control. Fig. 23 shows the logical concept of unified virtual control by taking the first variable-mode control scheme as an example. The unified virtual control is the integration of multiple negative feedback control loops by using the monotonic relation functions. The output result of the control loop is used as a unified virtual control variable $u_v$. Different mapping forms corresponding to different relation functions are used according to the value of $u_v$. The relation function of each segment satisfies the monotonicity of the corresponding range

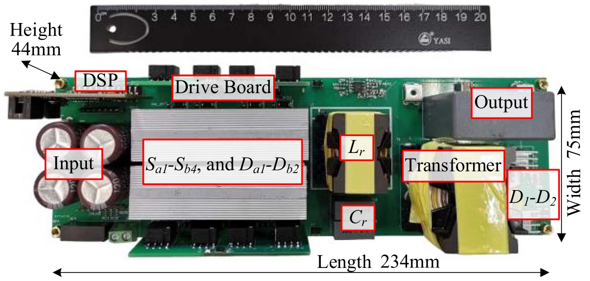


Fig. 24. Hardware prototype of the proposed converter.

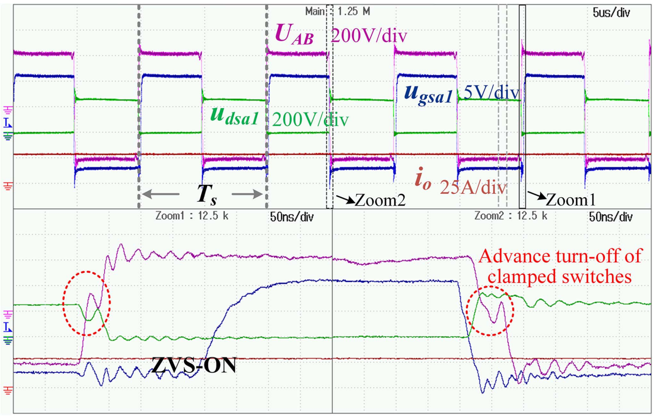


Fig. 25. Experimental waveforms in FBVF mode. ($U_{AB}$ is the chopper output voltage. $u_{gsa1}$ is the driving signal of $S_{a1}$. $u_{dsa1}$ is the voltage across $S_{a1}$. $i_o$ is the output current.).

and the negative feedback characteristic of the control loop. When using the unified virtual control variable, only the output results of the control loop need to be mapped to obtain the values of actual control variables. The control loop itself is continuously controlled, thus avoiding the influence and complexity of the control loop switching.

## V. EXPERIMENTAL RESULTS

A 400 V input, 1.5 kW output prototype in Fig. 24 is built to verify the proposed method and theoretical analysis. The specific parameters and selected components of the prototype are listed in Table II. First, four operation modes of the proposed converter are verified by experiments. In the experiment, a 1.8 Ω resistor load is used.

Fig. 25 shows the experimental waveforms of the converter working in FBVF mode. The switching frequency is 99 kHz, which is close to the resonance frequency of the *LLC* converter, and the converter is in the high gain region, as the output voltage is 50 V. At this time, the primary switching devices can realize ZVS-ON, and the secondary diodes can realize ZCS-OFF, so the system efficiency is high. As mentioned earlier, the clamped switches will be turned OFF for a short time in advance to balance the series switches' voltage stress. Therefore, it can be found from the figure that the chopper output voltage $U_{AB}$ has a zero-level stage of about 50 ns during level switching, as shown in the red dashed box. The voltage across $S_{a1}$ is close to half of the dc bus.

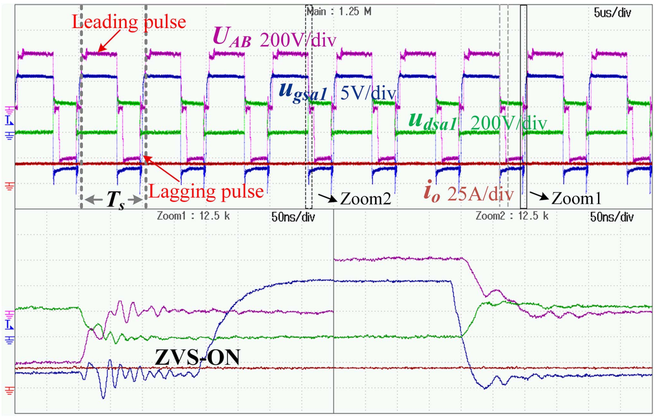


Fig. 26. Experimental waveforms in N-PSAS mode.

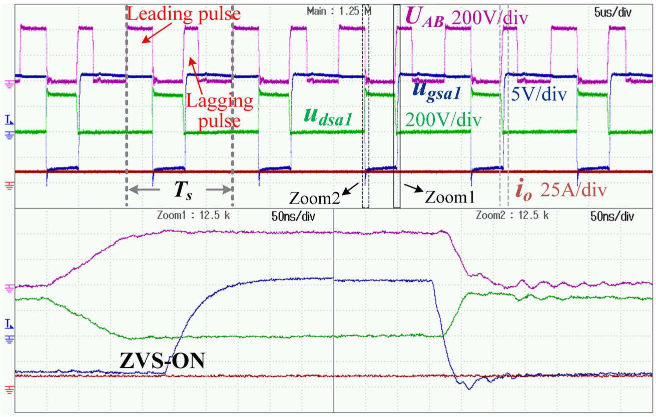


Fig. 27. Experimental waveforms in P-PSAS mode.

Figs. 26 and 27 show the experimental waveforms of the converter working in PSAS mode. Fig. 26 shows the case of the negative lagging pulse, i.e., N-PSAS mode. It can be seen from the figure that $U_{AB}$ contains three levels $V_{in}$, -$V_{in}$, and 0, and the pulse width of the negative lagging pulse is smaller than that of the positive leading pulse. At this time, the switching frequency is the highest value of 200 kHz, $d_A$ is equal to 0.68, $\theta$ is equal to 35°, and the output voltage is 32 V. Fig. 27 shows the case of the positive lagging pulse, i.e., P-PSAS mode. It can be seen from the figure that $U_{AB}$ only contains two levels $V_{in}$ and 0, and the polarity of the lagging pulse changes from negative to positive. In the waveforms, the switching frequency is 123 kHz, $d_A$ is equal to 0.72, $\theta$ is equal to 163°, and the output voltage is 20 V. Fig. 28 shows the experimental waveforms of the converter working in the endpoint of PSAS mode. As $\theta = \pi$ and $d_A = 0.75$, the lagging pulse is the same as the leading pulse, which means that the mode is equivalent to the frequency-doubled control. In the waveforms, the switching frequency is 200 kHz, and the output voltage is 15 V. All switches can realize ZVS-ON in PSAS mode.

Fig. 29 shows the experimental waveforms of the converter working in MPS mode. $U_{AB}$ in the mode contains five levels $V_{in}$, -$V_{in}$, $V_{in}$/2, -$V_{in}$/2, and 0. In the waveforms, the switching frequency is 200 kHz, $\Delta d_1$ is equal to 0.17, $\theta$ is equal to 38°, and

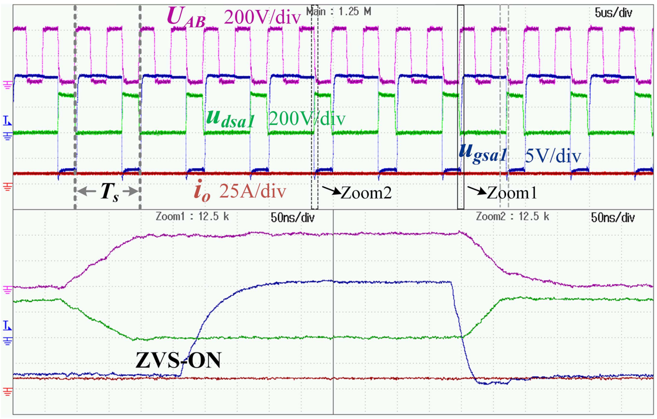


Fig. 28. Experimental waveforms in frequency-doubled control.

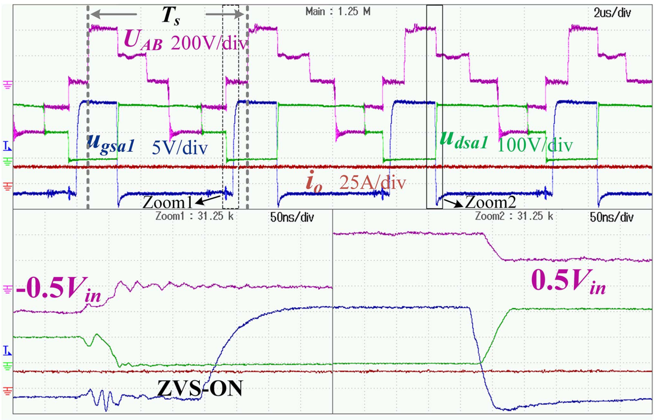


Fig. 29. Experimental waveforms in MPS mode.

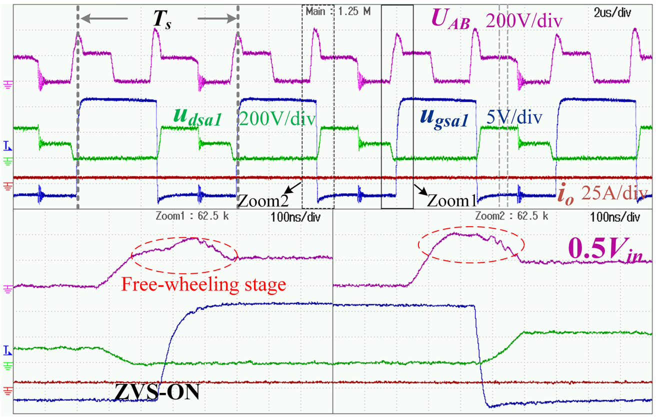
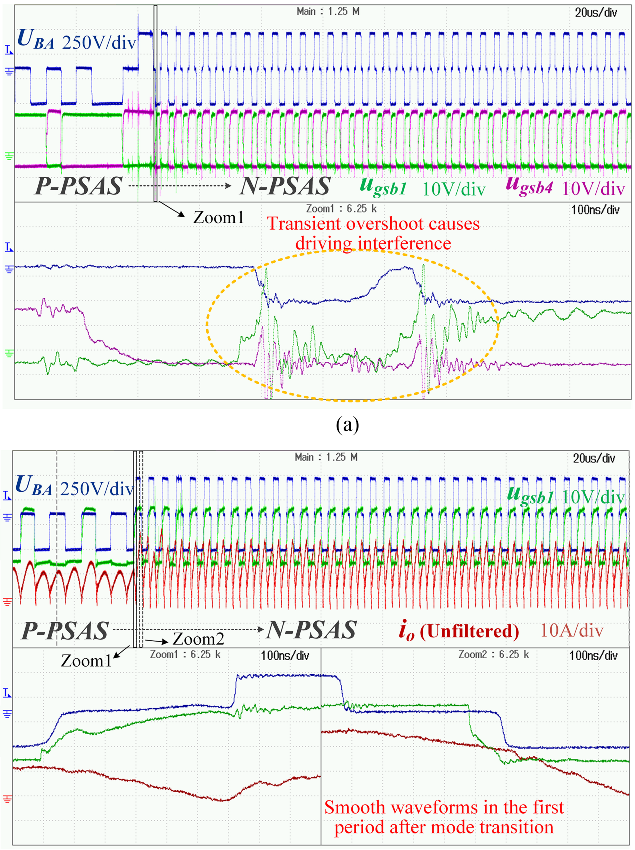


Fig. 30. Experimental waveforms in MFD mode.

the output voltage is 28 V. All switches can also realize ZVS-ON in MPS mode.

Fig. 30 shows the experimental waveforms of the converter working in MFD mode. In the waveforms, the switching frequency is 200 kHz, $d_A$ is equal to 0.725, $\Delta d_2$ is equal to 0.225, and the output voltage is 8.5 V. As shown by the red dotted circle, there is a freewheeling stage at the initial time of the $V_{in}/2$ level, which will affect the decrease of gain. The clamping diodes cannot conduct as the current flows through the reverse diodes of switch $S_{a1}$ or $S_{b4}$ due to the negative resonant current in stage 1 and stage 6. Therefore, even if the duration of $V_{in}$ level output on the control logic has dropped to 0, there is still a freewheeling stage of $V_{in}$ level output before entering the $V_{in}/2$ level output stage. As most of the MFD modes in the control schemes have a shorter freewheeling stage than that in Fig. 30, whose control variables are at the control boundary, the effect of a freewheeling stage on the gain is not significant.



(a)

(b)

Fig. 31. Mode transition process from P-PSAS to N-PSAS with two methods. (a) Transient process with the direct switching method. (b) Transient process with the phase optimization switching method. ($U_{BA}$ is the inversion of chopper output voltage. $u_{gsb1}$ is the driving signal of $S_{b1}$. $u_{gsb4}$ is the driving signal of $S_{b4}$.).

The experimental waveforms of several operation modes are consistent with the theoretical analysis, which verifies the feasibility of the proposed modes.

The mode transition process between P-PSAS and N-PSAS modes is tested in the experiment. Fig. 31 shows the experimental results of the transient process during the switching from P-PSAS mode to N-PSAS mode. Fig. 31(a) adopts the phase direct switching method. A large transient overshoot occurs in the mode transition process, which causes driving interference and affects the converter's operation. Fig. 31(b) adopts the proposed phase optimization switching method, which ensures that the output voltage of the transient period is stable. It can be seen from the figure that the waveform is smooth, and there is almost no transient overshoot in the switching process, which verifies the effectiveness of the proposed phase optimization switching method.

TABLE III
COMPARISONS WITH EXISTING WORK

| Reference | Ref [7] | Ref [10] | Ref [11] | Ref [16] | Ref [22] | Ref [31] | This paper |
|---|---|---|---|---|---|---|---|
| Characteristic | Integration of a half-bridge and full-bridge LLC | Two transformers in series | Two split resonant branches | Two resonant tanks with three modes | Variable frequency multiplier technique | Secondary side auxiliary MOSFET | Three-level LLC with variable-mode control |
| Input or output voltage range | 120 V–240 V (1–2) | 25 V–100 V (1–4) | 80 V–200 V (1–2.5) | 50 V–300 V (1–6) | 85 V–340 V (1–4) | 250 V–420 V (1–1.68) | 8 V–65 V (1–8) |
| Peak efficiency (Full-load) | 94.1% (500 W) | 98% (250 W) | 97.5% (1000 W) | 95% (250 W) | 96.6% (500 W) | 96.7% (1000 W) | 96.7% (1500 W) |
| Mode transition | - | Large transient | Smooth | Smooth | Large transient | - | Smooth |

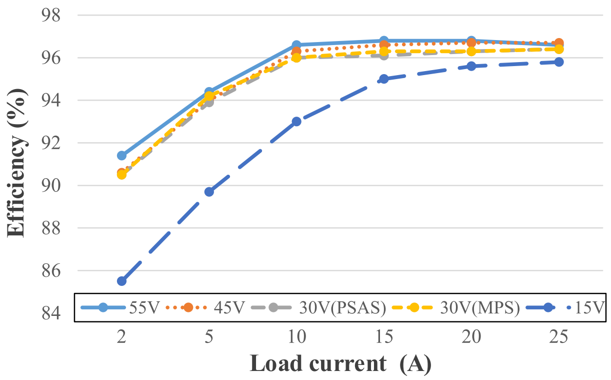


Fig. 32. Working efficiency curves of the converter.

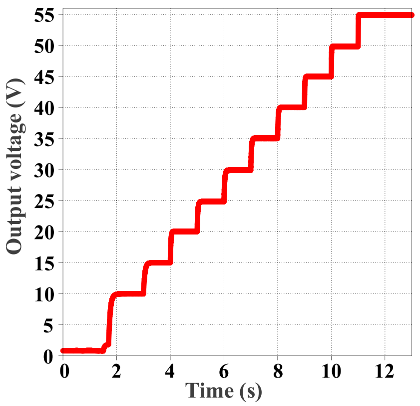


Fig. 33. Output voltage range test.

In this article, the working efficiency of the system is tested experimentally. Fig. 32 shows the working efficiency of the converter with different voltage gains and different loads. There are five efficiency curves in the figure, corresponding to the output voltages of 55 V, 45 V, 30 V, 30 V, and 15 V when the load current changes from 2 to 25 A. For the efficiency curves of 55 V and 45 V, the converter mainly works in FBVF mode. The two efficiency curves of 30 V correspond to the converter working in PSAS mode and MPS mode, respectively. For the efficiency curve of 15 V, the converter mainly works in P-PSAS mode and MFD mode.

The efficiency graph shows that the efficiency of output voltage range from 15 to 55 V is higher than 95% when the load current exceeds 80% of the rated load current (>20 A). Theoretically, the system efficiency is the highest when the converter works at the resonant frequency. In the experiment, the test points corresponding to the highest efficiency are 45 V/25 A and 55 V/15 A, the working points closest to the resonant frequency. It can be found from the figure that the working efficiency of PSAS mode and MPS mode with the output voltage of 30 V even exceeds that of FBVF mode with the output voltage of 45 V in the low load current section. This is mainly due to the relatively high switching frequency of FBVF mode at a low load current, close to PSAS mode and MPS mode. At this time, FBVF mode can only realize ZVS-ON of primary switching devices. However, PSAS and MPS modes can ensure ZVS-ON of the primary switching devices and realize ZCS-OFF of one or two secondary diodes in the set working area. Therefore, the proposed operation modes can actually improve the efficiency of the *LLC* converter under low load. In addition, according to the further analysis of loss, the conduction loss of the secondary rectifier diodes is significant (about 1.0%–1.5%), and the efficiency can be further improved by synchronous rectification.

The entire voltage working range of the system is tested, as shown in Fig. 33. The input voltage is constant at 400 V, and the resistor load is 1.8 Ω. Due to the power limitation, the maximum output voltage is 55 V in the experiment, causing no influence on the theoretical verification. The output voltage is gradually increased by changing the reference value of the output voltage (5 V as a step). Record the data of output voltage waveform in the whole process, which verifies the output voltage range. It can be seen that the converter achieves a very wide voltage gain range.

The comparisons with past work on output voltage range and efficiency are summarized in Table III. It can be seen that the proposed three-level *LLC* converter with variable-mode control in this article has a very wide gain range and high peak efficiency. Therefore, the proposed method is advantageous in wide gain range applications.

## VI. CONCLUSION

The article proposes a three-level *LLC* converter with two diode-clamped legs and its flexible variable-mode control method. The converter has four operation modes with different voltage gains, including FBVF mode, PSAS mode, MPS mode, and MFD mode. Next, the voltage gain, soft-switching, and current stress characteristics in each operation mode are obtained by theoretical analysis and simulation. Based on the performance analysis, two variable-mode control methods with a wide gain range are designed. The variable-mode control method with the design parameters can achieve a gain range from 65 to 8 V under a resistor load, while the traditional frequency control can only achieve a gain range from 65 to 37 V. The mode transition between different operation modes is flexible, ensuring no surge current in the switching process. A 1.5-kW prototype with 400-V input voltage is built. The experimental results show that the converter with the proposed method can achieve a very wide voltage gain range while maintaining high efficiency.

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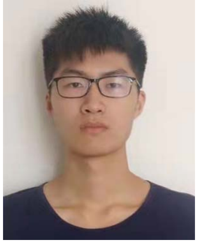

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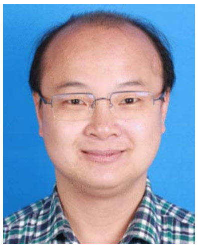

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