A Robust Open-Circuit Fault Diagnosis Method for Three-Level T-Type Inverters Based on Phase Voltage Vector Residual Under Modulation Mode Switching

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***Abstract*—This article proposes a new phase voltage vector residual-based fault diagnosis method to distinguish the similar open-circuit (OC) fault features of different switches in the three-level T-type inverter. The fault feature based on phase voltage residual can be generated with the designed expected phase voltage model considering different modulation strategies and modes. Under the zero-crossing (ZC) and non-ZC conditions of the faulty phase, the voltage vector residual characteristics caused by OC faults can be summarized. An adaptive residual vector amplitude threshold is designed based on uncertainty propagation using parameter error, dead time, and delay time as system error inputs. In addition, a hierarchical fault diagnosis scheme is proposed, which involves two steps. First, the group-level fault can be located according to voltage residual vector amplitude and angle. Next, the three-level modulation mode of all phase legs is switched to the two-level mode to further identify the faulty switch from the faulty group. The proposed method can achieve a reasonable balance between robustness and rapidity. Meanwhile, complexity and adaptability are also considered. Experimental results under various conditions sufficiently verify the robustness and effectiveness of the proposed fault diagnosis method.**

***Index Terms*—Adaptive threshold, fault diagnosis, open-circuit (OC) fault, three-level t-type (3L-T) inverter, voltage vector residual.**

I. INTRODUCTION

MULTILEVEL inverters [1], [2] have received extensive attention in medium-voltage and medium switching frequency applications, such as renewable energy generation, rail traction, and automotive driving systems [3], [4], [5]. Among multilevel inverters, the three-level neutral point clamped (3L-NPC) inverter and the three-level T-type (3L-T) inverter are the most commonly used topologies due to their advantage of simplicity and flexibility. Compared with the 3L-NPC inverter, the 3L-T inverter has more advantages in conversion efficiency and fault-tolerant control [6].

Nowadays, the reliability of three-level (3L) inverters is a critical issue in practice, which has aroused great interest. Generally, short-circuit (SC) faults can be detected by the hardware detection and protection circuits built into the driver board [7]. With the SC protection circuits, the driving signals are locked, and the faulty switch is turned OFF, which makes the SC faults turn into open-circuit (OC) faults. As for OC faults, they are usually manifested as distorted current and voltage. If OC faults are not handled immediately, they may cause further damage to the remaining devices. Hence, a fast and robust OC fault diagnosis method is worth studying [8].

The diagnosis method of power switch OC fault in the inverter mainly includes data-driven and knowledge-driven methods. The data-driven OC fault diagnosis is essentially a pattern classification problem containing feature extraction and fault classification. Principal component analysis [9], discrete wavelet transform, and fast Fourier transform are the traditional fault extraction methods. Fault classification methods successfully applied to OC fault diagnosis mainly contain support vector machines, convolution neural networks, Bayesian networks [9], and so on. The main challenges of the data-driven methods are the heavy computational burden and low real-time performance.

Various knowledge-driven fault diagnosis methods have recently been proposed for two-level (2L) and 3L converters. According to the electrical signals required for feature extraction, these knowledge-driven methods can be classified into the current-based methods [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25] and voltage-based [26], [27], [38] methods. The faulty current and the residual between the current reference value and the measured

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value can be used for fault feature extraction in the current-based methods. The Park's vector [10], average values [11], [12], root-mean-square values [13], the radius of the current pattern [14], current similarity [15], and zero-crossing (ZC) characteristics [16], [17], [18], [19] of the phase current can be analyzed directly for fault diagnosis without additional hardware. By adding an extra current sensor, the proposed method based on dc-link neutral point current [20] can further reduce the diagnosis time to several sampling cycles. For the current residual-based method, the vector [21], average value [22], and changing rate [23] of the current residual can be utilized for fault diagnosis. The estimated current can be obtained by a mixed-logical-dynamic model [21] and different types of observers, such as the Luenberger state observer and sliding mode observer [24], [25]. The robustness is improved by the idea of averaging in a basic period, adaptive threshold, and normalization. Nevertheless, the current-based fault diagnosis methods present poor rapidity.

In voltage-based methods with extra measurement circuits, the measured values include pole voltage [26], line-to-line voltage [27], and turn-on gate voltage [28]. Compared with the current-based method, these methods possess fast diagnosis speed. But, extra measurement circuits are required, which increases the system's cost and complexity. For economic reasons, the voltage model-based methods employ the phase voltage [29], [30], [31], line-to-line voltage [32], [33], and dc-link voltage model [34] to estimate the reference voltage and generate the corresponding voltage residual. Furthermore, improving the sampling rate [35], [36] can further increase the speed of fault diagnosis, but its anti-interference ability is limited. These methods are sensitive to system parameter variations, and threshold selection is still one of the critical issues to ensure effectiveness and improve robustness. Especially for the voltage-based method, the calculation process of the voltage reference value varies with the modulation strategy.

In particular, as the OC faults for 3L topologies often share similar distorted features, fault diagnosis requires additional fault location steps. The changing trends of dc-link voltage can be used to locate the faulty switch if no neutral point balance control is adopted [33]. For the invasive location method, the specific switching signal injection [14], [37], modulation strategy switching [38], and power factor regulation [39] can help to distinguish the faulty switch. Among them, as the closed-loop control is disabled under the specific switching signal injection method, the system has the risk of over-current. In conclusion, the development trend of fault diagnosis is to locate the OC fault in a way that has less impact on the system.

Through the above-mentioned analysis, the existing fault diagnosis methods are challenging to achieve a reasonable balance between robustness and rapidity. Meanwhile, further studies on complexity and adaptability are still necessary.

This article proposes a novel OC fault diagnosis method for the 3L-T inverters based on phase voltage vector residual under modulation mode switching. The group-level fault diagnosis is based on voltage residual vector amplitude and angle. For the device-level fault, the 3L modulation mode of all legs is switched to the 2L mode to further locate the specific faulty switch in the detected faulty group. Compared with the fixed threshold methods, the proposed method using an adaptive threshold shows strong robustness under various load transients. The rest of this article is organized as follows. The terminal voltage under normal and faulty cases is analyzed in Section II. An OC fault diagnosis method based on phase voltage residual vector is proposed in Section III. The experimental validation and comparison with previous methods are carried out in Section IV. Finally, Section V concludes this article.

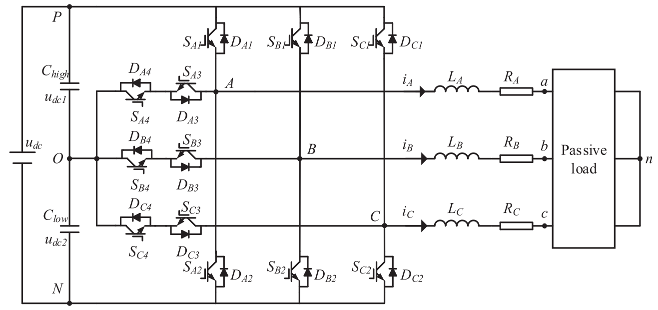


Fig. 1. Diagram of the three-phase 3L-T inverter topology.

II. Terminal Voltage Analysis

The terminal voltage (including phase voltage u_{Xn} and pole voltage u_{XO}) is the first electrical signal to be distorted after an OC fault, which can be utilized for fault diagnosis. Hence, analyzing the law of voltage residual between the expected and actual phase voltage is crucial.

A. Terminal Voltage Modeling

The circuit topology of the 3L-T inverter connected with the passive load is shown in Fig. 1. Ideally, the voltage equation under health conditions can be written as

$$u_{XO\_ref} + u_{On} = u_{Xn} = R_X i_X + L_X di_X/dt + u_{xn} \quad (1)$$

where u_{XO_ref}, u_{Xn}, and u_{xn} are the expected inverter output pole voltage, the actual phase voltage, and the load voltage. i_X is phase current and $X = A, B, C$, $x = a, b, c$. R_X and L_X are the line circuit resistance and inductance. u_{On} is the voltage between dc-link midpoint O and load common coupling point n.

For a symmetrical three-phase three-wire Y-type connect system, $R_A = R_B = R_C = R$, and $L_A = L_B = L_C = L$. Ideally, the load voltage u_{xn} is balanced, namely, $u_{an} + u_{bn} + u_{cn} = 0$. Then, u_{On} in (1) can be written as

$$u_{On} = -(u_{AO\_ref} + u_{BO\_ref} + u_{CO\_ref})/3. \quad (2)$$

According to Kirchhoff's voltage law $u_{An\_ref} = u_{AO\_ref} + u_{On}$, one can obtain

$$\begin{bmatrix} u_{An\_ref} \\ u_{Bn\_ref} \\ u_{Cn\_ref} \end{bmatrix} = K \begin{bmatrix} u_{AO\_ref} \\ u_{BO\_ref} \\ u_{CO\_ref} \end{bmatrix}, K = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}. \quad (3)$$

Ideally, $u_{On} = 0$, there is

$$u_{Xn\_ref} = u_{XO\_ref}. \quad (4)$$

As coefficient matrix K between u_{Xn} and u_{XO} is constant, their distortion characteristics are closely related after OC faults.

TABLE I
OUTPUT POLE VOLTAGE VALUE UXO_REF UNDER ALL POSSIBLE VARIABLE COMBINATIONS

Switching state (S_{X1}, S_{X3}, S_{X2}, S_{X4})	Pole voltage u_{XO_ref} when $i_X > 0$	Pole voltage u_{XO_ref} when $i_X < 0$
(1001)	u_{dc1}	u_{dc1}
(0101)	0	0
(0110)	$-u_{dc2}$	$-u_{dc2}$
(0000)	$-u_{dc2}$	u_{dc1}
(0001)	0	u_{dc1}
(0010)	$-u_{dc2}$	$-u_{dc2}$
(0100)	$-u_{dc2}$	0
(1000)	u_{dc1}	u_{dc1}

The output pole voltage u_{XO_ref} is a function of the dc-link voltage u_{dc1} and u_{dc2}, switching state from S_{X1} to S_{X4}, and the direction of i_X. Considering the impact of dead time, Table I shows the output pole voltage values under all possible variable combinations. The value of S_{XZ} (Z = 1, 2, 3, 4) stands for the switching signal, one means ON, and zero means OFF.

Defining the logical variable δ_X as

$$\delta_X = \begin{cases} 1 & i_X > 0 \\ 0 & i_X < 0 \end{cases}. \tag{5}$$

According to the logical derivation of the Karnaugh method, the mathematical expression of u_{XO_ref} is

$$\begin{aligned} u_{XO\_ref} &= \delta_X(S_{X1} \cdot u_{dc1} - \bar{S}_{X1}\bar{S}_{X4} \cdot u_{dc2}) \\ &\quad - \bar{\delta}_X(S_{X2} \cdot u_{dc2} - \bar{S}_{X2}\bar{S}_{X3} \cdot u_{dc1}). \end{aligned} \tag{6}$$

Equations (1)–(6) are the mixed logical dynamic model of the 3L-T inverter, which contains discrete and continuous variables. In normal operation, the actual terminal voltage u_{XO} equals the expected value u_{XO_ref}. The voltage residual Δu_{Xn} ($=$ u_{Xn_ref} - u_{Xn}) and Δu_{XO} ($= u_{XO\_ref}$ - u_{XO}) are close to 0. However, when an OC fault occurs, the corresponding driving signal is blocked, and the voltage residual will deviate from 0. The following analysis takes S_{X1} and S_{X4} OC faults as examples.

B. Terminal Voltage Distortion Feature Under OC Faults

The mixed logical dynamic model can be employed to analyze the voltage residual. When there is a single OC fault on switch S_{X1}, $S_{X1} \equiv 0$. According to (6), The expression of the actual phase voltage u_{XO} is expressed as

$$\begin{aligned} u_{XO} &= \delta_X(-\bar{S}_{X1}\bar{S}_{X4} \cdot u_{dc2}) \\ &\quad - \bar{\delta}_X(S_{X2} \cdot u_{dc2} - \bar{S}_{X2}\bar{S}_{X3} \cdot u_{dc1}). \end{aligned} \tag{7}$$

Then, by subtracting (7) from (6), the pole voltage residual Δu_{XO} can be described as

$$\Delta u_{XO} = \delta_X(S_{X1} \cdot u_{dc1} - \bar{S}_{X1}\bar{S}_{X4} \cdot u_{dc2} + \bar{S}_{X4} \cdot u_{dc2}). \tag{8}$$

When $i_X > 0$ and the switching state equals (1001) or (1000), Δu_{XO} is always great than 0. $\Delta u_{XO} = 0$ under the remaining variable combinations in Table I. The pole voltage residual of the remaining two phases is still 0. When $i_X \neq 0$, (3) is still satisfied under fault conditions. The further derivation leads to the following relationship:

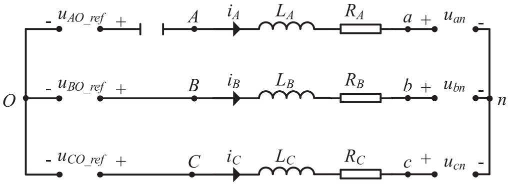


Fig. 2. Working state of 3L-T inverters when phase *A* is in ZC conditions.

$$\begin{bmatrix} \Delta u_{An} \\ \Delta u_{Bn} \\ \Delta u_{Cn} \end{bmatrix} = K \begin{bmatrix} \Delta u_{AO} \\ \Delta u_{BO} \\ \Delta u_{CO} \end{bmatrix}. \tag{9}$$

For the S_{A1} OC fault, the phase voltage residual Δu_{Xn} satisfies

$$\Delta u_{An} = -2\Delta u_{Bn} = -2\Delta u_{Cn} > 0. \tag{10}$$

When there is a single OC fault on switch S_{X4}, the actual pole voltage u_{XO} is

$$\begin{aligned} u_{XO} &= \delta_X(S_{X1} \cdot u_{dc1} - \bar{S}_{X1} \cdot u_{dc2}) \\ &\quad - \bar{\delta}_X(S_{X2} \cdot u_{dc2} - \bar{S}_{X2}\bar{S}_{X3} \cdot u_{dc1}). \end{aligned} \tag{11}$$

Likewise, Δu_{XO} is given by

$$\Delta u_{XO} = \delta\left(-\bar{S}_{X1}\bar{S}_{X4} \cdot u_{dc2} + \bar{S}_{X1} \cdot u_{dc2}\right). \tag{12}$$

Δu_{XO} is positive in two cases: $i_X > 0$, (S_{X1}, S_{X3}, S_{X2}, S_{X4}) = (0101) and $i_X > 0$, (S_{X1}, S_{X3}, S_{X2}, S_{X4}) = (0001).

However, when the affected faulty phase current is reduced to a near-zero value, the three-phase inverter switches to the single-phase state. The unique ZC conditions are overlooked in the above three-phase mixed logical dynamic model.

During ZC conditions, the three-phase balance and symmetrical characteristics are broken. As shown in Fig. 2, Kirchhoff's voltage law can be applied to the voltage loop *O-B-n-C-O* and the voltage equation can be summarized as follows:

$$\begin{cases} u_{On} = u_{Bn} - u_{BO\_ref} = u_{Cn} - u_{CO\_ref} \\ u_{An} + u_{Bn} + u_{Cn} = 0 \\ u_{An} = u_{an} \end{cases}. \tag{13}$$

By solving (13), the voltage u_{On} expression can be written by

$$u_{On} = (-u_{BO\_ref} - u_{CO\_ref} - u_{an})/2. \tag{14}$$

By substituting (14) into (13), the actual phase voltage can be obtained as follows:

$$\begin{cases} u_{An} = u_{an} \\ u_{Bn} = u_{BO\_ref} + (-u_{BO\_ref} - u_{CO\_ref} - u_{an})/2 \\ u_{Cn} = u_{CO\_ref} + (-u_{BO\_ref} - u_{CO\_ref} - u_{an})/2 \end{cases}. \tag{15}$$

Taking the switching cycle as the minimum time unit, the sum of the phase voltage commands input to the sinusoidal pulse width modulation (SPWM) or space vector pulse width modulation (SVPWM) module is zero $u_{AO\_ref} + u_{BO\_ref} + u_{CO\_ref} = 0$. Consequently, the voltage residual ($= u_{Xn\_ref}$ -

TABLE II
TERMINAL VOLTAGE RESIDUAL FEATURE UNDER SINGLE OC FAULTS

Group-level fault	Δu_{Xn}	(Δu_{AO}, Δu_{BO}, Δu_{CO})	Current direction
$S_{A1/4}$	$\Delta u_{An} = -2\Delta u_{Bn} = -2\Delta u_{Cn} > 0$	(+, 0, 0)	$i_A \geq 0$
$S_{A2/3}$	$\Delta u_{An} = -2\Delta u_{Bn} = -2\Delta u_{Cn} < 0$	(-, 0, 0)	$i_A \leq 0$
$S_{B1/4}$	$\Delta u_{Bn} = -2\Delta u_{An} = -2\Delta u_{Cn} > 0$	(0, +, 0)	$i_B \geq 0$
$S_{B2/3}$	$\Delta u_{Bn} = -2\Delta u_{An} = -2\Delta u_{Cn} < 0$	(0, -, 0)	$i_B \leq 0$
$S_{C1/4}$	$\Delta u_{Cn} = -2\Delta u_{An} = -2\Delta u_{Bn} > 0$	(0, 0, +)	$i_C \geq 0$
$S_{C2/3}$	$\Delta u_{Cn} = -2\Delta u_{An} = -2\Delta u_{Bn} < 0$	(0, 0, -)	$i_C \leq 0$

u_{Xn}) equation can be achieved

$$\begin{cases} \Delta u_{An} = u_{AO\_ref} - u_{an} \\ \Delta u_{Bn} = -(u_{AO\_ref} - u_{an})/2 \\ \Delta u_{Cn} = -(u_{AO\_ref} - u_{an})/2 \end{cases}. \tag{16}$$

Equation (16) shows that when $i_X = 0$, the linear relationship between the voltage residuals also satisfies (10). The residual polarity in ZC conditions cannot be obtained from (16). Hence, the hypothesis method is adopted for voltage residual polarity reasoning. Combining (14) with $u_{aO} = u_{an}$ - u_{On} and u_{AO_ref} + $u_{BO\_ref} + u_{CO\_ref} = 0$, u_{aO} can be derived as

$$u_{aO} = (3u_{an} - u_{AO\_ref})/2. \tag{17}$$

S_{X1} and S_{X4} OC faults affect the system during the reference voltage positive half period, which means $u_{AO\_ref} > 0$. From (16), assuming $\Delta u_{An} < 0$, then $u_{AO\_ref} < u_{an}$. Based on (17), then $u_{AO\_ref} < u_{an} < u_{aO}$. Based on the above assumptions, the antiparallel diodes D_{A1} will turn ON, and i_X will be less than 0, which is contrary to the preconditions ($i_X = 0$). Therefore, the assumption is erroneous, and Δu_{An} is great than 0.

The above-mentioned analyses suggest that S_{X1} and S_{X4} generate the same fault feature regarding voltage residual polarities and ratios. Similarly, the terminal voltage residual feature under different OC faults can be obtained, as given in Table II. The simulation waveforms of i_X, Δu_{Xn}, and Δu_{XO} under the S_{A4} and S_{B2} OC faults in a basic cycle $\mathrm{T_{ac}}$ are presented in Fig. 3(a) and (b), respectively, which confirms the theoretical analysis of the terminal voltage.

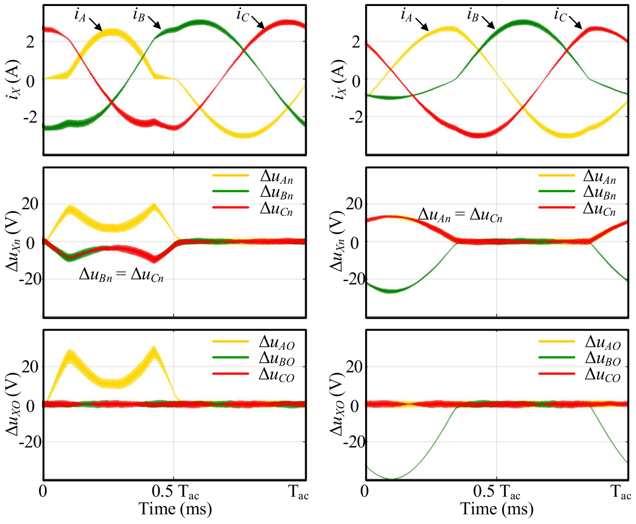
Table II shows that the terminal voltage residual can be used to detect the group-level OC fault, but it is impossible to determine which fault in the faulty group is true. In addition, through the transformation from *abc* to $\alpha\beta$ coordinate system, the polarities and ratios feature can be displayed in the form of amplitude and phase angle.

III. FAULT DIAGNOSIS METHOD

Fig. 4 shows the proposed fault diagnosis method, which can be divided into six parts.

1) Expected phase voltage module.
2) Phase voltage residual module.
3) Feature extraction module.
4) Adaptive threshold module.
5) Fault diagnosis module.

N is the working sector of the expected phase voltage vector. The space voltage vector distribution of 3L-T inverters is shown in Fig. 5.



(a) (b)

Fig. 3. Simulation waveforms of i_X, Δu_{Xn}, Δu_{XO}. (a) Under S_{A4} OC fault. (b) Under S_{B2} OC fault.

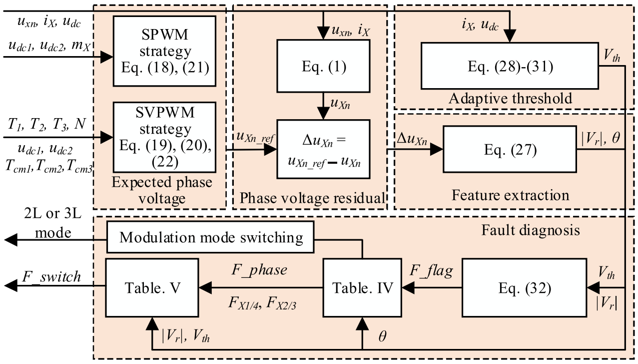


Fig. 4. Diagram of the proposed fault diagnosis method.

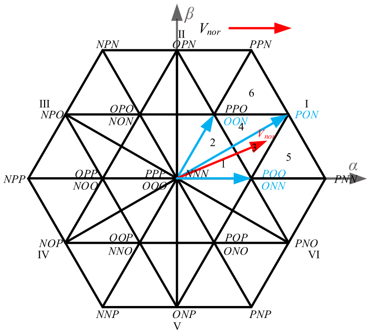


Fig. 5. Space voltage vector distribution of 3L-T inverters under the seven-segment SVPWM strategy.

The phase voltage module outputs the expected phase voltage u_{Xn_ref} under different modulation strategies (SPWM or SVPWM) and modes (2L or 3L). The phase voltage residual module calculates the voltage residual Δu_{Xn} between u_{Xn} and u_{Xn_ref}. The feature extraction module is responsible for calculating $|V_r|$ and θ, which can be employed for fault diagnosis.

The threshold V_{th} is updated in the adaptive threshold module according to the operating conditions. The fault detection module is responsible to controls the modulation modes and outputs the fault flag. The fault diagnosis module hierarchically diagnoses the group-level and device-level OC faults.

A. Expected Phase Voltage Calculation

In a switching period, the switching state of each phase changes only once, while the three-phase combination changes seven times under the seven-segment SVPWM strategy. It is impossible to obtain each actual switch state through one switching period. Since the changing frequency of switching state S_{X1}–S_{X4} is great than the sampling frequency, the real-time state of each switch state cannot be obtained. Thus, (6) containing discrete variables (switching states) cannot be used for u_{Xn} calculation. Using the switching period as the minimum time step to estimate the phase voltage is more suitable for embedded processing systems. The calculation of phase voltage differs depending on the modulation strategy.

Under the SPWM strategy and 3L mode, the pole voltage can be represented by the function of the normalized modulation index (m_X) and the dc-link voltage (u_{dc1} and u_{dc2}), which is

$$u_{XO\_ref} = \begin{cases} m_X \cdot u_{dc1} & m_X \geq 0 \\ m_X \cdot u_{dc2} & m_X < 0 \end{cases}. \tag{18}$$

The phase voltage u_{Xn_ref} can be obtained by combing (18) with (3). Under the SVPWM strategy and 3L mode. Considering that neutral point voltage deviation is not evident in a short time, the magnitude of each basic small-voltage (such as [*POO*]) vector is $u_{dc}/6$ (or $u_{dc1}/3$). Hence, the phase voltage vector $Vnor$ in the working sector I-3 can be expressed as

$$V_{nor} = \frac{2}{3}u_{dc1}(e^{j0}T_1 + e^{j\pi/3}T_2 + \sqrt{3}e^{j\pi/6}T_3). \tag{19}$$

T_1, T_2, and T_3 refer to the duty ratio of the corresponding basic voltage vectors in the 3L operation mode. The voltage vector $Vnor$ in other sectors can also be obtained similarly. Next, according to the inverse Clark transformation, the corresponding phase voltage uXn_ref under *abc* reference frame can be obtained as

$$\begin{bmatrix} u_{An\_ref} \\ u_{Bn\_ref} \\ u_{Cn\_ref} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{nor\_\alpha} \\ V_{nor\_\beta} \end{bmatrix} \tag{20}$$

where $Vnor\_\alpha$ and V_{nor_β} are the α-axis and β-axis voltage components, respectively.

The 3L-T inverter can also work under 2L mode when all legs' inner switch ($S_{X3/4}$) is locked and the outer switch ($S_{X1/2}$) works in a complementary manner. Under 2L mode, the phase voltage u_{Xn_ref} under the SPWM strategy can be derived as

$$u_{Xn\_ref} = \frac{m_X}{2} \cdot u_{dc}. \tag{21}$$

Under the SVPWM strategy and 3L mode, the phase voltage vector V_{nor} in the working sector I can be expressed as

$$V_{nor} = \frac{2}{3}u_{dc}(e^{j0}T_{cm1} + e^{j0}T_{cm2} + e^{j\pi/3}T_{cm3}) \tag{22}$$

where T_{cm1}, T_{cm2}, and T_{cm3} are the duty ratio of the corresponding basic voltage vectors in 2L operation mode.

B. Inherent Phase Voltage Residual

There exists a difference between expected (u_{Xn_ref}), estimated (u_{Xn}), and actual (u_{Xn_real}) phase voltage due to parameter errors, dead time, and delay time. The inherent phase voltage residual Δu_{Xn} ($= u_{Xn\_ref}$ - u_{Xn}) analysis under normal cases is given in this subsection.

Ignoring the voltage component $R_X i_X$ caused by the line resistance term and taking the parameter errors into account, the actual phase voltage u_{Xn_real} calculated on the load side can be written as

$$\begin{aligned} u_{Xn\_real} &= (L_X + \Delta L_X)di_X/dt + u_{xn} \\ &= u_{Xn} + \Delta L_X di_X/dt. \end{aligned} \tag{23}$$

ΔL_X, u_{Xn}, and u_{Xn_real} are the inductance error, estimated phase voltage, and actual phase voltage.

Considering the influence of dead time and delay time, the actual phase voltage u_{Xn_real} calculated on the inverter side can be expressed by

$$u_{Xn\_real} = u_{Xn\_ref} - \Delta u_{Xn\_dt} \tag{24}$$

where $\Delta u_{Xn\cdot dt}$ is the voltage component caused by dead time and delay time [40], which can be obtained by

$$\Delta u_{Xn\_dt} = \frac{u_{dc}}{2} \cdot \frac{|t_{dead} + t_{on} - t_{off}|}{T_s} \tag{25}$$

where t_{dead} represents the dead time, t_{on} and t_{off} are the turn-ON and turn-OFF delay.

With (23) and (24), the inherent voltage residual Δu_{Xn} can be calculated as

$$\Delta u_{Xn} = \Delta L_X \cdot di_X/dt + \Delta u_{Xn\_dt}. \tag{26}$$

To accurately calculate the inherent voltage residual, a lookup table can record each operating point's dynamic parameter errors, dead time, and delay time. For simplicity, the maximum value of them can also be used in (26).

C. Feature Extraction and Adaptive Threshold

The three-phase voltage residuals Δu_{Xn} can be used for fault diagnosis in *abc* coordinate system, but three thresholds are required. To detect the OC fault conveniently, the phase voltage residual vector V_r is defined as

$$V_r = \sqrt{(\Delta u_\alpha)^2 + (\Delta u_\beta)^2} \cdot \angle\theta \tag{27}$$

where Δu_α and Δu_β are voltage components of the V_r in the $\alpha\beta$ coordinate, which can be obtained by performing Clark transformation on Δu_{Xn}, and θ is the phase angle of the V_r.

The amplitude of the V_r can diagnose the OC fault. The phase angle θ can be used for group-level fault diagnosis. The normalized voltage residual vector, phase angle, and their corresponding OC fault group are listed in Table III.

$|V_r|$ and θ are the extracted features for fault diagnosis. The extraction process is simple, without any parameter choice, and

TABLE III
NORMALIZED VOLTAGE RESIDUAL VECTOR CHARACTERISTICS UNDER DIFFERENT OC FAULTS

Group-level OC fault	Normalized V_r	Angle θ of vector V_r
$S_{A1/4}$	$(2,-1,-1)/\sqrt{6}$	0°
$S_{A2/3}$	$(-2,1,1)/\sqrt{6}$	180°
$S_{B1/4}$	$(-1,2,-1)/\sqrt{6}$	120°
$S_{B2/3}$	$(1,-2,1)/\sqrt{6}$	300°
$S_{C1/4}$	$(-1,-1,2)/\sqrt{6}$	240°
$S_{C2/3}$	$(1,1,-2)/\sqrt{6}$	60°

the selected features combined with the adaptive threshold show strong robustness under various load transients.

The adaptive threshold V_{th} is designed to consider the impact of parameter error, dead time, and delay time. In healthy conditions, the adaptive threshold V_{th} should be larger than the upper bound of $|V_r|$. The voltage component of V_{nor} in the $\alpha\beta$ coordinate can be written as

$$\begin{cases} V_\alpha = (2/3)\cdot(u_{An} - 0.5u_{Bn} - 0.5u_{Cn}) \\ V_\beta = (\sqrt{3}/3)\cdot(u_{Bn} - u_{Cn}) \end{cases}. \tag{28}$$

According to the propagation of uncertainty theory

$$\Delta V_{\alpha/\beta} = \left\{ \sum_{X_i = u_{An}, u_{Bn}, u_{Cn},} \left(\frac{\partial V_{\alpha/\beta}}{\partial X_i} \Delta X_i \right) \right\}^{1/2}. \tag{29}$$

The standard error of (28) is calculated as

$$\begin{cases} \Delta V_\alpha = (2/3)\cdot\sqrt{\Delta u_{An}^2 + (0.5\Delta u_{Bn})^2 + (0.5\Delta u_{Cn})^2} \\ \Delta V_\beta = (1/\sqrt{3})\cdot\sqrt{\Delta u_{Bn}^2 + \Delta u_{Cn}^2} \end{cases}. \tag{30}$$

Furthermore, the propagation of uncertainty rule is applied on $V_{nor}\,(= \sqrt{V_\alpha^2 + V_\beta^2})$, and the adaptive threshold V_{th} is defined as

$$V_{th} = \Delta V_{nor} = \frac{\sqrt{(V_\alpha \Delta V_\alpha)^2 + (V_\beta \Delta V_\beta)^2}}{V_{nor}}. \tag{31}$$

The uncertainty of V_{nor} can indicate the influence of system errors, such as parameter error, dead time, and delay time, on voltage amplitude under normal cases. According to (27), (30), and (31), it is found that $|V_r|$ must be less than V_{th} under normal cases. The designed adaptive threshold is a function of the current slope and dc-link voltage, which can vary with working conditions.

For motor drive applications, changes in the model parameters of the ac speed control system, such as inductance and resistance, may also generate inherent phase voltage vector residuals that affect the fault diagnosis. One way to avoid misdiagnosis is to calculate the corresponding phase voltage residual components and obtain the adaptive threshold, similar to the method for dealing with filter inductance parameter errors. Another way is to use the online parameter identification method to update the system parameters in the phase voltage model in real-time to improve the model accuracy.

TABLE IV
PHASE VOLTAGE RESIDUAL VECTOR ANGLE FOR GROUP-LEVEL OC FAULT LOCATION

F_phase	Group-level fault flags ($F_{X1/4}$, $F_{X2/3}$)	Angle θ of vector V_r
1 (*A* phase)	$F_{X1/4} = 1$	$-30° < \theta < 30°$
	$F_{X2/3} = 1$	$150° < \theta < 210°$
2 (*B* phase)	$F_{X1/4} = 1$	$90° < \theta < 150°$
	$F_{X2/3} = 1$	$270° < \theta < 330°$
3 (*C* phase)	$F_{X1/4} = 1$	$210° < \theta < 270°$
	$F_{X2/3} = 1$	$30° < \theta < 90°$

TABLE V
LOCATION RULES FOR DEVICE-LEVEL OC FAULT

F_switch	Under 3L mode	Under 2L mode
1	$\lvert V_r\rvert > V_{th}$ & $F_{X1/4} = 1$	$\lvert V_r\rvert > V_{th}$ & $0.1\mathrm{T_{ac}} < t < \mathrm{T_{ac}}$
4		$\lvert V_r\rvert < V_{th}$ & $t = \mathrm{T_{ac}}$
2	$\lvert V_r\rvert > V_{th}$ & $F_{X2/3} = 1$	$\lvert V_r\rvert > V_{th}$ & $0.1\mathrm{T_{ac}} < t < \mathrm{T_{ac}}$
3		$\lvert V_r\rvert < V_{th}$ & $t = \mathrm{T_{ac}}$

D. Fault Diagnosis

As for fault detection, it is achieved based on judging the following conditions:

$$F\_flag = \begin{cases} 1 & |V_r| \geq V_{th} \\ 0 & |V_r| < V_{th} \end{cases} \tag{32}$$

where *F_flag* is the fault state variable, $F\_flag = 0$ represents healthy conditions, and $F\_flag = 1$ denotes OC fault event. The steps for fault location are divided into group-level and device-level fault locations. Once *F_flag* equals 1, group-level fault diagnosis is enabled. As analyzed in Section II, the group-level OC fault has a unique relationship with phase voltage residual vector angle, which can be summarized in Table IV. The group-level fault flags $F_{X1/4}$ equal to 1 indicate that the OC fault occurred on S_{X1} or S_{X4}. $F_{X2/3} = 1$ means that the possible faulty switch is S_{X2} or S_{X3}.

After the group-level fault is detected, the device-level fault diagnosis is enabled. And meanwhile, the modulation mode is changed from 3L to 2L mode. Under 2L mode, Two OC faults in the located faulty group can show different output characteristics. If the inner switch has an OC fault, the system will return to normal under 2L mode. If the outer switch is the faulty one, the system is still faulty under 2L mode. The location rules for device-level OC fault location are summarized in Table V. The device-level fault diagnosis zone is set as $[0.1\mathrm{T_{ac}}, \mathrm{T_{ac}}]$ within the next basic period. The blanking time is selected as $0.1\mathrm{T_{ac}}$ at the beginning of the next basic period to eliminate the misdiagnosis in modulation mode switching. $\mathrm{T_{ac}}$ represents the basic period of the output phase voltage or current. The modulation mode transition process affects the expected phase voltage and diagnosis variables calculation in approximately one switching period. Therefore, setting the prohibited zone to $0.1\ \mathrm{T_{ac}}$ is sufficient to eliminate false positives. Meanwhile, the OC fault characteristic occurs repeatedly with $\mathrm{T_{ac}}$ as a period. Hence, the Tac is enough as an upper limit of the device-level fault diagnosis zone.

Li et al. [38] propose a fault location method by changing the 3L modulation strategy of the faulty phase into the 2L mode, and the other two healthy phases still work in the 3L mode. The above-mentioned method can be realized by adding an offset value to the action time of three-phase reference voltages [41]. However, adding a compensation algorithm to the 3L modulation strategy is more complex than using 2L modulation directly. Meanwhile, the blanking time during modulation mode switching is not discussed clearly in [38].

The device-level fault diagnosis step switches all phases from 3L to 2L modulation mode. The expected phase voltage should be adjusted to (21) under the SVPWM strategy and to (20) and (22) under the SVPWM strategy. In the fault diagnosis zone $[0.1\mathrm{T}_{\mathrm{ac}}, \mathrm{T}_{\mathrm{ac}}]$, if the event $|V_r| > V_{th}$ ($F\_flag = 1$) occurs, it indicates that the OC fault occurs in two outer switches ($F\_switch = 1$ or 2). On the contrary, if the event $|V_r| < V_{th}$ ($F\_flag = 0$) is always met, the fault occurs in both inner switches ($F\_switch = 3$ or 4). Combined with the group-level fault diagnosis results $F_{X1/4}$ and $F_{X2/3}$, the device-level fault diagnosis results will be obtained.

In conclusion, the fault diagnosis process is simple without any parameter choice and shows strong robustness under various load transients through the designed adaptive threshold. A hierarchical fault diagnosis scheme is designed, which can satisfy complexity and adaptability requirements.

The input variables for fault diagnosis, such as input phase current and load voltage, are directly from existing controllers. Generally, the variables used for closed-loop control need to be processed by the filter, such as the sigma-delta filter and low-pass filter. Hence, the impact of environmental noises on the fault diagnosis method is significantly reduced by the embedded filter in the controller. In addition, a counter filter (i.e., a time threshold comparator) can be added to eliminate environmental noise influence when the voltage vector residual is compared with the adaptive threshold. Since the sigma-delta filter is a digital filter, which can remove quantization noise outside the frequency band and prevent aliasing, the sigma-delta filter is adopted in the hardware for environmental noise elimination. The dc bias of sensors can be eliminated by adding a compensation offset in the analog-to-digital converter. As the dc bias of sensors is constant, the dc bias of sensors can be viewed as a system error input. Thus, the inherent residual component due to dc bias can also be considered when calculating the adaptive residual vector amplitude threshold.

IV. EXPERIMENTAL RESULTS

A. Experimental Setup

The experiments are conducted on the 3L-T inverter platform, as shown in Fig. 6. The model number of DSP is TMS320F28377S, which can be used for programming to realize inverter control and fault diagnosis. Various OC faults are simulated manually by the software forcing function in the enhanced pulse width modulator (ePWM). The diagnostic variables and results are saved in the DSP and plotted by MATLAB. The main parameters of the system are listed in Table VI.

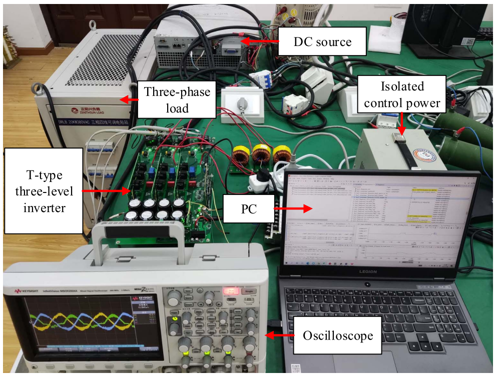


Fig. 6. 3L-T inverter experimental platform.

TABLE VI
MAIN PARAMETERS OF THE TESTING PLATFORM

Parameters	Symbols	Values
DC-link Voltage	u_{dc}	150 V
Sampling/Switching Frequency	f_s	10 kHz
Dead Time	t_{dead}	5 µs
Turn-on delay	t_{on}	20 ns
Turn-off delay	t_{off}	20 ns
Filter Inductances	L_X	4 mH
DC-link Capacitance	$C_{high/low}$	480 µF
Load resistances	R_X	30/15 Ω
Rated frequency	f_{ac}	50 Hz

The dead-band submodule and action-qualifier submodule in DSP's ePWM can be used for OC fault simulation. Switch S_{A1} and S_{A3} work in a complementary manner under normal conditions. Take the S_{A1} OC fault as an example to explain the configuration method for the OC fault. S_{A1} and S_{A3} are controlled separately, and the software forcing function is enabled, which forces a continuous low on output S_{A1}. The software forcing function shields the expected PWM signal output by the SVPWM module. Based on this, the open circuit fault can be simulated manually in the experiments.

The fault diagnosis method can be applied to the occasions where the ac side voltage u_{xn} can be measured or estimated, such as grid-connected and motor drive systems. Without loss of generality, the fault diagnosis method under open-loop and closed-loop current control strategy is verified.

For the convenience of analysis, all electrical signals are normalized. The reference value of voltage (such as $u_{Xn\_ref\_pu}$, u_{Xn_pu}, and V_{th_pu}) and current signals (such as i_{X_pu} and $i_{d\_ref\_pu}$) are $u_{dc}/2$ V and 2.2 A, respectively. The artificially generated internal reference angle is featured at 50 Hz, and the initial phase angle of phase A is zero degrees ($t = 0$ ms).

B. Robustness of the Method

The experiment under closed-loop control with the current command $i_{d\_ref\_pu}$ changing from 0.1 to 0.9 is conducted to verify the robustness of the proposed method, as shown in Fig. 7. From Fig. 7(a) and (b), it can be seen that there is a small inherent voltage residual between $u_{Xn\_ref\_pu}$ and u_{Xn_pu} under light load conditions. But, $|V_r|_{\_pu}$ is consistently below the adaptive threshold V_{th_pu} [see Fig. 7(d)]. At the moment of load change at $t = 20$ ms, both i_{X_pu} and $|V_r|_{\_pu}$ undergo abrupt change [see Fig. 7(a) and (b)]. As V_{th_pu} is the function of the current slope [see formula (28)–(31)], V_{th_pu} will increase

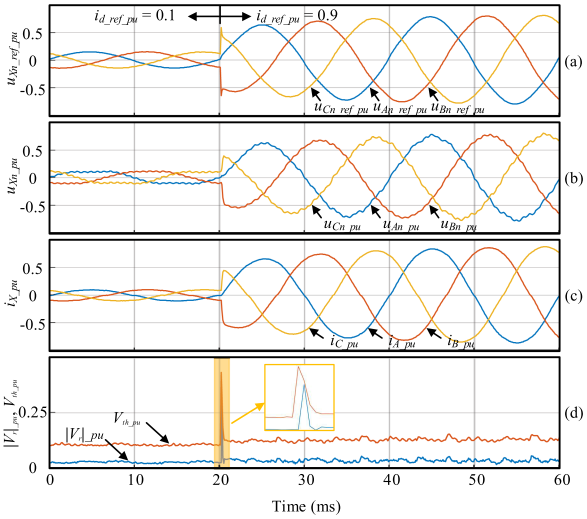


Fig. 7. Experimental results for robustness under load transient changes from $i_{d\_ref\_pu} = 0.1$ to $i_{d\_ref\_pu} = 0.9$. (a) $u_{Xn\_ref\_pu}$. (b) u_{Xn_pu}. (c) i_{X_pu}. (d) V_{th_pu} and $|V_r|\_{pu}$.

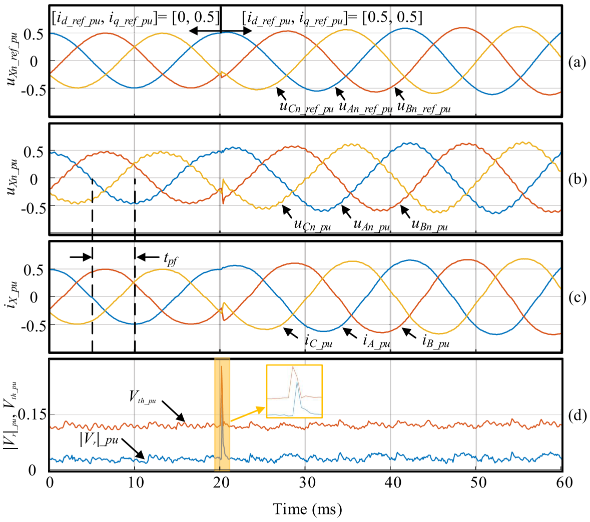


Fig. 8. Robustness experimental results with current command ranging from $[i_{d\_ref\_pu}, i_{q\_ref\_pu}] = [0.5, 0]$ to [0.5, 0.5]. (a) $u_{Xn\_ref\_pu}$. (b) u_{Xn_pu}. (c) i_{X_pu} and $|V_r|\_{pu}$. (d) V_{th_pu} and $|V_r|\_{pu}$.

correspondingly, as described in Fig. 7(d). It can be seen that $|V_r|\_{pu}$ is consistently below the threshold V_{th_pu} under load transient and stable heavy load conditions ($i_{d\_ref\_pu} = 0.9$). Under normal conditions, V_{th_pu} and $|V_r|\_{pu}$ are nearly in phase. However, under OC fault conditions, there is a moment of V_{th_pu} lag behind $|V_r|\_{pu}$. The main reason is that the variable V_{th_pu} is the function of the phase current slope, which is always 90° ahead of the current [see formula (27)–(31)].

The robustness of the proposed method under the current command ranging from $[i_{d\_ref\_pu}, i_{q\_ref\_pu}] = [0.5, 0]$ to [0.5, 0.5] is verified, as presented in Fig. 8. From Fig. 8(d), $|V_r|\_{pu}$ is consistently below $V_{th\_pu},$ and no false detection is triggered. Figs. 7 and 8 show that the robustness is strong against current command variation and modulation index regulation.

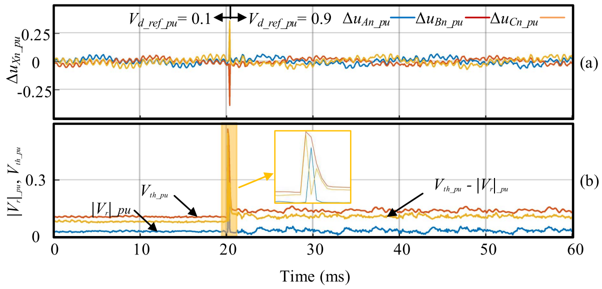


Fig. 9. Robustness experimental results under open-loop control. (a) Δu_{Xn_pu}. (b) V_{th_pu} and $|V_r|\_{pu}$.

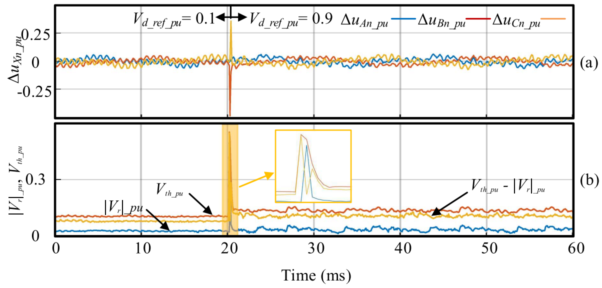


Fig. 10. Experimental results under unbalanced inductance parameters ($\Delta L_B = 0.3L_B$). (a) Δu_{Xn_pu}. (b) V_{th_pu} and $|V_r|\_{pu}$.

The robustness under open-loop control and unbalanced inductance parameters conditions are further studied, as shown in Figs. 9 and 10. In Fig. 9(a), compared with closed-loop control, the open-loop controller directly changes the voltage command, which makes the voltage residual Δu_{Xn_pu} change more drastically. In Fig. 9(b), the adaptive threshold can quickly respond to load changes without delay. The maximum value of Δu_{Bn_pu} under unbalanced inductance parameters conditions is larger than that under balanced conditions [see Figs. 9(a) and 10(a)]. Figs. 9(b) and (b) show that V_{th_pu} varies with the current slope, which makes V_{th_pu} always larger than $|V_r|\_{pu}$ in steady or dynamic conditions.

To further verify the robustness of the proposed method, the simulation and experimental results under various conditions are supplemented below. In PMSM drive applications, the robustness simulation results under variable speed and variable load torque conditions are presented in Fig. 11(a) and (b), respectively. The experimental results under variable current frequency and load resistance are shown in Figs. 12 –14. Owing to the self-adjusting characteristics of the adaptive threshold, the proposed method provides reliable diagnostic results in various operating states of 3L-T inverters and has good robustness against transient changes.

C. Effectiveness of the Method

Fig. 15 evaluates the method's effectiveness under light load conditions ($i_{d\_ref\_pu} = 0.1$), and the S_{A1} OC fault occurred at $t =$ 20 ms. With these settings, detailed experiments are conducted, and the diagnosis waveforms are presented in Fig. 15. From Fig. 15(a) and (b), it can be seen that the distorted phase voltage

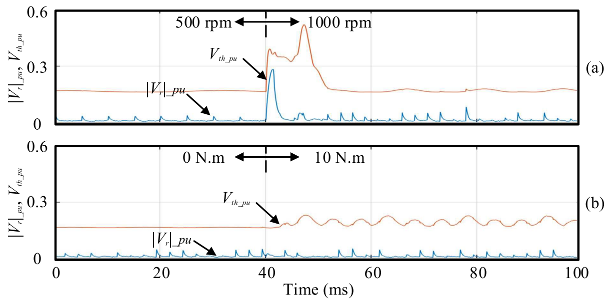


Fig. 11. Robustness results under variable speed and load torque conditions in PMSM drive applications rated at 2000 r/min. (a) V_{th_pu} and $|V_r|_{\_pu}$ with speed reference range from 500 to 1000 r/min. (b) V_{th_pu} and $|V_r|_{\_pu}$ with a load torque range from 0 to 10 N·m.

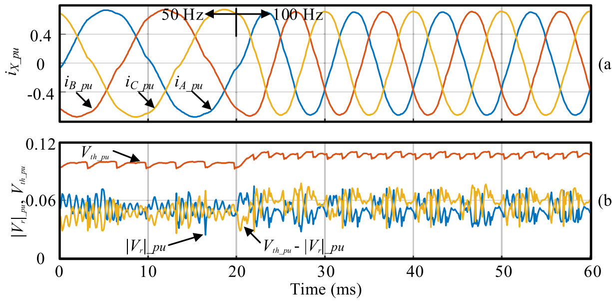


Fig. 12. Robustness results under variable current frequency from 50 to 100 Hz. (a) i_{A_pu}, i_{B_pu} and i_{C_pu}. (b) V_{th_pu} and $|V_r|_{\_pu}$.

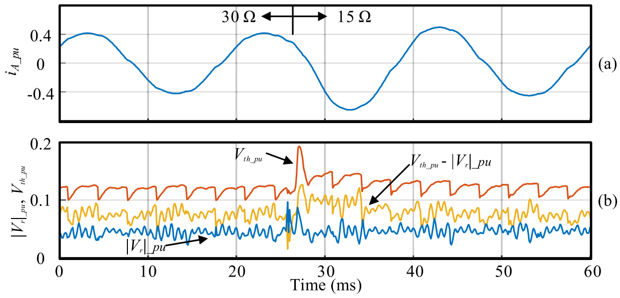


Fig. 13. Robustness results under variable load resistance in passive load applications with loads ranging from 30 to 15 Ω. (a) i_{A_pu}. (b) V_{th_pu} and $|V_r|_{\_pu}$.

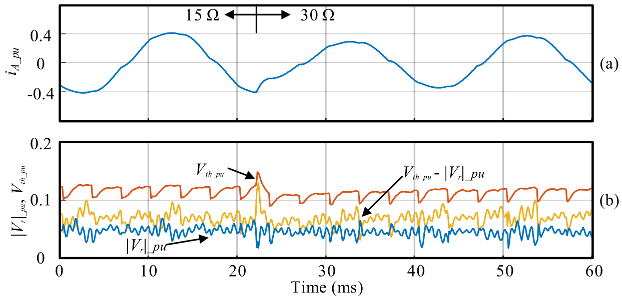


Fig. 14. Robustness results under variable load resistance in passive load applications with loads ranging from 15 to 30 Ω. (a) i_{A_pu}. (b) V_{th_pu} and $|V_r|_{\_pu}$.

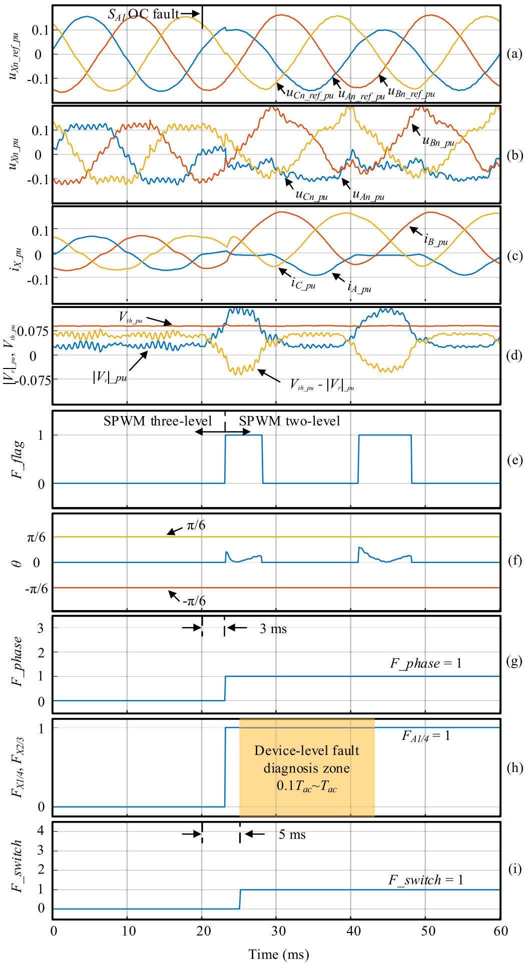


Fig. 15. Experimental results for S_{A1} OC fault under light load condition ($i_{d\_ref\_pu} = 0.1$). (a) $u_{Xn\_ref\_pu}$. (b) $u_{Xn'\_pu}$. (c) i_{X_pu}. (d) V_{th_pu} and $|V_r|_{\_pu}$. (e) *F_flag*. (f) θ. (g) *F_phase*. (h) $F_{X1/4}$, $F_{X2/3}$. (i) *F_switch*.

u_{An_pu} deviates from the reference value $u_{An\_ref\_pu}$ seriously. Meanwhile, the corresponding phase current i_{A_pu} is affected greatly [see Fig. 15(c)]. The threshold V_{th_pu} is higher than $|V_r|_{\_pu}$ in healthy conditions but lower than $|V_r|_{\_pu}$ in faulty conditions [see Fig. 15(d)]. *F_flag* is set to one immediately, as shown in Fig. 15(e), and group-level fault diagnosis is enabled. As shown in Fig. 15(f), θ is about zero (between -π/6 and π/6), which means the faulty phase is A (*F_phase* $= 1$) and $F_{X1/4} = 1$ (S_{A1} or S_{A4} has OC fault) at the instant $t = 23$ ms according to Table IV.

Once the group-level fault diagnosis is done, the 3L mode is switched to the 2L mode, and the equation for calculating the expected voltage should be changed to (21). As shown in Fig. 15(e) and (h), the fault state is not disappearing (*F_flag* $= 1$) within the device-level fault diagnosis zone [0.1T$_{\mathrm{ac}}$, T$_{\mathrm{ac}}$]. *F_switch* is set to one at the instant $t = 25$ ms, shown in Fig. 15(i).

Fig. 16 indicates the diagnosis result of OC fault on switch S_{B4} under heavy load conditions. The OC fault is artificially set at the instant $t = 20$ ms, but the OC fault does not disturb the system until t reaches 27.1 ms ($u_{Bn\_ref\_pu} > 0$). The voltage residual vector angle is between π/2 and 5π/6, and the

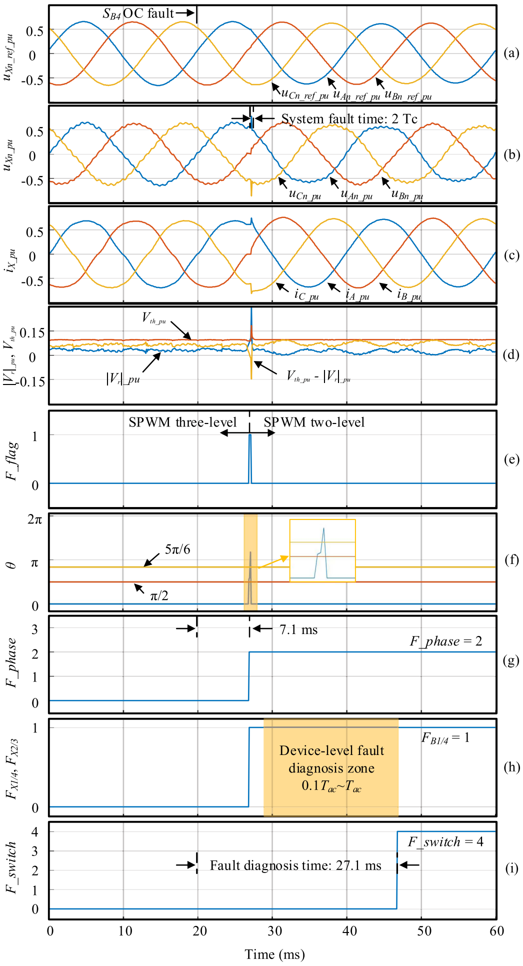


Fig. 16. Experimental results for S_{B4} OC fault under heavy load condition ($i_{d\_ref\_pu} = 0.7$). (a) $u_{Xn\_ref\_pu}$. (b) $u_{Xn'\_pu}$. (c) i_{X_pu}. (d) V_{th_pu} and $|V_r|\_{pu}$. (e) *F_flag*. (f) θ. (g) *F_phase*. (h) $F_{X1/4}$, $F_{X2/3}$. (i) *F_switch*.

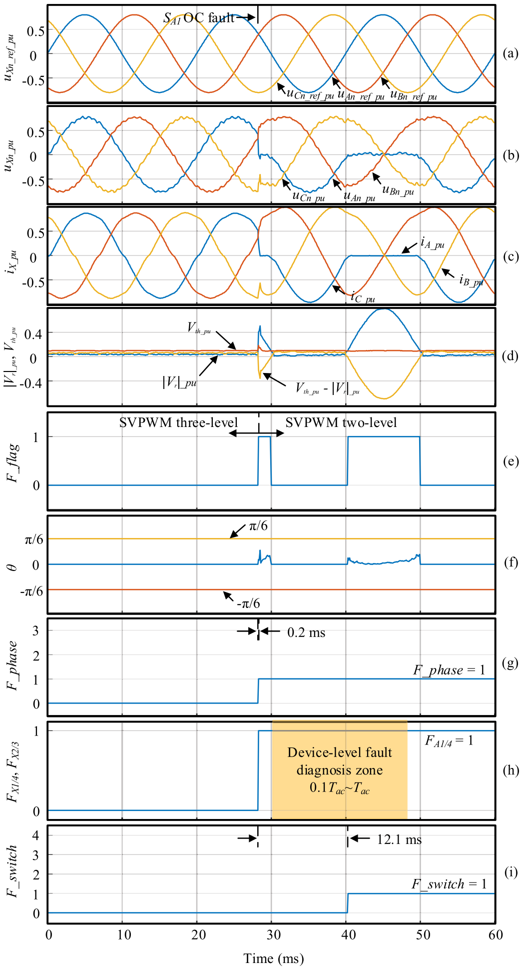


Fig. 17. Experimental results for S_{A1} OC fault under open-loop control condition in SVPWM strategy ($V_{d\_ref\_pu} = 0.8$). (a) $u_{Xn\_ref\_pu}$. (b) $u_{Xn'\_pu}$. (c) i_{X_pu}. (d) V_{th_pu} and $|V_r|\_{pu}$. (e) *F_flag*. (f) θ. (g) *F_phase*. (h) $F_{X1/4}$, $F_{X2/3}$. (i) *F_switch*.

group-level fault is detected (*F_phase* $= 2$ and $F_{X1/4} = 1$) at $t = 27.1$ ms, according to Table IV. Variable *F_flag* is continuously observed once the device-level fault diagnosis is enabled at $t = 27.1$ ms. As shown in Fig. 16(e) and (h), no fault is detected in the entire fault diagnosis zone, which means the system returns to normal under 2L mode. Based on Table V, the diagnosis variable *F_switch* equals four at the instant $t = 47.1$ ms. Although the total fault diagnosis time between the fault initiation and the fault localization is relatively long (27.1 ms), the effective time (namely the system fault time at the fault diagnosis stage) that the OC fault distorts the system is only 0.4 ms (from 26.7 to 27.1 ms). It should be noticed that the modulation mode switching may disturb the diagnosis variables *F_flag* and θ, as shown in Fig. 16(e) and (f). However, the false detection probability can be effectively eliminated owing to the prohibited zone [0, 0.1T$_{\text{ac}}$].

Fig. 17 presents the waves of the S_{A1} OC fault in the SVPWM strategy. Comparing Figs. 16(c) and 17(c), it can be seen that there is a slight difference in current waves between SVPWM and SPWM strategies under normal operation. Before the OC fault occurs, the diagnosis variable $|V_r|\_{pu}$ is below the threshold V_{th_pu}. After the OC fault is triggered at $t = 28$ ms, *F_flag* changes to one soon, and the vector angle θ points to 0°. Based on Tables IV and V, the group-level and device-level OC faults are diagnosed at $t = 28.2$ ms and $t = 40.1$ ms, respectively. Considering that the faulty switch does not participate in the system operating within the current negative half cycle, the fault of S_{A1} can not be detected in the interval [30 ms, 40 ms].

Similar experiments have been carried out under the nonunity power factor condition of load ($R_X = 0\ \Omega$ and $L_X = 4$ mH), as shown in Fig. 18. It can be seen that the proposed diagnosis method is suitable for applications with various power factors. The fault diagnosis time in the above-mentioned four tests is different. It can be found that the diagnosis speed is related to the fault occurring time. For example, the fault can be detected immediately when the $S_{A1/4}$ OC fault occurs in the positive half period. However, if the OC fault happens during the negative half period, the fault cannot be detected until the next positive half period.

In Fig. 17, the S_{A1} OC fault occurs at $t = 28$ ms. Once the group-level fault diagnosis is complete ($t = 28.2$ ms), the counter for the following basic period starts counting. The next basic

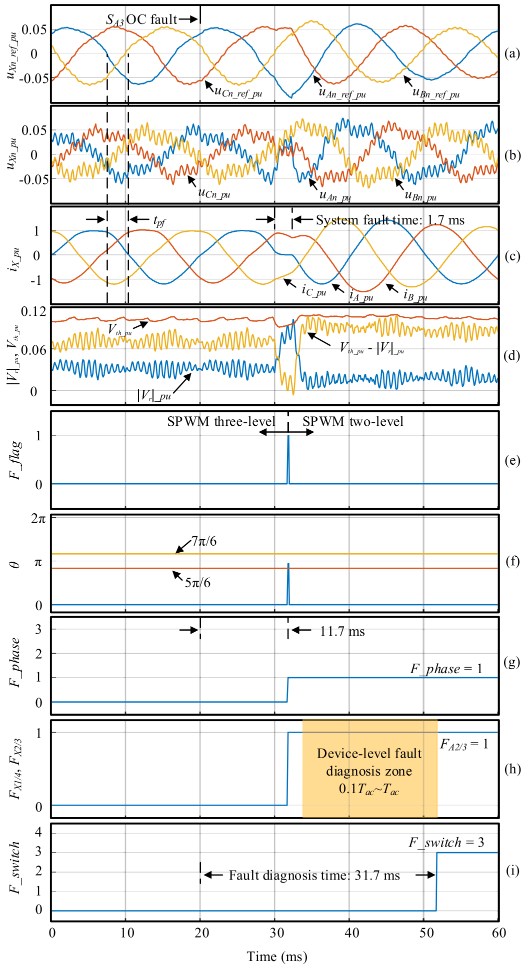


Fig. 18. Experimental results for S_{A3} OC fault under non-unity power factor load condition ($i_{d\_ref\_pu} = 1$). (a) $u_{Xn\_ref\_pu}$. (b) $u_{Xn'\_pu}$. (c) i_{X_pu}. (d) V_{th_pu} and $|V_r|\_{pu}$. (e) *F_flag*. (f) θ. (g) *F_phase*. (h) $F_{X1/4}$, $F_{X2/3}$. (i) *F_switch*.

period starts at $t = 28.2$ ms and ends at $t = 48.2$ ms. The group-level and device-level OC fault is diagnosed at $t = 28.2$ ms and $t = 40.1$ ms, respectively. The device-level fault detection time in Fig. 17 is 12.1 ms. In Fig. 18, the OC fault diagnosis time is 1.58 times the fundamental cycle. The main reason is that there is an inherent undetectable region ([$t = 20$ ms, $t = 30$ ms]). In the device-level fault diagnosis zone, the system returns to normal operation as the faulty switch is isolated from the system by the proposed modulation mode switching method, as shown in Fig. 18(b) and (c). Therefore, while the device-level fault detection time is relatively long [about a basic period, as shown in Fig. 18(h)], the abnormal time of the system is short (from $t = 30$ ms to $t = 31.7$ ms).

The S_{A2} and S_{A3} OC faults are simulated to verify the effectiveness of the proposed method in the PMSM control systems, as shown in Figs. 19 and 20. For the motor drive systems, the actual pole voltage u_{Xn} can be estimated from the electrical speed, electrical angle and the back electromotive forces. The basic period T_{ac} [$= 60/(P{\cdot}n)$] is a function of pole pairs P and the speed n of the motor. As illustrated in Fig. 19(a), once the S_{A3} OC fault occurs, $|V_r|\_{pu}$ is larger than V_{th_pu}, and the faulty phase and faulty group ($S_{A2/3}$) are identified according to Table IV. After that, the 3L modulation strategy becomes the 2L modulation strategy. As shown in Fig. 19(b), the abnormal state disappears, indicating that the faulty switch is S_{A3}. However, the fault still exists under the 2L modulation strategy, which implies that the faulty switch is not bypassed, as shown in Fig. 20(b). Thus, the S_{A2} OC fault can be located by the location rules, as given in Table V.

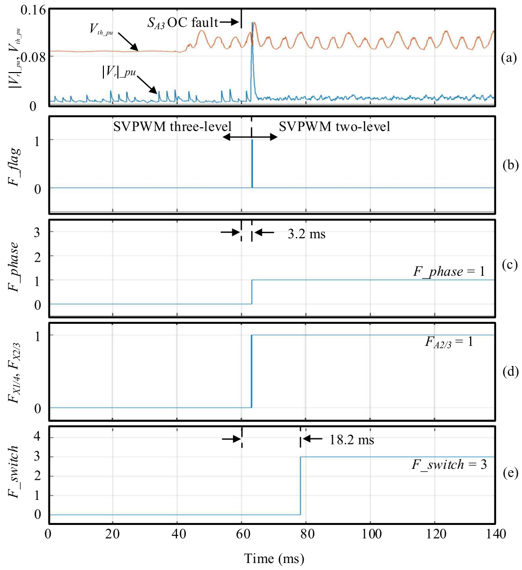


Fig. 19. Fault diagnosis simulation results for S_{A3} OC fault in PMSM drive applications. (a) V_{th_pu} and $|V_r|\_{pu}$. (b) *F_flag*. (c) *F_phase*. (d) $F_{X1/4}$, $F_{X2/3}$. (e) *F_switch*.

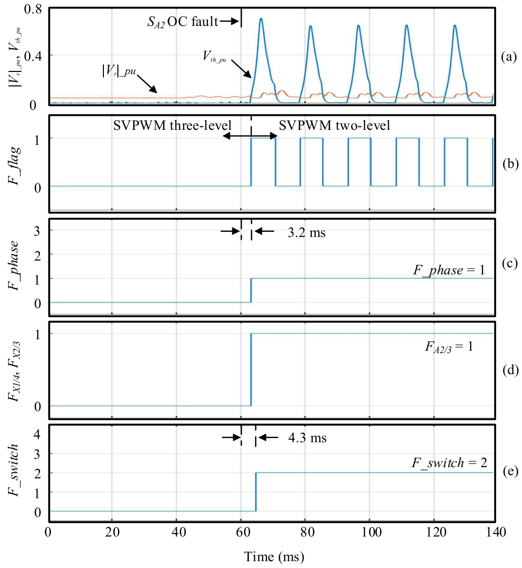


Fig. 20. Fault diagnosis simulation results for S_{A2} OC fault in PMSM drive applications. (a) V_{th_pu} and $|V_r|\_{pu}$. (b) *F_flag*. (c) *F_phase*. (d) $F_{X1/4}$, $F_{X2/3}$. (e) *F_switch*.

D. Comparison With Previous Methods

Comparison and analysis of the cited methods and the proposed fault diagnosis method for 3L topology converters are

TABLE VII
COMPARISON AND ANALYSIS WITH PREVIOUS METHODS

Method	Topology	Complexity	Robustness	Safety	Diagnosis time & System fault time			Threshold type (N: the number of thresholds)
					Average	Minimum	Maximum	
[17]	3L-T rectifier	Low	Low	High	0.325×Tac & 0.2×Tac	0.2×Tac & 0.2×Tac	0.7×Tac & 0.2×Tac	Fixed: Current amplitude and current slope ($N = 2$)
[19]	3L-T inverter	Low	Low	Low	0.3×Tac & 0.15×Tac	0.15×Tac & 0.15×Tac	0.65×Tac & 0.15×Tac	Fixed: Zero current time ($N = 1$)
[30]	3L-T inverter	Medium	High	High	1×Tac & 0.5×Tac	1×Tac & 0.5×Tac	1×Tac & 0.5×Tac	Adaptive: Voltage modulus of eigenvector ($N = 1$)
[33]	3L-T rectifier	Low	Low	Medium	1.4×Tac & 0.9×Tac	1.3×Tac & 0.8×Tac	1.7×Tac & 1.2×Tac	Fixed: Line voltage residual ($N = 3$)
[34]	3L-NPC converter	High	High	Low	0.125×Tac & 2×Tc	2×Tc & 2×Tc	0.5×Tac & 2×Tc	Adaptive: Dc-link voltage difference residual ($N = 2$)
[37]	3L-T inverter	Medium	High	Low	0.213×Tac & 0.07×Tac	0.06×Tac & 0.06×Tac	0.58×Tac & 0.08×Tac	Adaptive: Voltage residual vector in $\alpha\beta$ coordinate ($N = 2$)
[38]	3L-T inverter	Medium	Medium	High	0.125×Tac & 0.03×Tac	4×Ts & 4×Ts	0.5×Tac & 0.08×Tac	Adaptive: Line voltage residual ($N = 3$)
Proposed method	3L-T inverter	Medium	High	High	0.47×Tac & 0.02×Tac	0.1×Tac & 2×Tc	1.58×Tac & 0.08×Tac	Adaptive: Voltage residual vector amplitude ($N = 1$)

Notes: Tac: basic cycle, Ts: sampling cycle, Tc: switching cycle.

carried out in Table VII. The primary evaluation and analysis items include the topology structure, implementation complexity, average diagnosis time, and threshold type. The diagnosis time of the proposed method in Table VII means the average values in a basic period. The average fault diagnosis time is tested when an OC fault occurs at 20 evenly spaced moments within a current fundamental period.

The threshold types listed in Table VII can reflect the pros and cons of the selected fault diagnosis features to a certain degree. The robustness of the current signal-based method [17], [19] using phase current amplitude, slope, and zero value time as fault features are susceptible to load fluctuations. The calculation of the voltage modulus of the eigenvector in [30] requires storing large amounts of waveform data in one previous basic period. Obviously, it is not easy to apply in variable frequency output. In [34], the residual method based on the dc-link voltage difference presents challenges to the high-resolution dc-link voltage sampling, limiting their applications. Among the methods based on voltage residual, it has multiple diagnosis features in *abc* coordinate or $\alpha\beta$ coordinate in [33], [37], and [38]. However, the proposed method uses voltage residual vector amplitude in polar coordinates as fault features, reducing the threshold judgment's complexity while retaining all fault characteristics. Theoretically, the misdiagnosis rate and complexity can be reduced compared to the above-mentioned voltage residual-based methods.

1) Theoretical Analysis of Voltage Residual: Some voltage-based fault diagnosis methods have been proposed, which directly use phase or line voltage residual phenomenon but lack a detailed analysis of its mathematical feature. In this article, the mathematical expression of output voltage under OC faults is analyzed in detail, and the voltage vector residual feature under OC faults is summarized.

2) Adaptive Threshold: The methods based on a fixed threshold [17], [19], [33] are relatively simple, but the robustness is not high. For the methods adopting the adaptive threshold, including [30], [34], [37], [38], and the proposed method, owing to the self-adjusting ability of the designed threshold, superior robustness can be obtained without reducing the diagnosis speed. The proposed method in [30] is only suitable for the passive load. In [34], the complex threshold learning method is adopted, which increases the computing burden. The fault diagnosis process in this article requires only one adaptive threshold (voltage residual vector amplitude). However, the other adaptive threshold setting method has multiple threshold variables, such as voltage vector residual in $\alpha\beta$ coordinate [37] and line voltage residual [38] in abc coordinate. The number of thresholds can reflect the computational complexity to a certain degree. Meanwhile, the proposed fault detection method using voltage residual vector amplitude as the adaptive threshold is theoretically faster than the previous methods based on multiple threshold variables because all thresholds need to be met simultaneously for fault diagnosis methods based on multiple threshold variables.

3) Fault Location Step: The specific switching signal injection method is proposed in [37]. However, during the injection of the specific switching signals, the control system is disabled, which puts the system at risk in terms of overcurrent. For [38], it only explains the implementation under the SPWM strategy, and the modulation mode transition process is neglected. In addition, three thresholds are required. This article proposes a hierarchical diagnosis method that incorporates the modulation mode switching method into locating the fault location, which can be used for both SVPWM and SPWM strategies. Faulty switches sharing similar features can be distinguished effectively.

The proposed modulation mode switching method does not have much effect on the system other than adding some harmonic content. It should be pointed out that the tolerance controls [41] are enabled once the fault location step is completed. Therefore, the adverse effects of the 2L modulation mode on the system can be neglected.

4) Robustness, Safety, and Rapidity: Methods based on fixed threshold [17], [19], [33] have the possibility of misdiagnosis caused by changes in working conditions. The proposed method shows strong robustness against load, output frequency, parameter, and control command variations owing to the self-adjusting ability of the designed adaptive threshold. Since the specific signal injection methods need to bypass the normal control system, the existing methods [34], [37] with strong robustness put the system at risk of overcurrent during fault location. The proposed method achieves fault location by switching modulation mode and is based on ensuring system safety. Meanwhile, the system fault time, the effective time that the OC fault distorts the system during the fault diagnosis stage, is also an important indicator for evaluating the fault diagnosis method. As shown in Table VII, although the proposed method has no advantage in fault diagnosis time, it shows a similar superiority in system fault time to the methods in [34], [37], and [38]. Meanwhile, the proposed is more secure than [34] and [37] and more robust than [38]. In conclusion, it has better comprehensive performance in complexity, robustness, safety, and rapidity.

E. Limitations of the Method

The innovations include specific implementation methods for hierarchical fault diagnosis. For group-level fault diagnosis, the group-level fault is located according to voltage residual vector amplitude and angle, adopting the proposed adaptive threshold. The proposed method achieves fault location by modulation mode switching for device-level fault diagnosis. However, there is still room for improvement in fault diagnosis time.

The device-level fault diagnosis zone is set as $[0.1\mathrm{T}_{\mathrm{ac}}, \mathrm{T}_{\mathrm{ac}}]$ to deal with nonunity power factor conditions. Hence, the inner switch OC fault ($S_{X3/4}$) can only be detected at the end of the fault diagnosis zone, which increases the fault diagnosis time. The action zone of the two switches in the detected faulty group can be obtained according to the voltage and current command. The power switch action zone represents the accurate enable area of the power switch. In the power switch action zone, the switch command is “ON,” and the power switch is valid when the current command is positive (from the collector to the emitter). Fault diagnosis results are available at the end of the action zone without waiting for the end of a basic cycle. Performing fault diagnosis in the action zone will further improve the diagnosis speed.

Theoretically, the proposed method can be applied to applications using FOC control and voltage-second balancing theory. The proposed method is unsuitable for motor drive applications employing a simple six-step square wave control method.

V CONCLUSION

This article proposes a phase voltage vector residual model of the 3L-T inverter and applies it to the fault diagnosis. The diagnosis variables are the phase voltage vector residual characteristics caused by OC faults under ZC and non-ZC conditions. A hierarchical fault diagnosis scheme is proposed in this article. This way, the fault is detected by comparing the voltage residual vector amplitude with the designed adaptive threshold. The group-level fault is located according to voltage residual vector amplitude and angle. The device-level fault diagnosis is realized by switching the modulation mode from 3L mode to 2L mode. Many experiments have been conducted to verify the proposed method’s robustness and effectiveness under various conditions, such as different modulation strategies and control structures, unbalanced inductance parameters, light load conditions, various power factors, variable current frequency, and so on. Compared with the existing fault diagnosis method, the proposed method has better comprehensive performance in terms of complexity, robustness, safety, and rapidity. Part of our future work is to reduce the device-level fault diagnosis time and locate the multiple OC faults for the 3L-T inverter.

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