A Robust Controller With Integrated Plant Dynamics for Constant Power Loads in DC MicroGrid

Hossein Gholizadeh Narm, Suzan Eren, *Member, IEEE*, and Masoud Karimi-Ghartemani, *Senior Member, IEEE*

***Abstract*—Constant power loads (CPLs) pose a challenge for the control system of power electronic converters due to their negative damping characteristic. In this article, a fast and robust control system is introduced for a buck converter which can robustly feed and stabilize a dc bus with all kinds of loads, especially CPLs. The proposed controller properly takes advantage of the internal converter dynamics and removes the common integrating term used in the literature. In other words, the proposed controller does not increase the order of the control system. As a result, it provides a simple yet robust structure and performance, while at the same time provides a tight converter current-limiting feature. A simple two-step algorithm is presented to summarize the design stage of the controller, which only consists of two parameters. Detailed analyses, simulations, and laboratory-scale experimental results are presented to illustrate the desired performance of the proposed controller. The proposed controller is also compared with a state-of-the-art controller and its better performance is confirmed.**

***Index Terms*—Buck converter, constant power load (CPL), converter control, DC microgrid, plant-integrating controller.**

I. Introduction

ENERGY resource and environmental concerns are the major motivations to promote renewable energy technologies, such as photovoltaics (PVs) and wind generators. The proliferation of PV and battery energy storage (BES) systems, as well as dc charging stations for electric vehicles, signifies growing interest in the dc microgrid approach. One particular issue with such systems is the presence of so-called constant power loads (CPLs), which are converter-based loads drawing a constant power regardless of the voltage supplied to them. As a result, a CPL behaves similar to a negative resistor which compromises the system stability [1], [2], [3].

Manuscript received 10 August 2022; revised 1 November 2022; accepted 13 December 2022. Date of publication 19 December 2022; date of current version 14 February 2023. Recommended for publication by Associate Editor A. Davoudi. *(Corresponding author: Hossein Gholizadeh Narm.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3230640.

Digital Object Identifier 10.1109/TPEL.2022.3230640

A number of studies are performed to overcome the stability challenge posed by CPLs. While the majority of them have utilized linear approaches [2], [4], [5], [6], some have used nonlinear control approaches due to the inherent nonlinearity of a CPL [1], [7], [8], [9], [10], [11], [12], [13], [14]. However, the nonlinear approaches, in general, tend to hinder an efficient and systematic stability analysis, design stage, and may also require more computational resource. For instance, in [13], three parameters need to be selected which can require a long and complicated trial-and-error work. Both passive damping approaches [15], [16], and active damping approaches [2], [4], [11] have been proposed. While passive damping is simple and robust, it causes additional power losses. Active damping, on the other hand, avoids losses but can complicate the control system, its analysis, and design, as well as increasing the controller bandwidth which may compromise stability margins.

In [17], an adaptive virtual capacitor approach is used to enhance the stability. In [18], using the power balance principle, a virtual resistance is added to counter the effect of CPL. Application of reinforcement learning to obtain the coefficients of a model-free sliding mode controller that aims at reducing the impact of CPL on a dc energy system is reported in [19]. An online-based deep learning algorithm was reported in [20]. Observing the output voltage reveals that the excessive overshoot is due to the lack of initial state training. Overall, it appears that learning approaches for the primary controller is not yet a reliable approach, while using it as a compensator for unknown parameters or unexpected circumstances may be a good idea [21].

The effect of CPL becomes more critical when it is connected to the bus through an LC filter. While an LC filter makes the current pulled from the bus smoother, and the voltage at the input terminals of CPL would have smaller ripples, it will add a poorly-damped resonance mode to the system that must be passively or actively damped. In this regard, in [15] a passive damping approach is proposed and based on it, two active damping methods are suggested in [22] and [5]. In [22], the reference voltage of the source side converter is linearly drooped. The method is simple and effective but it requires an additional current sensor, and it also appears that the output voltage drops excessively as the load goes up. To address this problem, a technique is proposed in [5] based on [15] to apply a virtual resistor paralleled by an inductor. Although this fixes the output voltage, it suffers from the presence of a high-pass filter in the path of the current sensor, which can cause much noise. On the other hand,

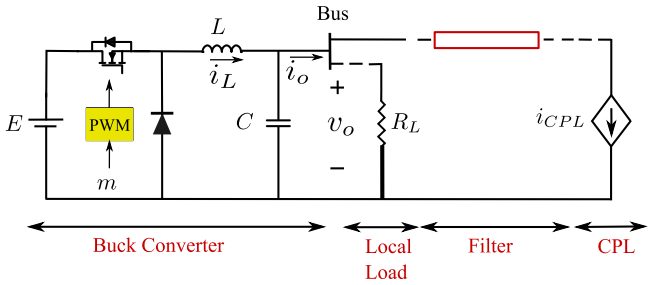

Fig. 1. Buck converter feeding a local load and a CPL.

a high bandwidth control system is necessary to track the created reference. In [23], an optimal control based linear approach is used to control a bidirectional dc/dc converter. This approach advantageously allows a small level of variations to the voltage to improve the system stability. To achieve current-limiting for the converter, it uses an internal feedback loop whose gains are optimally designed to yield fast and robust performance. It, however, needs multiple control gains and, particularly, one of them must be closely freezed during the current-limiting mode. In [23], when the power flows from the source towards the load, the converter is a boost converter.

Inspired by [23] and [24], in this article, a controller for a buck converter is proposed to particularly address the stability challenges of CPLs. It has the following features:

1) similar to [23], it allows a small variation of the bus voltage, to improve stability,
2) it deploys the internal dynamics of the converter to obviate the need for additional internal feedback loops for current-limiting,
3) it does not increase the system's order,
4) its design stage is very simple and transparent, and
5) it achieves a highly robust and swift performance.

In fact, the proposed controller is characterized by only two parameters. Thus, a step-by-step algorithm for their design is also presented. Through analyses, computer simulations, and laboratory-scale experimental tests, the article demonstrates the desired performance of the proposed controller to significantly counter stability problems associated with CPLs.

II. Study System and Modeling

Fig. 1 shows the circuit diagram of a buck converter, which has its output terminals connected to the bus such that a local load R_L and/or a CPL is fed from the bus. The CPL is modeled by a proper current source. It may also be interfaced through a filter in general.

Without a filter, the averaged state space model is

$$L\frac{di_L(t)}{dt} = mE - v_o \quad C\frac{dv_o(t)}{dt} = i_L - i_o$$
$$= i_L - \frac{v_o}{R_L} - \frac{P_{\rm CPL}}{v_o} \tag{1}$$

where L and C are the converter's filter inductance and capacitance values, respectively, i_L and v_o are the inductor current and capacitor voltage, respectively, and m is the modulation index.

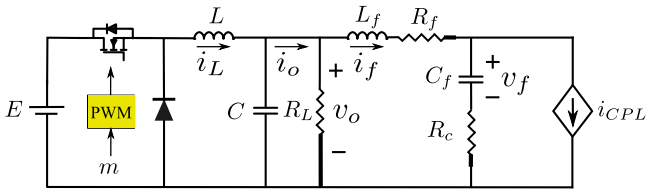

Fig. 2. Buck converter feeding a CPL through an LC filter.

The dc source amplitude is E, the converter output current is i_o, and $P_{\rm CPL}$ is the CPL power. This indicates a nonlinear system with two state variables.

The nonlinearity introduced by the CPL has a destabilizing nature because linearizing the function $i = \frac{P_{\rm CPL}}{v_o}$ around the operating point V_o results in $i = \frac{P_{\rm CPL}}{V_o} - \frac{P_{\rm CPL}}{V_o^2}(v_o - V_o)$ which means a "negative" resistance $-R_{CPL} = -\frac{V_o^2}{P_{\rm CPL}}$ in parallel with a current source of $2\frac{P_{\rm CPL}}{V_o}$. More precisely, the system becomes open-loop unstable when the CPL is larger than the local load.

When the CPL is connected through an LC filter, as shown in Fig. 2, the equations change to

$$L\frac{di_L(t)}{dt} = mE - v_o$$
$$C\frac{dv_o(t)}{dt} = i_L - \frac{v_o}{R_L} - i_f$$
$$L_f\frac{di_f(t)}{dt} + R_f i_f = v_o - v_f - R_c C_f \frac{d}{dt}v_f$$
$$C_f\frac{dv_f(t)}{dt} = i_f - \frac{P_{\rm CPL}}{v_f + R_c C_f \frac{d}{dt}v_f} \tag{2}$$

where L_f and C_f are the filter's inductance and capacitance values, each one having a resistance in series with them (i.e., R_f and R_c), and i_f and v_f are their current and voltage, respectively. This indicates a highly nonlinear system with four state variables. If the small voltage across R_c compared with the voltage across C_f is neglected in the fourth equation, (2) simplifies to

$$L\frac{di_L(t)}{dt} = mE - v_o$$
$$C\frac{dv_o(t)}{dt} = i_L - \frac{v_o}{R_L} - i_f$$
$$L_f\frac{di_f(t)}{dt} = -(R_f + R_c)i_f + v_o - v_f + R_c\frac{P_{\rm CPL}}{v_f}$$
$$C_f\frac{dv_f(t)}{dt} = i_f - \frac{P_{\rm CPL}}{v_f}. \tag{3}$$

We use (3) to represent this system in this article.

III. Proposed Controller

Fig. 3 shows the control diagram of the buck converter. The main control objectives may be summarized as follows: 1) regulate the output voltage v_o to (or close to) the desired value V_o^*. 2) limit the converter current below a maximum value

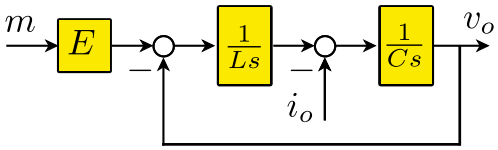

Fig. 3. Control block diagram of buck converter.

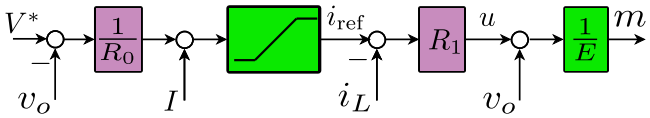

Fig. 4. Block diagram of proposed controller.

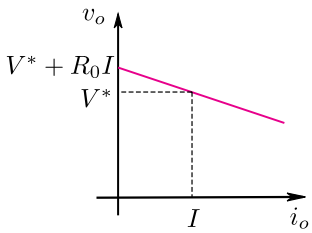

Fig. 5. Steady-state V-I characteristics of proposed controller.

$I_{\max}$. 3) Maintain the above two objectives in the presence of system uncertainties, disturbances, and CPL.

The proposed controller is summarized by

$$mE - v_o = u = R_1(i_{\text{ref}} - i_L) = R_1\left[I + \frac{1}{R_0}(V_o^* - v_o) - i_L\right] \tag{4}$$

and its block diagram is illustrated in Fig. 4. To explain the proposed controller, one can notice that the internal feedback on v_o cancels the natural voltage feedback of the converter shown in Fig. 3. The feedback of i_L forms a middle closed-loop on the inductor current. The most external feedback on v_o generates the inductor current reference which is limited using a saturation block before being forwarded to the middle loop.

In the steady state, $i_o = i_L = i_{\text{ref}}$ on average (i.e., ignoring the switching ripples). Therefore, the proposed controller establishes

$$v_o = V_o^* - R_0(i_o - I). \tag{5}$$

This means that the output voltage v_o drops linearly as the converter current i_o goes up. Fig. 5 shows this droop behavior of the proposed controller. The output voltage is equal to V_o^* when the converter current is equal to I, and it goes up/down as its current goes down/up away from I. For the selection of I equal to the current rating of the converter, its output voltage will be equal to V_o^* when it supplies its rated current.

Remark 1: If i_o is used for I, the output voltage will be regulated to V_o^* for all loading conditions, i.e., without any offset. While this may be interesting from a theoretical point of view, but it is not recommended in this article for the following reasons: 1) another current sensor is needed; 2) this will be another node for feeding ripple and noise to the loop. Moreover, the droop characteristic has inherent stability and helps to increase the stability margins of the entire system.

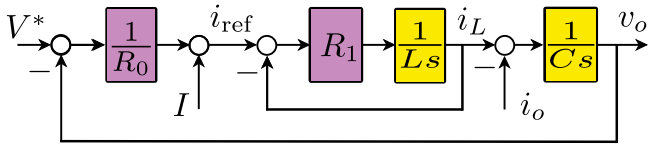

Fig. 6. Equivalent diagram of proposed control system by applying (4).

The proposed controller takes advantage of the natural dynamics of the converter. More precisely, it establishes a type-1 feedback loop and removes the steady-state error from the converter current without using an integrator. This is further illustrated in Fig. 6. Thus, the proposed controller accomplishes the control without adding a new state variable into the system. This prevents possible generation of sluggish dynamics. Moreover, it greatly simplifies the design stage into the design of only two constants R_0 and R_1 which is discussed as follows.

A. Design of Proposed Controller Gains

According to (5) and the steady-state characteristics shown in Fig. 5, the feedback gain R_0 determines the level of steady-state voltage offset for the entire range of operation. This must be sufficiently small to avoid excessive output voltage offsets. Meanwhile, it should be large enough to allow sufficient dynamic range for stability. Assuming that the maximum allowable voltage offset is α percent. This means that $R_0 I = 0.01\alpha V_o^*$. Sine $P = IV_o^*$, R_0 will be derived as

$$R_0 = 0.01\alpha\frac{V_o^{*2}}{P} \tag{6}$$

where P is the converter rated power.

To design R_1, we note that the current loop has a single pole at $s_{\text{current}} = -\frac{R_1}{L}$. This indicates a time-constant of $\tau_{\text{current}} = \frac{L}{R_1}$. To achieve a fast current dynamics that can enable current limiting, this time-constant must be sufficiently small but at least several times larger than the switching cycle of the converter. Therefore, its design equation may be proposed as

$$\tau_{\text{current}} = MT_{\text{sw}}, \;\Rightarrow\; R_1 = \frac{L}{MT_{\text{sw}}} \tag{7}$$

where $f_{\text{sw}} = \frac{1}{T_{\text{sw}}}$ is the converter switching frequency, and M is a positive number larger than 4.

In order to derive the design algorithm, treating i_o as an external disturbance, the closed-loop characteristic equation of this loop may be expressed as

$$\Delta(s) = s^2 + \frac{R_1}{L}s + \frac{R_1}{R_0CL} = 0. \tag{8}$$

Comparing (8) with the standard second order characteristic equation, i.e., $s^2 + 2\zeta\omega_n s + \omega_n^2$, implies

$$2\zeta\omega_n = \frac{R_1}{L}, \;\; \omega_n^2 = \frac{R_1}{R_0CL}, \;\Rightarrow\; \zeta = \sqrt{\frac{R_0R_1\,C}{4\,L}}. \tag{9}$$

TABLE I
SYSTEMS' PARAMETERS

Parameter	Definition	Value
R_0	Control parameter	0.2 Ω
R_1	Control parameter	5 Ω
L	Converter inductor	1 mH
C	Converter capacitor	1 mF
L_f	Inductor of the CPL filter	170 μH
R_f	CPL Inductor's internal resistance	10 mΩ
C_f	Capacitor of the CPL filter	220 μF
R_c	Damping resistance (series with C_f)	120 mΩ
E	Source voltage	70 V
V^*	Reference voltage of buck converter (bus)	50 V
P	Rated power	250 W
f_{sw}	Switching frequency	20 kHz

If this damping ratio ζ is sufficiently large for the selected R_0 and R_1, it means that the overall system responses are also well-damped.

According to the above analysis and discussion, the following design algorithm is proposed.

Proposed Design Algorithm: Given: Converter power rating P, its desired output voltage V_o^*, inductance L, capacitance C.

1) Choose a value $1 \leq \alpha \leq 10$ representing allowable percentage output voltage offset. Calculate R_0 from (6).
2) Choose a value $M \geq 4$ representing number of switching cycles within the time-constant of current loop. Calculate R_1 from (7).
3) Check the damping ration ζ from (9). If it is not sufficient, for the maximum allowable selection of α and minimum M, the capacitance value must be increased.

As an example, assume $P = 250\,\text{W}$, $V_o^* = 50\,\text{V}$, $L = 0.001\,\text{H}$, $C = 0.001\,\text{F}$, and $f_{\text{sw}} = 20\,\text{kHz}$, the algorithm results in: 1) for the selection of $\alpha = 5$, $R_0 = 0.01 \times 2 \times \frac{50^2}{250} = 0.2$, 2) for the selection of $M = 4$, $R_1 = \frac{0.001}{4 \times 0.00005} = 5$, 3) the damping ratio is $\zeta = \sqrt{\frac{0.2 \times 5 \times 0.001}{4 \times 0.001}} = 0.5$ which indicates a well-damped system. Therefore, the closed-loop bandwidth is $\omega_b = \omega_n \sqrt{1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}} = 6360$ rad/s and the no-load closed-loop poles, i.e., the roots of (8), are at $-2500 \pm j4330$. It is noteworthy that by this choice of M, and choosing sampling frequency equal to f_{sw}, there are at least four samples within a time-constant of response. Hence, it has no adverse impact on the stability. These values of parameters are used in this article, as shown in Table I.

IV. COMPLETE STABILITY ANALYSIS

The approximate stability analysis presented in Section III is based on ignoring the load dynamics. More specifically, the converter output current i_o was treated as an external disturbance. In this section, the impact of a resistive local load and also a CPL on the stability of this system are analytically studied. In the case of a CPL, two cases of without and with an interfacing filter are treated separately.

A. Stability Analysis for Resistive Local Load

In this preliminary case, only a simple local resistive load with resistance R_L is connected across the output terminals of the converter. Therefore, $i_o = \frac{v_o}{R_L}$ and the characteristic equation of the closed-loop system is given by

$$s^2 + \left(\frac{G_L}{C} + \frac{R_1}{L}\right) s + \frac{R_1 G_L}{CL} + \frac{R_1}{R_0 CL} = 0 \tag{10}$$

where $G_L = R_L^{-1}$. This indicates an always-stable system.

B. Stability Analysis for CPL Directly Connected

Assume that a CPL of power P_{CPL} is also connected to the bus in parallel with R_L. As mentioned, it introduces a negative resistance $-R_{\text{CPL}} = -\frac{V_o^{*2}}{P_{\text{CPL}}}$. This changes G_L in (10) to $G_L - G_{\text{CPL}}$, where $G_{\text{CPL}} = R_{\text{CPL}}^{-1}$

$$s^2 + \left(\frac{G_L - G_{\text{CPL}}}{C} + \frac{R_1}{L}\right) s + \frac{R_1 (G_L - G_{\text{CPL}})}{CL} + \frac{R_1}{R_0 CL} = 0. \tag{11}$$

Therefore, the stability conditions are

$$L(G_L - G_{\text{CPL}}) + R_1 C > 0, \quad R_0 (G_L - G_{\text{CPL}}) + 1 > 0.$$

This reduces to

$$G_{\text{CPL}} < \min(G_L + G_0, G_L + R_1 C L^{-1})$$

where $G_0 = R_0^{-1}$. The worst case is when there is no passive local load, i.e., $G_L = 0$. Now, $G_0 = R_0^{-1}$, according to (6), and in view of $1 \leq \alpha \leq 10$, corresponds to the case that the CPL power is at least ten times larger than the converter power. Therefore, the stability condition for the worst case can be simplified and stated as

$$G_{\text{CPL}} < R_1 C L^{-1} \quad \Rightarrow P_{\text{CPL}} < R_1 C L^{-1} V_o^{*2}. \tag{12}$$

For the numerical values in Table I, this indicates that the CPL power must be below 12 500 W which is way above the converter power. Therefore, the system is stable for all acceptable values of the CPL power.

C. Stability Analysis for CPL Connected Through Filter

This case is shown in Fig. 2 and its state space equations are listed in (3). Linearization of (3), and using the proposed control law of (4), results in

$$\begin{aligned}
L \frac{d\tilde{i}_L(t)}{dt} &= -R_1 \tilde{i}_L - \frac{R_1}{R_0} \tilde{v}_o \\
C \frac{d\tilde{v}_o(t)}{dt} &= \tilde{i}_L - \frac{\tilde{v}_o}{R_L} - \tilde{i}_f \\
L_f \frac{d\tilde{i}_f(t)}{dt} &= \tilde{v}_o - (R_f + R_c)\tilde{i}_f - \left(1 + R_c \frac{P_{\text{CPL}}}{V_o^{*2}}\right) \tilde{v}_f \\
C_f \frac{d\tilde{v}_f(t)}{dt} &= \tilde{i}_f + \frac{P_{CPL}}{V_o^{*2}} \tilde{v}_f
\end{aligned} \tag{13}$$

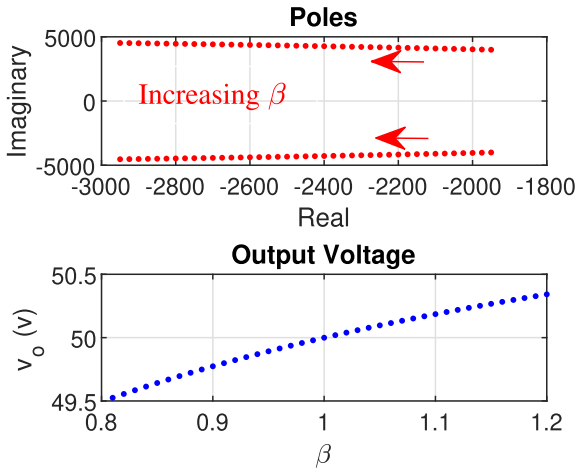

Fig. 7. Impact of $\pm 20\%$ variation in E on (top) closed-loop poles, (bottom) Steady state output voltage.

where the symbol $(\tilde{\cdot})$ represents the small signal variables. For the extreme case, i.e., $G_L = 0$ and $P_{CPL} = 250$ W, the eigenvalues are at $-2030 \pm j3760$ and $-630 \pm j5950$ which means the closed loop system is stable.

D. Robustness Study

Robustness of the proposed controller with respect to uncertainties in the system parameters and CPL variations are studied in this section.

1) Robustness to E: The only system parameter which is directly used by the controller is the voltage E, as shown in Fig. 4. Therefore, the controller responses when the value used by the controller does not match the one in the actual system must be studied. Assume that the value of voltage E, which is used in controller, Fig. 4 is E_1 and define $\beta = \frac{E}{E_1}$. The closed loop characteristic polynomial for the worst-case, i.e., when $G_L = 0$, changes from (11) to

$$s^2 + \left(-\frac{G_{\rm CPL}}{C} + \beta\frac{R_1}{L}\right)s - \beta\frac{R_1 G_{\rm CPL}}{CL} + \beta\frac{R_1}{R_0 CL} + \frac{1}{CL}(\beta - 1). \tag{14}$$

Fig. 7 (top) shows the variation of roots of this equation when β changes from 0.8 to 1.2 indicating $\pm 20\%$ variation. It is observed that the closed-loop poles do not experience excessive changes. The effect of unmatched E on the steady-state output voltage is also illustrated in Fig. 7 (bottom) which indicates a maximum of 1% in the output voltage for this entire range of variation in E.

Remark 2: If need be, this issue can be fully addressed by sensing E and using it in the controller.

2) Robustness to L and C: Fig. 8 shows the closed-loop poles of the control system, i.e., the characteristic equation (11), for the worst-case scenario, where $G_L = 0$, $P_{\rm CPL} = P$, when the inductance or capacitance values vary in the range of $\pm 20\%$ around their nominal values. The change in C causes practically no change in the system poles. The change in L causes about 20% change in the location of closed-loop poles which is still acceptable. This is the extent of impact of uncertainties in L and C on the system's transient response. As far as the steady-state response, those uncertainties cause no error.

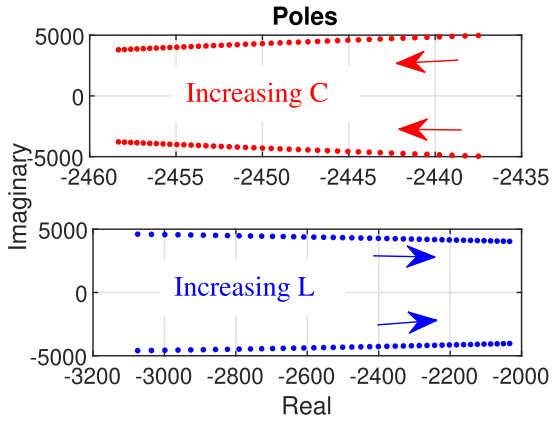

Fig. 8. Impact of $\pm 20\%$ change in C and L on closed-loop poles.

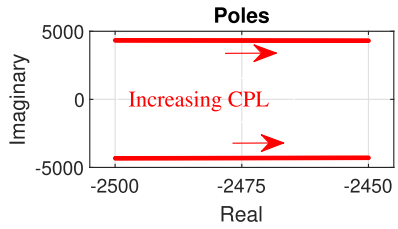

Fig. 9. Closed-loop poles when the CPL power varies from 0 to 250 W.

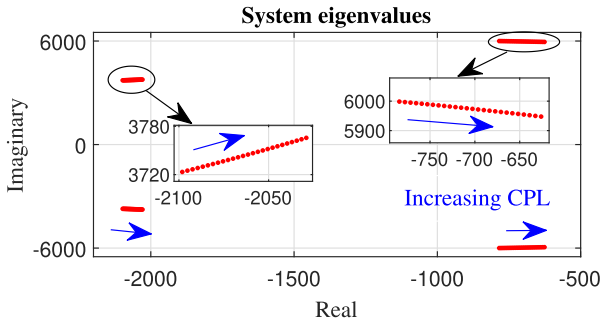

Fig. 10. Closed-loop poles when the CPL power varies from 0 to 250 W.

3) Robustness to CPL Directly Connected: When the power of the CPL changes from 0 to 250 W, the amount of change in the closed-loop poles is shown in Fig. 9. It is observed that the poles are highly robust and experience only about 2% change.

4) Robustness to CPL Connected Through Filter: Fig. 10 shows the closed-loop system eigenvalues while CPL is connected through an LC filter and varies from 0 to 250 W. The poles are originally at $-2100 \pm j3723$ (current loop) and $-784 \pm j6000$ (resonance mode) when CPL power is zero. The current loop poles are close to those predicted by the algorithm; and the resonance poles have a damping of about 0.13. When the CPL is at max, the poles move to $-2030 \pm j3760$ and the resonance poles to $-630 \pm j5950$ (damping ratio of about 0.1). It is noticed that the system is highly robust and the eigenvalues do not experience much change for the entire range of the CPL power.

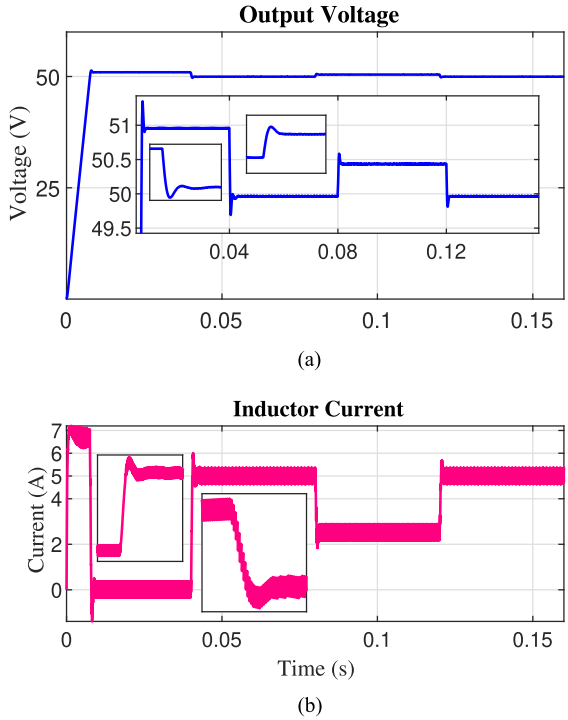

Fig. 11. Output voltage and converter current in response to resistive load changes. (a) Output voltage. (b) Inductor current.

V. Simulation Results

In this section, performance of the proposed controller is shown in the following three modes: 1) a resistive load; 2) a CPL without filter; and 3) a CPL connected through an LC filter. The system and control parameters are given in Table I. The rated converter current is 5 A. The current limiter is set at 7 A.

Fig. 11 shows the output voltage and inductor current when a resistive load is connected and experiences abrupt changes, i.e., no-load to full-load to half-load to full-load at times 0.04 s, 0.08 s, and 0.12 s, respectively. The output voltage has a smooth and fast response during the start-up process and in response to load changes. The converter current is successfully limited below 7 A at all times. The output voltage experiences a maximum offset of $\alpha = 2\%$, i.e., 1 V, for the entire range of load changes. The responses confirm validity of analytical conclusions.

The CPL is realized using the nonlinear equivalent model consist of a controlled current source ($\frac{P}{v}$). Fig. 12(a) and (b) show the converter's output voltage and the converter (inductor) current. The power of CPL at full load is 250 W. It is observed that the converter succeeds to smoothly and robustly respond to the CPL power changes, and to limit the converter current.

The ability of the controller to respond to bus voltage reference variations, 50 V to 42.5 V (15%) and back to 50 V at 0.08 s and 012 s, respectively, is illustrated in Fig. 13 (for CPL of 250 W). The controller tracks the command closely while limiting the current for all times.

Fig. 14 illustrates the performance of the control system when the CPL is connected to the bus through an LC filter. In this case, some oscillations are seen on the output voltage which are

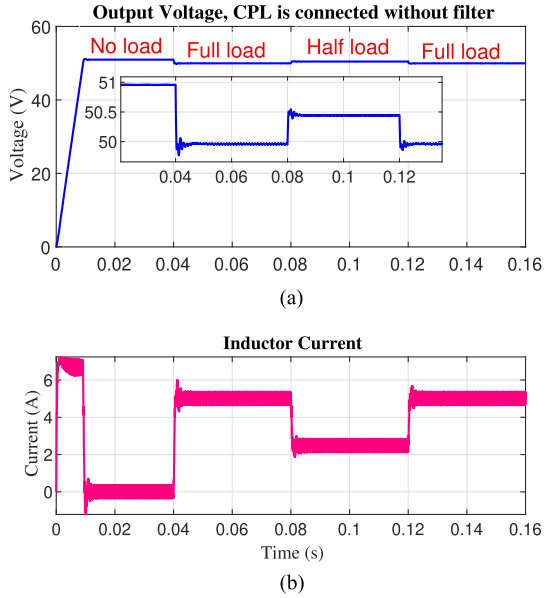

Fig. 12. Responses of proposed controller to a CPL power changes. (a) Converter output voltage. (b) Converter current.

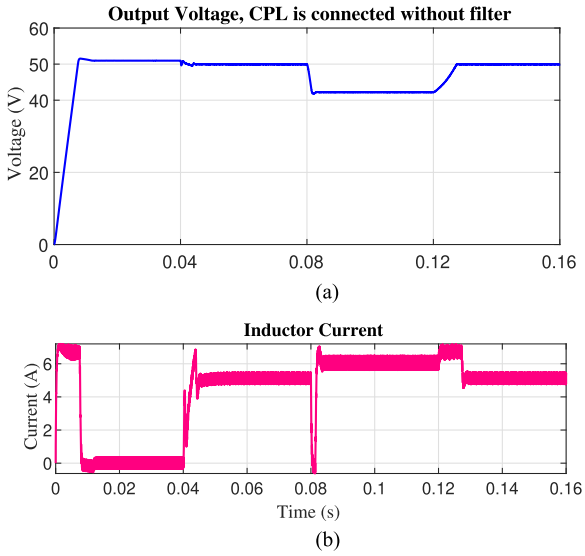

Fig. 13. Response of the controller to track bus voltage commands. (a) Converter output voltage. (b) Converter current.

damped in less than 10 ms. The oscillations denote a frequency of about 940 Hz and a damping ratio of about 0.13 which comply with analysis shown in Section IV-C and the location of resonance poles.

VI. Comparison With a Recent Study

Performance of proposed method is compared with that of a recently reported method [23]. Fig. 15 shows the control block diagram of [23] in which the first (outer) loop is similar to our proposed method while [23] uses a full state feedback control along with an integrator to ensure complete control and current-limiting is achieved. In our proposed method, the system dynamics are deployed which means no integrator is used. A

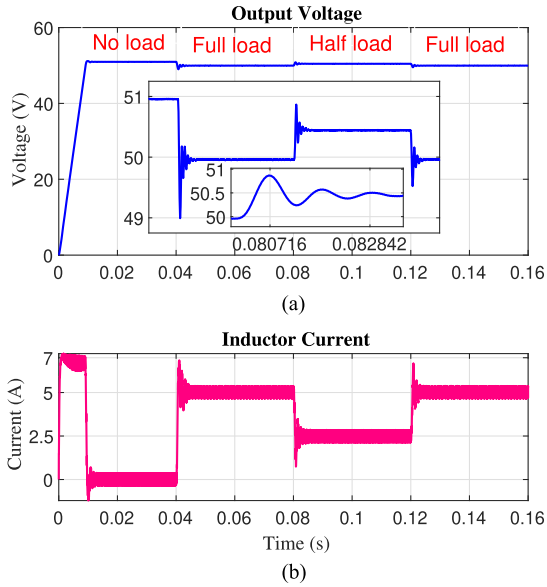

Fig. 14. Responses of the proposed controller to the CPL power changes when it is connected to the bus through an LC filter. (a) Converter output voltage. (b) Inductor current.

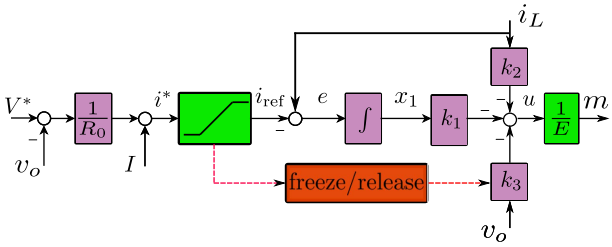

Fig. 15. Control block diagram of [23].

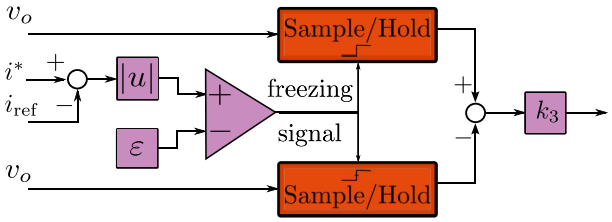

Fig. 16. Freeze/release mechanism.

freeze/release method is used for the feedback path k_3 as shown in Fig. 16. Here, the objective is to disable this branch when the system is in current-limiting mode and bring it back smoothly when this mode is over.

In [23], the optimal linear quadratic tracking introduced in [25] is used to determine the feedback gains (K). The entire system's linearized state space equations may be written as $\dot{x} = Ax + Bu + B_1$ where

$$A = \begin{bmatrix} 0 & 1 & \frac{1}{R_0} \\ 0 & 0 & -\frac{1}{L} \\ 0 & \frac{1}{C} & \frac{P}{CV_o^2} \end{bmatrix}, \; B = \begin{bmatrix} 0 \\ \frac{1}{L} \\ 0 \end{bmatrix}, \; B_1 = \begin{bmatrix} -\frac{V^*}{R_0} - I \\ 0 \\ 0 \end{bmatrix}$$

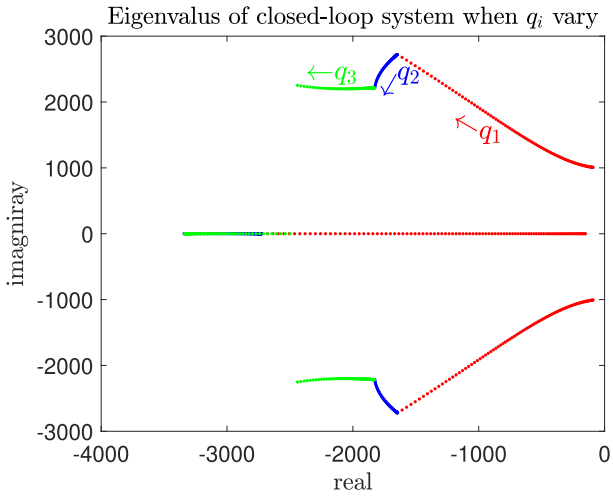

Fig. 17. Movement of closed-loop poles for the method proposed in [23] when q_1 (red), q_2 (blue), q_3 (green) varies from 10^3 to $10^{7.5}$, 10^{-1} to 10^1, and 10^0 to 10^2, respectively.

and $x = [x_1, i_L, v_o]^T$ where x_1 is the output of integrator. The control law is $u = -Kx$. By applying the operator $\frac{d}{dt}$, the state equation converts to $\dot{z} = Az + Bw$ and the control law to $w = -Kz$ where $z = \dot{x}$ and $w = \dot{u}$. We specifically notice that $z_1 = \dot{x}_1 = e$ is the tracking error of current, shown in Fig. 15. The optimal control approach, thus, minimizes $J = \int_0^\infty (q_1 e^2 + q_2 z_2^2 + q_3 z_3^2 + w^2) dt$. The approach to find $q_i's$ is as follows. Set $q_2 = q_3 = 0$. Increase q_1 and obtain K using lqr command and observe eigenvalues of $A - BK$. Freeze q_1 and move to q_2 and q_3. A typical root-locus graph is shown in Fig. 17. In this graph q_1 varies from 10^3 to $10^{7.5}$, then q_2 varies from 10^{-1} to 10^1, and finally q_3 varies from 10^0 to 10^2. At the final location, the eigenvalues are at $-2441 \pm j2252$, -2498 and the controller gains are $K = [5623, \; 7.5, \; 17.3]$. These poles are properly selected such that they closely correspond to the location of proposed controller, and the comparison is fair. The following comparison cases are presented.

Scenario 1: Resistive load. Fig. 18 shows the output voltages and inductor currents for both controllers when the load is resistive. The converter starts at full-load at time zero. At $t = 0.05$ s, the load is excessively increased and the current is limited. The load returns to its nominal value at $t = 0.1$ s. The following four observations are made.

1) Both methods perform well.
2) The proposed method has slightly smoother voltage responses.
3) The proposed method performs more accurate current-limiting (at 7 A).
4) The voltage drop of the method of [23] only during current limiting mode is slightly lower than the proposed method.

The reason is because the method of [23] limits the average current, while our proposed method limits the peak.

Scenario 2: Constant Power Load. The converters start at no-load and then a 250 W CPL is added at $t = 0.03$ s. Fig. 19 shows the output voltages and inductor currents. It is clearly observed that the proposed method exhibits much smoother

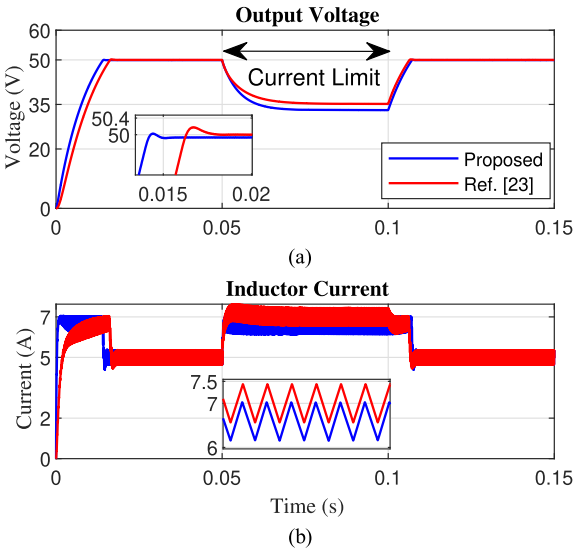

Fig. 18. Performance comparison with method of [23] for resistive load. (a) Output voltages. (b) Inductor currents.

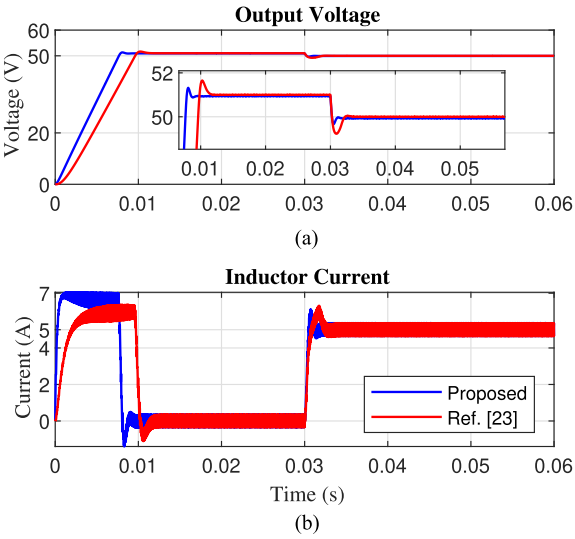

Fig. 19. Performance comparison with method of [23] for CPL. (a) Output voltages. (b) Inductor currents.

and faster responses. Specifically, when the CPL is connected, the output voltage undershoots to 48.24 V in the conventional method while the proposed method shows much smaller over/undershoots.

These results can be explained by the fact that the proposed method does not augment any additional dynamics to the original system while the conventional controller adds an integrator which increases the system's order and causes more transients. In comparison with a conventional PI controller, it could be stated that the PI controller adds another extra pole to the system which increases the loop order. As a result, additional dynamics are introduced which may compromise stability margin, and increase transient overshoots. Moreover, our design stage is much simpler and systematic.

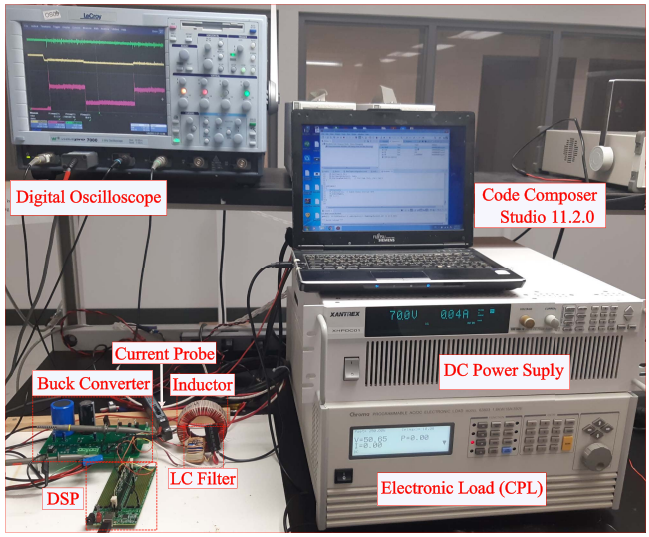

Fig. 20. Laboratory-scale experimental setup.

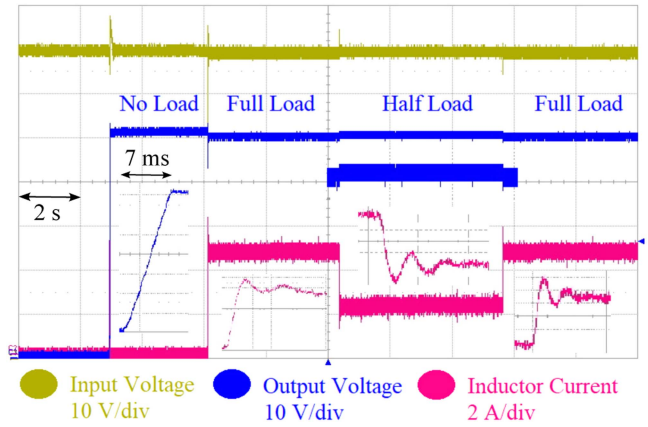

Fig. 21. Response of proposed controller to resistive load: Starting transient and transitions to full-load (250 W, 10 Ω), half-load, and back to full-load.

VII. Experimental Results

A laboratory experimental setup is built to test the proposed method. A photograph of this setup is shown in Fig. 20. The setup comprises a dc power supply XANTREX model XHPDC01 as the input voltage source, a Chroma programmable model 63803 is used as resistive and also CPL, a TMS320f28335 microcontroller to host the proposed controller, a LeCory Wavepro 7000 1 GHz oscilloscope. The following three scenarios are tested: 1) resistive load; 2) CPL without filter; 3) CPL with an LC filter. For each case, various disturbances are applied and the traces of input voltage, output voltage, and the inductor current are shown.

Scenario-I: Resistive load. Fig. 21 shows the results for resistive load. The starting transient (at no load), transitions to full-load (250 W, 10 Ω), half-load, and back to full-load are obtained and shown. The output voltage is almost 51.5 V at no-load, and 50 V at full-load. The controller's responses are fast, smooth, and robust. During the starting transient, the controller limits the current at the predefined value of 7 A. Thus,

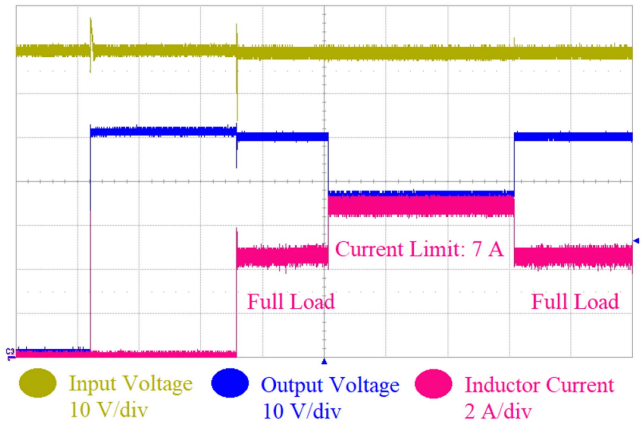

Fig. 22. Current-limiting performance of proposed controller.

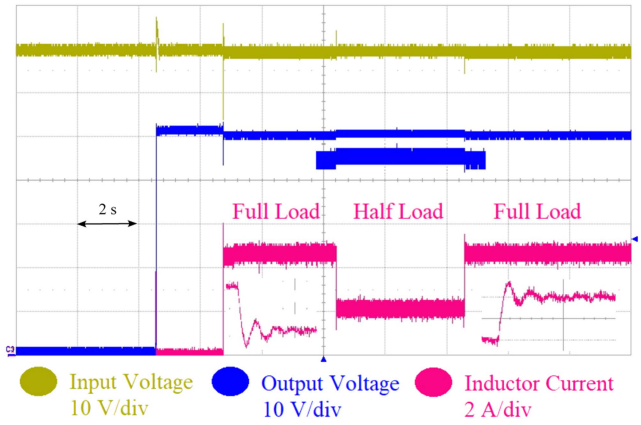

Fig. 23. Response of proposed controller to CPL without filter: Starting transient and transitions to full-load (250 W, 10 Ω), half-load, and back to full-load.

the output voltage linearly increases and reaches 50 V in about 7 ms. Fig. 22 shows the current limiting performance of the proposed controller. A transient load disturbance, its resistive reducing to 5 Ω, happens which causes the current to tend to increase beyond the limit. The controller successfully limits it to 7 A to protect the converter switches. As a result, the output voltage drops to $5 \times 7 = 35$ V. The current returns to normal when the transient period is passed.

Scenario-II: CPL without filter. In this scenario, the Chroma programmable load model 63803 is used in constant power mode. The rated power is set at 250 W. Fig. 23 shows the system responses which confirm fast and smooth responses much similar to the resistive load scenario.

Scenario-III: CPL with filter. In this scenario, the CPL is connected to the output terminals through an LC filter. Fig. 24 shows the controller responses. The voltage and current traces experience slightly more overshoots and longer settling times.

Fig. 25 shows the responses of the system (Scenario-III) when the output voltage reference is changed from 50 V to 42.5 V and back to 50 V. It confirms a fast and smooth execution of this command.

To check the impacts of input voltage change/uncertainty on the system's performance, the input voltage is reduced from

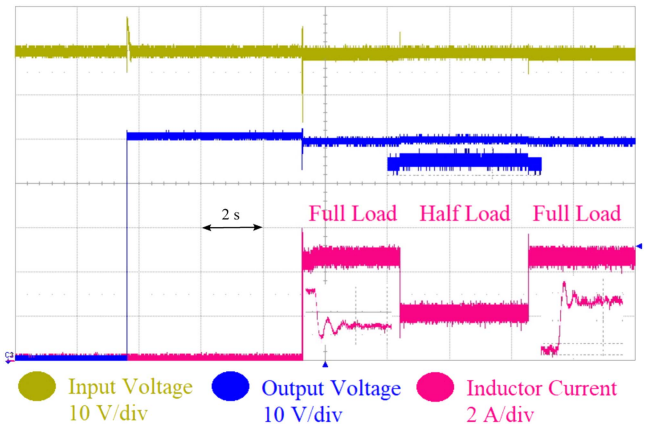

Fig. 24. Response of the proposed controller to CPL with LC filter: Starting transient and transitions to full-load (250 W, 10 Ω), half-load, and back to full-load.

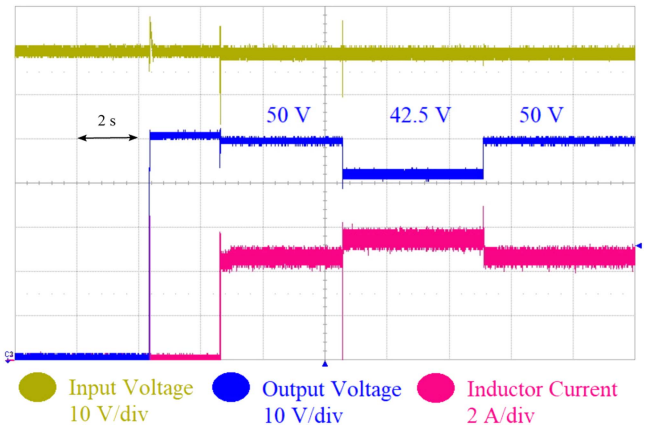

Fig. 25. Response of proposed controller to changes in the output voltage reference (50 V to 42.5 V and back to 50 V).

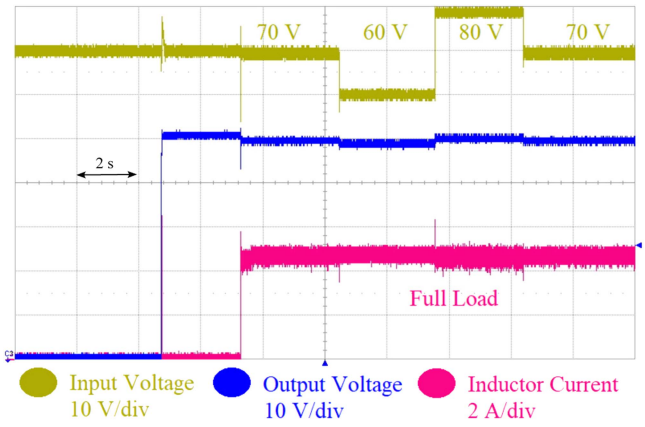

Fig. 26. Response of the proposed controller to changes in the input voltage (70 V to 60 V to 80 V and back to 70 V).

rated 70 V to 60 V, then increased to 80 V, and returned to its rated value of 70 V. Fig. 26 shows that the output voltage experiences a change under 2% for all this entire range of change in the input voltage.

VIII. Conclusion

This article presented a new controller for a buck converter interfacing two dc terminals in a dc microgrid. The particular challenge to address was the stability issues pertaining to constant power loads (CPLs). The proposed controller has two main properties: 1) it allows a small variation of the voltage, which has recently been shown to improve the stability; 2) it integrates the internal dynamics of the converter within the control system, thus obviating the need for using addition integrating compensators. As a result, the controller is simple, and does not increase the order of the control system. In fact, it is characterized by only two parameters whose design aspects are systematically addressed in a presented algorithm. The article illustrated superior performance of the proposed controller as compared with some state-of-the-art approaches. The (more challenging) case where the CPL is interfaced through an input filter is also examined, and robust performance of the controller is shown. Formulation of the same concept for different converter topologies may be considered as future research directions.

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